BURR-BROWN®

PCM3006

16-Bit, Single-Ended Analog Input/Output SoundPLUS™ STEREO AUDIO CODEC

FEATURES

- MONOLITHIC 16-BIT ΔΣ ADC AND DAC
- STEREO ADC:
  - Single-Ended Voltage Input
  - 64X Oversampling
  - High Performance
    - THD+N: –84dB
    - SNR: 89dB
    - Dynamic Range: 89dB
  - Digital High Pass Filter
- STEREO DAC:
  - Single-Ended Voltage Output
  - Analog Low Pass Filter
  - 8X Oversampling Digital Filter
  - High Performance
    - THD+N: –85dB
    - SNR: 93dB
    - Dynamic Range: 93dB
- SPECIAL FEATURES
  - Digital De-emphasis
  - Power Down: ADC/DAC Independent
- SAMPLING RATE: Up to 48kHz
- SYSTEM CLOCK: $256f_S$, $384f_S$, $512f_S$
- SINGLE +3V POWER SUPPLY
- SMALL PACKAGE: 24-Lead TSSOP

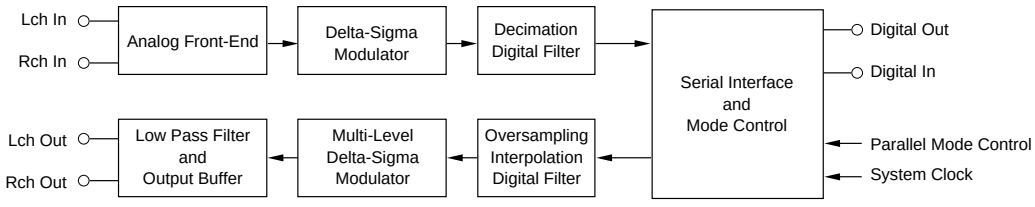
DESCRIPTION

The PCM3006 is a low cost single chip stereo audio CODEC (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter, and the DACs include an 8X oversampling digital interpolation filter. The DACs also include a de-emphasis function. PCM3006 operates with 16-bit, left-justified for ADC, right-justified for DAC data formats.

PCM3006 provides a Power-Down Mode that operates on the ADCs and DACs independently.

Fabricated on a highly advanced 0.6µs CMOS process, PCM3006 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Applications include sampling keyboards, digital mixers, effects processors, hard-disk recorders, data recorders and digital video cameras.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1436A
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SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, and 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3006T MIN	PCM3006T TYP	PCM3006T MAX	UNITS
DIGITAL INPUT/OUTPUT					
Input Logic					
Input Logic Level: V_{IH}(1)		0.7 x V_{DD}			VDC
V_{IL}(1)				0.3 x V_{DD}	VDC
Input Logic Current: I_{IN}(2)				±1	µA
Input Logic Current: I_{IN}(3)				100	µA
Output Logic					
Output Logic Level: V_{OH}(4)	I_{OUT} = –1mA	V_{DD} –0.3			VDC
V_{OL}(4)	I_{OUT} = +1mA			0.3	VDC
CLOCK FREQUENCY					
Sampling Frequency (f_S)		32	44.1	48	kHz
System Clock Frequency	256f_S	8.1920	11.2896	12.2880	MHz
	384f_S	12.2880	16.9344	18.4320	MHz
	512f_S	16.3840	22.5792	24.5760	MHz
ADC CHARACTERISTICS					
RESOLUTION			16		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3.0	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Disabled(6)		±1.7		% of FSR
Bipolar Zero Drift	High-Pass Filter Disabled(6)		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(5)					
THD+N: V_{IN} = –0.5dB			–84	–77	dB
V_{IN} = –60dB			–26		dB
Dynamic Range	A-Weighted	84	89		dB
Signal-to-Noise Ratio	A-Weighted	84	89		dB
Channel Separation		82	86		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time			17.4/f_S		sec
HPF Frequency Response	–3dB		0.019f_S		mHz
ANALOG INPUT					
Voltage Range			0.60 V_{CC}		Vp-p
Center Voltage			0.50 V_{CC}		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	–3dB		150		kHz
DAC CHARACTERISTICS					
RESOLUTION			16		Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±3	% of FSR
Gain Error			±1.0	±5	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error			±2.5		% of FSR
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(6)					
THD+N: V_{OUT} = 0dB (Full Scale)			–85	–77	dB
V_{OUT} = –60dB			–30		dB
Dynamic Range	EIAJ, A-Weighted	86	93		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted	86	93		dB
Channel Separation		84	90		dB

SPECIFICATIONS (CONT)

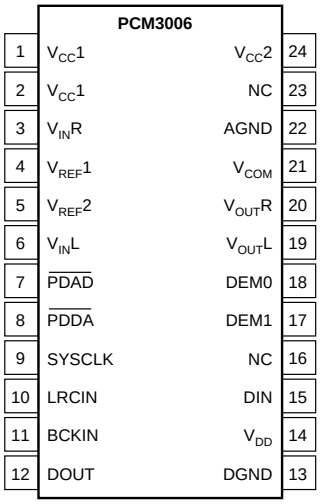
All specifications at +25°C, V_{DD} = V_{CC} = 3.0V, f_S = 44.1kHz, SYSCLK = 384f_S, CLKIO Input, 16-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3006T MIN	PCM3006T TYP	PCM3006T MAX	UNITS
DAC CHARACTERISTICS (CONT)					
DIGITAL FILTER PERFORMANCE					
Passband				0.445f_S	Hz
Stopband		0.555f_S			Hz
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			11.1/f_S		sec
ANALOG OUTPUT					
Voltage Range			0.6 x V_{CC}		Vp-p
Center Voltage			0.5 x V_{CC}		VDC
Load Impedance	AC-Coupling	10			kΩ
LPF Frequency Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range: V_{CC}, V_{DD}	–25°C to +85°C	2.7	3.0	3.6	VDC
	0° C to +70°C[7]	2.4	3.0	3.6	VDC
Supply Current: ADC/DAC Operation	V_{CC} = V_{DD} = 3.0V		18	24	mA
ADC Operation	V_{CC} = V_{DD} = 3.0V		12	16	mA
DAC Operation	V_{CC} = V_{DD} = 3.0V		7	10	mA
ADC/DAC Power-Down[8]	V_{CC} = V_{DD} = 3.0V		50		µA
Power Dissipation: ADC/DAC Operation	V_{CC} = V_{DD} = 3.0V		54	72	mW
ADC Operation	V_{CC} = V_{DD} = 3.0V		36	48	mW
DAC Operation	V_{CC} = V_{DD} = 3.0V		21	30	mW
ADC/DAC Power-Down[8]	V_{CC} = V_{DD} = 3.0V		150		µW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, Θ_{JA}			100		°C/W

NOTES: (1) Pins 7, 8, 9, 10, 11, 15, 17, 18: $\overline{PDAD}$, $\overline{PDDA}$, SYSCLK, LRCIN, BCKIN, DIN, DEM1, DEM0 (Schmitt-Trigger input with 100kΩ typical internal pull-down resistor). (2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt-Trigger input). (3) Pins 7, 8, 17, 18: $\overline{PDAD}$, $\overline{PDDA}$, DEM1, DEM0 (Schmitt-Trigger input, 100kΩ typical internal pull-down resistor). (4) Pin 12: DOUT. (5) f_{IN} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (6) f_{OUT} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (7) Applies for voltages between 2.4V to 2.7V for 0°C to +70°C and 256f_S/512f_S operation (384f_S not available). (8) SYSCLK, BCKIN, and LRCIN are stopped.

PIN CONFIGURATION

Top View **TSSOP**



NC = No Connection

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
$+V_{DD}$, $+V_{CC}1$, $+V_{CC}2$	+6.5V
Supply Voltage Differences	±0.1V
GND Voltage Differences	±0.1V
Digital Input Voltage	–0.3 to V_{DD} + 0.3V
Analog Input Voltage	–0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3V
Power Dissipation	300mW
Input Current	±10mA
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
(reflow, 10s)	+235°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM3006T	24-Lead TSSOP	350

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	$V_{CC}1$	—	ADC Analog Power Supply
2	$V_{CC}1$	—	ADC Analog Power Supply
3	$V_{IN}R$	IN	ADC Analog Input, Rch
4	$V_{REF}1$	—	ADC Reference, 1
5	$V_{REF}2$	—	ADC Reference, 2
6	$V_{IN}L$	IN	ADC Analog Input, Lch
7	$\overline{PDAD}$	IN	ADC Power Down, Active LOW(1, 2)
8	$\overline{PDDA}$	IN	DAC Power Down, Active LOW(1, 2)
9	SYSCLK	IN	System Clock Input(2)
10	LRCIN	IN	Sample Rate Clock Input (f_S)(2)
11	BCKIN	IN	Bit Clock Input(2)
12	DOUT	OUT	Data Output
13	DGND	—	Digital Ground
14	V_{DD}	—	Digital Power Supply
15	DIN	IN	Data Input
16	NC	IN	No Connection
17	DEM1	IN	De-emphasis Control(1, 2)
18	DEM0	IN	De-emphasis Control 0(1, 2)
19	$V_{OUT}L$	OUT	DAC Analog Output, Lch
20	$V_{OUT}R$	OUT	DAC Analog Output, Rch
21	V_{COM}	—	ADC/DAC Common
22	AGND	—	Analog Ground
23	NC	—	No Connection
24	$V_{CC}2$	—	DAC Analog Power Supply

NOTES: (1) With 100kΩ typical internal pull-down resistor. (2) Schmitt-Trigger input.

ELECTROSTATIC DISCHARGE SENSITIVITY

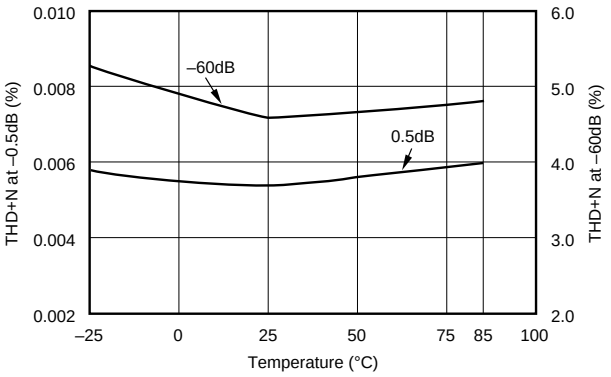
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

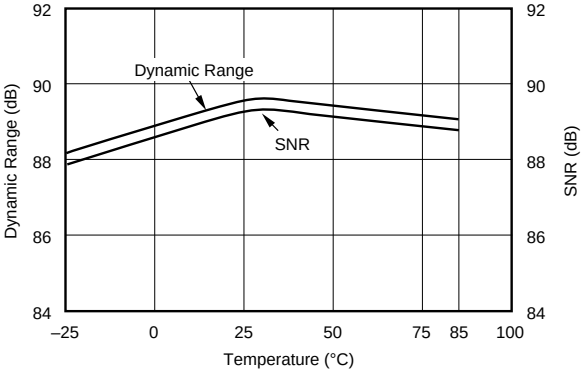
TYPICAL PERFORMANCE CURVES
ADC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and f_{SIGNAL} = 1kHz, unless otherwise noted.

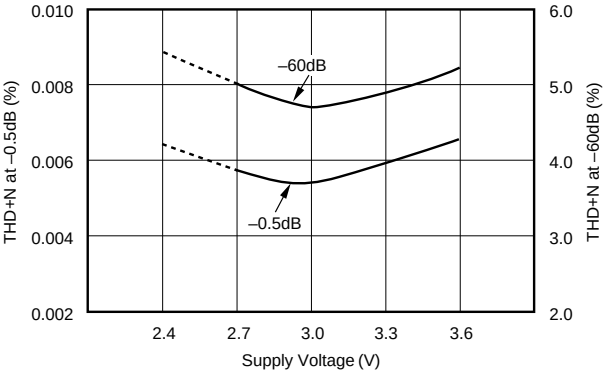
THD+N vs TEMPERATURE



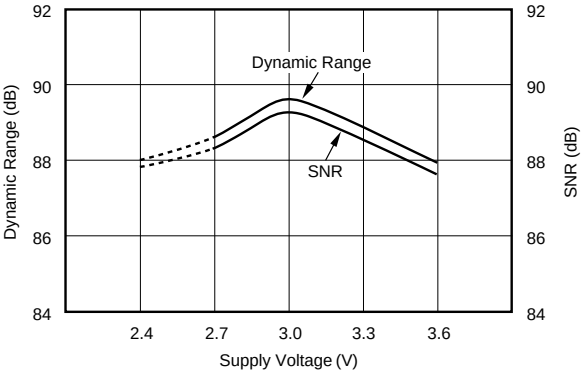
DYNAMIC RANGE and SNR vs TEMPERATURE



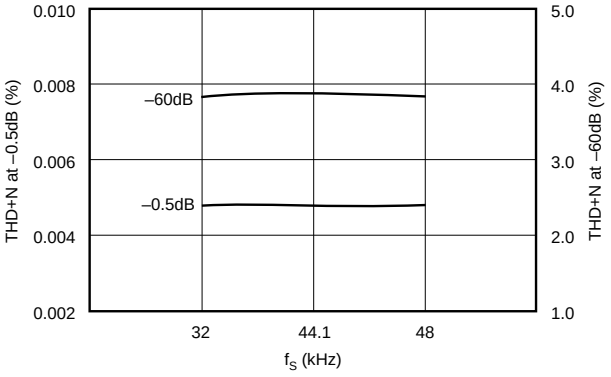
THD+N vs SUPPLY VOLTAGE



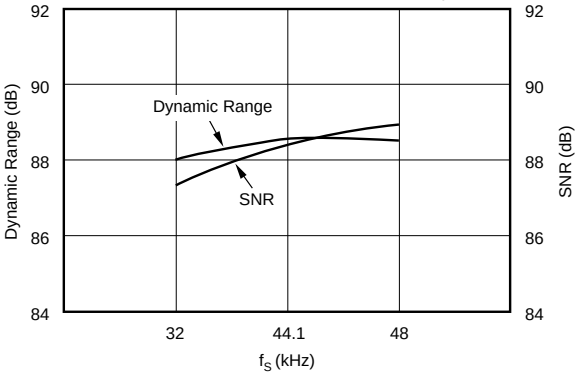
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY



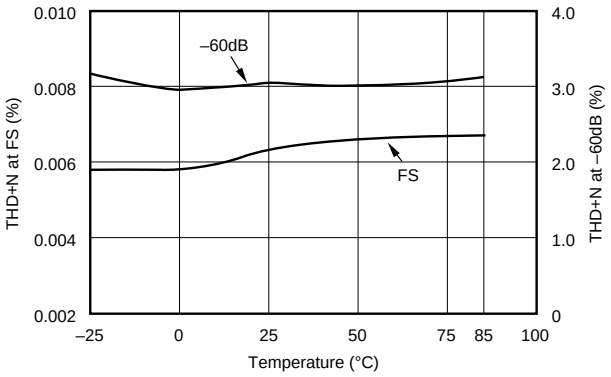
DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY



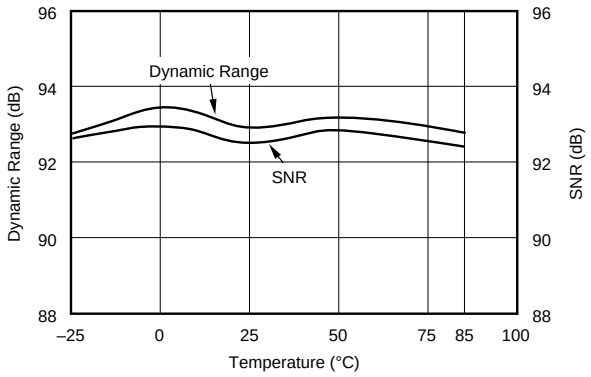
TYPICAL PERFORMANCE CURVES
DAC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, f_{SYSCLK} = 384f_S, and f_{SIGNAL} = 1kHz, unless otherwise noted.

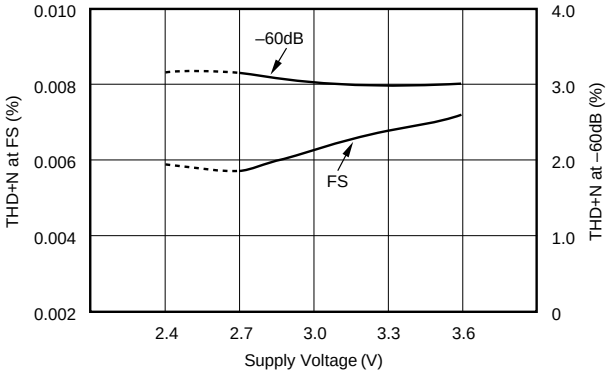
THD+N vs TEMPERATURE



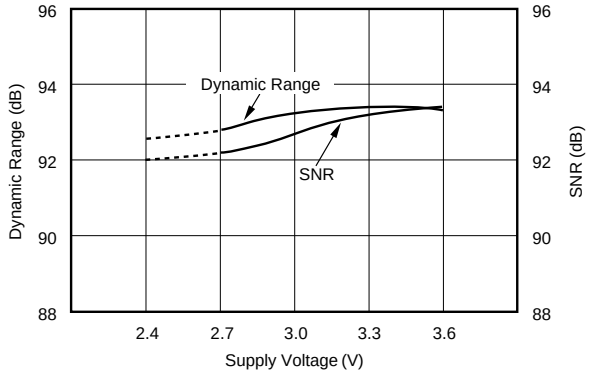
DYNAMIC RANGE and SNR vs TEMPERATURE



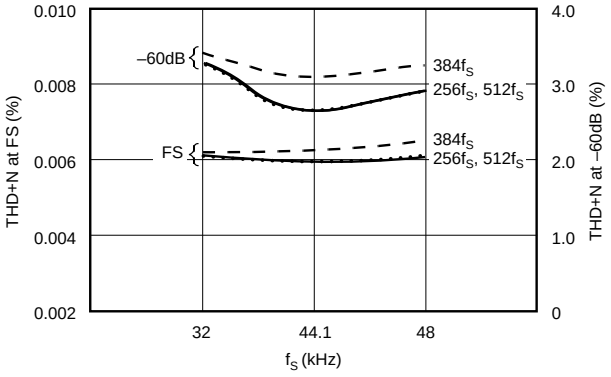
THD+N vs SUPPLY VOLTAGE



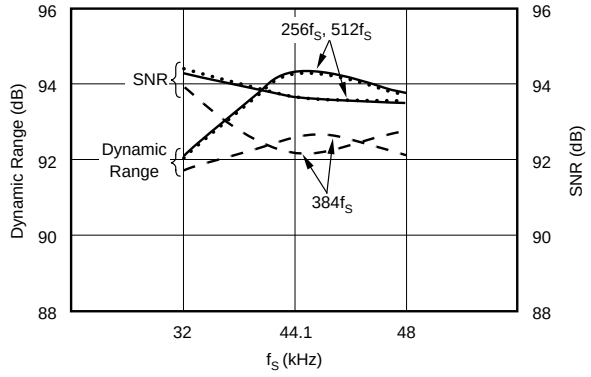
DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE



THD+N vs SAMPLING FREQUENCY
and SYSTEM CLOCK



DYNAMIC RANGE and SNR
vs SAMPLING FREQUENCY and SYSTEM CLOCK

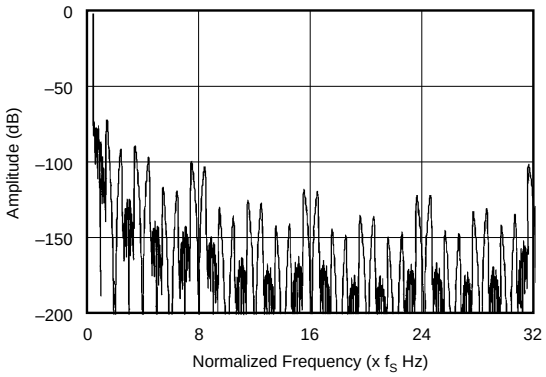


TYPICAL PERFORMANCE CURVES

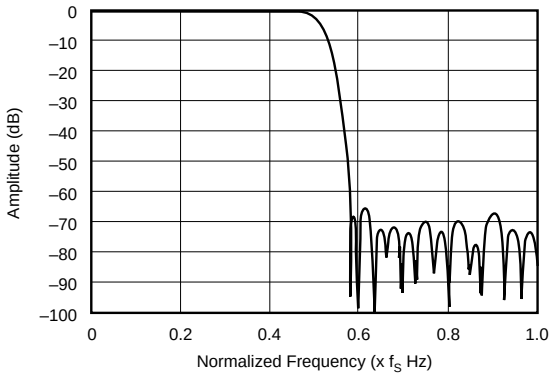
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ADC DIGITAL FILTER

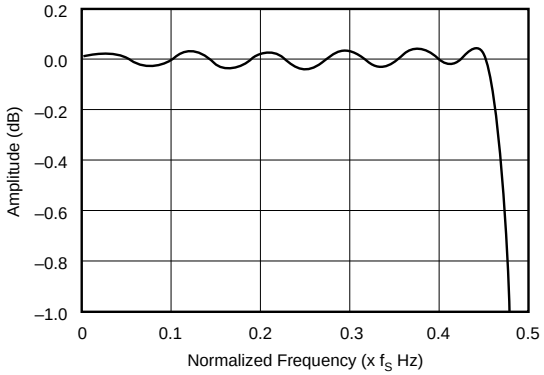
OVERALL CHARACTERISTICS



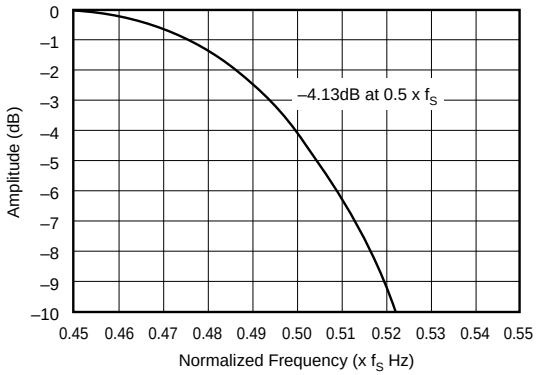
STOPBAND ATTENUATION CHARACTERISTICS



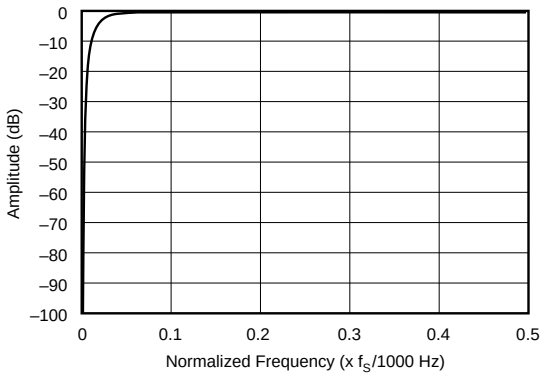
PASSBAND RIPPLE CHARACTERISTICS



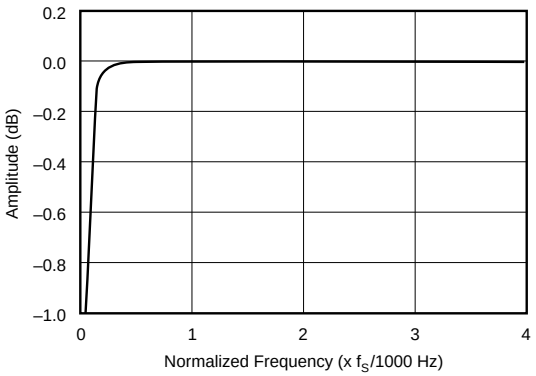
TRANSIENT BAND CHARACTERISTICS



HIGH PASS FILTER RESPONSE



HIGH PASS FILTER RESPONSE

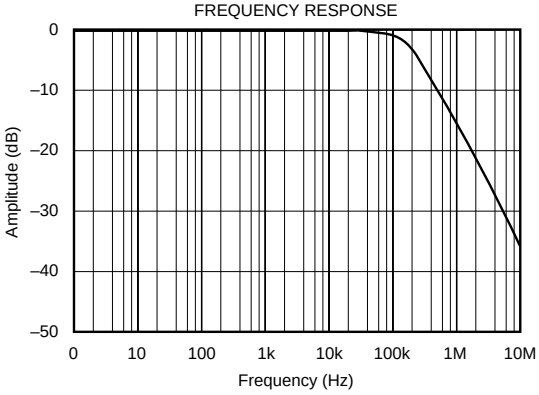


TYPICAL PERFORMANCE CURVES

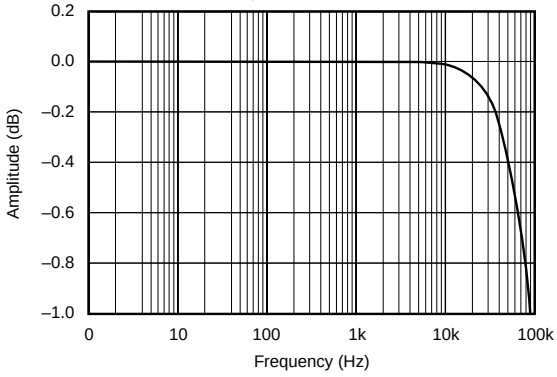
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

ANTI-ALIASING FILTER

ANTI-ALIASING FILTER OVERALL FREQUENCY RESPONSE



ANTI-ALIASING FILTER PASSBAND FREQUENCY RESPONSE

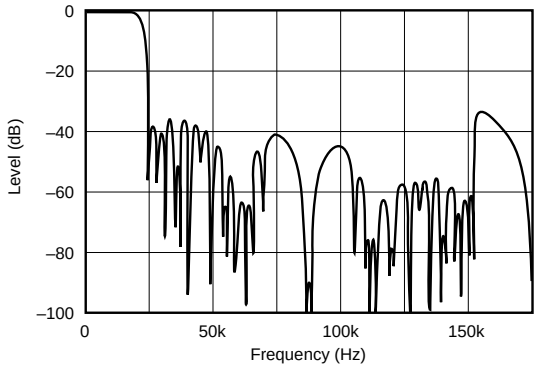


TYPICAL PERFORMANCE CURVES

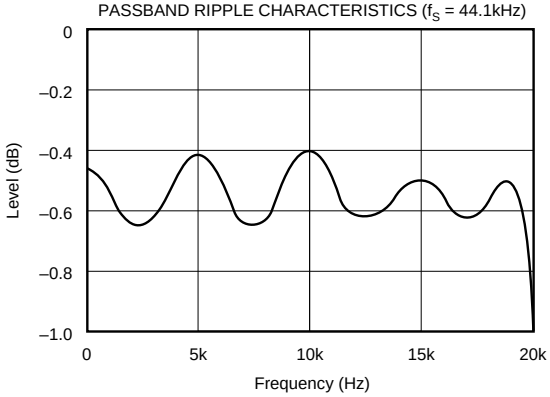
At T_A = +25°C, V_{CC} = V_{DD} = 3.0V, f_S = 44.1kHz, and f_{SYSCLK} = 384f_S, unless otherwise noted.

DAC DIGITAL FILTER

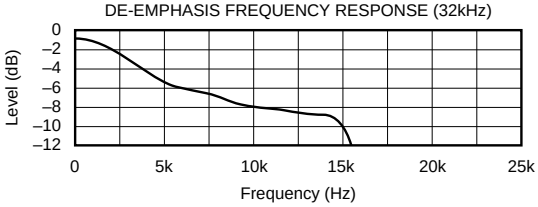
OVERALL FREQUENCY CHARACTERISTICS (f_S = 44.1kHz)



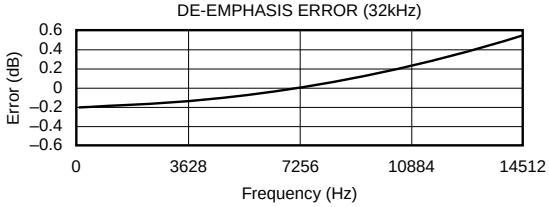
PASSBAND RIPPLE CHARACTERISTICS (f_S = 44.1kHz)



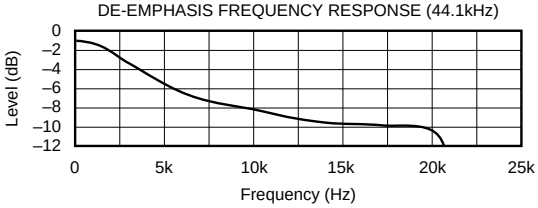
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



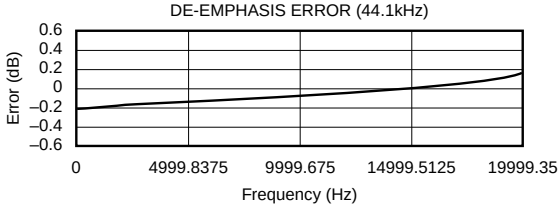
DE-EMPHASIS ERROR (32kHz)



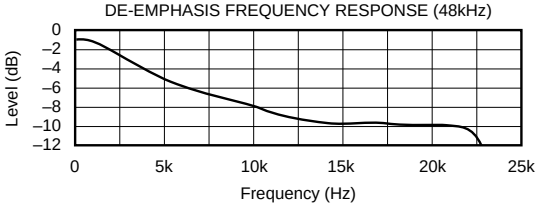
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



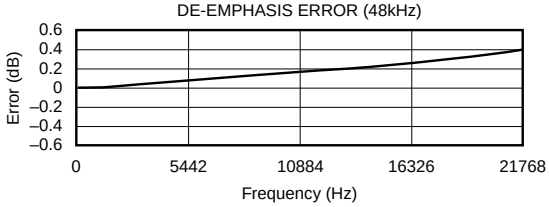
DE-EMPHASIS ERROR (44.1kHz)



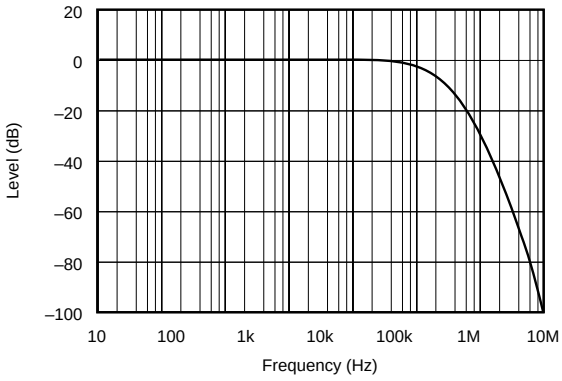
DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



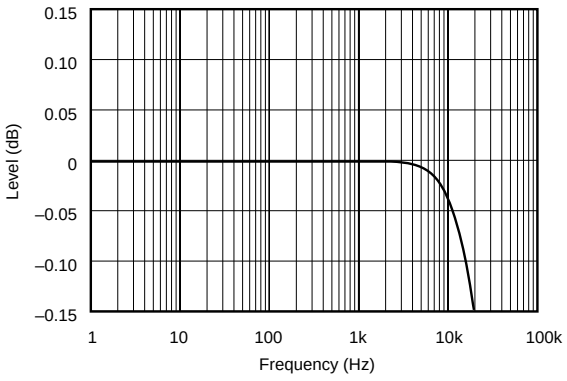
DE-EMPHASIS ERROR (48kHz)



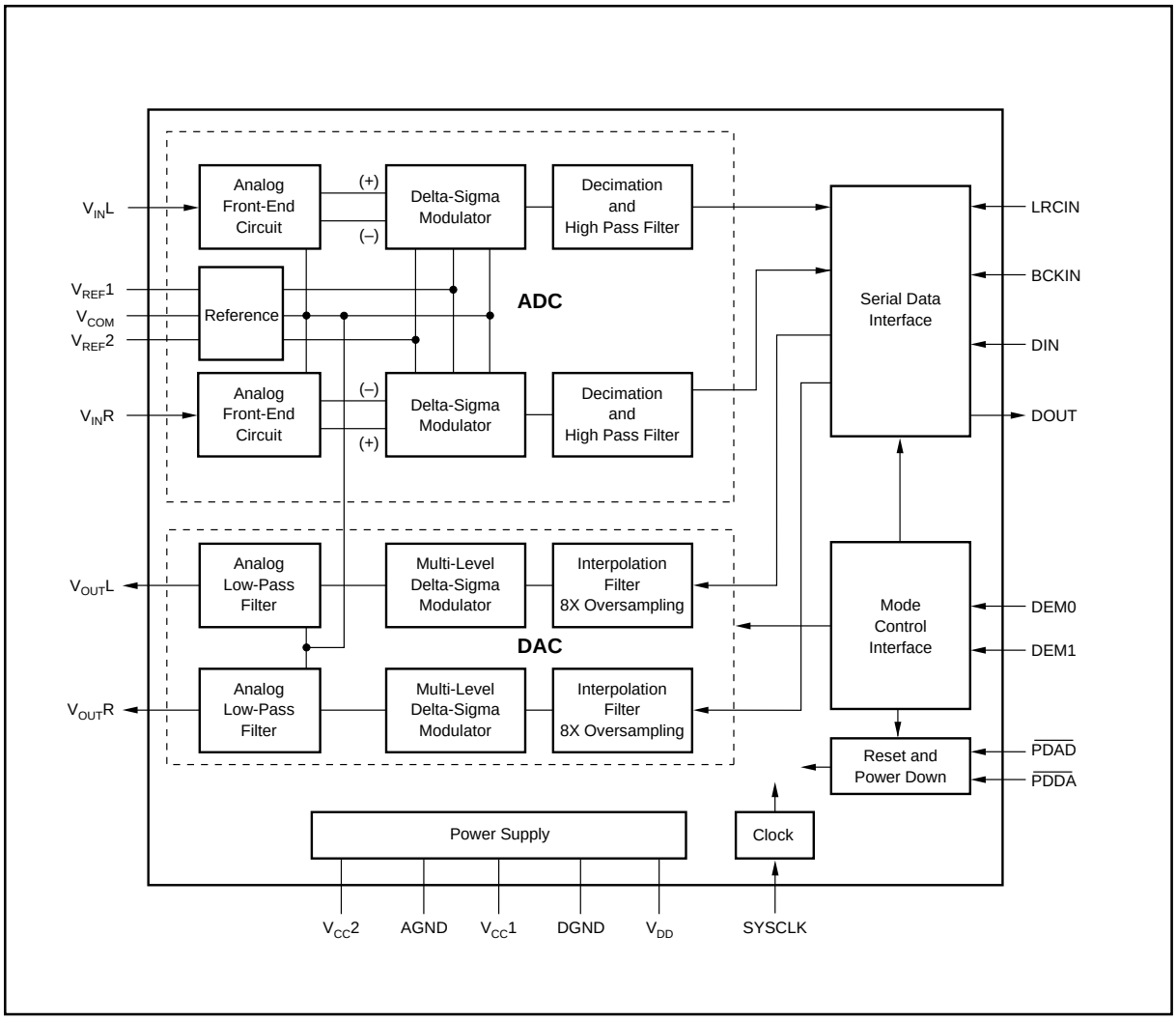
INTERNAL ANALOG FILTER FREQUENCY RESPONSE (10Hz~10MHz)



INTERNAL ANALOG FILTER FREQUENCY RESPONSE (1Hz~20kHz)



BLOCK DIAGRAM



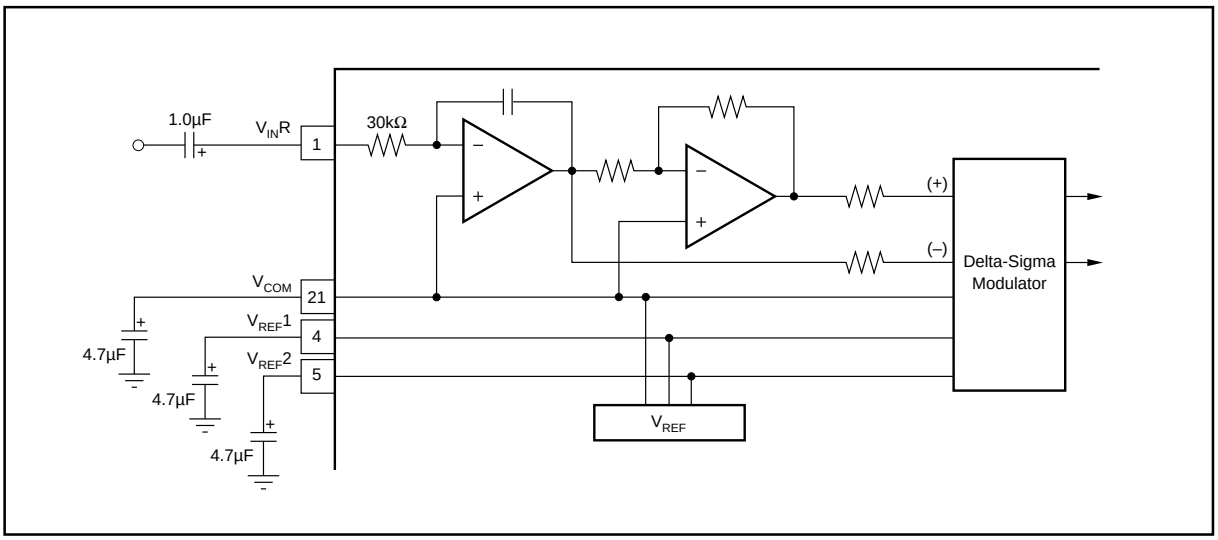


FIGURE 1. Analog Front-End (Single-Channel).

PCM AUDIO INTERFACE

The four-wire digital audio interface for PCM3006 is comprised of: LRCIN (pin 10), BCKIN (pin 11), DIN (pin 15), and DOUT (pin 12). PCM3006 accepts 16-bit Most Significant Bit (MSB) First. Figures 2 and 3 illustrate audio data input/output format and timing.

PCM3006 can accept 32-, 48-, or 64-bit clocks (BCKIN) in one clock of LRCIN.

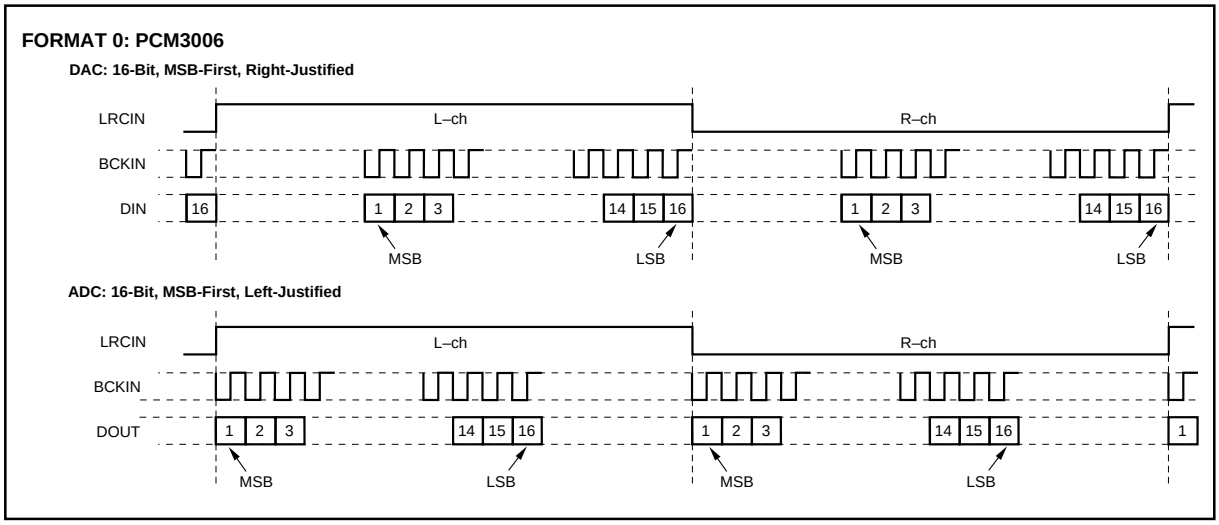
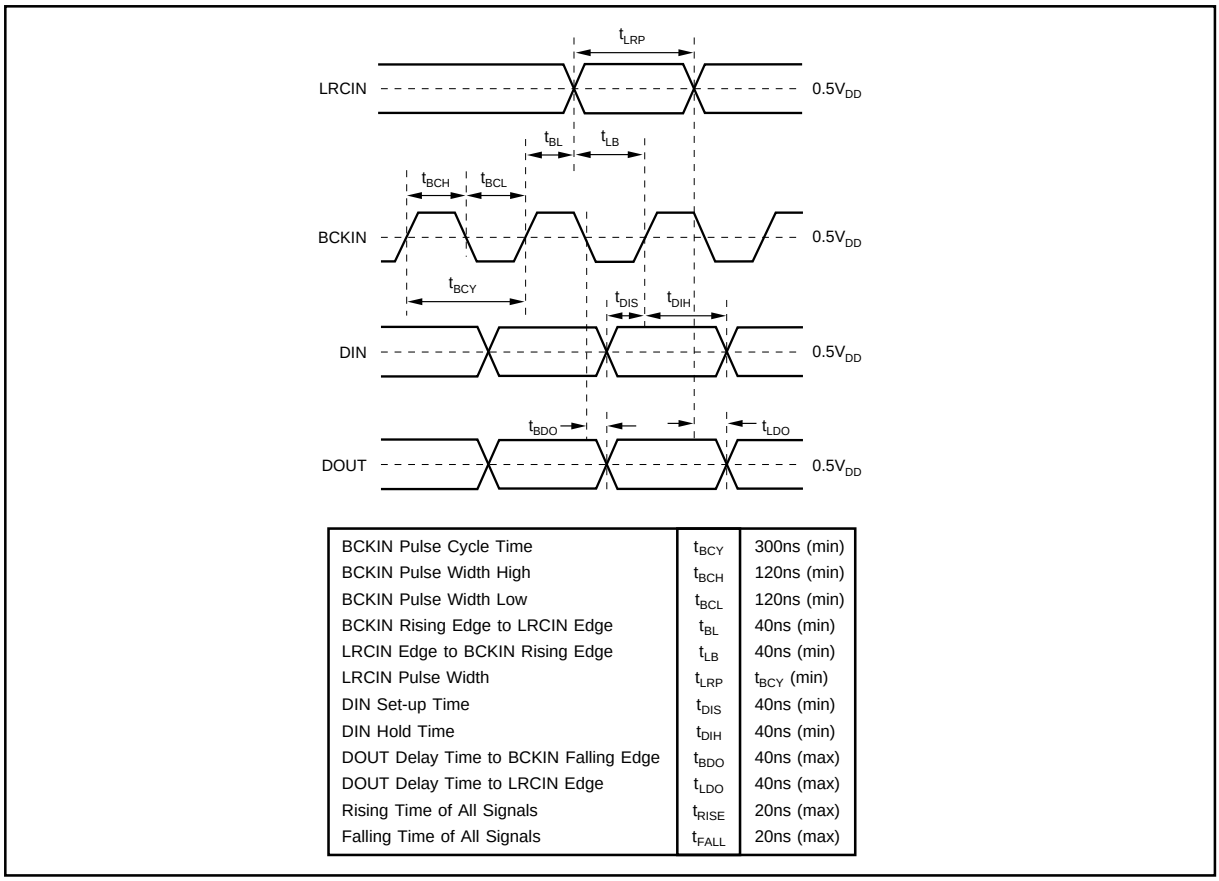


FIGURE 2. Audio Data Input/Output Format.



BCKIN Pulse Cycle Time	t_{BCY}	300ns (min)
BCKIN Pulse Width High	t_{BCH}	120ns (min)
BCKIN Pulse Width Low	t_{BCL}	120ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	40ns (min)
LRCIN Edge to BCKIN Rising Edge	t_{LB}	40ns (min)
LRCIN Pulse Width	t_{LRP}	t_{BCY} (min)
DIN Set-up Time	t_{DIS}	40ns (min)
DIN Hold Time	t_{DIH}	40ns (min)
DOUT Delay Time to BCKIN Falling Edge	t_{BDO}	40ns (max)
DOUT Delay Time to LRCIN Edge	t_{LDO}	40ns (max)
Rising Time of All Signals	t_{RISE}	20ns (max)
Falling Time of All Signals	t_{FALL}	20ns (max)

FIGURE 3. Audio Data Input/Output Timing.

SYSTEM CLOCK

The system clock for PCM3006 must be either $256f_S$, $384f_S$ or $512f_S$, where f_S is the audio sampling frequency. The system clock should be provided to SYSCLK (pin 9).

PCM3006 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$. When $384f_S$ or $512f_S$ system clock is used, the clock is divded into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filter and the delta-sigma modulator.

Table I lists the relationship of typical sampling frequencies and system clock frequencies and Figure 4 illustrates the system clock timing.

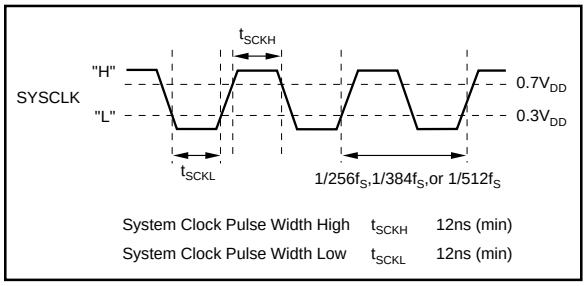


FIGURE 4. System Clock Timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

RESET

PCM3006 has an internal Power-On Reset circuit, as well as an external forced reset. The internal Power-On Reset initializes (resets) when the supply voltage V_{DD} >2.0V (typ). External forced reset occurs when $\overline{PDAD}$ = LOW or $\overline{PDDA}$ = LOW. Figure 5 shows the internal Power-On reset timing and Figure 6 shows the external forced reset timing by $\overline{PDAD}$ or $\overline{PDDA}$. During external forced reset, the outputs of the DAC are forced to GND (see Figure 7). The analog outputs are then forced to $0.5V_{CC}$ during $t_{DACDLY1}$ ($16384/f_S$) after reset removal. The outputs of ADC are also invalid, digital outputs are forced to all zero during $t_{ADCDLY1}$ ($18432/f_S$) after reset removal.

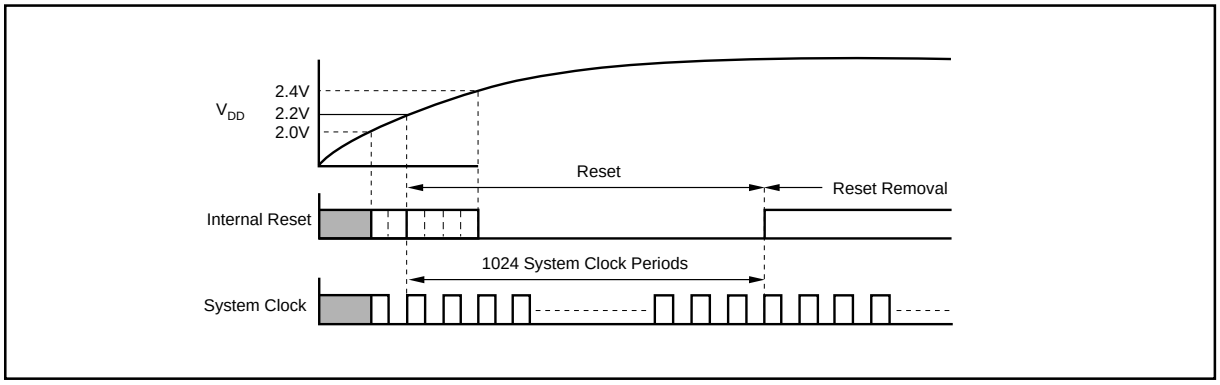


FIGURE 5. Internal Power-On Reset Timing.

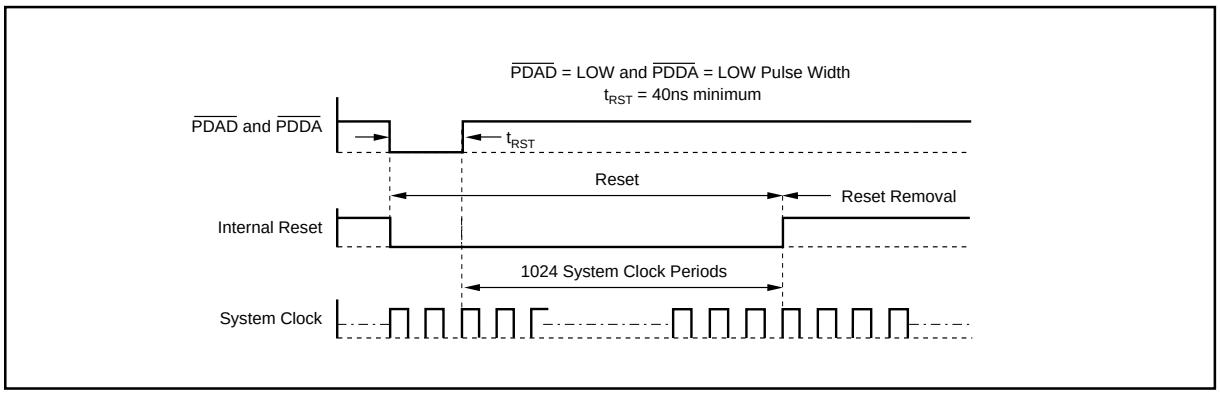


FIGURE 6. External Forced Reset Timing.

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

PCM3006 operates with LRCIN synchronized to the system clock. PCM3006 does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization. If the synchronization between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC will stop within $1/f_S$, and the analog output will be forced to bipolar zero ($0.5V_{CC}$) until the system clock is re-synchronized to LRCIN followed by $t_{DACDLY2}$ delay time. Internal operation of the ADC will also stop within $1/f_S$, and the digital output codes will be set to bipolar zero until re-synchronization occurs followed by $t_{ADCDLY2}$ delay time. If LRCIN is synchronized with 5 or less bit clocks to the system clock, operation will be normal. Figures 7 and 8 illustrate the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero (<$1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which will cause output noise.

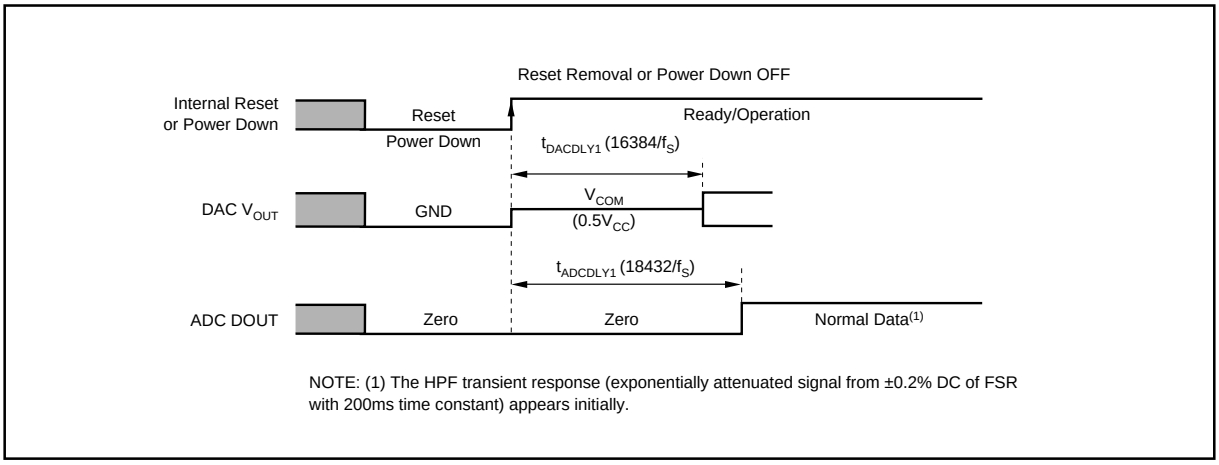


FIGURE 7. DAC Output and ADC Output for Reset and Power Down.

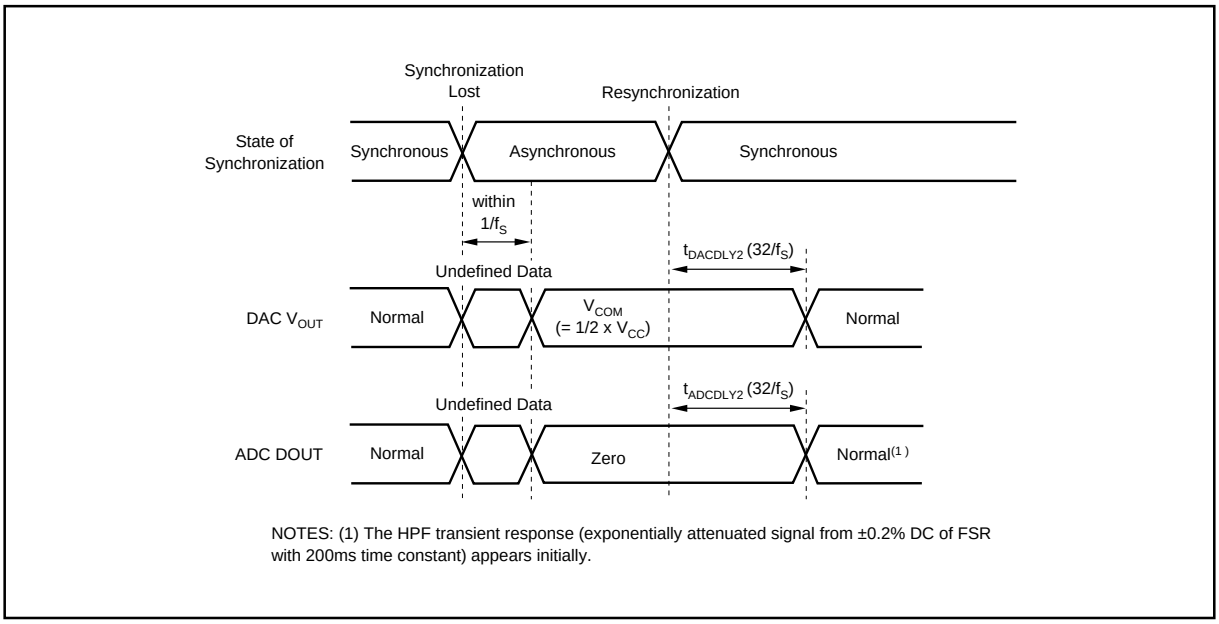


FIGURE 8. DAC Output and ADC Output for Loss of Synchronization.

OPERATIONAL CONTROL

PCM3006 has hardwire functional control using $\overline{\text{PDAD}}$ (pin 7) and $\overline{\text{PDDA}}$ (pin 8) for Power-Down Control and DEM0 (pin 18) and DEM1 (pin 17) for de-emphasis.

$\overline{\text{PDAD}}$: **ADC Power-Down Control (Pin 7)**

This pin places the ADC section in the lowest power consumption mode. The ADC operation is stopped by cutting the supply current to the ADC section, and DOUT is fixed to zero during ADC Power-Down Mode enable. Figure 7 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

$\overline{\text{PDAD}}$	POWER-DOWN
Low	ADC Power-Down Mode Enabled
High	ADC Power-Down Mode Disabled

$\overline{\text{PDDA}}$: **DAC Power-Down Control (Pin 8)**

This pin places the DAC section in the lowest power consumption mode. The DAC operation is stopped by cutting the supply current to the DAC section and V_{OUT} is fixed to GND during DAC Power-Down Mode enable. Figure 8 illustrates the DAC V_{OUT} response for DAC Power-Down ON/OFF. This does not affect the ADC operation.

$\overline{\text{PDDA}}$	POWER-DOWN
Low	DAC Power-Down Mode Enabled
High	DAC Power-Down Mode Disable

DEM1, 0: **DAC De-emphasis Control (Pin 17 and Pin 18)**

These pins select the de-emphasis mode as shown below:

DEM1	DEM0	
Low	Low	De-emphasis 44.1kHz ON
Low	High	De-emphasis OFF
High	Low	De-emphasis 48kHz ON
High	High	De-emphasis 32kHz ON

APPLICATION AND LAYOUT CONSIDERATIONS

POWER SUPPLY BYPASSING

The digital and analog power supply lines to PCM3006 should be bypassed to the corresponding ground pins with both 0.1µF ceramic and 10µF tantalum capacitors as close to the device pins as possible. Although PCM3006 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize the dynamic performance of PCM3006, the analog and digital grounds are not connected internally. The PCM3006 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3006 ground pins with low impedance connections to the analog ground plane. PCM3006 should reside entirely over this plane to avoid coupling high frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT PINS

A tantalum capacitor, between 1µF and 10µF, is recommended as an AC-coupling capacitor at the inputs. Combined with the 30kΩ characteristic input impedance, a 1.0µF coupling capacitor will establish a 5.3Hz cut-off frequency for blocking DC. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 30kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} Pins

A 4.7µF to 10µF tantalum capacitor is recommended between $V_{REF}1$, $V_{REF}2$, and AGND to ensure low source impedance for the ADC's references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

V_{COM} Pin

A 4.7µF to 10µF tantalum capacitor is recommended between V_{COM} and AGND to insure low source impedance of the ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the DAC common.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3006. The duty cycle and jitter at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN) and a word clock (LCRIN) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long term reliability if the maximum power dissipation limit is exceeded.

RST CONTROL

If the capacitance between V_{REF} and V_{COM} exceeds 2.2µF, an external reset control delay time circuit must be used.

EXTERNAL MUTE CONTROL

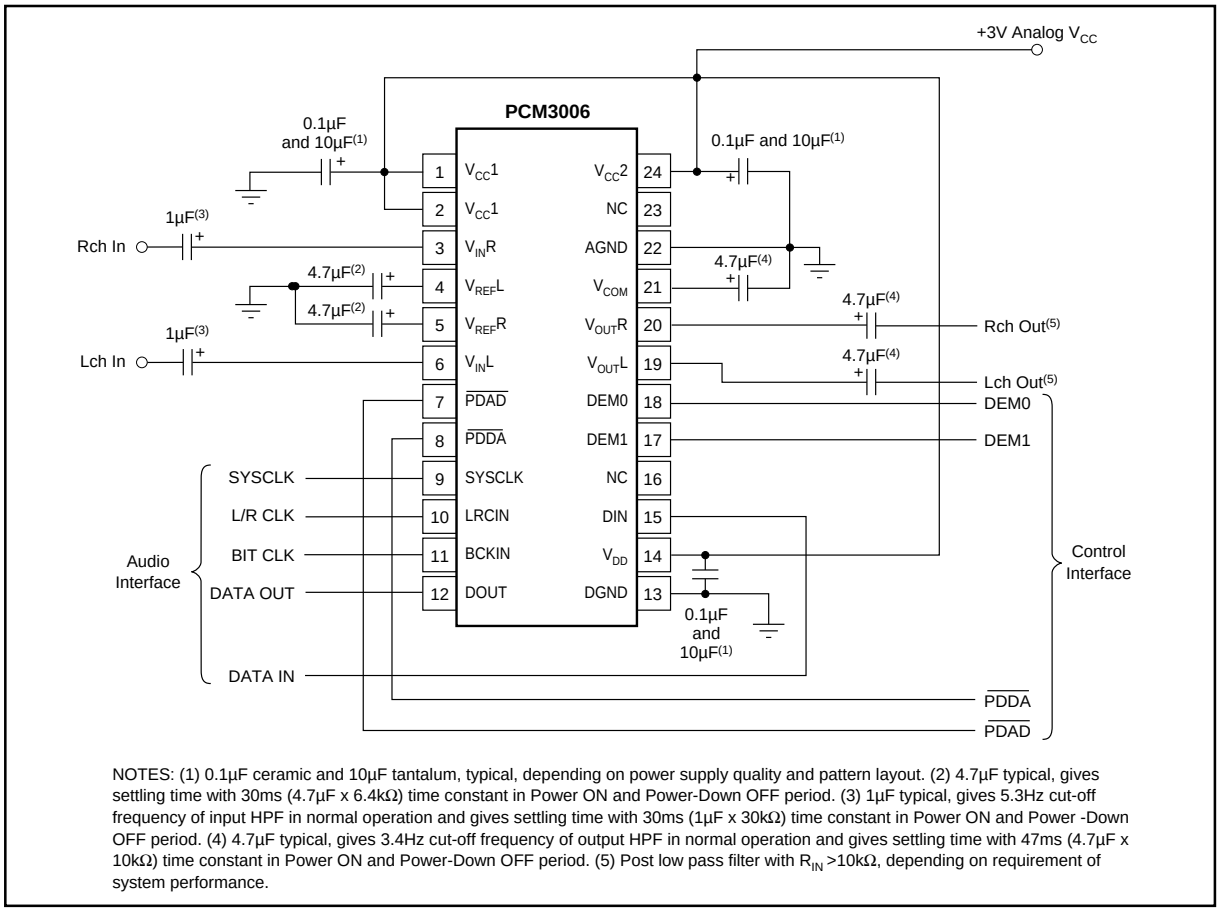
Click noises are caused by DC level changes at the DAC output. To avoid any click noises going in and out of Power-Down Mode, an External Mute Control is generally required. The recommended control sequence is as follows: External Mute ON, CODEC Power-Down OFF, and then, External Mute OFF.

NOTE: If SYSCLK is stopped when the PCM3006 is in Power-Down Mode, the device is internally reset.

THEORY OF OPERATION

ADC SECTION

The PCM3006 ADC consists of two reference circuits, a stereo single-to-differential converter, a fully differential 5th-level delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram in this data sheet illustrates the architecture of the ADC section, Figure 1 shows the single-to-differential converter, and Figure 10 illustrates the architecture of the 5-level delta-sigma modulator and transfer functions.



NOTES: (1) 0.1µF ceramic and 10µF tantalum, typical, depending on power supply quality and pattern layout. (2) 4.7µF typical, gives settling time with 30ms (4.7µF x 6.4kΩ) time constant in Power ON and Power-Down OFF period. (3) 1µF typical, gives 5.3Hz cut-off frequency of input HPF in normal operation and gives settling time with 30ms (1µF x 30kΩ) time constant in Power ON and Power -Down OFF period. (4) 4.7µF typical, gives 3.4Hz cut-off frequency of output HPF in normal operation and gives settling time with 47ms (4.7µF x 10kΩ) time constant in Power ON and Power-Down OFF period. (5) Post low pass filter with R_{IN} >10kΩ, depending on requirement of system performance.

FIGURE 9. Typical Connection Diagram for PCM3006.

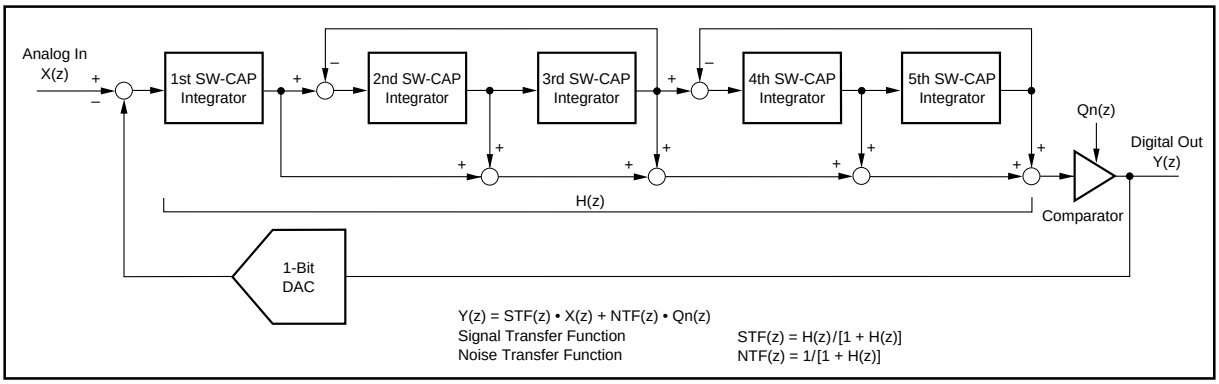


FIGURE 10. Simplified 5-Level Delta-Sigma Modulator.

An internal reference circuit with three external capacitors provides all reference voltages which are required by the ADC, which defines the full-scale range for the converter. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at 64X oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5-level delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$ 16-bit data words by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The DC components are removed by a high pass filter function contained within the decimation filter.

THEORY OF OPERATION

DAC SECTION

The delta-sigma DAC section of PCM3006 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 11. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 12.

Multi Level Delta Sigma

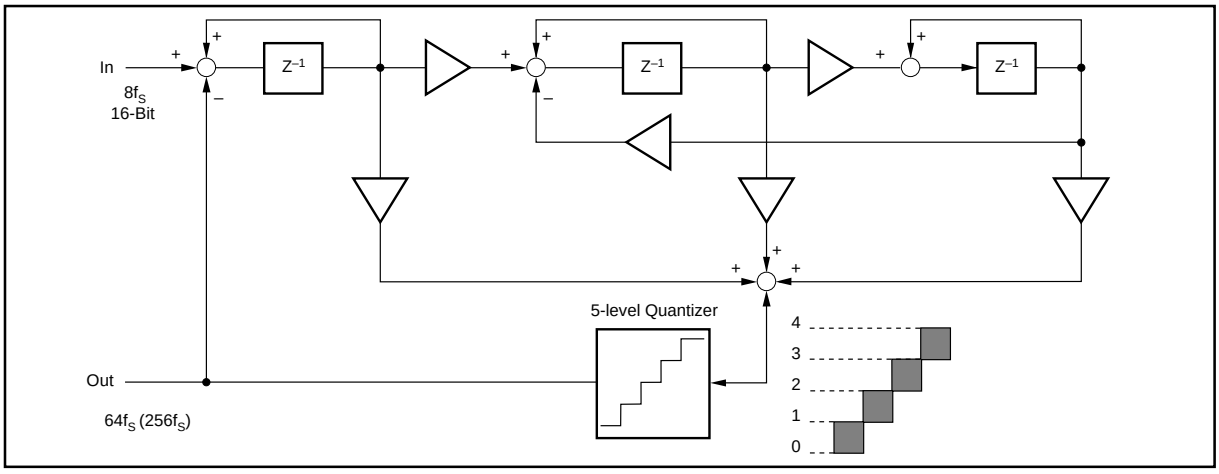


FIGURE 11. 5-Level ΔΣ Modulator Block Diagram.

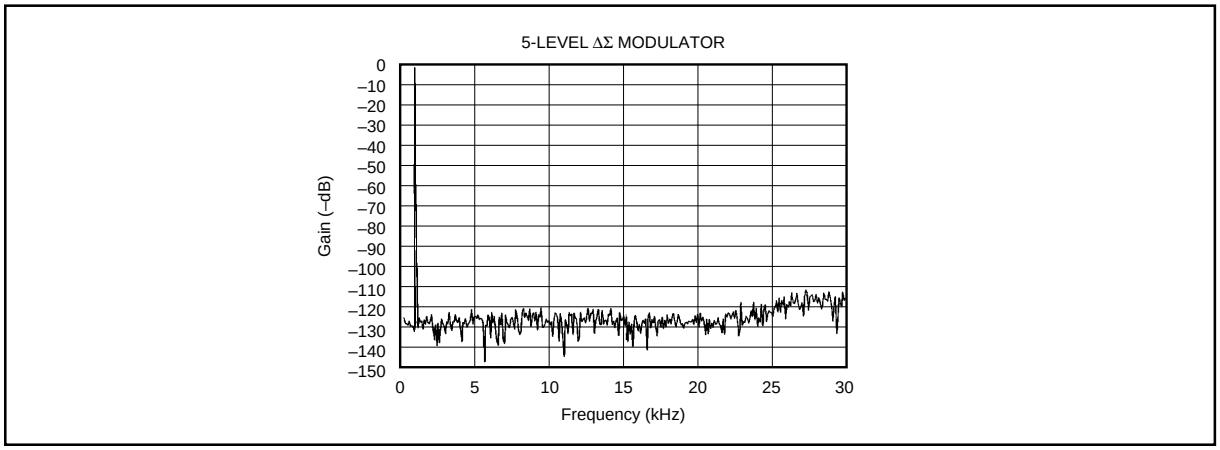


FIGURE 12. Quantization Noise Spectrum.