PM5362

TUPP-PLUS

SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR / PERFORMANCE MONITOR

DATA SHEET

ISSUE 6: MARCH 1998

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1 FEATURES

- Configurable, multi-channel, payload processor for aligning SONET virtual tributaries (VTs) or SDH tributary units (TUs) in an STS-3 or STM-1 byte serial data stream.
- Transfers all incoming tributaries in the three STS-1 synchronous payload envelopes of an STS-3 byte serial stream to the three STS-1 synchronous payload envelopes of an outgoing STS-3 byte serial stream.
- Transfers all incoming tributaries in the single AU4 or three AU3 administrative units of an STM-1 byte serial stream to the single AU4 or three AU3 administrative units of an outgoing STM-1 byte serial stream.
- Compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) payload frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, or TU11) tributary pointers.
- Configurable to process any legal mix of tributaries such as VT1.5, VT2, VT3, VT6, TU11, TU12, TU2, or TU3. Each VT group or TUG2 can be configured to carry one of four tributary types. TUG2s can be multiplexed into VC3s or TUG3s. Each TUG3 can also be configured to carry a single TU3.
- Independently configurable for AU3 or AU4 frame format on incoming and outgoing interfaces.
- Configurable to process 16-byte or 64-byte format tributary path trace messages (tributary trail trace identifiers).
- Optionally frames to the H4 byte in the path overhead to determine tributary multiframe boundaries. Inserts internally generated H4 bytes with leading logic 1 bits into the outgoing administrative units.
- Extracts and serializes the entire tributary path overhead for each tributary into lower speed serial streams.
- Extracts tributary size (SS) bits for each tributary into internal registers.
- Detects loss of pointer (LOP) and re-acquisition for each tributary and optionally generates interrupts.

- Detects tributary path alarm indication signal (AIS) and return to normal state for each tributary and optionally generates interrupts.
- Detects tributary elastic store underflow and overflow errors and optionally generates interrupts.
- Extracts tributary path trace message (trail trace identifier) for each tributary into internal buffers.
- Provides individual tributary path trace message buffer that holds the expected message and detects tributary path trace mismatch (trail trace identifier mismatch) alarms (TIM) and return to matched state for each tributary and optionally generates interrupts.
- Detects tributary path trace unstable (trail trace identifier unstable) alarms (TIU) and return to stable state for each tributary and optionally generates interrupts.
- Extracts tributary path signal label for each tributary into internal registers and detects change of tributary path signal label events (COPSL) for each tributary and optionally generates interrupts.
- Provides individual tributary path signal label register that hold the expected label and detects tributary path signal label mismatch alarms (PSLM) and return to matched state for each tributary and optionally generates interrupts.
- Detects tributary path signal label unstable alarms (PSLU) and return to stable state for each tributary and optionally generates interrupts.
- Detects tributary unequipped defect (UNEQ) and tributary path defect indication (PDI-V).
- Detects assertion and removal of tributary extended remote defect indications (RDI) for each tributary and optionally generates interrupts.
- Calculates and compares the tributary path BIP-2 error detection code for each tributary and configurable to accumulate the BIP-2 errors, on block or bit basis, in internal registers.
- Calculates and compares the TU3 path BIP-8 error detection code for each TU3 stream and accumulates the BIP-8 errors, on block or bit basis, in internal registers.

- Accumulates TU3 tributary far end block errors (FEBE) on a bit or a block basis, in internal registers.

- Allows insertion of all-zeros or all-ones tributary idle code with unequipped indication and valid pointer into any tributary under software control. Idle tributaries are identified by an output signal.

- Identifies outgoing tributaries that are in AIS state by an output signal. Allows software to force the AIS insertion on a per tributary basis.

- Inserts valid H4 byte and all-zeros fixed stuff bytes on the outgoing stream. Remaining path overhead bytes (J1, B3, C2, G1, F2, Z3, Z4, and Z5) can be configured to be set to all-zeros or to reflect the value of the corresponding POH bytes in the incoming stream.

- Inserts valid pointers, and all-zeros transport overhead bytes on the outgoing stream with valid "TeleCombus" control signals when configured to operate in locked mode.

- Supports in-band error reporting by updating the FEBE, RDI and auxiliary RDI bits in the V5 byte (G1 in TU3) with the status of the incoming stream.

- Provides low maximum tributary processing delay of 33 µs for VT1.5, 25 µs for VT2, 17 µs for VT3, and 9 µs for VT6 streams.

- Verifies parity on the IC1J1 and ISPE signals and on the incoming data stream and generates parity on the outgoing data stream.

- May be used for multiframe synchronization or ring closure at the head-end node of a SONET/SDH ring.

- Operates in conjunction with the PM5344 SPTX SONET/SDH Path Terminating Transceiver to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect. Provides backwards compatibility with the PM5361 TUPP SONET/SDH Tributary Unit Payload Processor.

- Independently configurable incoming and outgoing interfaces that operate in byte interface mode from a single 19.44 MHz clock or in nibble interface mode from a single 38.88 MHz clock.

- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a standard 5 signal IEEE P1149.1 JTAG test port for boundary scan test purposes.
- Low power, +5 Volt, CMOS technology, TTL compatible inputs and outputs.
- 160 pin plastic quad flat pack (PQFP) package

2 APPLICATIONS

- SONET/SDH Wideband Cross-Connect
- SONET/SDH Add-Drop Multiplexer

3 REFERENCES

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3. Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.

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5. Committee T1 Contribution, "Proposed ITU-T Contribution on Enhanced Path RDI for SDH", T1X1.5/94-117, 1994.

6. ITU, Recommendation G.708 - "Network Node Interface For The Synchronous Digital Hierarchy", 1993.

7. ITU, Recommendation G.709 - "Synchronous Multiplexing Structure", 1993.

8. ITU, Recommendation G.782 - "Types and general characteristics of synchronous digital hierarchy (SDH) equipment", 1990.

9. ITU, Recommendation G.783 - "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks", 1990.

10. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 2, December 1991.

11. Bell Communications Research - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 1, December 1994.

12. Bell Communications Research - SONET Add-Drop Multiplex Equipment (SONET ADM) Generic Criteria, TR-NWT-000496, Issue 3, May 1992.

13. Bell Communications Research - SONET Dual-Fed Unidirectional Path Switched Ring (UPSR) Equipment Generic Criteria, GR-1400-CORE, Issue 1, March 1994.

14. European Telecommunications Standards Institute, Transmission and Multiplexing (TM); Generic Functional Requirements for SDH Transmission Equipment, Part 1, Generic Process and Performance, prETS 300 417-1-1, June 1995.

4 DESCRIPTION

The PM5362 TUPP-PLUS SONET/SDH Tributary Unit Payload Processor / Performance Monitor is a monolithic integrated circuit that implements a configurable, multi-channel, payload processor that aligns and monitors performance of SONET virtual tributaries (VTs) or SDH tributary units (TUs.).

When configured for SONET compatible operation, the TUPP-PLUS transfers all tributaries in the three STS-1 synchronous payload envelopes of an incoming STS-3 byte serial stream to the three STS-1 synchronous payload envelopes of an outgoing STS-3 byte serial stream. Similarly, when configured for SDH compatible operation, the TUPP-PLUS transfers all tributaries in the single AU4 or three AU3 administrative units of an incoming STM-1 byte serial stream to a single AU4 or three AU3 administrative units of an outgoing STM-1 byte serial stream. The TUPP-PLUS compensates for pleisiochronous relationships between incoming and outgoing higher level (STS-1, AU4, AU3) synchronous payload envelope frame rates through processing of the lower level (VT6, VT3, VT2, VT1.5, TU3, TU2, TU12, TU11) tributary pointers.

The TUPP-PLUS is configurable to process any legal mix of tributaries. Each VT group can be configured to carry any one of the four tributary types (VT1.5, VT2, VT3, or VT6) and each TUG2 can be configured to carry any one of three tributary types (TU11, TU12, or TU2). TUG2s can be multiplexed into a VC3 or a TUG3. Alternatively, each TUG3 can be configured to carry a TU3.

The TUPP-PLUS operates in conjunction with the PM5344 SONET/SDH Path Terminating Transceiver to align tributaries such that they can be switched by the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect.

The TUPP-PLUS provides useful maintenance functions. They include, for each tributary, detection of loss of pointer, detection of AIS alarm, detection of tributary path signal label mismatch and unstable alarms, detection of tributary path trace mismatch and unstable alarms. Optionally, interrupts can be generated due to the assertion and removal of any of the above alarm conditions. The TUPP-PLUS counts received tributary path BIP-2 (BIP-8 for TU3) errors on a block or bit basis and counts FEBE indications. The TUPP-PLUS also allows insertion of tributary path AIS as a consequence of any of the above alarm conditions. In addition, the TUPP-PLUS may insert tributary idle (unequipped) into any tributary. Incoming tributary path trace messages and path signal labels are stored in a set of microprocessor accessible registers. The TUPP-PLUS can

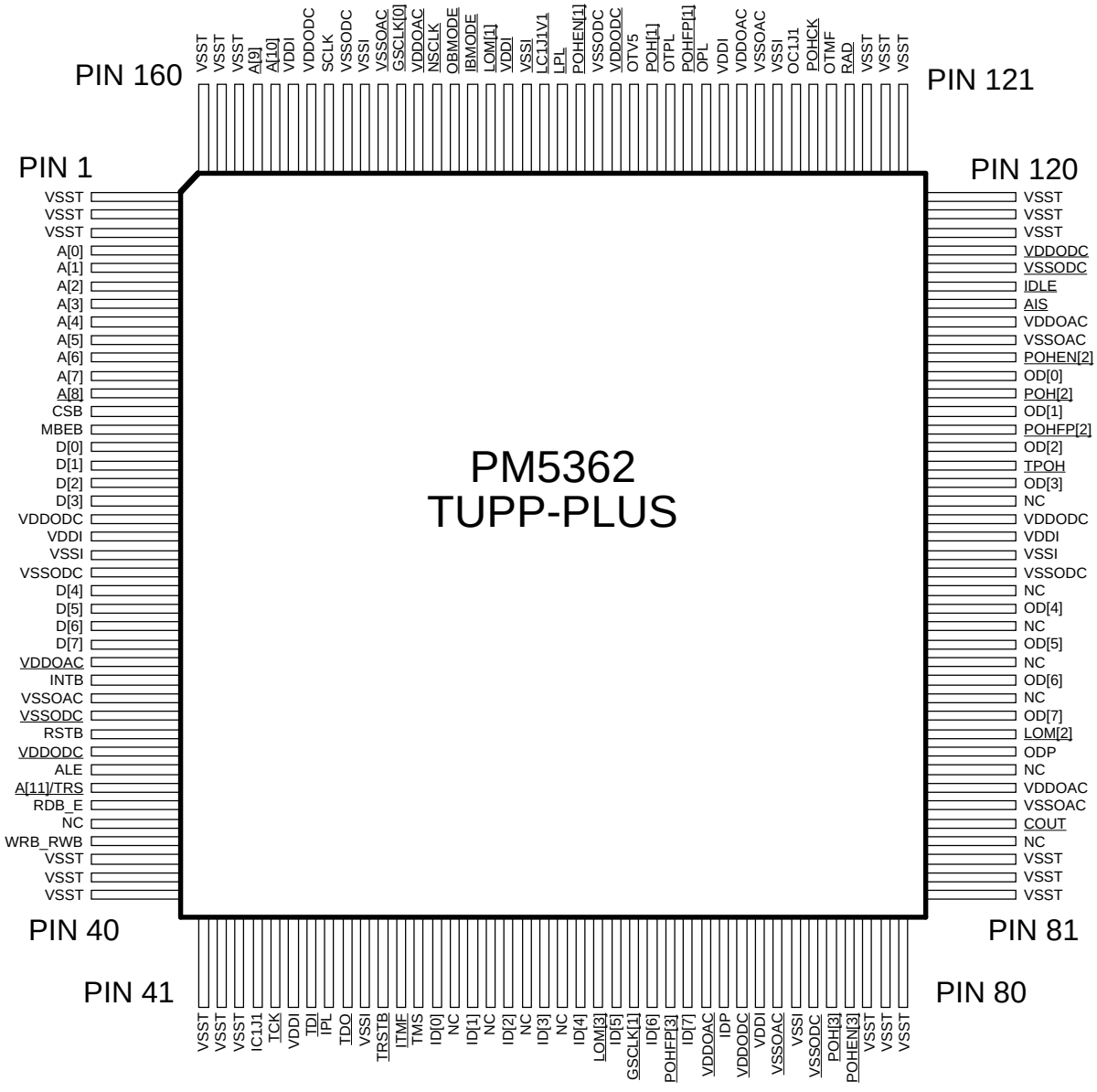
also insert inverted new data flag fields that can be used to diagnose downstream pointer processing elements.

No auxiliary high speed clocks are required as the TUPP-PLUS operates from either a single 19.44 MHz or a single 38.88 MHz line rate clock. The TUPP-PLUS is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

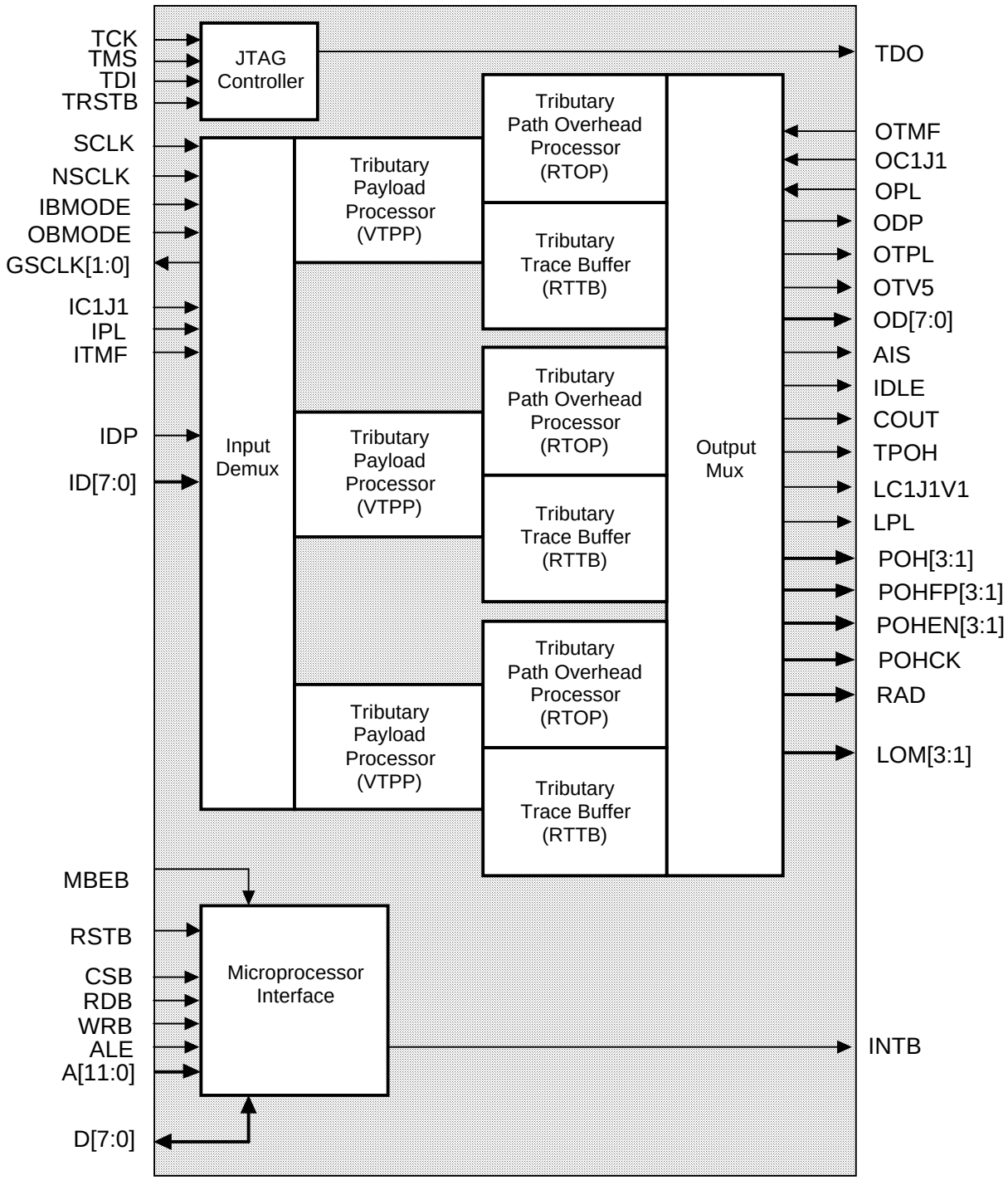
The TUPP-PLUS is implemented in low power, +5 Volt, CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 160 pin HPPQFP package.

5 PIN DIAGRAM

The TUPP-PLUS is packaged in an 160 pin PQFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.65 mm. Pins added since the PM5361-TUPP are underlined.



6 BLOCK DIAGRAM



7 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
SCLK/	Input	153	The system clock (SCLK) provides timing for TUPP-PLUS internal operations. SCLK is a 19.44 MHz, nominally 50% duty cycle, clock. When either incoming interface is in nibble mode (IBMODE set low) or the outgoing interface is in nibble mode (OBMODE set low), SCLK must be connected to GSCLK[0] externally. In incoming byte interface mode (IBMODE set high), IC1J1, IPL, ITMF, IDP, ID[7:0], OTMF, OC1J1 and OPL are sampled on the rising edge of SCLK. In outgoing byte interface mode (OBMODE set high), ODP, OTPL, OTV5, OD[7:0], AIS, IDLE, TPOH, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of SCLK.
VCLK			The test vector clock (VCLK) signal is used during TUPP-PLUS production testing to verify manufacture.

Pin Name	Type	Pin No.	Function
NSCLK	Input	147	The nibble interface mode system clock (NSCLK) provides timing for TUPP-PLUS internal operations in incoming or outgoing nibble interface mode (IBMODE or OBMODE set low). NSCLK is a 38.88 MHz, nominally 50% duty cycle, clock. In incoming nibble interface mode (IBMODE set low), IC1J1, IPL, ITMF, IDP, ID[3:0] are sampled on the rising edge of NSCLK. In outgoing nibble interface mode (OBMODE set low), OTMF, OC1J1 and OPL are sampled on the rising edge of NSCLK, and ODP, OTPL, OTV5, OD[7:0], AIS, IDLE, TPOH, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of NSCLK. When the incoming and the outgoing interfaces are in byte mode (IBMODE and OBMODE both set high), NSCLK may be left unconnected. NSCLK has an integral pull-up resistor.
IBMODE	Input	145	The incoming byte interface mode signal (IBMODE) configures the incoming interface mode of the TUPP-PLUS. When IBMODE is set low, nibble interface mode is selected. SCLK must be connected to GSCLK[0]. IC1J1, IPL, ITMF, IDP, ID[3:0] are sampled on the rising edge of NSCLK. When IBMODE is set high, byte interface mode is selected. IC1J1, IPL, ITMF, IDP, ID[7:0] are sampled on the rising edge of SCLK. IBMODE has an integral pull-up resister.

Pin Name	Type	Pin No.	Function
OBMODE	Input	146	The outgoing byte interface mode signal (OBMODE) configures the outgoing interface mode of the TUPP-PLUS. When OBMODE is set low, nibble interface mode is selected. SCLK must be connected to GSCLK[0]. OTMF, OC1J1 and OPL are sampled on the rising edge of NSCLK. ODP, OTPL, OTV5, OD[3:0], AIS, IDLE, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of NSCLK. When OBMODE is set high, byte interface mode is selected. OTMF, OC1J1 and OPL are sampled on the rising edge of SCLK. ODP, OTPL, OTV5, OD[7:0], AIS, IDLE, LC1J1V1, LPL, and LOM[3:1] are updated on the rising edge of SCLK. OBMODE has an integral pull-up resister.
GSCLK[1] GSCLK[0]	Output	65 149	The generated system clock (GSCLK[1:0]) signals provide timing for the TUPP-PLUS when nibble mode is selected at the incoming or outgoing interface (IBMODE or OBMODE set low). GSCLK[1:0] are a divide by two of NSCLK. GSCLK[0] must only be connected to SCLK externally when IBMODE or OBMODE is set low. GSCLK[1] is a exact replica of GSCLK[0] and can be used to supply timing to external devices that are operating in byte mode. GSCLK[1:0] are updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
IC1J1	Input	44	The input C1/J1 frame pulse (IC1J1) identifies the transport envelope and synchronous payload envelope frame boundaries on the incoming stream. In incoming byte interface mode (IBMODE set high), IC1J1 is set high while IPL is low to mark the first C1 byte of the transport envelope frame on the ID[7:0] bus. IC1J1 is set high while IPL is high to mark each J1 byte of the synchronous payload envelope(s) on the ID[7:0] bus. IC1J1 must be present at every occurrence of the first C1 and all J1 bytes. The TUPP-PLUS will ignore a pulse on IC1J1 at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1 is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), IC1J1 is set high while IPL is low to mark the more significant nibble of the first C1 byte of the transport envelope frame on the ID[3:0] bus. IC1J1 is set high while IPL is high to mark the more significant nibble of each J1 byte of the synchronous payload envelope(s) on the ID[3:0] bus. IC1J1 must be present at every occurrence of the first C1 and all J1 bytes. The TUPP-PLUS will ignore a pulse on IC1J1 at the byte position of the V1 byte of the first tributary of each VC3 or the top byte of the first fixed stuff column of each TUG3. IC1J1 must be set low during the less significant nibble timeslots. IC1J1 is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
IPL	Input	48	The active high incoming payload active (IPL) signal identifies the bytes within the transport envelope frame on the incoming stream that carry the VC3 or VC4 virtual containers, or the STS-1 synchronous payload envelopes. In incoming byte interface mode (IBMODE set high), IPL must be brought high to mark each payload byte on ID[7:0]. IPL is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), IPL must be brought high to mark the more significant nibble of each payload byte on ID[3:0]. IPL is ignored during the less significant nibble timeslots. IPL is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
ITMF	Input	52	The active high incoming tributary multiframe (ITMF) signal identifies the first frame of the tributary multiframe for each STS-1 synchronous payload envelope, AU3, or AU4 administrative unit. ITMF is enabled by the setting the ITMFEN register bit high. When ITMFEN bit is low, the path overhead H4 byte is used to determine tributary multiframe boundaries. ITMF is selectable to pulse high during the third byte after J1 of the first tributary or during the H4 byte which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking each H4 or the third byte after each J1 is controlled by the ITMFH4 register bit. Pulses on ITMF are only effective during the H4 or third byte after each J1 byte positions, as appropriate. ITMF is ignored at other byte positions. In incoming byte interface mode (IBMODE set high), ITMF is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), ITMF marks the more significant nibble of H4 or the third byte after J1, as appropriate. It is ignored at the less significant nibble timeslots. ITMF is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
IDP	Input	70	The incoming data parity (IDP) signal carries the parity of the incoming signals. In incoming byte interface mode (IBMODE set high), the parity calculation encompasses the ID[7:0] bus and optionally the IC1J1 and the IPL signals. IC1J1 and IPL can be included in the parity calculation by setting the INCC1J1 and INCPL register bits high, respectively. Odd parity is selected by setting the IOP register bit high, and even parity is selected by setting the IOP bit low. IDP is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), The parity calculation encompasses the ID[3:0] bus and optionally the IC1J1 and the IPL signals. IC1J1 and IPL can be included in the parity calculation by setting the INCC1J1 and INCPL register bits high, respectively. Odd parity is selected by setting the IOP register bit high, and even parity is selected by setting the IOP bit low. IDP is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
ID[0] ID[1] ID[2] ID[3] ID[4] ID[5] ID[6] ID[7]	Input	54 56 58 60 62 64 66 68	The incoming data bus (ID[7:0]) carries SONET/SDH frame data in byte serial format. In incoming byte interface mode (IBMODE set high), ID[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. ID[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. The ID[7:0] bus is sampled on the rising edge of SCLK. In incoming nibble interface mode (IBMODE set low), ID[3] is the most significant bit of each nibble, corresponding to bit 1 or bit 5 of each serial word, the bit transmitted first and fifth, respectively. ID[0] is the least significant bit of each nibble, corresponding to bit 4 or bit 8 of each serial word, the fourth or last bit transmitted, respectively. ID[7:4] is ignored. The ID[3:0] bus is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
OC1J1	Input	127	The outgoing composite frame pulse (OC1J1) marks the transport frame and synchronous payload envelope frame boundaries on the outgoing stream. In outgoing byte interface mode (OBMODE set high), and the OJ1EN register bit is set low, OC1J1 pulses high to mark the first C1 byte of the transport envelope frame on the OD[7:0] bus. The OPL input must be held low. The position of the J1 byte(s) is implicit and fixed to the bytes immediately following the last C1 byte. When the OJ1EN register bit is set high, the OC1J1 signal pulses high while OPL is low to mark the first C1 byte of the transport frame on the OD[7:0] bus and pulses high while OPL is high to mark each of the J1 bytes of the synchronous payload envelope(s) on the OD[7:0] bus. OC1J1 must be present at every occurrence of the first C1 byte and all J1 bytes. A V1 pulse added to the OC1J1 input will be ignored by the TUPP-PLUS. OC1J1 is sampled on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), and the OJ1EN register bit is set low, OC1J1 pulses high to mark the more significant nibble of the first C1 byte of the transport envelope frame on the OD[3:0] bus. The OPL input must be held low. The position of the J1 byte(s) is implicit and fixed to the bytes immediately following the last C1 byte. When the OJ1EN register bit is set high, the OC1J1 signal pulses high while OPL is low to mark the more significant nibble of the first C1 byte of the transport frame on the OD[3:0] bus and pulses high while OPL is high to mark each of the J1 bytes of the synchronous payload envelope(s) on the OD[3:0] bus. OC1J1 must be present at every occurrence of the first C1 byte and all J1 bytes. A V1 pulse added to the OC1J1 input will be ignored by the TUPP-PLUS. OC1J1 must be set low during the less significant nibble timeslots. OC1J1 is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
OTMF	Input	125	The active high outgoing tributary multiframe (OTMF) signal identifies the first frame of the tributary multiframe for each AU3, or AU4 administrative unit, or STS-1 synchronous payload envelope. OTMF is selectable to pulse high during the third byte after J1 of the first tributary or during the H4 byte of the path overhead which indicates that the next frame is the first frame of the tributary multiframe. Selection between marking the third byte after each J1 or H4 bytes is controlled by the OTMFH4 bit. Pulses on OTMF are only effective during the H4 or third byte after each J1 byte positions, as appropriate. OTMF is ignored at other byte positions. In outgoing byte interface mode (OBMODE set high), OTMF is sampled on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), OTMF is ignored at the less significant nibble timeslots. OTMF is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
COUT	Output	85	The controlled output signal (COUT) is a software programmable output that is controlled by the COUTx register bit associated with each tributary. In outgoing byte interface mode (OBMODE set high), COUT is synchronized to the OD[7:0] bus. In floating mode, COUT contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, COUT is set low for transport overhead bytes. COUT is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), COUT is synchronized to the OD[3:0] bus. In floating mode, COUT contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, COUT is set low for transport overhead bytes. COUT is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
OPL	Input	132	The active high outgoing payload active (OPL) signal identifies the bytes within the transport envelope frame on the OD[7:0] bus that carry the VC3 or VC4 virtual container(s), and the STS-1 synchronous payload envelopes. In outgoing byte interface mode (OBMODE set high), and floating mode is enabled, OPL must be set high to mark each payload byte. OD[7:0], OTPL, OTV5, AIS and IDLE contain valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Their contents should be ignored for bytes in the transport overhead as indicated by a low level on the OPL input. In locked mode, the outgoing virtual container (synchronous payload envelope) is locked with the J1 byte immediately following the C1 byte and OPL should be held low. During transport overhead byte locations on the outgoing stream, OTPL, OTV5, AIS and IDLE are set low. OD[7:0] is set to a valid pointer with offset of 522 and all-zeros for other transport overhead bytes. OPL is sampled on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), and floating mode is enabled, OPL must be set high to mark the more significant nibble of each payload byte. OPL is ignored during the less significant nibble. OD[3:0], OTPL, OTV5, AIS and IDLE contain valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Their contents should be ignored for bytes in the transport overhead as indicated by a low level on the OPL input. In locked mode, the outgoing virtual container (synchronous payload envelope) is locked with the J1 byte immediately following the C1 byte and OPL should be held low. During transport overhead byte locations on the outgoing stream, OTPL, OTV5, AIS and IDLE are set low. OD[3:0] is set to a valid pointer with offset of 522 and all-zeros for other transport overhead bytes. OPL is ignored during the less significant nibble timeslots. OPL is sampled on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
OD[0] OD[1] OD[2] OD[3] OD[4] OD[5] OD[6] OD[7]	Output	110 108 106 104 97 95 93 91	The outgoing data bus (OD[7:0]) carries SONET/SDH frame data in byte serial format. In outgoing byte interface mode (OBMODE set high), OD[7] is the most significant bit, corresponding to bit 1 of each serial word, the bit transmitted first. OD[0] is the least significant bit, corresponding to bit 8 of each serial word, the last bit transmitted. In floating mode, OD[7:0] contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OD[7:0] is set to all-zeros at transport overhead bytes, except for a valid pointer with offset 522 at H1, H2 bytes. The OD[7:0] bus is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), OD[3] is the most significant bit of each nibble, corresponding to bit 1 or bit 5 of each serial word, the bit transmitted first or fifth, respectively. OD[0] is the least significant bit, corresponding to bit 4 or bit 8 of each serial word, the fourth or last bit transmitted, respectively. OD[7:4] are set low. In floating mode, OD[3:0] contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OD[3:0] is set to all-zeros at transport overhead bytes, except for a valid pointer with offset 522 at H1, H2 bytes. The OD[7:0] bus is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
ODP	Output	89	The outgoing data parity (ODP) signal carries the parity of the outgoing data stream, OD[7:0]. Odd parity is selected by setting the OOP register bit high, and even parity is selected by setting the OOP bit low. ODP is updated on the rising of SCLK in outgoing byte interface mode (OBMODE set high) and on the rising edge of NSCLK in outgoing nibble interface mode (OBMODE set low).
OTPL	Output	134	The outgoing tributary payload active (OTPL) signal marks the bytes carrying the tributary payload. In outgoing byte interface mode (OBMODE set high), OTPL is set high to mark each tributary payload byte on the OD[7:0] bus. In floating mode, OTPL contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OTPL is set low for transport overhead. OTPL is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), OTPL is set high to mark each tributary payload byte on the OD[3:0] bus. In floating mode, OTPL contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OTPL is set low for transport overhead. OTPL is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
OTV5	Output	136	The outgoing tributary V5 byte (OTV5) signal marks the various tributary V5 bytes. In outgoing byte interface mode (OBMODE set high), OTV5 is set high to mark each tributary V5 byte on the OD[7:0] bus. When the outgoing tributary is a TU3, OTV5 marks the J1 byte of the TU3. In floating mode, OTV5 contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OTV5 is set low for transport overhead bytes. OTV5 is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), OTV5 is set high to mark each tributary V5 byte on the OD[3:0] bus. When the outgoing tributary is a TU3, OTV5 marks the J1 byte of the TU3. In floating mode, OTV5 contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, OTV5 is set low for transport overhead bytes. OTV5 is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
AIS	Output	114	The tributary alarm indication signal output (AIS) marks tributaries on the outgoing stream that are in AIS state. In outgoing byte interface mode (OBMODE set high), AIS is set high when AIS is inserted in the associated tributary on the OD[7:0] and is set low when the AIS is not inserted. In floating mode, AIS contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its value should be ignored for bytes in the transport overhead. In locked mode, AIS is set low for transport overhead bytes. AIS is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), AIS is set high when AIS is inserted in the associated tributary on the OD[3:0] and is set low when the AIS is not inserted. In floating mode, AIS contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its value should be ignored for bytes in the transport overhead. In locked mode, AIS is set low for transport overhead bytes. AIS is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
IDLE	Output	115	The tributary idle indication signal output (IDLE) marks tributaries on the outgoing stream that are in idle state. In outgoing byte interface mode (OBMODE set high), IDLE is set high when idle code is inserted in the associated tributary on the OD[7:0] and is set low when the idle code is not inserted. In floating mode, IDLE contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its value should be ignored for bytes in the transport overhead. In locked mode, IDLE is set low for transport overhead bytes. IDLE is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), IDLE is set high when idle code is inserted in the associated tributary on the OD[3:0] and is set low when the idle code is not inserted. In floating mode, IDLE contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its value should be ignored for bytes in the transport overhead. In locked mode, IDLE is set low for transport overhead bytes. IDLE is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
TPOH	Output	105	The outgoing tributary path overhead byte (OTV5) signal marks the tributary path overhead bytes in the outgoing stream. For streams in TU3 mode, the J1, B3,C2, G1, F2, H4, Z3, Z4 and Z5 bytes are marked. For streams out of TU3 mode, V5, J2, Z6 an Z7 bytes are marked. In outgoing byte interface mode (OBMODE set high), TPOH is set high to mark each tributary path overhead byte on the OD[7:0] bus. In floating mode, TPOH contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, TPOH is set low for transport overhead bytes. TPOH is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), TPOH is set high to mark each tributary path overhead byte on the OD[3:0] bus. In floating mode, TPOH contains valid data only for bytes in the VC3 or VC4 virtual container(s), or the STS-1 synchronous payload envelopes. Its contents should be ignored for bytes in the transport overhead. In locked mode, TPOH is set low for transport overhead bytes. TPOH is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
LOM[3] LOM[2] LOM[1]	Output	63 90 144	The loss of multiframe signals (LOM[3:1]) reports the tributary multiframe synchronization status. LOM is set low when a correct sequence on the H4 byte has been detected for four frames. LOM is set high if a correct four frame sequence is not detected in 1 millisecond. LOM[3], LOM[2] and LOM[1] report the synchronization status of STS-1 #1, #2 and #3, respectively. In AU4 mode, LOM[3], LOM[2] and LOM[1] report the synchronization status of TUG3 #1, #2 and #3, respectively. LOM[3:1] are updated on the rising edge of SCLK.

Pin Name	Type	Pin No.	Function
LC1J1V1	Output	141	The locked mode composite frame pulse (LC1J1V1) marks the transport, synchronous payload envelope and tributary multiframe frame boundaries on the outgoing stream. LC1J1V1 is only active in locked mode (OJ1EN register bit set low). LC1J1V1 is held low in floating mode (OJ1EN set high). In outgoing byte interface mode (OBMODE set high), and locked mode is enabled (OJ1EN set low), LC1J1V1 pulses high to mark the first C1 byte of the transport envelope frame on the OD[7:0] bus. It also pulses high to mark the J1 byte(s) which is (are) register selectable to be implicitly fixed to immediately follow the C1 bytes or the H3 bytes. Optionally, LC1J1V1 also marks the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the LV1EN register bit is set high. LC1J1V1 is updated on the rising edge of SCLK. In outgoing nibble interface mode (OBMODE set low), and locked mode is enabled (OJ1EN set low), LC1J1V1 pulses high to mark the more significant nibble of the first C1 byte of the transport envelope frame on the OD[3:0] bus. It also pulses high to mark the more significant nibble of the J1 byte(s) which is (are) register selectable to be implicitly fixed to immediately follow the C1 bytes or the H3 bytes. Optionally, LC1J1V1 also marks the more significant nibble of the third byte after J1 of the first tributary in each STS-1 (TUG3) stream when the LV1EN register bit is set high. LC1J1V1 is updated on the rising edge of NSCLK.

Pin Name	Type	Pin No.	Function
LPL	Output	140	The locked mode payload active signal (LPL) identifies synchronous payload envelope bytes on the outgoing stream. LPL is only active in locked mode (OJ1EN register bit set low). LPL is held low in floating mode (OJ1EN set high). If locked mode is enabled (OJ1EN set low), LPL is set high to mark synchronous payload envelop bytes and set low to mark transport overhead bytes. LPL is updated on the rising edge of SCLK in outgoing byte interface mode (OBMODE set high) or on the rising edge of NSCLK in outgoing nibble interface mode (OBMODE set low).
POHCK	Output	126	The tributary path overhead clock signal (POHCK) provides timing to sample the extracted tributary path overhead stream and the receive alarm port. POHCK is nominally 9.72 MHz clock signals. The POH[3:1], POHEN[3:1], POHFP[3:1] and RAD outputs are updated on the falling edge of POHCK.
POH[3] POH[2] POH[1]	Output	76 109 135	The tributary path overhead signals (POH[3:1]) contains the tributary path overhead bytes (V5, J2, Z6 and Z7) extracted from the ID[7:0] bus. POH[3], POH[2] and POH[1] contain the tributary path overhead bytes from STS-1 #1, #2 and #3, respectively. In AU4 mode, POH[3], POH[2] and POH[1] contain the tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. All four tributary overhead bytes of each tributary is shifted out once per payload frame. The corresponding POHEN signal is set high to identify overhead bytes that are presented for the first time. Each POH signal is updated on the falling edge of POHCK.

Pin Name	Type	Pin No.	Function
POHFP[3] POHFP[2] POHFP[1]	Output	67 107 133	The tributary path overhead frame pulse signals (POHFP[3:1]) may be used to locate the individual path overhead bits of each tributary for the corresponding STS-1 (TUG3) stream. Each POHFP signal is set high to mark bit 1 (the most significant bit) of the V5 byte of the first tributary. POHFP[3], POHFP[2] and POHFP[1] identify frame boundaries of the tributary path overhead bytes from STS-1 #1, #2 and #3, respectively. In AU4 mode, POHFP[3], POHFP[2] and POHFP[1] identify frame boundaries of TUG3 #1, #2 and #3, respectively. Each POHFP signal is updated on the falling edge of POHCK.
POHEN[3] POHEN[2] POHEN[1]	Output	77 111 139	The tributary path overhead enable signals (POHEN[3:1]) may be used to identify tributary path overhead bytes that are being presented on the corresponding POH stream for the first time. Each POHEN signal is set high when a fresh overhead byte is available on the corresponding POH stream. POHEN is set low when the tributary path overhead byte available on the corresponding POH stream has already been shifted out in a previous frame. POHEN[3], POHEN[2] and POHEN[1] identify the status of tributary path overhead bytes from STS-1 #1, #2 and #3, respectively. In AU4 mode, POHFP[3], POHFP[2] and POHFP[1] identify the status of tributary path overhead bytes from TUG3 #1, #2 and #3, respectively. Each POHEN signal is updated on the falling edge of POHCK.
RAD	Output	124	The receive alarm port (RAD) contains the tributary path BIP error count, the RDI status and the PDI status of each tributary in the ID[7:0] bus. RAD is updated on the falling edge of POHCK.

Pin Name	Type	Pin No.	Function
MBEB	Input	14	The active low Motorola bus enable (MBEB) signal configures the TUPP-PLUS for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the TUPP-PLUS is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
CSB	Input	13	The active low chip select (CSB) signal is low during TUPP-PLUS register accesses. If CSB is not required (i.e., register accesses are controlled by using the RDB/E and WRB/RWB signals only), CSB must be connected to an inverted version of RSTB.
RDB/ E	Input	35	The active low read enable (RDB) signal is low during TUPP-PLUS register read accesses while in Intel bus mode. The TUPP-PLUS drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. The active high external access (E) signal is high during TUPP-PLUS register access while in Motorola bus mode.
WRB/ RWB	Input	37	The active low write strobe (WRB) signal is low during a TUPP-PLUS register write accesses while in Intel bus mode. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. The read/write select (RWB) signal selects between TUPP-PLUS register read and write accesses while in Motorola bus mode. The TUPP-PLUS drives the D[7:0] bus with the contents of the addressed register while CSB is low and RWB and E are high. The D[7:0] bus contents are clocked into the addressed register on the falling E edge while CSB and RWB are low.

Pin Name	Type	Pin No.	Function
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	15 16 17 18 23 24 25 26	The bidirectional data bus D[7:0] is used during TUPP-PLUS register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	4 5 6 7 8 9 10 11 12 157 156	The address bus A[11:0] selects specific registers during TUPP-PLUS register accesses.
A[11]/TRS		34	The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input	31	The active low reset (RSTB) signal provides an asynchronous TUPP-PLUS reset. RSTB is a Schmitt triggered input with an integral pull up resistor.

Pin Name	Type	Pin No.	Function
ALE	Input	33	The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the TUPP-PLUS to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	OD Output	28	The active low interrupt (INTB) signal goes low when a TUPP-PLUS interrupt source is active. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
TCK	Input	45	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. TCK has an integral pull up resistor.
TMS	Input	53	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	47	The test data input (TDI) signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate	49	The test data output (TDO) signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output that is always tristated except when scanning of data is in progress.
TRSTB	Input	51	The active low test reset (TRSTB) signal provides an asynchronous test access port reset. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence.

Pin Name	Type	Pin No.	Function
VDDI1 VDDI2 VDDI3 VDDI4 VDDI5 VDDI6 VDDI7	Power	20 46 72 101 131 143 155	The core power (VDDI1 - VDDI7) pins should be connected to a well decoupled +5 V DC in common with VDDOAC and VDDODC.
VSSI1 VSSI2 VSSI3 VSSI4 VSSI5 VSSI6 VSSI7	Ground	21 50 74 100 128 142 151	The core ground (VSSI1 - VSSI7) pins should be connected to GND in common with VSSOAC and VSSODC.
VDDOAC1 VDDOAC2 VDDOAC3 VDDOAC4 VDDOAC5 VDDOAC6	Power	27 69 87 113 130 148	The pad ring switching power (VDDOAC1 - VDDOAC6) pins should be connected to a well decoupled +5 V DC in common with VDDI and VDDODC.
VSSOAC1 VSSOAC2 VSSOAC3 VSSOAC4 VSSOAC5 VSSOAC6	Ground	29 73 86 112 129 150	The pad ring ground (VSSOAC1 - VSSOAC6) pins should be connected to GND in common with VSSI and VSSODC

Pin Name	Type	Pin No.	Function
VDDODC1 VDDODC2 VDDODC3 VDDODC4 VDDODC5 VDDODC6 VDDODC7	Power	19 32 71 102 117 137 154	The pad ring static power (VDDODC1 - VDDODC7) pins should be connected to a well decoupled +5 V DC in common with VDDI and VDDOAC.
VSSODC1 VSSODC2 VSSODC3 VSSODC4 VSSODC5 VSSODC6 VSSODC7	Ground	22 30 75 99 116 138 152	The pad ring ground (VSSODC1 - VSSODC7) pins should be connected to GND in common with VSSI and VSSOAC.

Pin Name	Type	Pin No.	Function
VSST1	Ground	1	The thermal ground (VSST1 - VSST24) pins should be connected to GND in common with VSSI and VSSOAC.
VSST2		2	
VSST3		3	
VSST4		38	
VSST5		39	
VSST6		40	
VSST7		41	
VSST8		42	
VSST9		43	
VSST10		78	
VSST11		79	
VSST12		80	
VSST13		81	
VSST14		82	
VSST15		83	
VSST16		118	
VSST17		119	
VSST18		120	
VSST19		121	
VSST20		122	
VSST21		123	
VSST22		158	
VSST23		159	
VSST24		160	

Notes on Pin Description:

1. All TUPP-PLUS inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

2. All TUPP-PLUS digital outputs and bidirectionals have 4 mA drive capability, except the INTB open drain output, the D[7:0] bidirectionals, the POHCK output and the GSCLK[1] output have 8 mA drive capability.

3. The VSSOAC ground pins are not internally connected to the VSSODC nor the VSSI ground pins. Failure to connect these pins externally may cause malfunction or damage the TUPP-PLUS. The VSSODC and the VSSI ground pins are internally connected.

4. The VDDOAC power pins are not internally connected to the VDDODC nor the VDDI power pins. Failure to connect these pins externally may cause malfunction or damage the TUPP-PLUS. The VDDODC and the VDDI power pins are internally connected.

5. Pin numbers that are underlined are additions to the TUPP-PLUS that were no-connects in the TUPP (PM5361).

8 FUNCTIONAL DESCRIPTION

8.1 Input Bus Demultiplexer

The input bus demultiplexer captures data sampled on the ID[7:0] bus and distributes this data to the three tributary payload processors within the TUPP-PLUS.

The input bus demultiplexer also provides timing signals for the other blocks within the TUPP-PLUS. Frame alignment signals for the incoming data stream, IC1J1, ITMF, and IPL, are sampled, buffered and distributed to the tributary payload processors (VTPPs). In order to have synchronous operation of the VTPPs with a single clock, the incoming data and control signals may be delayed by up to two system clock cycles before distribution to the VTPPs. The delay is used to align the incoming data with the outgoing data at each VTPP. The amount of delay is adjusted such that the separation of the incoming STS/AU frame and the outgoing frame at each VTPP appears to be in multiples of three SCLK or six NSCLK periods.

When configured for AU4 mode, the input bus demultiplexer provides the necessary timing coordination between the three tributary payload processors. The single J1 byte marker input on IC1J1 is retimed and distributed to each of the three tributary payload processors. The tributary multiframe detected by VTPP #1 is distributed to the two other VTPPs, as VTPP #1 is the only one receiving a valid H4 byte.

8.2 Output Bus Multiplexer

The output bus multiplexer gathers payload data from the three tributary payload processors within the TUPP-PLUS and multiplexes this data onto the OD[7:0] bus. It also multiplexes signals from each tributary payload processor that mark tributary SPEs and tributary V5 bytes onto the shared OTPL and OTV5 signals. The extracted tributary path overhead serial signals (POH[3:1], POHFP[3:1], POHEN[3:1], POHCK[3:1] and RAD) are buffered by the output bus multiplexer block.

The output bus multiplexer also provides timing signals for other blocks within the TUPP-PLUS. Frame alignment signals for the outgoing data stream, OC1J1, OPL and OTMF, are sampled, buffered and distributed to the tributary payload processors (VTPPs), the tributary path overhead processors (RTOPs) and the

tributary trace buffers (RTTBs). The output bus multiplexer contains a four frame counter that will flywheel in the absence of an active OTMF input, internally generating tributary multiframe timing for the outgoing data stream. When configured for locked output mode, i.e. when OJ1EN is low, the output bus multiplexer will internally generate J1 and SPE timing for the outgoing data stream that corresponds to the J1 bytes following the C1 bytes and no pointer justifications at the STS-1 (AU3) or AU4 level. The locked transport and payload frame boundaries are reported on the LC1J1V1 and LPL outputs. This timing drives the outputs of the three VTPPs, RTOPs and RTTBs, substituting for the function otherwise provided by the OC1J1 and OPL inputs.

When configured for AU4 mode, the output bus multiplexer provides the necessary timing coordination between the three tributary payload processors. This consists of deriving VC4 framing from the single J1 byte marker input on OC1J1 and distributing this to each VTPP, RTOP and RTTB blocks.

8.3 Tributary Payload Processor

Each tributary payload processor (VTPP) processes the tributaries within an STS-1, AU3, or TUG3. Each VTPP can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each VTPP ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or equivalently all TU11s).

8.3.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary payload processor. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary payload processor.

8.3.2 Incoming Timing Generator

The incoming timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the VTPP (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The H4 byte is identified for the

incoming multiframe detector so that it can determine the incoming tributary multiframe boundaries. The identification of specific tributaries allows the pointer interpreter to be time-sliced across the mix of tributaries present in the incoming data stream. The identification of the V1-V3 bytes of VTs, or TUs (or H1-H3 bytes in the case of TU3s) allows the pointer interpreter to function.

8.3.3 Incoming Multiframe Detector

The multiframe alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, 11 in the two least significant bits. If an unexpected value is detected, the primary multiframe will be kept, and a second multiframe process will, in parallel, check for a phase shift. The primary process will enter out of multiframe state (OOM). A new multiframe alignment is chosen, and OOM state is exited when four consecutive correct multiframe patterns are detected. Loss of multiframe (LOM) is declared after residing in the OOM state at the ninth H4 byte without re-alignment. In counting to nine, the out of sequence H4 byte that triggered the transition to the OOM state is counted as the first. A new multiframe alignment is chosen, and LOM state is exited when four consecutive correct multiframe patterns are detected. Changes in multiframe alignments are detected and reported.

8.3.4 Pointer Interpreter

The pointer interpreter is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM as directed by the incoming timing generator. The pointer interpreter processes the incoming tributary pointers such that all bytes within the tributary synchronous payload envelope can be identified and written into the unique payload first-in first-out buffer for the tributary in question. A marker that tags the V5 byte (or J1 byte in the case of a TU3) is passed through the payload buffer. The incoming timing generator directs the pointer interpreter to the correct payload buffer for the tributary being processed.

The pointer interpreter processes the incoming pointers (V1/V2 or H1/H2 in TU3 mode) as specified in the references. The pointer value is used to determine the location of the tributary path overhead byte (V5 or J1 in TU3) in the incoming TUG3 or STS-1 (AU3) stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined (as shown in Figure 1):

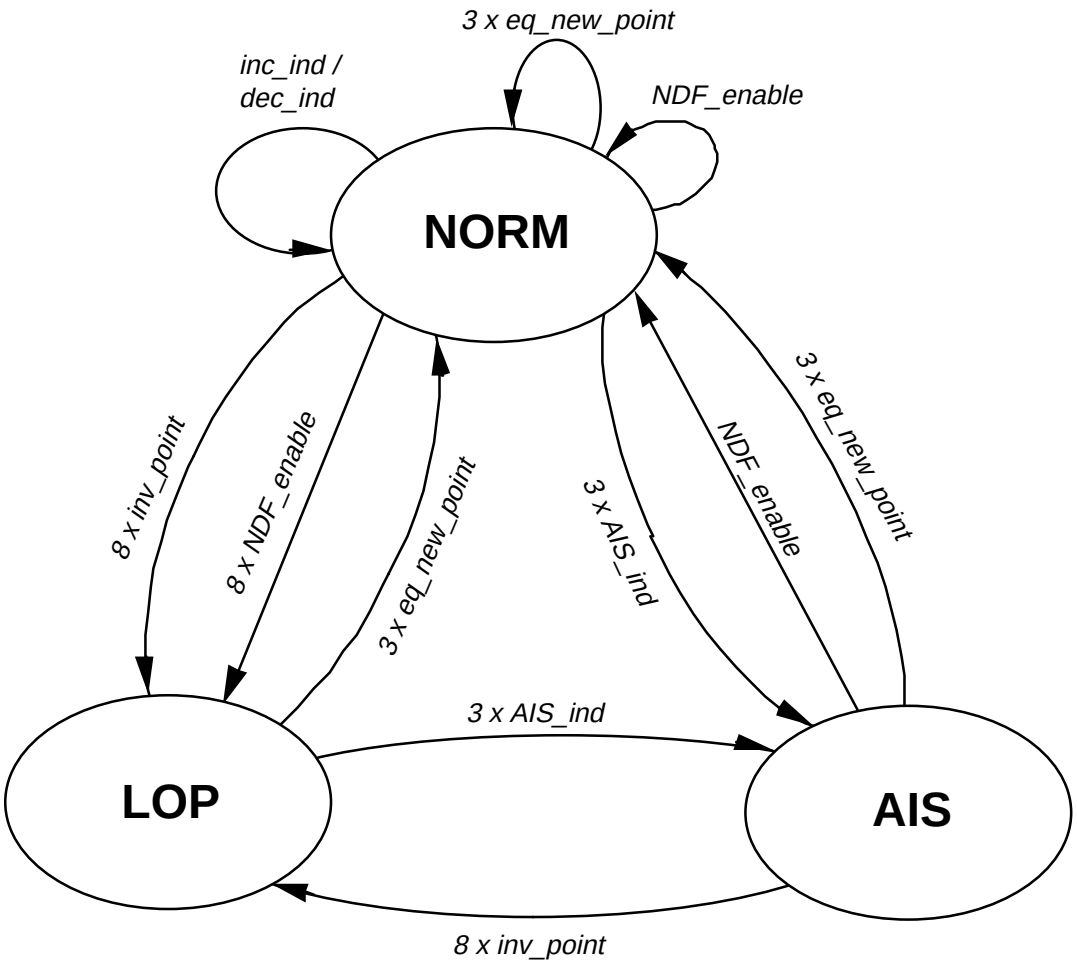
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 1 - Pointer Interpretation State Diagram



The following events (indications) are defined

norm_point :	disabled NDF + ss + offset value equal to active offset
NDF_enable:	enabled NDF + ss + offset value in range for the configured tributary type
AIS_ind:	H1 = 'hFF, H2 = 'hFF
inc_ind:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point:	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point:	disabled_NDF + ss + offset value in range for the configured tributary type but not equal to active offset
inc_req:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted
dec_req:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted

Notes:

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

2. Enabled NDF is defined as the following bit patterns:

   1001, 0001, 1101, 1011, 1000.

3. Disabled NDF is defined as the following bit patterns:

   0110, 1110, 0010, 0100, 0111.

4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.

5. The legal range of pointer values for the five supported tributary types are:

   VT1.5 : 0 .. 103

   VT2 : 0 .. 139

   VT3 : 0 .. 211

   VT6 : 0 .. 427

   TU3 : 0 .. 764

6. The requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.

7. New_point is also an inv_point.

8. The requirement for 3 consecutive AIS indications may be optionally disabled.

The transitions indicated in the state diagram are defined as follows:

inc_ind/dec_ind: offset adjustment (increment or decrement indication)

3 x eq_new_point: three consecutive equal new_point indications

NDF_enable: single NDF_enable indication

3 x AIS_ind: three consecutive AIS indications

8 x inv_point: eight consecutive inv_point indications

8 x NDF_enable eight consecutive NDF_enable indications

Notes:

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

2. 3 x eq_new_point takes precedence over other events.

3. All three offset values received in 3 x eq_new_point must be identical.

4. "consecutive event counters" are reset to zero on a change of state.

The pointer interpreter block detects loss of pointer (LOP) in the incoming tributaries. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed when the same valid pointer with normal NDF is detected for three consecutive frames. Incoming tributary path AIS (pointer bytes set to all ones) does not cause entry into the LOP state.

The pointer interpreter block also detects tributary path AIS in the incoming tributaries. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. PAIS is removed when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid pointer with NDF enabled is detected.

8.3.5 Payload Buffer

The payload buffer is a bank FIFO buffers. It is synchronous in operation and is based on a time-sliced RAM. The three 19.44 MHz clock cycles in each 6.48 MHz period are shared between the read and write operations. The pointer interpreter writes tributary payload data and the V5 (or TU3 J1) tag into the payload buffer. A 16 byte FIFO buffer is provided for each of the (up to 28) tributaries. Address information is also passed through the payload buffer to allow FIFO fill status to be determined by the pointer generator.

8.3.6 Outgoing Timing Generator

The outgoing timing generator identifies the outgoing tributary byte being processed. Based on the configuration of the VTPP, the outgoing timing generator effectively constructs the STS-1 SPE, VC3, or VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and bytes that carry specific tributaries. The identification of specific tributaries allows the pointer generator to be time-sliced across the mix of tributaries to be sourced in the outgoing data stream. The identification of the V1-V3 bytes of VTs, or TUs (H1-H3 bytes of TU3s) allows the pointer generator to function.

The sequence of H4 bytes is generated by each tributary payload processor and inserted into the outgoing administrative units. The six most significant bits of H4 are set to logic 1. The sequence of the remaining two H4 bits is determined by the OTMF input.

8.3.7 Pointer Generator

The pointer generator block generates the tributary pointers (V1/V2 or H1/H2 in TU3 mode) as specified in the references. The pointer value is used to determine the location of the tributary path overhead byte (V5 or J1 in TU3 mode) on the outgoing stream. The algorithm can be modeled by a finite state machine. Within the pointer generator algorithm, five states are defined (as shown in Figure 2):

NORM_state (NORM)

AIS_state (AIS)

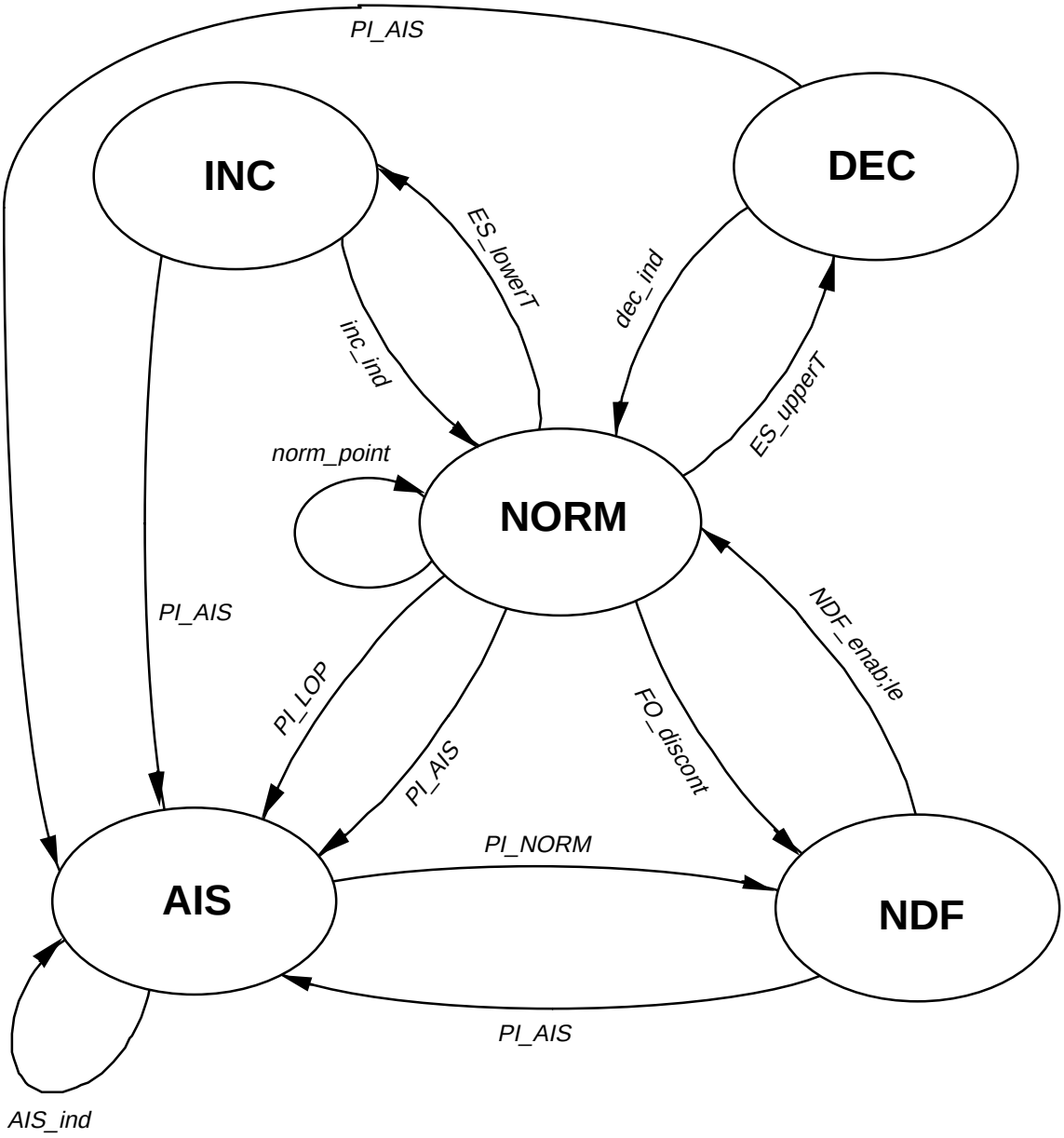
NDF_state (NDF)

INC_state (INC)

DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the payload buffer block. The transition to/from the AIS state are controlled by the pointer interpreter block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 2 - Pointer Generation State Diagram



The following events, indicated in the state diagram (Figure 2), are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind,dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

FO_discont: frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Notes

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an elastic store overflow/underflow occurred.

2. Transition to AIS state due to PI_LOP event may be optionally disabled.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: transmit the pointer with NDF disabled and active offset.

AIS_ind: active offset is undefined, transmit an all-1's pointer and payload.

Notes:

1. Active offset is defined as the phase of the SPE (VC).

2. Enabled NDF is defined as the bit pattern 1001.

3. Disabled NDF is defined as the bit pattern 0110.

The pointer generator is a time-sliced state machine that can process up to 28 independent tributaries. The state vector is saved in RAM at the address associated with the current tributary. The pointer generator fills the outgoing tributary synchronous payload envelopes with bytes read from the associated FIFO in the payload buffer for the current tributary. The pointer generator creates pointers in the V1-V3 bytes (or H1-H3 bytes in the case of TU3s) of the outgoing data stream. The marker that tags the V5 byte (or J1 byte in the case of a TU3) that is passed through the payload buffer is used to align the pointer. The outgoing timing generator directs the pointer generator to the FIFO in the payload buffer that is associated with the tributary being processed. The pointer generator monitors the fill levels of the payload buffers and inserts outgoing pointer justifications as necessary to avoid FIFO spillage. Normally, the pointer generator has a FIFO dead band of two bytes. The dead band can be collapse to one so that any incoming pointer justifications will be reflected by a corresponding outgoing justification with no attenuation. Signals are output by the pointer generator that identify outgoing V5 bytes (or J1 bytes in the case of a TU3) and the tributary synchronous payload envelopes. These simplify the design of mappers downstream of the TUPP-PLUS. On a per tributary basis, tributary path AIS and tributary idle (unequipped) can be inserted as controlled by microprocessor accessible registers. The idle code is selectable globally for the entire VC3 or TUG3 to be all-zeros or all-ones. It is also possible to force an inverted new data flag on individual tributaries for the purpose of diagnosing downstream pointer processors. Tributary path AIS is automatically inserted into outgoing tributaries if the pointer interpreter detects tributary path AIS on the corresponding incoming tributary.

8.4 Tributary Path Overhead Processor

Each tributary path overhead processor (RTOP) monitors the outgoing stream of an associated tributary payload processor (VTPP) and processes the tributaries within an STS-1, AU3, or TUG3. Each RTOP can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each RTOP ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or all TU11s).

The RTOP provides tributary performance monitoring of incoming tributaries. Bit interleaved parity of the incoming tributaries is computed and compared with the BIP-2 code encoded in the V5 byte of the tributary. Errors between the computed and received values are accumulated. RTOP also accumulates far end block error codes. Incoming path signal label is debounced and compared with the

provisioned value. Path signal label unstable, path signal label mismatch and change of path signal label event are identified.

8.4.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary payload processor. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary path overhead processor.

8.4.2 Timing Generator

The timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the RTOP (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The identification of specific tributaries allows the error monitor and extract blocks to be time-sliced across the mix of tributaries present in the incoming data stream.

8.4.3 Error Monitor

The error monitor block is a time-sliced state machine. It relies on the timing generator block to identify the tributary being processed. The error monitor block contains a set of 12-bit counters that are used to accumulate tributary path BIP-2 errors, and a set of 11-bit counters to accumulate far end block errors (FEBE). The contents of the counters may be transferred to a holding RAM, and the counters reset under microprocessor control.

Tributary path BIP-2 errors are detected by comparing the tributary path BIP-2 bits in the V5 byte extracted from the current multiframe, to the BIP-2 value computed for the previous multiframe. BIP-2 errors may be accumulated on a block or nibble basis as controlled by software configurable registers. Far end block errors (FEBEs) are detected by extracting the FEBE bit from the tributary path overhead byte (V5).

Tributary path remote defect indication (RDI) and remote failure indication (RFI) are detected by extracting bit 8 and bit 4 respectively of the tributary path overhead byte (V5). The RDI is recognized when bit 8 of the V5 byte is set high for five or ten consecutive multiframes while RFI is recognized when bit 4 of V5 is

set high for five or ten consecutive frames. In TU3 mode, RDI is recognized when bit 5 of the G1 byte is set high for five or ten consecutive frames. Bit 5 of the G1 byte is similarly processed for the status of the auxiliary RDI state. The RDI and RFI bits, and similarly bits 4 and 5 of a TU3 stream, may be treated as a two-bit code word. A code change is only recognized when the code is unchanged for five or ten frames.

The tributary path signal label (PSL) found in the tributary path overhead byte (V5) is processed. (C2 in TU3 mode). An incoming PSL is accepted when it is received unchanged for five consecutive multiframes. The accepted PSL is compared with the associated provisioned value. The PSL match/mismatch state is determined by the following:

Table 1 - Path Signal Label Mismatch State

Expected PSL	Accepted PSL	PSLM State
000	000	Match
000	001	Mismatch
000	PDI Code	Mismatch
000	XXX ≠ 000, 001, PDI Code	Mismatch
001	000	Mismatch
001	001	Match
001	PDI Code	Match
001	XXX ≠ 000, 001, PDI Code	Match
PDI Code	000	Mismatch
PDI Code	001	Match
PDI Code	PDI Code	Match
PDI Code	XXX ≠ 000, 001, PDI Code	Mismatch
XXX ≠ 000, 001, PDI Code	000	Mismatch
XXX ≠ 000, 001, PDI Code	001	Match
XXX ≠ 000, 001, PDI Code	XXX	Match

Expected PSL	Accepted PSL	PSLM State
XXX ≠ 000, 001, PDI Code	YYY	Mismatch

Each time an incoming PSL differs from the one in the previous multiframe, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive multiframes.

8.4.4 In-band Error Report

The in-band error report block optionally modifies the G1 byte of outgoing TU3 streams or the V5 byte of outgoing non-TU3 streams to report the number of detected BIP errors and tributary path alarms. In-band error reporting is enabled by the IBER regisiter bits in the RTOP In-band Error Reporting Configuration registers.

When in-band error reporting is enabled for TU3 streams, bits 1 to 4 of the G1 byte is set to reflect the count of the number of BIP-8 errors detected in the previous frame. Bit 5 is reports the RDI status. It is set high when the tributary path alarms named in the Tributry Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Similarly, bit 6 reports the auxiliary RDI status. It is set high when the tributary path alarms named in the Tributry Auxiliary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Bits 7 and 8 are unmodified.

When in-band error reporting is enabled for non-TU3 streams, bit 3 of the V5 byte is set high when a BIP-2 error is detected in the previous multiframe. Bit 4 is reports the RDI status. It is set high when the tributary path alarms named in the Tributry Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Similarly, bit 8 reports the auxiliary RDI status. It is set high when the tributary path alarms named in the Tributry Auxiliary Remote Defect Indication Control registers is detected and the corresponding enable register bits is also set high. Bits 1, 2, 5, 6 and 7 are unmodified.

8.4.5 Extract

The extract block uses timing information from the timing generator block to extract, serialize and output the tributary path overhead bytes (V5, J2, Z6, Z7) of all the processed tributaries on the POH output. The POHFP output is provided to identify the most significant bit of the V5 byte of the first tributary on the POH output. All four tributary path overhead bytes are shifted out within each payload frame period. Therefore, each byte is shifted out more than once. The POHEN output is used to identify fresh overhead bytes. POHEN is set high when the tributary path overhead byte is shifted out for the first time. POHEN is set low when the overhead byte is merely repeated. The tributary path overhead clock, POHCK is nominally a 9.72 MHz clock.

8.5 Tributary Trace Buffer

Each tributary trace buffer (RTTB) monitors the outgoing stream of an associated tributary payload processor (VTPP) and processes the tributaries within an STS-1, AU3, or TUG3. Each RTTB can be configured to process any legal mix of VT1.5s, VT2s, VT3s, or VT6s that can be carried in an STS-1 or any legal mix of TU11s, TU12s, TU2s, or TU3s, that can be carried in an AU3 or TUG3. The number of tributaries managed by each RTTB ranges from 1 (when configured to process a single TU3) to 28 (when configured to process all VT1.5s or all TU11s).

The RTTB extracts the tributary path trace message contained in the J2 byte (J1 byte in TU3) to a set of internal buffers. The buffers are microprocessor accessible to allow system software to examine the messages. Another set of buffers is provided for system software to download the expected message. The RTTB compares the received message with the provisioned message and reports on the state of match. The RTTB also monitors for unstable incoming tributary path trace messages.

8.5.1 Clock Generator

The clock generator derives various clocks from the 19.44 MHz system clock and distributes them to other blocks within the tributary trace buffer. The overall design is totally synchronous, with processing occurring at a 6.48 MHz rate in each tributary trace buffer.

8.5.2 Timing Generator

The timing generator identifies the incoming tributary being processed at any given point in time. Based on the configuration of the RTTB (it can process various mixes of tributary types), the incoming timing generator extracts the STS-1 SPE, VC3, or a single TUG3 from a VC4, and identifies the bytes within these envelopes that correspond to various types of overhead and those that carry specific tributaries to be processed. The identification of specific tributaries allows the alarm monitor and extract blocks to be time-sliced across the mix of tributaries present in the incoming data stream.

8.5.3 Extract

The extract block is a time-sliced state machine. It uses timing information from the timing generator block to extract the tributary path trace message bytes (J2) from all the processed tributaries in the incoming stream. Each tributary in the incoming stream is allocated an individual receive buffer in the buffer block. The length of the message and, consequently, the depth of the corresponding buffer are register programmable to be 16 or 64 bytes. Bytes in the message may be written to the corresponding buffer in a circular fashion or optionally be synchronized to the framing pattern embedded in the message. For a 16 byte message, the first byte is identified by a logic one in the most significant bit. For a 64 byte message, the last two bytes are set to the ASCII characters of carriage-return (0DH) and linefeed (0AH).

8.5.4 Alarm Monitor

The alarm monitor block is a time-sliced state machine. It relies on the timing generator block to identify the tributary being processed. The alarm monitor block accesses an individual capture and expected buffers in the buffer block for each tributary in the incoming stream. It also monitors the received message for consistency. When the identical message is received three or five times, as controlled by the PER5 register bit, the message is accepted. This accepted message is then compared with the expected message provision in the buffer block. If the accepted message differs from the expected message, the trail trace identifier mismatch (TIM) alarm is raised. TIM alarm is negated if the accepted and expected messages match. An accepted message that contains all-zero bytes is treated specially. If the expected messages is not also all-zeros, the TIM alarm is not affected upon accepting of an all-zero message. If the expected message is all-zeros, accepting an all-zeros message would negate TIM.

The alarm monitor block also monitors the incoming messages for stability. Two algorithms are provided. In the first algorithm, each time the current incoming message differs from the previous message, the corresponding unstable counter is incremented by one. Thus, a single bit error in a message of a sequence of constant messages will cause the counter to increment twice, once on the corrupted message, and again on the first error free message. A trail trace identifier unstable (TIU) alarm is raised when the counter exceeds the register programmable threshold. The counter is cleared and TIU negated when a set of identical messages is received and becomes the accepted message. In the second algorithm, when the current incoming message differs from the previous message, the corresponding counter starts incrementing once per message. A trail trace identifier unstable (TIU) alarm is raised when the counter exceeds the register programmable threshold. The counter is cleared and TIU negated when a set of identical messages is received and becomes the accepted message.

8.5.5 Buffer

The buffer block contains two pages of memory, one page for capturing the receive tributary path trace messages and the other for storing the expected messages. Each tributary in the incoming stream is allocated a range of addresses using high order interleaving keyed on the tributary group number and the tributary number within the group. At the J2 byte (J1 byte in TU3 mode) of each tributary, the receive and expected pages are read. The data from the incoming stream, the receive page and the expected page are supplied to the alarm monitor block for determination of trace identifier mismatch (TIM) and trace identifier unstable (TIU) alarms. At the end of the cycle, the incoming data is written to the receive page. The buffer block also contains an arbiter to allow access to the receive and expected pages by the microprocessor when neither the extract nor alarm monitor block requires access.

8.6 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The TUPP-PLUS identification code is 053620CD hexadecimal.

8.7 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode

registers are required for normal operation, and test mode registers are used to enhance the testability of the TUPP-PLUS. Tributary based normal mode registers are arranged in order of transmission; TU #1 in TUG2 #1 of STS-1 #1 is the first tributary transmitted, while TU #4 in TUG2 #7 of STS-1 #3 is the last. The register set is accessed as follows:

8.8 Register Memory Map

Address	Register
00H	TUPP-PLUS Master Incoming Configuration
01H	TUPP-PLUS Master Outgoing Configuration
02H	Input Signal Activity Monitor, Accumulation Trigger
03H	TUPP-PLUS Master Reset and Identity
04H	VTPP #1 Configuration
05H	VTPP #2 Configuration
06H	VTPP #3 Configuration
07H	Tributary Payload Processor and LOM Interrupt Enable
08H	Tributary Payload Processor Interrupt and LOM Status
09H	Parity Error and LOM Interrupt
0AH	RTOP and RTTB Interrupt Enable
0BH	RTOP and RTTB Interrupt Status
0CH	RTOP #1 Configuration
0DH	RTOP #2 Configuration
0EH	RTOP #3 Configuration
0FH	Reserved
10H	Tributary Alarm AIS Control
11H	Tributary Remote Defect Indication Control
12H	Tributary Auxiliary Remote Defect Indication Control
13H	Tributary Path Defect Indication Control
14H-1FH	Reserved

Address	Register
20H	VTPP #1, TU3 or TU #1 in TUG2 #1, Configuration and Status
21H	VTPP #1, TU #1 in TUG2 #2, Configuration and Status
22H	VTPP #1, TU #1 in TUG2 #3, Configuration and Status
23H	VTPP #1, TU #1 in TUG2 #4, Configuration and Status
24H	VTPP #1, TU #1 in TUG2 #5, Configuration and Status
25H	VTPP #1, TU #1 in TUG2 #6, Configuration and Status
26H	VTPP #1, TU #1 in TUG2 #7, Configuration and Status
27H	VTPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt
28H-2EH	VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status
2FH	VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt
30H-36H	VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status
37H	VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt
38H-3EH	VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status
3FH	VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt
40H-5FH	VTPP #2 Configuration and Status, and LOP Interrupt Registers
60H-7FH	VTPP #3 Configuration and Status, and LOP Interrupt Registers
80H-9FH	Reserved
A0H	VTPP #1, TU3, or TU #1 in TUG2 #1, Alarm Status
A1H	VTPP #1, TU #1 in TUG2 #2, Alarm Status
A2H	VTPP #1, TU #1 in TUG2 #3, Alarm Status
A3H	VTPP #1, TU #1 in TUG2 #4, Alarm Status
A4H	VTPP #1, TU #1 in TUG2 #5, Alarm Status

Address	Register
A5H	VTPP #1, TU #1 in TUG2 #6, Alarm Status
A6H	VTPP #1, TU #1 in TUG2 #7, Alarm Status
A7H	VTPP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt
A8H-AEH	VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status
AFH	VTPP #1, TU #2 in TUG2 #1 to TUG2 #7, AIS Interrupt
B0H-B6H	VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status
B7H	VTPP #1, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt
B8H-BEH	VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status
BFH	VTPP #1, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt
C0H-DFH	VTPP #2 Alarm Status, and AIS Interrupt Registers
E0H-FFH	VTPP #3 Alarm Status, and AIS Interrupt Registers
100H	RTOP #1, TU3 or TU #1 in TUG2 #1, Configuration
101H	RTOP #1, TU3 or TU #1 in TUG2 #1, Config. and Alarm Status
102H	RTOP #1, TU3 or TU #1 in TUG2 #1, Expected Path Signal Label
103H	RTOP #1, TU3 or TU #1 in TUG2 #1, Accepted Path Signal Label
104H	RTOP #1, TU3 or TU #1 in TUG2 #1, BIP Count LSB
105H	RTOP #1, TU3 or TU #1 in TUG2 #1, BIP Count MSB
106H	RTOP #1, TU3 or TU #1 in TUG2 #1, FEBE Count LSB
107H	RTOP #1, TU3 or TU #1 in TUG2 #1, FEBE Count MSB
108H-10FH	RTOP #1, TU #1 in TUG2 #2, Configuration and Status Registers
110H-117H	RTOP #1, TU #1 in TUG2 #3, Configuration and Status Registers
118H-11FH	RTOP #1, TU #1 in TUG2 #4, Configuration and Status Registers

Address	Register
120H-127H	RTOP #1, TU #1 in TUG2 #5, Configuration and Status Registers
128H-12FH	RTOP #1, TU #1 in TUG2 #6, Configuration and Status Registers
130H-137H	RTOP #1, TU #1 in TUG2 #7, Configuration and Status Registers
138H	RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt
139H	RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt
13AH	RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt
13BH	RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt
13CH	RTOP #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, RFI Interrupt
13DH	RTOP #1, TU #1 In Band Error Reporting Configuration
13EH	RTOP #1, TU #1 Controllable Output Configuration
13FH	Reserved
140H-147H	RTOP #1, TU #2 in TUG2 #1, Configuration and Status Registers
148H-14FH	RTOP #1, TU #2 in TUG2 #2, Configuration and Status Registers
150H-157H	RTOP #1, TU #2 in TUG2 #3, Configuration and Status Registers
158H-15FH	RTOP #1, TU #2 in TUG2 #4, Configuration and Status Registers
160H-167H	RTOP #1, TU #2 in TUG2 #5, Configuration and Status Registers
168H-16FH	RTOP #1, TU #2 in TUG2 #6, Configuration and Status Registers

Address	Register
170H-177H	RTOP #1, TU #2 in TUG2 #7, Configuration and Status Registers
178H	RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt
179H	RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt
17AH	RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt
17BH	RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt
17CH	RTOP #1, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt
17DH	RTOP #1, TU #2 In Band Error Reporting Configuration
17EH	RTOP #1, TU #2 Configurable Output Control
17FH	Reserved
180H-187H	RTOP #1, TU #3 in TUG2 #1, Configuration and Status Registers
188H-18FH	RTOP #1, TU #3 in TUG2 #2, Configuration and Status Registers
190H-197H	RTOP #1, TU #3 in TUG2 #3, Configuration and Status Registers
198H-19FH	RTOP #1, TU #3 in TUG2 #4, Configuration and Status Registers
1A0H-1A7H	RTOP #1, TU #3 in TUG2 #5, Configuration and Status Registers
1A8H-1AFH	RTOP #1, TU #3 in TUG2 #6, Configuration and Status Registers
1B0H-1B7H	RTOP #1, TU #3 in TUG2 #7, Configuration and Status Registers
1B8H	RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt
1B9H	RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt
1BAH	RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt
1BBH	RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt
1BCH	RTOP #1, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt

Address	Register
1BDH	RTOP #1, TU #3 In Band Error Reporting Configuration
1BEH	RTOP #1, TU #3 Configurable Output Control
1BFH	Reserved
1C0H-1C7H	RTOP #1, TU #4 in TUG2 #1, Configuration and Status Registers
1C8H-1CFH	RTOP #1, TU #4 in TUG2 #2, Configuration and Status Registers
1D0H-1D7H	RTOP #1, TU #4 in TUG2 #3, Configuration and Status Registers
1D8H-1DFH	RTOP #1, TU #4 in TUG2 #4, Configuration and Status Registers
1E0H-1E7H	RTOP #1, TU #4 in TUG2 #5, Configuration and Status Registers
1E8H-1EFH	RTOP #1, TU #4 in TUG2 #6, Configuration and Status Registers
1F0H-1F7H	RTOP #1, TU #4 in TUG2 #7, Configuration and Status Registers
1F8H	RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt
1F9H	RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt
1FAH	RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt
1FBH	RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt
1FCH	RTOP #1, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt
1FDH	RTOP #1, TU #4 In Band Error Reporting Configuration
1FEH	RTOP #1, TU #4 Configurable Output Control
1FFH	RTOP #1 Status
200H-2FFH	RTOP #2 Registers
300H-3FFH	RTOP #3 Registers
400H	RTTB #1, TU3 or TU #1 in TUG2 #1 Configuration and Status

Address	Register
401H	RTTB #1, TU #1 in TUG2 #2 Configuration and Status
402H	RTTB #1, TU #1 in TUG2 #3 Configuration and Status
403H	RTTB #1, TU #1 in TUG2 #4 Configuration and Status
404H	RTTB #1, TU #1 in TUG2 #5 Configuration and Status
405H	RTTB #1, TU #1 in TUG2 #6 Configuration and Status
406H	RTTB #1, TU #1 in TUG2 #7 Configuration and Status
407H	Reserved
408H-40EH	RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status
40FH	Reserved
410H-416H	RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status
417H	Reserved
418H-41EH	RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status
41FH	Reserved
420H	RTTB #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt
421H	RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, TIM Interrupt
422H	RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, TIM Interrupt
423H	RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, TIM Interrupt
424H	RTTB #1, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt
425H	RTTB #1, TU #2 in TUG2 #1 to TUG2 #7, TIU Interrupt
426H	RTTB #1, TU #3 in TUG2 #1 to TUG2 #7, TIU Interrupt
427H	RTTB #1, TU #4 in TUG2 #1 to TUG2 #7, TIU Interrupt
428H	RTTB #1, TIU Threshold
429H	RTTB #1, Indirect Tributary Select

Address	Register
42AH	RTTB #1, Indirect Buffer Address
42BH	RTTB #1, Indirect Data
42CH-43FH	Reserved
440H-47FH	RTTB #2 Registers
480H-4BFH	RTTB #3 Registers
4C0H-7FFH	Reserved
800H	Master Test
801H-FFFH	Reserved for Test

For all register accesses, CSB must be low.

9 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TUPP-PLUS. Normal mode registers (as opposed to test mode registers) are selected when A[11] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TUPP-PLUS to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect TUPP-PLUS operation unless otherwise noted.

9.1 Master Registers

Register 00H: Master Incoming Configuration

Bit	Type	Function	Default
Bit 7	R/W	IPE	0
Bit 6	R/W	LOPAIS	0
Bit 5	R/W	INCIPL	0
Bit 4	R/W	INCIC1J1	0
Bit 3	R/W	IOP	0
Bit 2	R/W	ITMFH4	0
Bit 1	R/W	ITMFEN	0
Bit 0	R/W	ICONCAT	0

This register configures the TUPP-PLUS functionality that are related to the incoming data stream.

ICONCAT:

When set high, the ICONCAT bit configures the incoming section of the TUPP-PLUS to operate in AU4 mode. When the ICONCAT bit is set low, the incoming section operates in AU3 mode (or equivalently, STS-1 mode).

ITMFEN:

When set high, the ITMFEN bit enables the TUPP-PLUS to use the ITMF input signal to locate tributary multiframe boundaries. The H4 bytes in the incoming data stream are ignored. When ITMFEN is set low, the H4 bytes are used to locate the boundaries, and the ITMF signal is ignored.

ITMFH4:

The ITMFH4 bit selects the location of the ITMF in the tributary multiframe. When ITMFH4 is set high, ITMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary multiframe. When ITMFH4 is set low, ITMF marks the third byte after J1. ITMFH4 is ignored if ITMF is disabled by setting the ITMFEN bit low.

IOP:

The IOP bit controls the expected parity on the incoming parity signal IDP. When IOP is set high, the parity of the parity signal set, together with IDP is expected to be odd. When IOP is set low, the expected parity is even. Membership of the parity signal set always includes ID[7:0], and may include input signals IC1J1 and IPL as controlled by the INCIC1J1 and INCIPL bits, respectively.

INCIC1J1:

The INCIC1J1 bit controls whether the IC1J1 input signal participates in the incoming parity calculations. When INCIC1J1 is set high, the parity signal set includes the IC1J1 input. When INCIC1J1 is set low, parity is calculated without regard to the state of IC1J1. Selection of odd or even parity is controlled by the IOP bit.

INCIPL:

The INCIPL bit controls the whether the IPL input signal participates in the incoming parity calculations. When INCIPL is set high, the parity signal set includes the IPL input. When INCIPL is set low, parity is calculated without regard to the state of IPL. Selection of odd or even parity is controlled by the IOP bit.

LOPAIS:

The LOPAIS bit is an active high AIS insertion enable. When LOPAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in loss of pointer state. When LOPAIS is set low, the generation of AIS on the outgoing data stream is inhibited. This bit is logically OR'ed with the bit of the same name in Tributary Alarm AIS Control register.

IPE:

The IPE bit is an active high interrupt enable. When IPE is set high, the occurrence of a parity error on the incoming parity signal set will cause an interrupt to be asserted on the interrupt (INTB) output. When IPE is set low, incoming parity errors will not cause an interrupt.

Register 01H: Master Outgoing Configuration

Bit	Type	Function	Default
Bit 7	R/W	LOCK0	0
Bit 6		Unused	X
Bit 5	R/W	POHPT	0
Bit 4	R/W	LV1EN	0
Bit 3	R/W	OOP	0
Bit 2	R/W	OTMFH4	0
Bit 1	R/W	OJ1EN	0
Bit 0	R/W	OCONCAT	0

This register configures the TUPP-PLUS functionality that are related to the outgoing data stream.

OCONCAT:

When set high, the OCONCAT bit configures the outgoing section of the TUPP-PLUS to operate in AU4 mode. When the OCONCAT bit is set low, the outgoing section operates in AU3 mode (or equivalently, STS-1 mode).

OJ1EN:

The OJ1EN bit selects the operation of the outgoing data stream to be in floating or locked mode. When OJ1EN is set high, TUPP-PLUS output bus to operate in floating mode where the OC1J1 signal marks the first C1 byte and the J1 bytes in the outgoing data stream, OD[7:0]. The OPL input is used to distinguish between bytes in the transport overhead and the payload envelope, and consequently C1 and J1. Only one J1 byte, and one VC or concatenated SPE, are expected to be marked when configured for AU4 mode (OCONCAT set high). Outputs LC1J1V1 and LPL are held low in floating mode.

When the OJ1EN bit is low, the TUPP-PLUS output bus operates in locked mode where the OC1J1 signal marks the first C1 byte only in the outgoing data stream, OD[7:0]. In this mode, the OPL input must be logic zero for the C1 byte. The TUPP-PLUS defaults to fixed output timing where the J1 bytes

of the STS-1, AU3 or AU4 synchronous payload envelopes can be controlled by the LOCK0 bit to immediately follow the C1 bytes or the H3 bytes.

In either floating or locked mode, the OTMF input is used to establish the transmit tributary multiframe boundaries on the outgoing data stream OD[7:0].

OTMFH4:

The OTMFH4 bit selects the location of the OTMF in the tributary multiframe. When OTMFH4 is set high, OTMF is pulsed high to mark the H4 byte which indicates that the next AU3/4 or STS-1 frame is the first frame of the tributary multiframe. When OTMFH4 is set low, OTMF marks the third byte after J1.

OOP:

The OOP bit controls the parity placed on the outgoing parity signal ODP. When OOP is set low, the parity of outgoing data stream OD[7:0], together with ODP is even. When OOP is set high, the parity is odd.

LV1EN:

The LV1EN bit controls the identification of the third byte after J1 in the V1 frame in locked mode (OJ1EN set low). When LV1EN is set low, the LC1J1V1 output only indicates the C1 and J1 bytes. The third byte after J1 is not indicated. When LV1EN is set high, the LC1J1V1 output indicates the C1, J1 and the third byte after J1. LV1EN is ignored in floating mode (OJ1EN set high).

POHPT:

The POHPT bit controls the data of the path overhead column on the outgoing STS-1 (AU3, AU4) streams. When POHPT is set low, the outgoing POH columns (except the H4 byte) are set to all-zeros. When POHPT is set high, the POH column (except the H4 byte) of the incoming stream is transferred to the outgoing stream. A two frame elastic store buffer is provided to absorb phase variations between the incoming and outgoing frames.

LOCK0:

The LOCK0 bit controls the payload offset of the outgoing data stream in locked mode (OJ1EN set low). When LOCK0 is set high, the J1 byte in the outgoing data stream is forced to the byte immediately following the H3 bytes (pointer offset zero). When LOCK0 is set low, the J1 byte is force to the byte

immediately following the C1 bytes (pointer offset 522). LOCK0 is ignored in floating mode (OJ1EN set high).

Register 02H: Input Signal Activity Monitor, Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R	OTMFA	X
Bit 6	R	OPLA	X
Bit 5	R	OC1J1A	X
Bit 4	R	IDA	X
Bit 3	R	ITMFA	X
Bit 2	R	IPLA	X
Bit 1	R	IC1J1A	X
Bit 0	R	SCLKA	X

This register provides activity monitoring on major TUPP-PLUS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the RTOP accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 0.5 second or shorter. The bits in this register are not affected by write accesses.

SCLKA:

The SCLK active (SCLKA) bit monitors for low to high transitions on the SCLK input. SCLKA is set high on a rising edge of SCLK, and is set low when this register is read.

IC1J1A:

The IC1J1 active (IC1J1A) bit monitors for low to high transitions on the IC1J1 input. IC1J1A is set high on a rising edge of IC1J1, and is set low when this register is read.

IPLA:

The IPL active (IPLA) bit monitors for low to high transitions on the IPL input. IPLA is set high on a rising edge of IPL, and is set low when this register is read.

ITMFA:

The ITMF active (ITMFA) bit monitors for low to high transitions on the ITMF input. ITMFA is set high on a rising edge of ITMF, and is set low when this register is read.

IDA:

The ID bus active (IDA) bit monitors for low to high transitions on the ID[7:0] inputs. IDA is set high when rising edges have been observed on all the signals on the ID[7:0] bus, and is set low when this register is read.

OC1J1A:

The OC1J1 active (OC1J1A) bit monitors for low to high transitions on the OC1J1 input. OC1J1A is set high on a rising edge of OC1J1, and is set low when this register is read.

OPLA:

The OPL active (OPLA) bit monitors for low to high transitions on the OPL input. OPLA is set high on a rising edge of OPL, and is set low when this register is read.

OTMFA:

The OTMF active (OTMFA) bit monitors for low to high transitions on the OTMF input. OTMFA is set high on a rising edge of OTMF, and is set low when this register is read.

Register 03H: Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE	1
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

This register allows the revision of the TUPP-PLUS to be read by software permitting graceful migration to support for newer, feature enhanced versions of the TUPP-PLUS, should revision of the TUPP-PLUS occur. It also provides software reset capability.

ID[5:0]:

The ID bits can be read to provide a binary TUPP-PLUS revision number.

TYPE:

The TYPE bit can be read to distinguish between the TUPP-PLUS and the TUPP devices. The TYPE bit is set high in the TUPP-PLUS and set low in the TUPP device.

RESET:

The RESET bit allows the TUPP-PLUS to be reset under software control. If the RESET bit is a logic 1, the entire TUPP-PLUS is held in reset. This bit is not self-clearing. Therefore, a logic 0 must be written to bring the TUPP-PLUS out of reset. Holding the TUPP-PLUS in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise the effect of a software reset is equivalent to that of a hardware reset.

Register 04H: VTPP #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TUGEN	0
Bit 6	R/W	SOS	0
Bit 5	R/W	MONIS	0
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to enable the processing of STS-1 #1 (TUG3 #1) and configure the major operational modes of VTPP #1.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 20H and 27H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written

is ignored, data read is invalid. When not in TU3 mode, register 20H reflects status and configuration of TUG2 #1, TU #1 and register 27H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Idle insertion only affects the tributary payload bytes which are overwritten with the selected idle pattern. The outgoing pointer remains a function of the incoming pointer and the relative multiframe alignment of the incoming and outgoing streams. ICODE has no effect on pointer processing. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change.

TUGEN:

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #1 (TUG3 #1). When TUGEN is low, VTPP #1, RTOP #1 and RTTB #1 are held in a low power, reset state. The data in STS-1 #1 (TUG3 #1) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details. When TUGEN is toggled low, the VTTP #1, RTOP #1, and RTTB #1 registers with addresses 0x20H and higher are reset to their default states.

Register 05H: VTPP #2 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TUGEN	0
Bit 6	R/W	SOS	0
Bit 5	R/W	MONIS	0
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to enable the processing of STS-1 #2 (TUG3 #2) and configure the major operational modes of VTPP #2.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 40H and 47H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written

is ignored, and read data is invalid. When not in TU3 mode, register 40H reflects status and configuration of TUG2 #1, TU #1 and register 47H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Idle insertion only affects the tributary payload bytes which are overwritten with the selected idle pattern. The outgoing pointer remains a function of the incoming pointer and the relative multiframe alignment of the incoming and outgoing streams. ICODE has no effect on pointer processing. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change.

TUGEN:

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #2 (TUG3 #2). When TUGEN is low, VTPP #2, RTOP #2 and RTTB #2 are held in a low power, reset state. The data in STS-1 #2 (TUG3 #2) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details. When TUGEN is toggled low, the VTTP #2, RTOP #2, and RTTB #2 registers with addresses 0x40H and higher are reset to their default states.

Register 06H: VTPP #3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	TUGEN	0
Bit 6	R/W	SOS	0
Bit 5	R/W	MONIS	0
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2	R/W	TU3	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to enable the processing of STS-1 #3 (TUG3 #3) and configure the major operational modes of VTPP #1.

OTUG3:

When set high, the OTUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the outgoing data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

ITUG3:

When set high, the ITUG3 bit configures the tributary payload processor to process a TU3 or TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1.

TU3:

When set high, the TU3 bit configures the tributary payload processor to process a single TU3 that has been mapped into a TUG3. The programming of the ITUG3 and OTUG3 bits are ignored. Both the incoming and outgoing streams are affected simultaneously by the TU3 bit. When in TU3 mode, registers 60H and 67H reflect TU3 status and configuration, all other registers relating to TUG2s and the tributaries within TUG2s are disabled; data written

is ignored and read data is invalid. When not in TU3 mode, register 60H reflects status and configuration of TUG2 #1, TU #1 and register 67H reflect LOP interrupt status of TU #1 in all seven TUG #2s. When changing the value of the TU3 bit, tributary processing must be disabled (TUGEN must have a value of logic zero).

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Idle insertion only affects the tributary payload bytes which are overwritten with the selected idle pattern. The outgoing pointer remains a function of the incoming pointer and the relative multiframe alignment of the incoming and outgoing streams. ICODE has no effect on pointer processing. In TU3 mode, ICODE must be set to 0 for the C2 byte to indicate unequipped.

MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change.

TUGEN:

When set high, the TUGEN bit enables the processing of tributaries in STS-1 #3 (TUG3 #3). When TUGEN is low, VTPP #3, RTOP #3 and RTTB #3 are held in a low power, reset state. The data in STS-1 #3 (TUG3 #3) is re-transmitted unchanged on the outgoing data stream. The amount of delay from the incoming to the outgoing data stream is a function of the separation between the IC1J1 and OC1J1 inputs. See the bypass functional timing diagram for details. When TUGEN is toggled low, the VTTP #3, RTOP #3, and RTTB #3 registers with addresses 0x60H and higher are reset to their default states.

Register 07H: Tributary Payload Processor and LOM Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	LOM3E	0
Bit 4	R/W	LOM2E	0
Bit 3	R/W	LOM1E	0
Bit 2	R/W	VTPP3E	0
Bit 1	R/W	VTPP2E	0
Bit 0	R/W	VTPP1E	0

This register provides interrupt enable of the three H4 byte framers and of the three tributary payload processors in the TUPP-PLUS.

VTPP1E:

VTPP1E is the interrupt enable bit for tributary payload processor #1 in the TUPP-PLUS. Interrupts enabled at tributary processor #1 but masked by VTPP1E will still be reported by the VTPP1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #1 will not be reported by the VTPP1I bit.

VTPP2E:

VTPP2E is the interrupt enable bit for tributary processor #2 in the TUPP-PLUS. Interrupts enabled at tributary payload processor #2 but masked by VTPP2E will still be reported by the VTPP2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #2 will not be reported by the VTPP2I bit.

VTPP3E:

VTPP3E is the interrupt enable bit for tributary payload processor #3 in the TUPP-PLUS. Interrupts enabled at tributary processor #3 but masked by VTPP3E will still be reported by the VTPP3I bit, although the interrupt output will not be activated. Interrupts disabled at tributary payload processor #3 will not be reported by the VTPP3I bit.

LOM1E:

The LOM1E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #1. When LOM1E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low.

LOM2E:

The LOM2E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #2. When LOM2E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

LOM3E:

The LOM3E bit is an interrupt enable bit for the H4 framer out of frame interrupt in tributary payload processor #3. When LOM3E is set high, a change in the framer out of frame status will cause an interrupt to be generated on the INTB output. Interrupts are masked when LOME is set low. When ICONCAT is set to logic 1 this interrupt enable bit should be set to logic 0. In the AU4 mode the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

Register 08H: Tributary Payload Processor Interrupt and LOM Status

Bit	Type	Function	Default
ZBit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LOM3V	0
Bit 4	R	LOM2V	0
Bit 3	R	LOM1V	0
Bit 2	R	VTPP3I	0
Bit 1	R	VTPP2I	0
Bit 0	R	VTPP1I	0

This register provides interrupt status of the three H4 byte framers and of the three tributary payload processors in the TUPP-PLUS.

VTPP1I:

VTPP1I identifies tributary payload processor #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #1 will not be reported by the VTPP1I bit.

VTPP2I:

VTPP2I identifies tributary payload processor #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #2 will not be reported by the VTPP2I bit.

VTPP3I:

VTPP1I identifies tributary payload processor #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary payload processor #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary payload processor #3 will not be reported by the VTPP3I bit.

LOM1V:

The LOM1V bit indicates the status of the H4 byte framer in tributary payload processor #1. LOM1V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment.

LOM2V:

The LOM2V bit indicates the status of the H4 byte framer in tributary payload processor #2. LOM2V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

LOM3V:

The LOM3V bit indicates the status of the H4 byte framer in tributary payload processor #3. LOM3V is set high when the H4 framer is in loss of multiframe state and is set low when it re-acquires multiframe alignment. When ICONCAT is set to logic 1 this status bit should be ignored since the multiframe alignment is determined by the H4 byte framer in tributary payload processor #1.

Register 09H: Parity Error and LOM Interrupt

Bit	Type	Function	Default
Bit 7	R	IPI	0
Bit 6		Unused	X
Bit 5	R	LOM3I	0
Bit 4	R	LOM2I	0
Bit 3	R	LOM1I	0
Bit 2	R/W	Reserve3	1
Bit 1	R/W	Reserve2	1
Bit 0	R/W	Reserve1	1

This register provides interrupt status of the H4 byte framers in the three tributary payload processor and of the input parity checker in the TUPP-PLUS.

Reserved[3:1]:

The Reserved[3:1] bits must be set high for the correct operation of the TUPP-PLUS.

LOM1I:

The LOM1I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #1 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM1I bit is set high on entry and exit to the loss of multiframe state and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOMI bit remains valid when interrupts are not enabled (LOM1E set low) and may be polled to detect out of frame events.

LOM2I:

The LOM2I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #2 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM2I bit is set high on entry and exit to the loss of multiframe state and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOM2I bit remains valid when

interrupts are not enabled (LOM2E set low) and may be polled to detect out of frame events.

LOM3I:

The LOM3I bit indicates a change of status in the H4 byte framer. Interrupts are generated when the H4 framer in tributary payload processor #3 enters loss of multiframe state and when it re-acquires multiframe alignment. The LOM3I bit is set high on entry and exit to the loss of multiframe state and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. The LOM3I bit remains valid when interrupts are not enabled (LOM3E set low) and may be polled to detect out of frame events.

IPI:

The incoming parity error interrupt bit (IPI) is set high when a parity error is detected on the incoming parity signal set. If the IPE bit in the master incoming configuration register is set high, the interrupt output (INTB) is activated. When this register is read, IPI (and the corresponding interrupt) is cleared.

Register 0AH: Tributary Path Overhead Processor and Tributary trace Buffer Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RTTB3E	0
Bit 4	R/W	RTTB2E	0
Bit 3	R/W	RTTB1E	0
Bit 2	R/W	RTOP3E	0
Bit 1	R/W	RTOP2E	0
Bit 0	R/W	RTOP1E	0

This register provides interrupt enable of the three tributary path overhead processors and of the three tributary trace buffers in the TUPP-PLUS.

RTOP1E:

RTOP1E is the interrupt enable bit for tributary path overhead processor #1 in the TUPP-PLUS. Interrupts enabled at tributary path overhead processor #1 but masked by RTOP1E will still be reported by the RTOP1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #1 will not be reported by the RTOP1I bit.

RTOP2E:

RTOP2E is the interrupt enable bit for tributary path overhead processor #2 in the TUPP-PLUS. Interrupts enabled at tributary path overhead processor #2 but masked by RTOP2E will still be reported by the RTOP2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #2 will not be reported by the RTOP2I bit.

RTOP3E:

RTOP3E is the interrupt enable bit for tributary path overhead processor #3 in the TUPP-PLUS. Interrupts enabled at tributary path overhead processor #3 but masked by RTOP3E will still be reported by the RTOP3I bit, although the interrupt output will not be activated. Interrupts disabled at tributary path overhead processor #3 will not be reported by the RTOP3I bit.

RTTB1E:

RTTB1E is the interrupt enable bit for tributary trace buffer #1 in the TUPP-PLUS. Interrupts enabled at tributary trace buffer #1 but masked by RTTB1E will still be reported by the RTTB1I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #1 will not be reported by the RTTB1I bit.

RTTB2E:

RTTB2E is the interrupt enable bit for tributary trace buffer #2 in the TUPP-PLUS. Interrupts enabled at tributary trace buffer #2 but masked by RTTB2E will still be reported by the RTTB2I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #2 will not be reported by the RTTB2I bit.

RTTB3E:

RTTB3E is the interrupt enable bit for tributary trace buffer #3 in the TUPP-PLUS. Interrupts enabled at tributary trace buffer #3 but masked by RTTB3E will still be reported by the RTTB3I bit, although the interrupt output will not be activated. Interrupts disabled at tributary trace buffer #3 will not be reported by the RTTB3I bit.

Register 0BH: Tributary Path Overhead Processor and Tributary Trace Buffer Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	RTTB3I	0
Bit 4	R	RTTB2I	0
Bit 3	R	RTTB1I	0
Bit 2	R	RTOP3I	0
Bit 1	R	RTOP2I	0
Bit 0	R	RTOP1I	0

This register provides interrupt status of the three tributary path overhead processor and of the three tributary trace buffers in the TUPP-PLUS.

RTOP1I:

RTOP1I identifies tributary path overhead processor #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #1 will not be reported by the RTOP1I bit.

RTOP2I:

RTOP2I identifies tributary path overhead processor #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #2 will not be reported by the RTOP2I bit.

RTOP3I:

RTOP1I identifies tributary path overhead processor #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary path overhead processor #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary path overhead processor #3 will not be reported by the RTOP3I bit.

RTTB1I:

RTTB1I identifies tributary trace buffer #1 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #1 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #1 will not be reported by the RTTB1I bit.

RTTB2I:

RTTB2I identifies tributary trace buffer #2 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #2 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #2 will not be reported by the RTTB2I bit.

RTTB3I:

RTTB1I identifies tributary trace buffer #3 as the source of a pending interrupt. It is necessary to read the various interrupt status registers in tributary trace buffer #3 to determine the event causing the interrupt and to clear the interrupt. Interrupts disabled at tributary trace buffer #3 will not be reported by the RTTB3I bit.

Register 0CH: RTOP #1 and RTTB #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	ALGO2	0
Bit 6	R/W	PER5	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RDI10	0
Bit 2	R/W	PDI[2]	1
Bit 1	R/W	PDI[1]	1
Bit 0	R/W	PDI[0]	0

This register configures the operation of RTOP #1 and RTTB #1.

PDI[2:0]:

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (out of TU3 mode) or the C2 byte (in TU3 mode). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

PER5:

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

ALGO2:

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first

dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.

Register 0DH: RTOP #2 and RTTB #2 Configuration

Bit	Type	Function	Default
Bit 7	R/W	ALGO2	0
Bit 6	R/W	PER5	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RDI10	0
Bit 2	R/W	PDI[2]	1
Bit 1	R/W	PDI[1]	1
Bit 0	R/W	PDI[0]	0

This register configures the operation of RTOP #2 and RTTB #2.

PDI[2:0]:

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (for non-TU3 payloads) or the C2 byte (for TU3 payloads). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

PER5:

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

ALGO2:

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first

dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.

Register 0EH: RTOP #3 and RTTB #3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	ALGO2	0
Bit 6	R/W	PER5	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RDI10	0
Bit 2	R/W	PDI[2]	1
Bit 1	R/W	PDI[1]	1
Bit 0	R/W	PDI[0]	0

This register configures the operation of RTOP #3 and RTTB #3.

PDI[2:0]:

The PDI[2:0] bits specifies the code used to convey tributary path defect indication (PDI-V) in the V5 byte (for non-TU3 payloads) or the C2 byte (for TU3 payloads). For TU3 payloads, the PDI[2] bit is sign extended to form the byte value used for the PDI-V detection.

RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

PER5:

The PER5 bit controls the number of identical tributary path trace messages needed for the message to become accepted. When PER5 is set high, a messages is accepted when it is received unchanged five times. When PER5 is set low, the message is accepted after three identical repetitions.

ALGO2:

The ALGO2 bit controls the algorithm used to detect trail trace identifier unstable alarms. When ALGO2 is set high, a counter starts on the first

dissimilar identifier and cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold. When ALGO2 is set low, the counter increments on each dissimilar identifier and is cleared to zero when the same identifier is received enough times to be accepted. TIU is declared when the count exceeds the programmable TIU threshold.

Register 10H: Tributary Alarm AIS Control

Bit	Type	Function	Default
Bit 7	R/W	LOMAIS	0
Bit 6	R/W	LOPAIS	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PSLMAIS	0
Bit 2	R/W	PSLUAIS	0
Bit 1	R/W	TIMAIS	0
Bit 0	R/W	TIUAIS	0

This register controls the insertion of tributary path AIS as a result of tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

TIUAIS:

The TIUAIS bit is an active high AIS insertion enable. When TIUAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIUAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

TIMAIS:

The TIMAIS bit is an active high AIS insertion enable. When TIMAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIMAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

PSLUAIS:

The PSLUAIS bit is an active high AIS insertion enable. When PSLUAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in path signal label unstable state. When PSLUAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

PSLMAIS:

The PSLMAIS bit is an active high AIS insertion enable. When PSLMAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

LOPAIS:

The LOPAIS bit is an active high AIS insertion enable. When LOPAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in loss of pointer state. When LOPAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries. This bit is logically OR'ed with the bit of the same name in TUPP-PLUS Master Incoming Configuration register.

LOMAIS:

The LOMAIS bit is an active high AIS insertion enable. When LOMAIS is set high, AIS is automatically generated on the outgoing data stream for all tributaries that are in loss of tributary multiframe state. When LOMAIS is set low, the generation of AIS on the outgoing data stream is inhibited. LOMAIS has no effect on TU3 streams.

Register 11H: Tributary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	LOMRDI	0
Bit 6	R/W	LOPRDI	0
Bit 5	R/W	AISRDI	0
Bit 4	R/W	UNEQRDI	0
Bit 3	R/W	PSLMRDI	0
Bit 2	R/W	PSLURDI	0
Bit 1	R/W	TIMRDI	0
Bit 0	R/W	TIURDI	0

This register controls the insertion of tributary path RDI on the receive alarm port (RAD) and optionally on the V5 byte (G1 in TU3 mode) as a result of tributary pointer alarms, tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

TIURDI:

The TIURDI bit is an active high RDI insertion enable. When TIURDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIURDI is set low, reporting of RDI due to TIU is inhibited.

TIMRDI:

The TIMRDI bit is an active high RDI insertion enable. When TIMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIURDI is set low, reporting of RDI due to TIM is inhibited.

PSLURDI:

The PSLURDI bit is an active high RDI insertion enable. When PSLURDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path

signal label unstable state. When PSLURDI is set low, reporting of RDI due to PSLU is inhibited.

PSLMRDI:

The PSLMRDI bit is an active high RDI insertion enable. When PSLMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMRDI is set low, reporting of RDI due to PSLM is inhibited.

UNEQRDI:

The UNEQRDI bit is an active high RDI insertion enable. When UNEQRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in unequipped state. When UNEQRDI is set low, reporting of RDI due to UNEQ is inhibited.

AISRDI:

The AISRDI bit is an active high RDI insertion enable. When AISRDI is set high, RDI is reported on RAD and optionally the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in incoming AIS state. When AISRDI is set low, reporting of RDI due to AIS is inhibited.

LOPRDI:

The LOPRDI bit is an active high RDI insertion enable. When LOPRDI is set high, RDI is reported on RAD and optionally the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of pointer state. When LOPRDI is set low, reporting of RDI due to LOP is inhibited.

LOMRDI:

The LOMRDI bit is an active high RDI insertion enable. When LOMRDI is set high, RDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of multiframe state. When LOMRDI is set low, reporting of RDI due to LOM is inhibited.

Register 12H: Tributary Auxiliary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	NOLOMARDI	1
Bit 6	R/W	NOLOPARDI	1
Bit 5	R/W	NOAISARDI	1
Bit 4	R/W	UNEQARDI	0
Bit 3	R/W	PSLMARDI	0
Bit 2	R/W	PSLUARDI	0
Bit 1	R/W	TIMARDI	0
Bit 0	R/W	TIUARDI	0

This register controls the insertion of tributary path auxiliary RDI on the receive alarm port (RAD) and optionally on the V5 byte (G1 in TU3 mode) as a result of tributary pointer alarms, tributary path signal label alarms, tributary trace identifier alarms and tributary multiframe alarms.

TIUARDI:

The TIUARDI bit is an active high auxiliary RDI insertion enable. When TIUARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier unstable state. When TIURDI is set low, reporting of auxiliary RDI due to TIM is inhibited.

TIMARDI:

The TIMARDI bit is an active high auxiliary RDI insertion enable. When TIMARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in trace identifier mismatch state. When TIUARDI is set low, reporting of auxiliary RDI due to TIM is inhibited.

PSLUARDI:

The PSLUARDI bit is an active high auxiliary RDI insertion enable. When PSLUARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are

in path signal label unstable state. When PSLUARDI is set low, reporting of auxiliary RDI due to PSLU is inhibited.

PSLMARDI:

The PSLMARDI bit is an active high auxiliary RDI insertion enable. When PSLMARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMARDI is set low, reporting of auxiliary RDI due to PSLM is inhibited.

UNEQARDI:

The UNEQARDI bit is an active high auxiliary RDI insertion enable. When UNEQARDI is set high, ARDI is reported on RAD and optionally in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in unequipped state. When UNEQARDI is set low, the reporting of auxiliary RDI due to UNEQ is inhibited.

NOLOPARDI:

The NOLOPARDI bit is an active high auxiliary RDI insertion disable. When NOLOPARDI is set high, ARDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of pointer state. NOLOPARDI has precedence over TIUARDI, TIMARDI, PSLUARDI and PSLMARDI. When NOLOPARDI is set low, reporting of RDI is according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOAISARDI:

The NOAISARDI bit is an active high auxiliary RDI insertion disable. When NOAISARDI is set high, auxiliary RDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in incoming AIS state. NOAISARDI has precedence over TIUARDI, TIMARDI, PSLUARDI and PSLMARDI. When NOAISARDI is set low, reporting of RDI is according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOLOMARDI:

The NOLOMARDI bit is an active high auxiliary RDI insertion disable. When NOLOMARDI is set high, ARDI is not reported on RAD nor in the V5 byte (G1 byte in TU3 mode) of the outgoing data stream for all tributaries that are in loss of multiframe state. When NOLOMARDI is set low, reporting of RDI is

according to TIUARDI, TIMARDI, PSLUARDI and PSLMARDI and the associated alarm states.

Register 13H: Tributary PDI Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LOPPDI	0
Bit 5	R/W	AISPDI	0
Bit 4	R/W	UNEQPDI	0
Bit 3	R/W	PDIVPDI	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the insertion of tributary path defect indications (PDI) on the receive alarm port (RAD) as a result of tributary pointer alarms, tributary unequipped alarms, and tributary path defect indication alarms.

PDIVPDI:

The PDIVPDI bit is an active high path PDI insertion enable. When PDIVPDI is set high, PDI-P is reported on RAD when tributary path defect indication (nominally 'b110) is detected in the tributary path signal label of the associated incoming tributary. When PDIVPDI is set low, reporting of path PDI due to PDI-V is inhibited.

UNEQPDI:

The UNEQPDI bit is an active high path PDI insertion enable. When UNEQPDI is set high, PDI-P is reported on RAD when tributary unequipped indication ('b000) is detected in the tributary path signal label of the associated incoming tributary. When UNEQPDI is set low, reporting of path PDI due to UNEQ is inhibited.

AISPDI:

The AISPDI bit is an active high path PDI insertion enable. When AISPDI is set high, PDI-P is reported on RAD when the associated incoming tributary is in AIS state. When AISPDI is set low, reporting of path PDI due to AIS is inhibited.

LOPPDI:

The LOPPDI bit is an active high path PDI insertion enable. When LOPPDI is set high, PDI-P is reported on RAD when the associated incoming tributary is in loss of pointer state. When LOPPDI is set low, reporting of path PDI due to LOP is inhibited.

9.2 VTPP #1, VTPP #2 and VTPP #3 Registers

Register 20H, 40H, 60H: VTPP, TU3 or TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the VTPP. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When IIDLE is set high, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labeled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has precedence over the IPAIS bit.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode, is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 21H-26H, 41H-46H, 61H-66H: VTPP, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #1 in the corresponding TUG2 . When IIDLE is set high, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labeled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has precedence over the IPAIS bit.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is

inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the TUG2 tributary group. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 27H, 47H, 67H: VTPP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 loss of pointer interrupts.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. In TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of the TU3 pointer. Out of TU3 mode, the LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set high when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also

acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TUPP-PLUS.

Register 28H-2EH, 48H-4EH, 68H-6EH: VTPP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #2 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labeled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has precedence over the IPAIS bit.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 2FH, 4FH, 6FH: VTPP, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 30H-36H, 50H-56H, 70H-76H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #3 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labeled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has precedence over the IPAIS bit.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 37H, 57H, 77H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 38H-3EH, 58H-5EH, 78H-7EH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	IIDLE	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or, TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes. The IPAIS bit has no effect when IIDLE is set high.

IIDLE:

The IIDLE bit enables the insertion of path idle for tributary TU #4 in the corresponding TUG2. When IIDLE is set high, tributary payload bytes, except V5 is replaced by the idle code. The V5 byte is always set to all-zero to yield correct BIP-2 and to indicate tributary unequipped. The outgoing pointer is computed from the incoming pointer value and the relative frame offsets as per normal. The idle code is selectable to be all zeros or all ones as controlled by the ICODE bit. In order for the C2 byte to be labeled unequipped, the ICODE bit must be set low in TU3 mode. The IIDLE bit has precedence over the IPAIS bit.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication as directed by the IIDLE bit. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

CONFIG[1:0]:

The CONFIG[1:0] bits are read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 3FH, 5FH, 7FH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3, or TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register A0H, C0H, E0H: VTPP, TU3 or TU #1 in TUG2 #1, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the alarm status of the TU3 mapped into a TUG3 handled by the VTPP. Out of TU3 mode, this register reports the alarm status of TU #1 in TUG2 #1.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in TUG2 #1 or TU3 depending on whether the VTPP is in TU3 mode. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in TUG2 #1 or the H1 byte of tributary TU3 depending on whether the VTPP is in TU3 mode. The SS[1:0] bits are not filtered and must be software de-bounced.

Register A1H-A6H, C1H-C6H, E1H-E6H: VTPP, TU #1 in TUG2 #2 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register A7H, C7H, E7H: VTPP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 AIS interrupts.

AIS1I:

The AIS1I bit identifies the source of tributary path AIS interrupts. In TU3 mode, the AIS1I bit reports and acknowledges AIS interrupt of the TU3 stream. Out of TU3 mode, the AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set high when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

AIS2I-AIS7I:

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which

also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register A8H-AEH, C8H-CEH, E8H-EEH: VTPP, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low.

Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register AFH, CFH, EFH: VTPP, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register B0H-B6H, D0H-D6H, F0H-F6H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low.

Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register B7H, D7H, F7H: VTPP, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register B8H-BEH, D8H-DEH, F8H-FEH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low.

Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register BFH, DFH, FFH: VTPP, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

9.3 RTOP #1, RTOP #2 and RTOP #3 Registers

Register 100H, 200H, 300H: RTOP, TU3 or TU #1 in TUG2 #1, Configuration

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTOP is in TU3 mode. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in TUG2 #1 or TU3 depending on whether the RTOP is in TU3 mode. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in TUG2 #1 or TU3. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in TUG2 #1 or TU3. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in TUG2 #1 or TU3. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in TUG2 #1 or the TU3 mapped into a TUG3. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, BIP-2 two errors are counted on a nibble basis; the BIP error count is incremented once for each BIP-2 bit that is in error.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 101H, 201H, 301H: RTOP, TU3 or TU #1 in TUG2 #1, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	PDIVEN	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

In TU3 mode, this register reports the alarm status of the TU3 mapped into a TUG3. Out of TU3 mode, this register reports alarm status and configures TU #1 in TUG2 #1.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in TUG2 #1 or the TU3 mapped in a TUG3 when RDIZ7EN is low. Out of TU3 mode, RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

In TU3 mode, RDIV is set high when the RDI bit in the G1 byte is set high for five or ten consecutive frames as determined by the RDI10 bit. RDIV is set low when the RDI bit is set low for five or ten consecutive frames as determined by the RDI10 bit.

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in TUG2 #1 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses

0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit. RFIV is not used when TU3 mode is enabled.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in TUG2 #1 or the TU3 mapped in a TUG3 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte or the G1 byte is seen for five or ten consecutive multiframes (frames in TU3 mode) as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in TUG2 #1 or TU3. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in TUG2 #1 or TU3. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN

The PDIVEN bit controls the insertion of tributary path defect indication for tributary TU #1 in TUG2 #1 or TU3 in the receive alarm port (RAD). When PDIVEN is set high, PDI-V is asserted regardless of the state of the path signal label. When PDIVEN is set low, PDI-V is asserted if the incoming path signal label matches the PDI code in the PDI[2:0] bit of the corresponding RTOP Configuration register.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in TUG2 #1 or TU3 mapped in TUG3. TUPTE is set high if tributary TU #1 or the TU3 is to be terminated in the network element

containing this TUPP-PLUS device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #1 or the TU3 is part of the through traffic in the network element containing this TUPP-PLUS device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

Out of TU3 mode, the RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits. When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

In TU3 mode, the RDIZ7EN bit is used to control whether RDI or enhanced RDI is reported. When RDIZ7EN is set low, the RDI bit in the G1 byte is used to control the RDIV register bit. When RDIZ7EN is set high, the three bit extended RDI code in the G1 byte is used to control the ERDIV[2:0] register bits.

Register 102H, 202H, 302H: RTOP, TU3 or TU #1 in TUG2 #1, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register configures the expected path signal label of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register configures the expected path signal label of TU #1 in TUG2 #1.

EPSL[7:0]:

In TU3 mode, the EPSL[7:0] bits specifies the expected path signal label of the TU3 stream. Out of TU3 mode, EPSL[2:0] specifies the expected path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 103H, 203H, 303H: RTOP, TU3 or TU #1 in TUG2 #1, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	APSL[7]	0
Bit 6	R/W	APSL[6]	0
Bit 5	R/W	APSL[5]	0
Bit 4	R/W	APSL[4]	0
Bit 3	R/W	APSL[3]	0
Bit 2	R/W	APSL[2]	0
Bit 1	R/W	APSL[1]	0
Bit 0	R/W	APSL[0]	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the accepted path signal label of the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the accepted path signal label of TU #1 in TUG2 #1.

APSL[7:0]:

In TU3 mode, the APSL[7:0] bits reports the accepted path signal label of the TU3 stream. Out of TU3 mode, APSL[2:0] specifies the accepted path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 104H, 204H, 304H: RTOP, TU3 or TU #1 in TUG2 #1, BIP-2/BIP-8 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 105H, 205H, 305H: RTOP, TU3 or TU #1 in TUG2 #1, BIP-2/BIP-8 Error Count MSB

Bit	Type	Function	Default
Bit 7	R	BIP[15]	X
Bit 6	R	BIP[14]	X
Bit 5	R	BIP[13]	X
Bit 4	R	BIP[12]	X
Bit 3	R	BIP[11]	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

In TU3 mode (TU3 bit in VTPP Configuration register set high), these registers report the number of block interleave parity (BIP-8) errors detected in the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #1. These registers do not saturate.

BIP[15:0]:

The BIP[15:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2/BIP-8 registers were polled. The BIP-2/BIP-8 registers are polled by writing to the Input Signal Activity, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2/BIP-8 registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2/BIP-8 errors may be accumulated on a nibble/bit basis or block basis as controlled by the BLKBIP register bit. In TU3 mode, all BIP[15:0] are valid. Out of TU3 mode, only BIP[10:0] are valid, BIP[15:11] are held low.

Register 106H, 206H, 306H: RTOP, TU3 or TU #1 in TUG2 #1, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 107H, 207H, 307H: RTOP, TU3 or TU #1 in TUG2 #1, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

In TU3 mode (TU3 bit in VTPP Configuration register set high), these registers report the number of far end block errors (FEBE) detected in the TU3 mapped into a TUG3 handled by the RTOP. Out of TU3 mode, this register reports the number of far end block errors (FEBE) detected in TU #1 in TUG2 #1.

FEBE[15:0]:

The FEBE[15:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity, Accumulate Trigger register. The write access transfers the internally accumulated error counts to the FEBE registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.In TU3 mode, all FEBE[15:0] are valid. Out of TU3 mode, only FEBE[10:0] are valid, FEBE[15:11] are held low.

Register 108H, 110H, 118H, 120H, 128H, 130H:
Register 208H, 210H, 218H, 220H, 228H, 230H:
Register 308H, 310H, 318H, 320H, 328H, 330H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the correspondiing TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 109H, 111H, 119H, 121H, 129H, 131H:
Register 209H, 211H, 219H, 221H, 229H, 231H:
Register 309H, 311H, 319H, 321H, 329H, 331H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	PDIVEN	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R/W	ERDIV[2]	0
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #1 in the corresponding TUG2 . The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] register bits for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in the corresponding TUG2. TUPTE is set high if tributary TU #1 is to be terminated in the network element containing this TUPP-PLUS device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #1 is part of the through traffic in the network

element containing this TUPP-PLUS device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #1 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 10AH, 112H, 11AH, 122H, 12AH, 132H:
Register 20AH, 212H, 21AH, 222H, 22AH, 232H:
Register 30AH, 312H, 31AH, 322H, 32AH, 332H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #1 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 10BH, 113H, 11BH, 123H, 12BH, 133H:
Register 20BH, 213H, 21BH, 223H, 22BH, 233H:
Register 30BH, 313H, 31BH, 323H, 32BH, 333H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted path signal label of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #1 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 10CH, 114H, 11CH, 124H, 12CH, 134H:
Register 20CH, 214H, 21CH, 224H, 22CH, 234H:
Register 30CH, 314H, 31CH, 324H, 32CH, 334H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 10DH, 115H, 11DH, 125H, 12DH, 135H:
Register 20DH, 215H, 21DH, 225H, 22DH, 235H:
Register 30DH, 315H, 31DH, 325H, 32DH, 335H:
RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These sets of registers report the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval. These registers have no effect in TU3 mode. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to any of the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2 errors may be accumulated on a nibble basis or block basis as controlled by the BLKBIP register bit.

Register 10EH, 116H, 11EH, 126H, 12EH, 136H:
Register 20EH, 216H, 21EH, 226H, 22EH, 236H:
Register 30EH, 316H, 31EH, 326H, 32EH, 336H:
TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 10FH, 117H, 11FH, 127H, 12FH, 137H:
Register 20FH, 217H, 21FH, 227H, 22FH, 237H:
Register 30FH, 317H, 31FH, 327H, 32FH, 337H:
TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval. These registers have no effect in TU3 mode.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by applying by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 138H, 238H, 338H: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 change of path signal label interrupts.

COPSL1I:

The COPSL1I bit identifies the source of change of path signal label interrupts. In TU3 mode, the COPSL1I bit reports and acknowledges COPSL interrupts of the TU3 stream. Out of TU3 mode, the COPSL1I bit reports and acknowledges COPSL interrupt of TU #1 in TUG2 #1. Interrupts are generated when the accepted PSL changes. The COPSL1I bit is set high when a change of PSL event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL1I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

COPSL2I-COPSL7I:

The COPSL2I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, COPSL2I to COPSL7I bits report and acknowledge COPSL interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this

register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TUPP-PLUS.

Register 139H, 239H, 339H: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 path signal label mismatch interrupts.

PSLM1I:

The PSLM1I bit identifies the source of path signal label mismatch interrupts. In TU3 mode, the PSLM1I bit reports and acknowledges PSLM interrupts of the TU3 stream. Out of TU3 mode, the PSLM1I bit reports and acknowledges PSLM interrupt of TU #1 in TUG2 #1. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. The PSLM1I bit is set high when a change of in the PSL matched state occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM1I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, PSLM2I to PSLM7I bits report and acknowledge PSLM interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when

a change of PSL matched state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 13AH, 23AH, 33AH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 path signal label unstable interrupts.

PSLU1I:

The PSLU1I bit identifies the source of path signal label unstable interrupts. In TU3 mode, the PSLU1I bit reports and acknowledges PSLU interrupts of the TU3 stream. Out of TU3 mode, the PSLU1I bit reports and acknowledges PSLU interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received PSL becomes unstable or returns to stable. The PSLU1I bit is set high when a change of in the PSL unstable state occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU1I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

PSLU2I-PSLU7I:

The PSLU2I to PSLU7I bits identify the source of path signal label mismatch interrupts. PSLU2I to PSLU7I bits report and acknowledge PSLU interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this

register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 13BH, 23BH, 33BH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 remote defect indication interrupts.

RDI1I:

The RDI1I bit identify the source of remote defect indication interrupts. In TU3 mode, the RDI1I bit reports and acknowledges RDI interrupt of the TU3 stream. Out of TU3 mode, the RDI1I bit reports and acknowledges RDI interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received RDI state changes. The RDI1I bit is set high when a change of RDI state event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI1I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

RDI2I-RDI7I:

The RDI2I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. Out of TU3 mode, the RDI2I to RDI7I bits report and acknowledge RDI interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which

also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 13CH, 23CH, 33CH: RTOP, TU3 Auxiliary RDI Interrupt or TU #1 in TUG2 #1 to TUG2 #7 RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 auxiliary remote defect indication interrupts.

RFI1I:

The RFI1I bit identify the source of remote defect indication interrupts. In TU3 mode, the RFI1I bit reports and acknowledges auxiliary RDI interrupt of the TU3 stream. Out of TU3 mode, the RFI1I bit reports and acknowledges RFI interrupt of TU #1 in TUG2 #1. Interrupts are generated when the received RFI state changes. The RFI1I bit is set high when a change of RDI state event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI1I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote defect indication events.

RFI2I-RFI7I:

The RFI2I to RFI7I bits identify the source of remote failure indication interrupts. RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled

(RFIE set low) and may be polled to detect change of remote failure indication events.

Register 13DH, 23DH, 33DH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode of the tributaries TU #1 in TUG2 #1 to TUG2 #7 and the IBER mode of the TU3 mode.

IBER1:

The IBER1 bit controls in band error reporting for tributary TU #1 in TUG2 #1 or TU3 in a TUG3. In TU3 mode, setting the IBER1 high causes in band error reporting information to be inserted in the G1 byte of the TU3. In non-TU3 modes, setting the IBER1 bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of TUG2 #1. When the IBER1 bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of TUG2 #1 or the G1 byte of the TU3 is not modified.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of the corresponding TUG2 is not modified.

Register 13EH, 23EH, 33EH: RTOP, TU3 or TU #1 in TUG2 #1 to TUG2 #7, Controllable Output Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	COUT7	0
Bit 5	R/W	COUT6	0
Bit 4	R/W	COUT5	0
Bit 3	R/W	COUT4	0
Bit 2	R/W	COUT3	0
Bit 1	R/W	COUT2	0
Bit 0	R/W	COUT1	0

This register controls the configurable output (COUT) output for the tributaries TU #1 in TUG2 #1 to TUG2 #7and COUT output for the TU3 mode.

COUT1:

The COUT1 bit controls the COUT output for tributary TU #1 in TUG2 #1 or TU3 in a TUG3. In TU3 mode, setting the COUT1 high will cause the COUT output to be set high when the incoming data stream is part of the TU3 in a TUG3. In non-TU3 modes, setting the COUT1 high will cause the COUT output to be high when the incoming data stream is part of tributary TU #1 in TUG2 #1. When COUT1 is set low, the COUT output will be low when the incoming data stream is part of tributary TU #1 in TUG2 #1 or a TU3 in a TUG3.

COUT2-COUT7:

The COUT2 to COUT7 bits control the COUT output for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting a COUT*x* bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #1 of the corresponding TUG2. When an COUT*x* bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #1 of the corresponding TUG2.

Register 140H, 148H, 150H, 158H, 160H, 168H, 170H:
Register 240H, 248H, 250H, 258H, 260H, 268H, 270H:
Register 340H, 348H, 350H, 358H, 360H, 368H, 370H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #2 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #2 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #2 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #2 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 141H, 149H, 151H, 159H, 161H, 169H, 171H:
Register 241H, 249H, 251H, 259H, 261H, 269H, 271H:
Register 341H, 349H, 351H, 359H, 361H, 369H, 371H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	PDIVEN	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #2 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #2 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #2 in the corresponding TUG2 . The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #2 in the corresponding TUG2. TUPTE is set high if tributary TU #2 is to be terminated in the network element containing this TUPP-PLUS device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #2 is part of the through traffic in the network element containing this TUPP-PLUS device. In this case, tributary AIS is only

inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #2 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 142H, 14AH, 152H, 15AH, 162H, 16AH, 172H:
Register 242H, 24AH, 252H, 25AH, 262H, 26AH, 272H:
Register 342H, 34AH, 352H, 35AH, 362H, 36AH, 372H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #2 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 143H, 14BH, 153H, 15BH, 163H, 16BH, 173H:
Register 243H, 24BH, 253H, 25BH, 263H, 26BH, 273H:
Register 343H, 34BH, 353H, 35BH, 363H, 36BH, 373H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted path signal label of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #2 in TUG2 #1 to TUG2 #7. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 144H, 14CH, 154H, 15CH, 164H, 16CH, 174H:
Register 244H, 24CH, 254H, 25CH, 264H, 26CH, 274H:
Register 344H, 34CH, 354H, 35CH, 364H, 36CH, 374H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 145H, 14DH, 155H, 15DH, 165H, 16DH, 175H:
Register 245H, 24DH, 255H, 25DH, 265H, 26DH, 275H:
Register 345H, 34DH, 355H, 35DH, 365H, 36DH, 375H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding

TUG2 tributary group is configured to TU2 (VT6) mode, the data in associated registers are invalid. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 146H, 14EH, 156H, 15EH, 166H, 16EH, 176H:
Register 246H, 24EH, 256H, 25EH, 266H, 26EH, 276H:
Register 346H, 34EH, 356H, 35EH, 366H, 36EH, 376H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 147H, 14FH, 157H, 15FH, 167H, 16FH, 177H:
Register 247H, 24FH, 257H, 25FH, 267H, 26FH, 277H:
Register 347H, 34FH, 357H, 35FH, 367H, 36FH, 377H:
RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group

is configured to TU2 (VT6) mode, the associated registers in this set contain invalid data.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger registers. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneoulsy to begin a new cycle of error accumulation.

Register 178H, 278H, 378H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated COPSL*x*I bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Register 179H, 279H, 379H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated PSLM*x*I bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 17AH, 27AH, 37AH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated PSLU*x*I bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 17BH, 27BH, 37BH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated RDI*x*I bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 17CH, 27CH, 37CH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated RFI*x*I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 17DH, 27DH, 37DH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #2 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #2 of the corresponding TUG2 is not modified.

Register 17EH, 27EH, 37EH: TU #2 in TUG2 #1 to TUG2 #7, Controllable Output Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	COUT7	0
Bit 5	R/W	COUT6	0
Bit 4	R/W	COUT5	0
Bit 3	R/W	COUT4	0
Bit 2	R/W	COUT3	0
Bit 1	R/W	COUT2	0
Bit 0	R/W	COUT1	0

This register controls the COUT output for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

COUT1-COUT7:

The COUT1 to COUT7 bits control the COUT output for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting a COUT*x* bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #2 of the corresponding TUG2. When an COUT*x* bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #2 of the corresponding TUG2.

Register 180H, 188H, 190H, 198H, 1A0H, 1A8H, 1B0H:
Register 280H, 288H, 290H, 298H, 2A0H, 2A8H, 2B0H:
Register 380H, 388H, 390H, 398H, 3A0H, 3A8H, 3B0H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored. The RFIE bit is not used when the RTOP is in TU3 mode is enabled.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #3 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #3 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #3 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #3 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 181H, 189H, 191H, 199H, 1A1H, 1A9H, 1B1H:
Register 281H, 289H, 291H, 299H, 2A1H, 2A9H, 2B1H:
Register 381H, 389H, 391H, 399H, 3A1H, 3A9H, 3B1H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	PDIVEN	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #3 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #3 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #3 in the corresponding TUG2 . The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #3 in the corresponding TUG2. TUPTE is set high if tributary TU #3 is to be terminated in the network element containing this TUPP-PLUS device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #3 is part of the through traffic in the network element containing this TUPP-PLUS device. In this case, tributary AIS is only

inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #3 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 182H, 18AH, 192H, 19AH, 1A2H, 1AAH, 1B2H:
Register 282H, 28AH, 292H, 29AH, 2A2H, 2AAH, 2B2H:
Register 382H, 38AH, 392H, 39AH, 3A2H, 3AAH, 3B2H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected the path signal label of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #3 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 183H, 18BH, 193H, 19BH, 1A3H, 1ABH, 1B3H:
Register 283H, 28BH, 293H, 29BH, 2A3H, 2ABH, 2B3H:
Register 383H, 38BH, 393H, 39BH, 3A3H, 3ABH, 3B3H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted the path signal label of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #3 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 184H, 18CH, 194H, 19CH, 1A4H, 1ACH, 1B4H:
Register 284H, 28CH, 294H, 29CH, 2A4H, 2ACH, 2B4H:
Register 384H, 38CH, 394H, 39CH, 3A4H, 3ACH, 3B4H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 185H, 18DH, 195H, 19DH, 1A5H, 1ADH, 1B5H:
Register 285H, 28DH, 295H, 29DH, 2A5H, 2ADH, 2B5H:
Register 385H, 38DH, 395H, 39DH, 3A5H, 3ADH, 3B5H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding

TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the data in the associated registers are invalid. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 186H, 18EH, 196H, 19EH, 1A6H, 1AEH, 1B6H:
Register 286H, 28EH, 296H, 29EH, 2A6H, 2AEH, 2B6H:
Register 386H, 38EH, 396H, 39EH, 3A6H, 3AEH, 3B6H:
TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 187H, 18FH, 197H, 19FH, 1A7H, 1AFH, 1B7H:
Register 287H, 28FH, 297H, 29FH, 2A7H, 2AFH, 2B7H:
Register 387H, 38FH, 397H, 39FH, 3A7H, 3AFH, 3B7H:
RTOP, TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invaild data in TU3 mode. When the corresponding TUG2 tributary group

is configured to TU2 (VT6) or VT3 mode, the associated registers in this set contain invalid data.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 1B8H, 2B8H, 3B8H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Reserved	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated COPSL*x*I bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bits must be written with a logic 0 for proper operation of the TUPP-PLUS.

Register 1B9H, 2B9H, 3B9H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated PSLM*x*I bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 1BAH, 2BAH, 3BAH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated PSLU*x*I bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 1BBH, 2BBH, 3BBH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated RDI*x*I bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 1BCH, 2BCH, 3BCH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated RFI*x*I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 1BDH, 2BDH, 3BDH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #3 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #3 of the corresponding TUG2 is not modified.

Register 1BEH, 2BEH, 3BEH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Controllable Output Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	COUT7	0
Bit 5	R/W	COUT6	0
Bit 4	R/W	COUT5	0
Bit 3	R/W	COUT4	0
Bit 2	R/W	COUT3	0
Bit 1	R/W	COUT2	0
Bit 0	R/W	COUT1	0

This register controls the COUT output for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

COUT1-COUT7:

The COUT1 to COUT7 bits control the COUT output for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting a COUT*x* bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #3 of the corresponding TUG2. When an COUT*x* bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #3 of the corresponding TUG2.

Register 1C0H, 1C8H, 1D0H, 1D8H, 1E0H, 1E8H, 1F0H:
Register 2C0H, 2C8H, 2D0H, 2D8H, 2E0H, 2E8H, 2F0H:
Register 3C0H, 3C8H, 3D0H, 3D8H, 3E0H, 3E8H, 3F0H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #4 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RDIV bit when RDIE is set high. Interrupts due to RDIV status change are masked when RDIE is set low.

When RDIZ7EN is set high, an interrupt is generated upon assertion or negation events of the ERDIV[2:0] bits when RDIE is set high. Interrupts due to ERDIV[2:0] status change are masked when RDIE is set low.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #4 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #4 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #4 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #4 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 1C1H, 1C9H, 1D1H, 1D9H, 1E1H, 1E9H, 1F1H:
Register 2C1H, 2C9H, 2D1H, 2D9H, 2E1H, 2E9H, 2F1H:
Register 3C1H, 3C9H, 3D1H, 3D9H, 3E1H, 3E9H, 3F1H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	PDIVEN	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers configures and reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP and RTTB Configuration registers (addresses 0CH, 0DH, and 0EH).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #4 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #4 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

PDIVEN:

The PDIVEN bit modifies the payload defect indication status PDIV of tributary TU #4 in the corresponding TUG2 . The PDIV output is set high when the PSL in the V5 byte is set to the bit pattern specified by the PDICODE[2:0] input for five consecutive multiframes. The PDIV output is set low when the PSL is set to any other bit pattern for five consecutive multiframes. When PDIVEN is set high, the PDIV output is permanently set high independent of the tributary's defect status until the PDIVEN is set low.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #4 in the corresponding TUG2. TUPTE is set high if tributary TU #4 is to be terminated in the network element containing this TUPP-PLUS device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 10H). TUPTE is set low if tributary TU #4 is part of the through traffic in the network element containing this TUPP-PLUS device. In this case, tributary AIS is only

inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #4 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 1C2H, 1CAH, 1D2H, 1DAH, 1E2H, 1EAH, 1F2H:
Register 2C2H, 2CAH, 2D2H, 2DAH, 2E2H, 2EAH, 2F2H:
Register 3C2H, 3CAH, 3D2H, 3DAH, 3E2H, 3EAH, 3F2H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #4 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 1C3H, 1CBH, 1D3H, 1DBH, 1E3H, 1EBH, 1F3H:
Register 2C3H, 2CBH, 2D3H, 2DBH, 2E3H, 2EBH, 2F3H:
Register 3C3H, 3CBH, 3D3H, 3DBH, 3E3H, 3EBH, 3F3H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of register reports the accepted path signal label of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated register in this set has no effect.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #4 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 1C4H, 1CCH, 1D4H, 1DCH, 1E4H, 1ECH, 1F4H:
Register 2C4H, 2CCH, 2D4H, 2DCH, 2E4H, 2ECH, 2F4H:
Register 3C4H, 3CCH, 3D4H, 3DCH, 3E4H, 3ECH, 3F4H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 1C5H, 1CDH, 1D5H, 1DDH, 1E5H, 1EDH, 1F5H:
Register 2C5H, 2CDH, 2D5H, 2DDH, 2E5H, 2EDH, 2F5H:
Register 3C5H, 3CDH, 3D5H, 3DDH, 3E5H, 3EDH, 3F5H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding

TUG2 tributary group is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated registers in this set contain invalid data. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 1C6H, 1CEH, 1D6H, 1DEH, 1E6H, 1EEH, 1F6H:
Register 2C6H, 2CEH, 2D6H, 2DEH, 2E6H, 2EEH, 2F6H:
Register 3C6H, 3CEH, 3D6H, 3DEH, 3E6H, 3EEH, 3F6H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1C7H, 1CFH, 1D7H, 1DFH, 1E7H, 1EFH, 1F7H:
Register 2C7H, 2CFH, 2D7H, 2DFH, 2E7H, 2EFH, 2F7H:
Register 3C7H, 3CFH, 3D7H, 3DFH, 3E7H, 3EFH, 3F7H:
RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. These registers contain invalid data in TU3 mode. When the corresponding TUG2 tributary group

is configured to TU2 (VT6), VT3 or TU12 (VT2) mode, the associated registers in this set contain invalid data.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneoulsly to begin a new cycle of error accumulation.

Register 1F8H, 2F8H, 3F8H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated COPSL*x*I bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Register 1F9H, 2F9H, 3F9H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated PSLM*x*I bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 1FAH, 2FAH, 3FAH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated PSLU*x*I bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 1FBH, 2FBH, 3FBH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated RDI*x*I bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 1FCH, 2FCH, 3FCH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated RFI*x*I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 1FDH, 2FDH, 3FDH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, In Band Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #4 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #4 of the corresponding TUG2 is not modified.

Register 1FEH, 2FEH, 3FEH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Controllable Output Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	COUT7	0
Bit 5	R/W	COUT6	0
Bit 4	R/W	COUT5	0
Bit 3	R/W	COUT4	0
Bit 2	R/W	COUT3	0
Bit 1	R/W	COUT2	0
Bit 0	R/W	COUT1	0

This register controls the COUT output for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

COUT1-COUT7:

The COUT1 to COUT7 bits control the COUT output for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting a COUT*x* bit high will force the COUT output to be high when the incoming data stream is part of tributary TU #4 of the corresponding TUG2. When an COUT*x* bit is low, the COUT output will be low when the incoming data stream is part of tributary TU #4 of the corresponding TUG2.

Register 1FFH, 2FFH, 3FFH: RTOP Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	BLKFEBE	0
Bit 0	R	BUSY	X

This register configures and reports the status of the various internal operations inside RTOP.

BUSY:

The BUSY bit indicates the status of the transfer of BIP and FEBE counts from the counters to the holding registers. BUSY is set high on the rising edge of the LCLK input or on a write access to any of the BIP or FEBE counters. BUSY is set low when all the counters values have been transferred to holding registers. The elapsed time shall be less than 10 µs.

BLKFEBE:

The block FEBE accumulation control bit selects between counting of FEBEs in the incoming TU3 stream on a block or bit basis. When BLKFEBE is set high, FEBE count codes in the range of 1 to 8 are accumulated on a block basis as a single FEBE event. All other codes are counted zero events. When BLKFEBE is set low, FEBE count codes in the range of 1 to 8 are accumulated on a bit basis as a up to 8 FEBE events. All other codes are counted zero events.

Reserved:

The Reserved bits must be written with a logic 0 for proper operation of the TUPP-PLUS.

9.4 RTTB #1, RTTB #2 and RTTB #3 Registers

Register 400H, 440H, 480H: RTTB, TU3 or TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

In TU3 mode (TU3 bit in VTPP Configuration register set high), this register reports the status and configures operational modes of the TU3 mapped into a TUG3 handled by the RTTB. Out of TU3 mode, this register reports the status and configures the operational modes of TU #1 in TUG2 #1.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in TUG2 #1 or TU3 When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in TUG2 #1 or TU3.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in TUG2 #1 or TU3. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #1 in TUG2 #1 or TU3.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in TUG2 #1 or TU3. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in TUG2 #1 or TU3. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of tributary group TUG2 #1. The CONFIG[1:0] bits have no effect in TU3 mode. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 401H-406H, 441H-446H, 481H-486H: RTTB, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	CONFIG[1]	1
Bit 6	R/W	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7. These registers have no effect in TU3 mode.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #1 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #1 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #1 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #1 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #1 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #1 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 408H-40EH, 448H-44EH, 488H-48EH: RTTB, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) mode, the associated register in this set has no effect.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #2 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #2 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #2 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #2 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #2 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #2 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 410H-416H, 450H-456H, 490H-496H: RTTB, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6) or VT3 mode, the associated register in this set has no effect.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #3 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #3 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #3 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

TIMV:

The TIMV bit indicates the trail trace identifier mismatch status of tributary TU #3 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #3 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #3 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 418H-41EH, 458H-45EH, 498H-49EH: RTTB, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	CONFIG[1]	1
Bit 6	R	CONFIG[0]	1
Bit 5	R/W	NOSYNC	0
Bit 4	R/W	LEN16	0
Bit 3	R	TIMV	X
Bit 2	R/W	TIME	0
Bit 1	R	TIUV	X
Bit 0	R/W	TIUE	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. These registers have no effect in TU3 mode. When the corresponding TUG2 tributary group is configured to TU2 (VT6), VT3 or, TU12 (VT2) mode, the associated register in this set has no effect.

TIUE:

The TIUE bit enables trail trace identifier unstable interrupts for tributary TU #4 in the corresponding TUG2. When TIUE is set high, an interrupt is generated upon detection of an unstable identifier and upon return to a stable identifier. Interrupts due to TIU status change are masked when TIUE is set low.

TIUV:

The TIUV bit indicates the trail trace identifier unstable status of tributary TU #4 in the corresponding TUG2.

TIME:

The TIME bit enables trail trace identifier mismatch interrupts for tributary TU #4 in the corresponding TUG2. When TIME is set high, an interrupt is generated upon detection of a mismatched identifier and upon return to a matched identifier. Interrupts due to TIM status change are masked when TIME is set low.

TIMV:

The TIUV bit indicates the trail trace identifier mismatch status of tributary TU #4 in the corresponding TUG2.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes for tributary TU #4 in the corresponding TUG2. When LEN16 is set high, the message length is set to 16 bytes. When LEN16 is set low, the message length is set to 64 bytes.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the synchronized writing of the path trace message into the trace buffer based on the contents of the message for tributary TU #4 in the corresponding TUG2. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set to logic one will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

CONFIG[1:0]:

The CONFIG[1:0] bits specify the tributary configuration of the corresponding tributary group TUG2. The configuration specified by the CONFIG[1:0] bits are selected as follows:

CONFIG[1]	CONFIG[0]	Configuration	Active TU (VT)
0	0	TU2 (VT6)	#1
0	1	VT3	#1, #2
1	0	TU12 (VT2)	#1, #2, #3
1	1	TU11 (VT1.5)	#1, #2, #3, #4

Register 420H, 460H, 4A0H: RTTB, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier mismatch interrupts.

TIM1I:

The TIM1I bit identifies the source of trail trace identifier mismatch interrupts. In TU3 mode, The TIM1I bit reports and acknowledges TIM interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIM1I bit reports and acknowledges TIM interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier mismatch state. The TIM1I bit is set high when a trail trace identifier mismatch event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIM1I bit remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

TIM2I-TIM7I:

The TIM2I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. TIM2I to TIM7I bits report and acknowledge TIM interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when

interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

Register 421H, 461H, 4A1H: RTTB, TU #2 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

Register 422H, 462H, 4A2H: RTTB, TU #3 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

Register 423H, 463H, 4A3H: RTTB, TU #4 in TUG2 #1 to TUG2 #7, TIM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIM7I	0
Bit 5	R	TIM6I	0
Bit 4	R	TIM5I	0
Bit 3	R	TIM4I	0
Bit 2	R	TIM3I	0
Bit 1	R	TIM2I	0
Bit 0	R	TIM1I	0

This register is used to identify and acknowledge trail trace identifier mismatch interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

TIM1I-TIM7I:

The TIM1I to TIM7I bits identify the source of trail trace identifier mismatch interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIM1I to TIM7I bits report and acknowledge TIM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier mismatch state. An TIM*x*I bit is set high when a trail trace identifier mismatch event on the corresponding tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIM*x*I remains valid when interrupts are not enabled (TIME set low) and may be polled to detect trail trace identifier mismatch events.

Register 424H, 464H, 4A4H: RTTB, TU3 or TU #1 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7. It is also used to identify and acknowledge TU3 trail trace identifier unstable interrupts.

TIU1I:

The TIU1I bit identifies the source of trail trace identifier unstable interrupts. In TU3 mode, The TIU1I bit reports and acknowledges TIU interrupt of the TU3 trail trace identifier. Out of TU3 mode, TIU1I bit reports and acknowledges TIU interrupt of TU #1 in TUG2 #1. Interrupts are generated upon change of identifier unstable state. The TIU1I bit is set high when a trail trace identifier unstable event and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. the TIU1I bit remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

TIU2I-TIU7I:

The TIU2I to TIU7I bits identify the source of trail trace identifier unstable interrupts. TIU2I to TIU7I bits report and acknowledge TIU interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts

are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

Register 425H, 465H, 4A5H: RTTB, TU #2 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) mode, the associated TIU*x*I bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #2 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

Register 426H, 466H, 4A6H: RTTB, TU #3 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6) or VT3 mode, the associated TIU*x*I bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #3 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

Register 427H, 467H, 4A7H: RTTB, TU #4 in TUG2 #1 to TUG2 #7, TIU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TIU7I	0
Bit 5	R	TIU6I	0
Bit 4	R	TIU5I	0
Bit 3	R	TIU4I	0
Bit 2	R	TIU3I	0
Bit 1	R	TIU2I	0
Bit 0	R	TIU1I	0

This register is used to identify and acknowledge trail trace identifier unstable interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

TIU1I-TIU7I:

The TIU1I to TIU7I bits identify the source of trail trace identifier unstable interrupts. In TU3 mode, these bits are unused and will return a logic 0 when read. When the corresponding TUG2 tributary group is configured for TU2 (VT6), VT3 or TU12 (VT2) mode, the associated TIM*x*I bit is unused and will return a logic 0 when read. When operational, the TIU1I to TIU7I bits report and acknowledge TIU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon change of identifier unstable state. An TIU*x*I bit is set high when a trail trace identifier unstable event on the corresponding tributary (TU #4 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. TIU*x*I remains valid when interrupts are not enabled (TIUE set low) and may be polled to detect trail trace identifier unstable events.

Register 428H, 468H, 4A8H: RTTB, TIU Threshold

Bit	Type	Function	Default
Bit 7	R/W	TIU64[3]	0
Bit 6	R/W	TIU64[2]	1
Bit 5	R/W	TIU64[1]	1
Bit 4	R/W	TIU64[0]	1
Bit 3	R/W	TIU16[3]	0
Bit 2	R/W	TIU16[2]	1
Bit 1	R/W	TIU16[1]	1
Bit 0	R/W	TIU16[0]	1

This register contains threshold for declaration of the trail trace identifier unstable alarm (TIU) for 16-byte and 64-byte tributary path trace messages.

TIU16[3:0]:

The 16-byte message trail trace identifier unstable threshold bits (TIU16[3:0]) controls level in the unstable counter at which to declare TIU. When ALGO2 is set low, each time a received message differs from the previous message, the unstable counter is incremented. When the count exceeds TIU16, the TIU alarm is declared. When ALGO2 is set high, a message that differs from the previous initiates the unstable counter to count once per message. When the count exceeds TIU16, the TIU alarm is declared. TIU is negated and the unstable counter cleared when a consistent message is repeated three or five times, as controlled by the PER5 bit, to become the accepted message.

TIU64[3:0]:

The 64-byte message trail trace identifier unstable threshold bits (TIU64[3:0]) controls level in the unstable counter at which to declare TIU. When ALGO2 is set low, each time a received message differs from the previous message, the unstable counter is incremented. When the count exceeds TIU64, the TIU alarm is declared. When ALGO2 is set high, a message that differs from the previous initiates the unstable counter to count once per message. When the count exceeds TIU64, the TIU alarm is declared. TIU is negated and the unstable counter cleared when a consistent message is repeated three or five times, as controlled by the PER5 bit, to become the accepted message.

Register 429H, 469H, 4A9H: RTTB, Indirect Tributary Select

Bit	Type	Function	Default
Bit 7	R/W	CPAGE	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TUG2[2]	0
Bit 3	R/W	TUG2[1]	0
Bit 2	R/W	TUG2[0]	0
Bit 1	R/W	TU[1]	0
Bit 0	R/W	TU[0]	0

This register contains the identity of the tributary buffer to be accessed in an indirect read or write operation.

TU[1:0]:

The tributary unit address bits (TU[1:0]) identifies the tributary within the tributary unit group which is identified by the TUG2[2:0] bits. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly.

TUG2[2:0]:

The tributary unit group address bits (TUG2[2:0]) identifies the tributary unit group. The combination of TUG2[2:0] and TU[1:0] identifies the tributary buffer to be accessed indirectly.

CPAGE:

The capture page control bit (CPAGE) selects between accessing the capture page and the expected page of the tributary buffer. When CPAGE is set high, the indirect register access is targeted at the capture page. Reading from the capture page returns the most recent tributary path trace message received from the incoming stream. No de-bouncing is provided. When CPAGE is set low, the indirect register access is targeted at the expected page. An expected trace message can be provisioned by writing to the expected page. Both the capture and expected pages may be read from or written to.

Register 42AH, 46AH, 4AAH: RTTB, Indirect Address Select

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register provides the byte address within the tributary buffer addressed by the Indirect Tributary Select register. Writing to this register triggers an indirect register access..

A[5:0]:

The indirect address bits (A[5:0]) index into the receive and expected pages of the tributary buffers.

RWB:

The indirect access control bit (RWB) selects between a read and write operation into the tributary buffers. Writing a logic zero to RWB triggers an indirect write operation. The tributary buffer is selected by the TUG2[2:0] and TU[1:0] bits in the Indirect Tributary register. Selection between the capture page and the expected page is controlled by the CPAGE bit also in the Indirect Tributary register. Bytes within the tributary buffer are indexed by A[5:0]. Data to be written is taken from D[7:0] of the Indirect Data register. Writing a logic one to RWB triggers an indirect read operation. Tributary buffer, page, and byte addressing is the same as in an indirect write operation. The data read can be found in D[7:0] of the Indirect Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when this register is written to trigger an indirect access and will stay high until the access is complete. At which point, BUSY

will be set low. This register should be polled to determine when data from an indirect read operation is available in the Indirect Data register or to determine when a new indirect write operation may commence.

Register 42BH, 46BH, 4ABH: RTTB, Indirect Data Select

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from a tributary buffer after an indirect read operation or the data to be inserted into a tributary buffer in an indirect write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a tributary buffer after an indirect read operation has complete. Data to be written to a tributary buffer in an indirect write operation must be set up in this register before triggering the write. Data in this register reflects the value written until the completion of a subsequent indirect read operation.

10 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs when the MBEB input is negated (high), causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TUPP-PLUS. Test mode registers (as opposed to normal mode registers) are selected when A[11] is high.

Test mode registers may also be used for board testing. When all of the tributary payload processors within the TUPP-PLUS are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Table 2 - Test Mode Register Memory Map

Address	Register
000H-7FFH	Normal Mode Registers
800H	Master Test Register
801H	I/O Test register 1
802H	I/O Test register 2
803H	I/O Test register 3
804H	I/O Test register 4
805H	I/O Test register 5
806H-81FH	Reserved
820H	VTPP #1 Test Register 0
821H	VTPP #1 Test Register 2
822H	VTPP #1 Test Register 4
823H-83FH	Reserved
8A0H	VTPP #1 Test Register 1
8A1H	VTPP #1 Test Register 3
8A2H	VTPP #1 Test Register 5

Address	Register
8A3H-8BFH	Reserved
840H	VTPP #2 Test Register 0
841H	VTPP #2 Test Register 2
842H	VTPP #2 Test Register 4
843H-85FH	Reserved
8C0H	VTPP #2 Test Register 1
8C1H	VTPP #2 Test Register 3
8C2H	VTPP #2 Test Register 5
8C3H-8DFH	Reserved
860H	VTPP #3 Test Register 0
861H	VTPP #3 Test Register 2
862H	VTPP #3 Test Register 4
863H-87FH	Reserved
8E0H	VTPP #3 Test Register 1
8E1H	VTPP #3 Test Register 3
8E2H	VTPP #3 Test Register 5
8E3H-8FFH	Reserved
900H	RTOP #1 Test Register 0
901H	RTOP #1 Test Register 1
902H	RTOP #1 Test Register 2
903H	RTOP #1 Test Register 3
904H	RTOP #1 Test Register 4
905H	RTOP #1 Test Register 5
906H	RTOP #1 Test Register 6
907H	RTOP #1 Test Register 7
908H	RTOP #1 Test Register 8
909H	RTOP #1 Test Register 9

Address	Register
90AH	RTOP #1 Test Register 10
90BH	RTOP #1 Test Register 11
90CH	RTOP #1 Test Register 12
90DH	RTOP #1 Test Register 13
90EH	RTOP #1 Test Register 14
90FH	RTOP #1 Test Register 15
910H-9FFH	Reserved
A00H - A0FH	RTOP #2 Test Register 0 - 15
A10H-AFFH	Reserved
B00H - B0FH	RTOP #3 Test Register 0 - 15
B10H-BFFH	Reserved
C00H	RTTB #1 Test Register 0
C01H	RTTB #1 Test Register 1
C02H	RTTB #1 Test Register 2
C03H	RTTB #1 Test Register 3
C04H-C3FH	Reserved
C40H - C43H	RTTB #2 Test Register 0 - 3
C44H-C7FH	Reserved
C80H - C83H	RTTB #3 Test Register 0 - 3
C84H-FFFH	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 800H: Master Test

Bit	Type	Function	Default
Bit 7	W	SSEL[1]	X
Bit 6	W	SSEL[0]	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	MOTOTST	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable TUPP-PLUS test features. All bits, except PMCTST, are reset to zero by a reset of the TUPP-PLUS.

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the TUPP-PLUS . While the HIZIO bit is a logic 1, all output pins of the TUPP-PLUS except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the TUPP-PLUS for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

MOTOTST:

The MOTOTST bit is used to test the decoding of the RDB_E and WRB_RWB control signals when MBEB is logic 0.

PMCTST:

The PMCTST bit is used to configure the TUPP-PLUS for PMC's manufacturing tests. When PMCTST is set to logic 1, the TUPP-PLUS microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "OR'ed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

SSEL[1:0]:

The test mode slice selection bits (SSEL[1:0]) controls CBI access to the VTPP[3:1], RTOP[3:1] and RTTB[3:1], when PMCTST is set high. When SSEL is set to 'b00, the selection among the TSBs is directly controlled by the address bus A[11:0]. When SSEL is set to the three higher values, TSB seletion is a combination of the address bus and the SSEL values. The selection among the VTPP, RTOP and RTTB TSBs is made by setting the address to the address range of VTPP #1, RTOP #1 and RTTB #1, respectively. The choice of TSB slice #1, #2 and #3 is controlled by writing 'b01, 'b10 and 'b11, respectively, to the SSEL bits. The SSEL bits are cleared by setting CSB to logic 1.

10.1 I/O Test Mode

In I/O test mode (IOTST in Master Test Register set high), the TUPP-PLUS allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

Test Register 801H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	OD[7]	X
Bit 6	W	OD[6]	X
Bit 5	W	OD[5]	X
Bit 4	W	OD[4]	X
Bit 3	W	OD[3]	X
Bit 2	W	OD[2]	X
Bit 1	W	OD[1]	X
Bit 0	W	OD[0]	X

Test Register 802H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	ODP	X
Bit 6	W	OTPL	X
Bit 5	W	OTV5	X
Bit 4	W	AIS	X
Bit 3	W	IDLE	X
Bit 2	W	LC1J1V1	X
Bit 1	W	LPL	X
Bit 0	W	INTB	X

Test Register 803H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	W	POH[3]	X
Bit 4	W	POH[2]	X
Bit 3	W	POH[1]	X
Bit 2	W	POHFP[3]	X
Bit 1	W	POHFP[2]	X
Bit 0	W	POHFP[1]	X

Test Register 804H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	W	POHEN[3]	X
Bit 4	W	POHEN[2]	X
Bit 3	W	POHEN[1]	X
Bit 2	W	POHCK[3]	X
Bit 1	W	POHCK[2]	X
Bit 0	W	POHCK[1]	X

Test Register 805H: (Write in I/O test mode)

Bit	Type	Function	Default
Bit 7	W	COUT	X
Bit 6	W	RAD	X
Bit 5	W	LOM[3]	X
Bit 4	W	LOM[2]	X
Bit 3	W	LOM[1]	X
Bit 2	W	TPOH	X
Bit 1		Unused	X
Bit 0		Unused	X

Test Register 801H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7	R	ID[7]	X
Bit 6	R	ID[6]	X
Bit 5	R	ID[5]	X
Bit 4	R	ID[4]	X
Bit 3	R	ID[3]	X
Bit 2	R	ID[2]	X
Bit 1	R	ID[1]	X
Bit 0	R	ID[0]	X

Test Register 802H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7	R	SCLK	X
Bit 6	R	IC1J1	X
Bit 5	R	IPL	X
Bit 4	R	ITMF	X
Bit 3	R	IDP	X
Bit 2	R	OTMF	X
Bit 1	R	OC1J1	X
Bit 0	R	OPL	X

Test Register 803H: (Read in I/O test mode)

Bit	Type	Function	Default
Bit 7	R	NSCLK	X
Bit 6	R	IBMODE	X
Bit 5	R	OBMODE	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

10.2 JTAG Test Port

The TUPP-PLUS JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

Table 3 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110

Instructions	Selected Register	Instruction Codes, IR[2:0]
BYPASS	Bypass	111

Identification Register

Length : 32 bits

Version number : 0x1

Part Number : 0x5362

Manufacturer's identification code : 0x0CD

Device identification : 0x153620CD

Boundary Scan Register

Length : 88 bits + 3 bit instruction register.

11 OPERATION

11.1 Configuration Options

The TUPP-PLUS consists of three tributary payload processors (VTPPs), three tributary path overhead processors (RTOPs) and three tributary trace buffers (RTTBs). Each VTPP, RTOP and RTTB deals with a portion of the SONET frame that corresponds to an STS-1 SPE. Equivalently, each VTPP, RTOP and RTTB deals with a portion of the SDH frame that corresponds to a VC3 together with the 2 columns of fixed stuff that are added when mapping a VC3 into an AU3. By coordinating the operation of the three VTPPs, RTOPs and RTTBs, they can process the portion of an SDH frame that corresponds to a VC4. The coordination that may be required between the three VTPPs relates to the J1 byte marker and the encoding of the tributary multiframe into the H4 byte. When processing a VC4 that carries three TUG3s, the alignment provided by the J1 byte marker and the H4 byte of the VC4 must be distributed to all VTPPs, RTOPs and RTTBs. When processing STS-1 SPEs, or equivalently, VC3s carried within AU3s, each VTPP, RTOP and RTTB receives its own J1 byte marker and H4 byte. Coordination is accomplished as follows: The tributary multiframe alignment that is detected by VTPP #1 is distributed to the two other VTPPs which do not receive valid H4 bytes. In addition, the input demultiplexer will stretch the pulse captured on the IC1J1 input that marks the VC4 J1 byte so that it marks the next two bytes. During the demultiplexing process this effectively feeds a "J1" marker to the two "slaved" VTPPs.

The modes of operation of the TUPP-PLUS are summarized as follows:

STS-1 Mode: This is default. Each STS-1 is assumed to carry seven VT groups, each of which can be independently configured to carry VT1.5s, VT2s, VT3s, or VT6s. The IC1J1 input is expected to mark the J1 byte of each STS-1 SPE and each VTPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

AU3 Mode: This is also the default, as is corresponds exactly to STS-1 mode, except for nomenclature. Each AU3 is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) The IC1J1 input is expected to mark the J1 byte of each VC3 and each VTPP detects the tributary multiframe encoded in the unique H4 byte that it receives.

AU4 Mode: This mode is enabled when the ICONCAT and OCONCAT bits are set high. In AU4 mode, individual VTPPs must be configured in either TUG3 mode or TU3 mode. The IC1J1 input is expected to mark the J1 byte of the VC4. This J1 marker is stretched to provide a "J1" marker to each VTPP. VTPP #2 and VTPP#3 are slaved to the tributary multiframe indication provided by VTPP #1 as it is the only one that receives a valid H4 byte.

TUG3 Mode: This mode is enabled when the TUG3 bit is set high in a VTPP. In addition, the ICONCAT and OCONCAT bits must be set high for the TUPP-PLUS. The TUG3 processed by the VTPP is assumed to carry seven TUG2s, each of which can be independently configured to carry TU11s, TU12s, or TU2s. (The equivalent of a VT3 is allowed but there is no SDH nomenclature to describe this.) When the TUPP-PLUS is in AU4 mode, each VTPP can be independently configured in TUG3 or TU3 mode.

TU3 Mode: This mode is enabled when the TU3 bit is set high in a VTPP. In addition the ICONCAT and OCONCAT bits must be set high for the TUPP-PLUS. The TUG3 processed by the VTPP is assumed to carry a TU3. When the TUPP-PLUS is in AU4 mode, each VTPP can be independently configured in TUG3 or TU3 mode.

For figures in the operation and functional timing sections (Figures 1 to 12), transport overhead and path overhead bytes are shown for notational convenience only. In the incoming direction, except for the H4 byte, ID[7:0] does not need to contain valid transport and STS/AU path overhead byte values. The H4 byte must be valid only if H4 framing is enabled (ITMFEN=0). Otherwise, it too may be invalid. However, the incoming parity must match the data supplied at all times. In the outgoing direction, TUPP-PLUS places random data on OD[7:0] for transport overhead bytes. It generates all zero bytes for the STS/AU path overhead except for the H4 byte which contains leading ones and an incrementing two bit pattern. The fixed stuff bytes in the tributary mapping to the synchronous payload envelope (virtual container) are also generated as all zero bytes. The outgoing parity reflects the data on OD[7:0] at all times.

11.2 STS-1 Mode

An example of the placement of tributaries assumed in STS-1 mode is illustrated in Figure 3. For simplicity, this figure shows the frame on the OD[7:0] bus when OJ1EN is low. In this case the outgoing STS-1 SPEs are locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the first frame of the tributary multiframe when the V1 bytes are present. This example illustrates a VT structured STS-1 SPE where all VT

groups are configured to carry VT1.5s. The more general case where OJ1EN is high would be similar, except that the STS-1 SPE would be floating within the transport envelope frame.

Figure 3 - SONET STS-3 Carrying VT1.5 Within STS-1

	COL 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	265	266	267	268	269	270
ROW 1	A1	A1	A1	A2	A2	A2	C1	C1	C1	J1	J1	J1	V1	V1	V1	SPE	SPE	SPE	SPE	SPE	SPE
2	B1	-	-	E1	-	-	F1	-	-	B3	B3	B3	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
3	D1	-	-	D2	-	-	D3	-	-	C2	C2	C2	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
4	H1	H1	H1	H2	H2	H2	H3	H3	H3	G1	G1	G1	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
5	B2	B2	B2	K1	-	-	K2	-	-	F2	F2	F2	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
6	D4	-	-	D5	-	-	D6	-	-	H4	H4	H4	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
7	D7	-	-	D8	-	-	D9	-	-	Z3	Z3	Z3	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
8	D10	-	-	D11	-	-	D12	-	-	Z4	Z4	Z4	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
9	Z1	-	-	Z2	-	-	E2	-	-	Z5	Z5	Z5	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE

First of 3 columns occupied by VT1.5 #1 of VT group #1 of STS-1 #1 of an STS-3 stream (column set is 13, 100, 187)

Last of 3 columns occupied by VT1.5 #4 of VT group #7 of STS-1 #3 of an STS-3 stream (column set is 96, 183, 270)

11.3 AU3 Mode

An example of the placement of tributaries assumed in AU3 mode is illustrated in Figure 4. For simplicity, this figure shows the frame on the OD[7:0] bus when OJ1EN is low. In this case the outgoing VC3s are locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates the case where the VC3s carry TUG2s and all TUG2s are configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC3s would be floating within the transport envelope frame.

Figure 4 - SDH STM-1 Carrying TU12 Within VC3/AU3

	COL 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	265	266	267	268	269	270
ROW 1	A1	A1	A1	A2	A2	A2	C1	C1	C1	J1	J1	J1	V4	V4	V4	SPE	SPE	SPE	SPE	SPE	SPE
2	B1	-	-	E1	-	-	F1	-	-	B3	B3	B3	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
3	D1	-	-	D2	-	-	D3	-	-	C2	C2	C2	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
4	H1	H1	H1	H2	H2	H2	H3	H3	H3	G1	G1	G1	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
5	B2	B2	B2	K1	-	-	K2	-	-	F2	F2	F2	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
6	D4	-	-	D5	-	-	D6	-	-	H4	H4	H4	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
7	D7	-	-	D8	-	-	D9	-	-	Z3	Z3	Z3	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
8	D10	-	-	D11	-	-	D12	-	-	Z4	Z4	Z4	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE
9	Z1	-	-	Z2	-	-	E2	-	-	Z5	Z5	Z5	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE	SPE

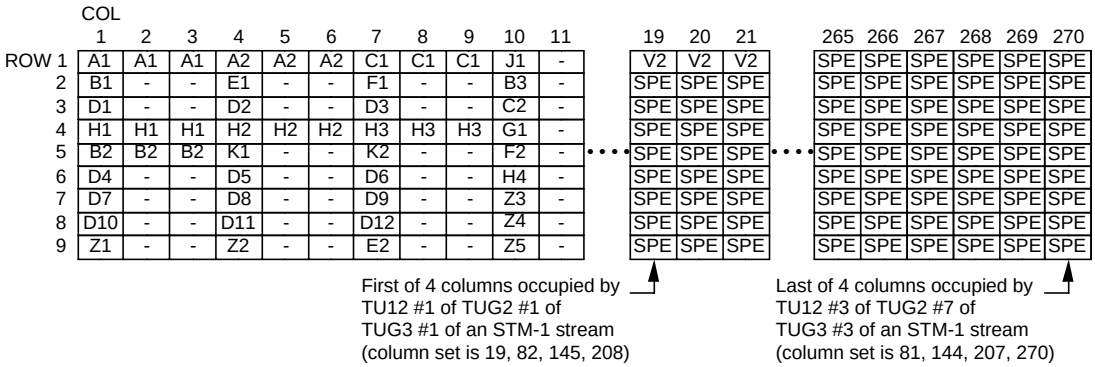
First of 4 columns occupied by TU12 #1 of TUG2 #1 of VC3/ AU3 #1 of an STM-1 stream (column set is 13, 76,142, 208)

Last of 4 columns occupied by TU12 #3 of TUG2 #7 of VC3/ AU3 #3 of an STM-1 stream (column set is 75, 141, 207, 270)

11.4 AU4 Mode

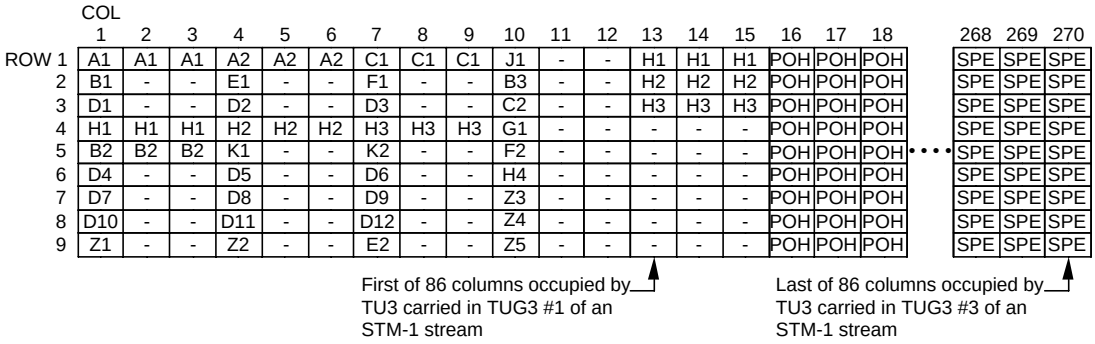
An example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 5. For simplicity, this figure shows the frame on the OD[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the second frame of the tributary multiframe when the V2 bytes are present. This example illustrates a case where the VC4 carries TUG3s, all TUG3s carry TUG2s, and all TUG2s are configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

Figure 5 - SDH STM-1 Carrying TU12 Within TUG3/AU4



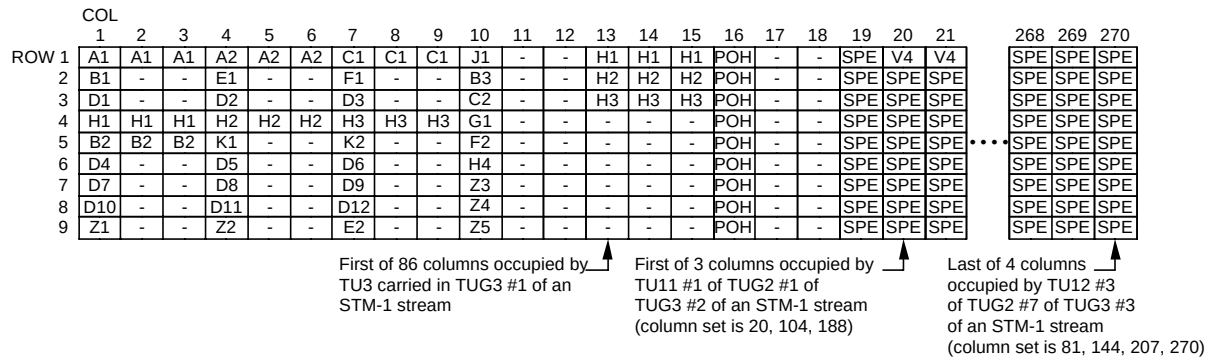
Another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 6. For simplicity, this figure shows the frame on the OD[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This example illustrates the case where the VC4 carries TUG3s that are all configured to carry TU3s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

Figure 6 - SDH STM-1 Carrying TU3 Within TUG3



Yet another example of the placement of tributaries assumed in AU4 mode is illustrated in Figure 7. For simplicity, this figure shows the frame on the OD[7:0] bus when OJ1EN is low. In this case the outgoing VC4 is locked with respect to the outgoing transport envelope frame. This particular example assumes a snapshot of the last frame of the tributary multiframe when the V4 bytes are present. This example illustrates a complex case where the VC4 carries TUG3s and where TUG3 #1 carries a TU3, TUG3 #2 carries TUG2s that are all configured to carry TU11s, and TUG3 #3 carries TUG2s that are all configured to carry TU12s. The more general case where OJ1EN is high would be similar, except that the VC4 would be floating within the transport envelope frame.

Figure 7 - SDH STM-1 Carrying Mix Of TU11, TU12, TU3 Within TUG3/AU4

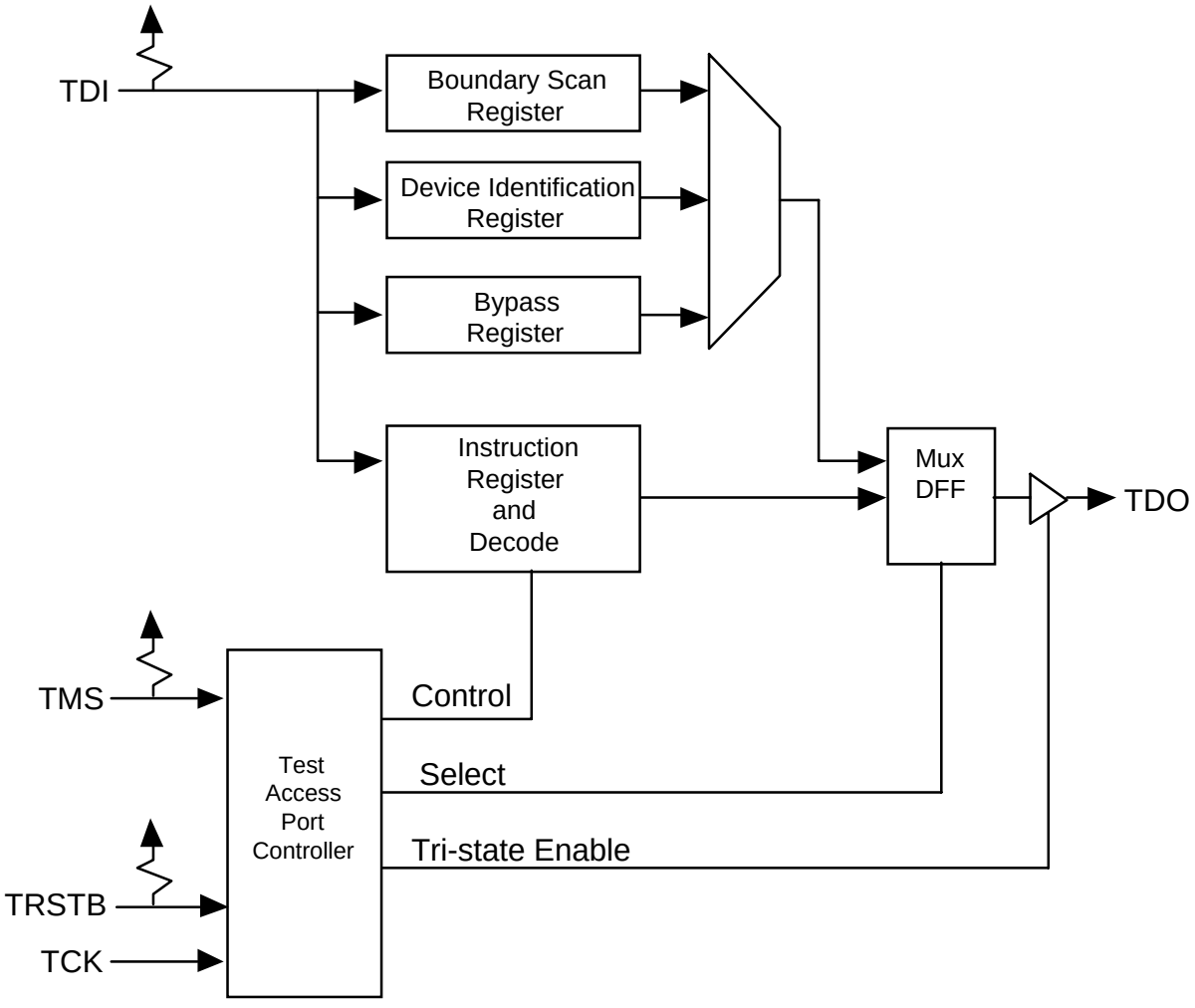


In Figure 7 above, the H1 to H3 byte in column 13 form the TU3 offset pointer. The H1 to H3 bytes in columns 14 and 15 are null pointer indications (NPI) for TUG3 #2 and #3.

11.5 JTAG Support

The TUPP-PLUS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO, used to control the TAP controller and the boundary scan registers. The TRSTB input is the active low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 8 - Boundary Scan Architecture



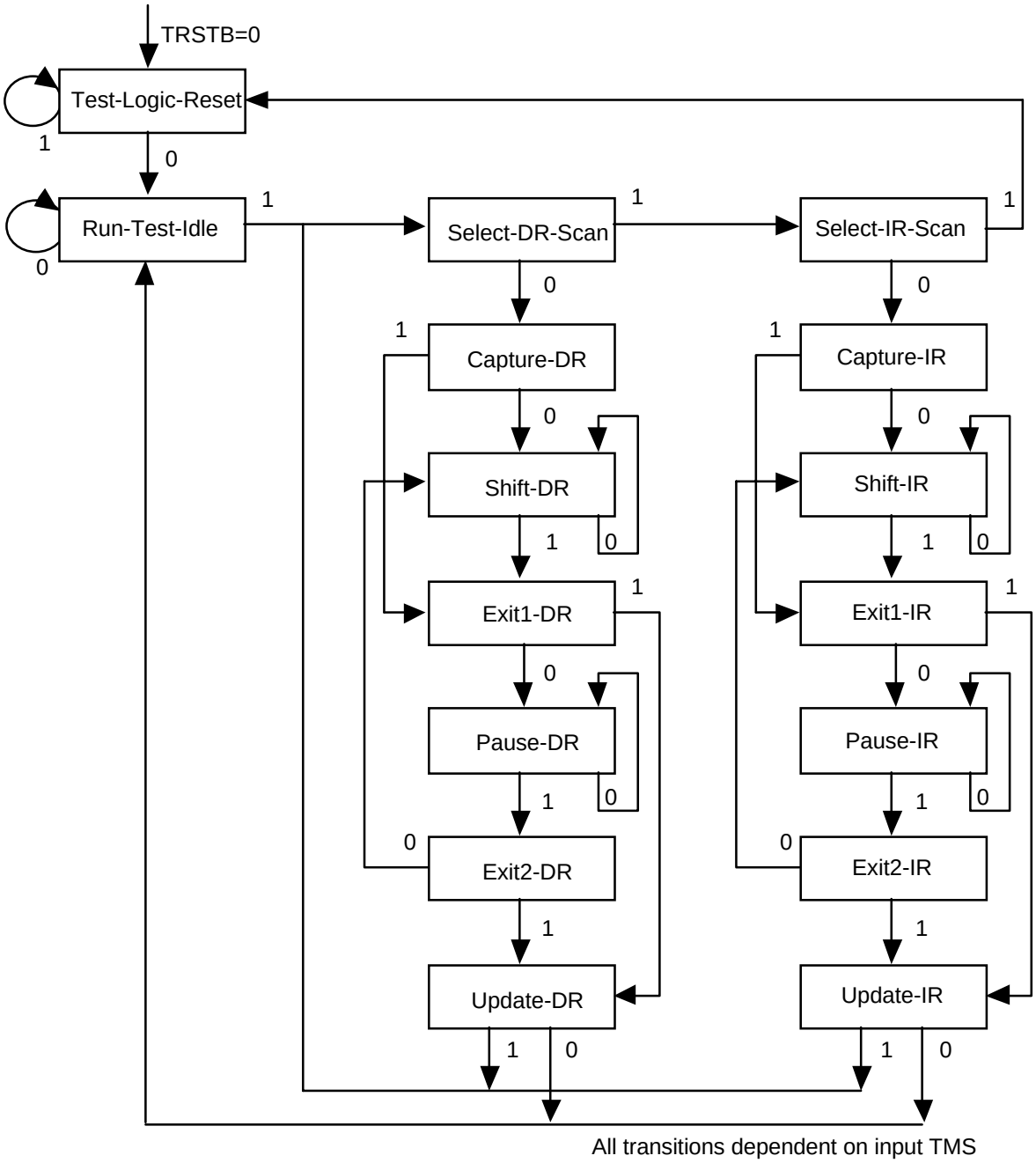
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

11.5.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 9 - TAP Controller Finite State Machine



Test-Logic-Reset:

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle:

The run test/idle state is used to execute tests.

Capture-DR:

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR:

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR:

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR:

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR:

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR:

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

The TDO output is enabled during states Shift-DR and Shift-IR. Otherwise, it is tri-stated.

11.5.2 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects an serial test data register path between input, TDI, and output, TDO.

BYPASS

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input TDI and output TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out on output TDO using the Shift-DR state.

Table 4 - Boundary Scan Pin Order

Order #	Pin #	Pin name	Pin Type	ID value
0		HIZ	Output Enable	-
1	105	TPOH	Output	-
2	149	GSCLK[0]	Clock Output	-
3	144	LOM[1]	Output	-
4	141	LC1J1V1	Output	-
5	140	LPL	Output	-
6	139	POHEN[1]	Output	-
7	136	OTV5	Output	-
8	135	POH[1]	Output	-
9	134	OTPL	Output	-

Order #	Pin #	Pin name	Pin Type	ID value
10	133	POHFP[1]	Output	-
11	126	POHCK	Clock Output	-
12	124	RAD	Output	-
13	115	IDLE	Output	-
14	114	AIS	Output	-
15	111	POHEN[2]	Output	-
16	110	OD[0]	Output	-
17	109	POH[2]	Output	-
18	108	OD[1]	Output	-
19	107	POHFP[2]	Output	-
20	106	OD[2]	Output	-
21	104	OD[3]	Output	-
22	97	OD[4]	Output	-
23	95	OD[5]	Output	-
24	93	OD[6]	Output	-
25	91	OD[7]	Output	-
26	90	LOM[2]	Output	-
27	89	ODP	Output	-
28	85	COUT	Output	-
29	77	POHEN[3]	Output	-
30	76	POH[3]	Output	-
31	67	POHFP[3]	Output	-
32	65	GSCLK[1]	Clock Output	-
33	63	LOM[3]	Output	-
34	28	INTB	OD Output	-
35		OENB[7]	OE	-
36	26	D[7]	I/O	-
37		OENB[6]	OE	-

Order #	Pin #	Pin name	Pin Type	ID value
38	25	D[6]	I/O	-
39		OENB[5]	OE	-
40	24	D[5]	I/O	-
41		OENB[4]	OE	-
42	23	D[4]	I/O	-
43		OENB[3]	OE	-
44	18	D[3]	I/O	-
45		OENB[2]	OE	-
46	17	D[2]	I/O	-
47		OENB[1]	OE	-
48	16	D[1]	I/O	-
49		OENB[0]	OE	-
50	15	D[0]	I/O	-
51	157	A[9]	Input	-
52	156	A[10]	Input	-
53	153	SCLK	Clock Input	-
54	147	NSCLK	Clock Input	-
55	146	OBMODE	Input	-
56	145	IBMODE	Input	1
57	132	OPL	Input	0
58	127	OC1J1	Input	1
59	125	OTMF	Input	1
60	70	IDP	Input	0
61	68	ID[7]	Input	0
62	66	ID[6]	Input	1
63	64	ID[5]	Input	1
64	62	ID[4]	Input	0
65	60	ID[3]	Input	0

Order #	Pin #	Pin name	Pin Type	ID value
66	58	ID[2]	Input	0
67	56	ID[1]	Input	0
68	54	ID[0]	Input	0
69	52	ITMF	Input	1
70	48	IPL	Input	0
71	44	IC1J1	Input	0
72	37	WRB_RWB	Input	0
73	35	RDB_E	Input	1
74	34	A[11]/TRS	Input	1
75	33	ALE	Input	0
76	31	RSTB	Input	1
77	14	MBEB	Input	1
78	13	CSB	Input	0
79	12	A[8]	Input	0
80	11	A[7]	Input	1
81	10	A[6]	Input	0
82	9	A[5]	Input	1
83	8	A[4]	Input	0
84	7	A[3]	Input	1
85	6	A[2]	Input	0
86	5	A[1]	Input	0
87	4	A[0]	Input	0
	45	TCK	TAP Clock	
	47	TDI	TAP Input	
	49	TDO	TAP Output	
	51	TRSTB	TAP Input	
	53	TMS	TAP Input	

Notes :

1. A[0] is the first bit of the scan chain (closest to TDI).

2. OENB[n] sets the corresponding D[n] pin to an output when set low.

In the diagram of boundary scan cells, CLOCK-DR is connected to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 10 - Input Observation Cell (Input, Clock Input)

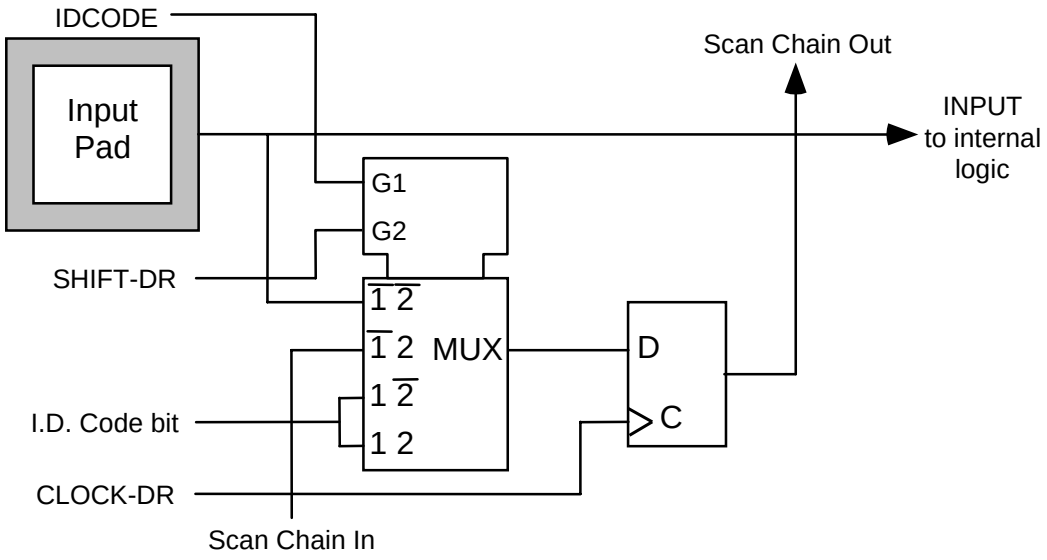


Figure 11 - Output Cell (Output, Clock Output, Output Enable)

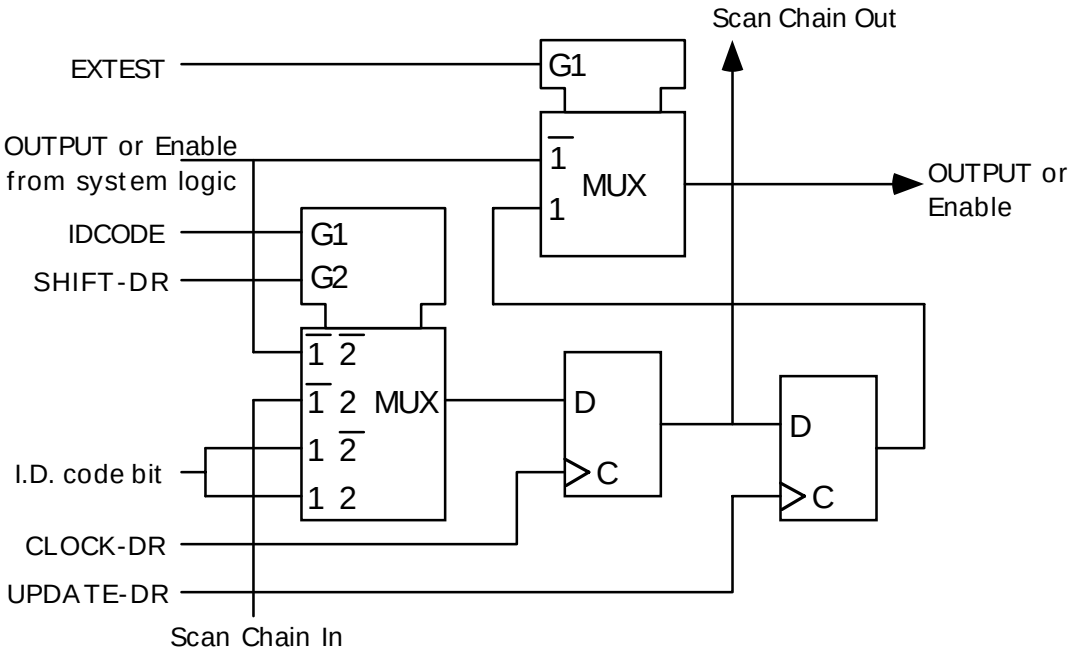


Figure 12 - Bidirectional Cell (IO_CELL)

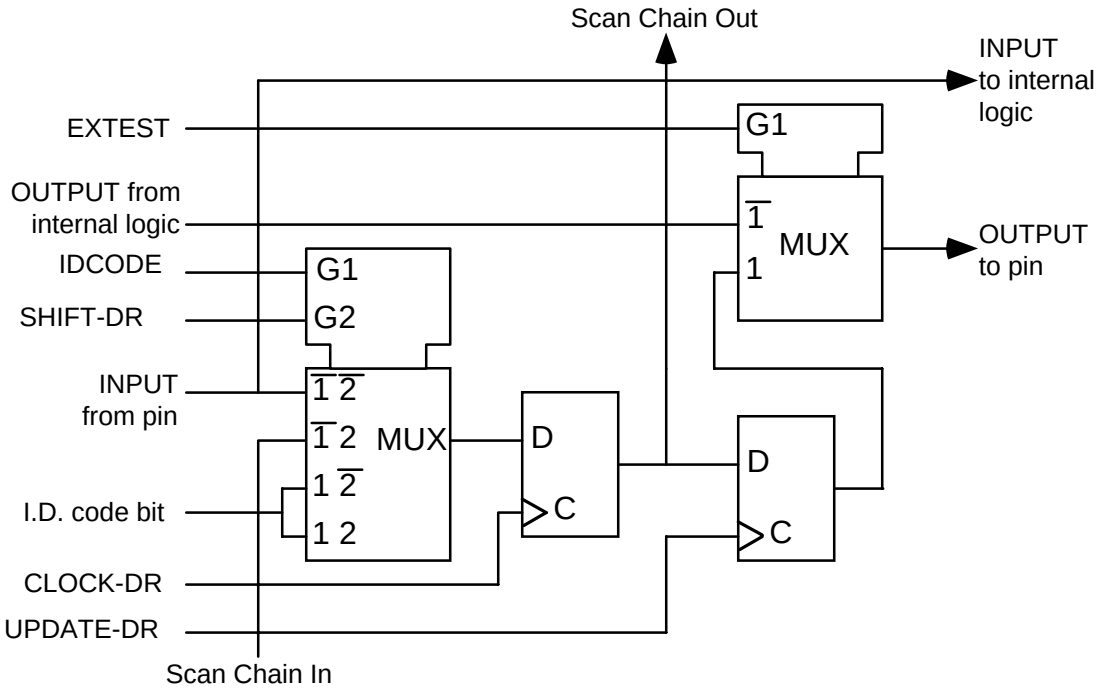
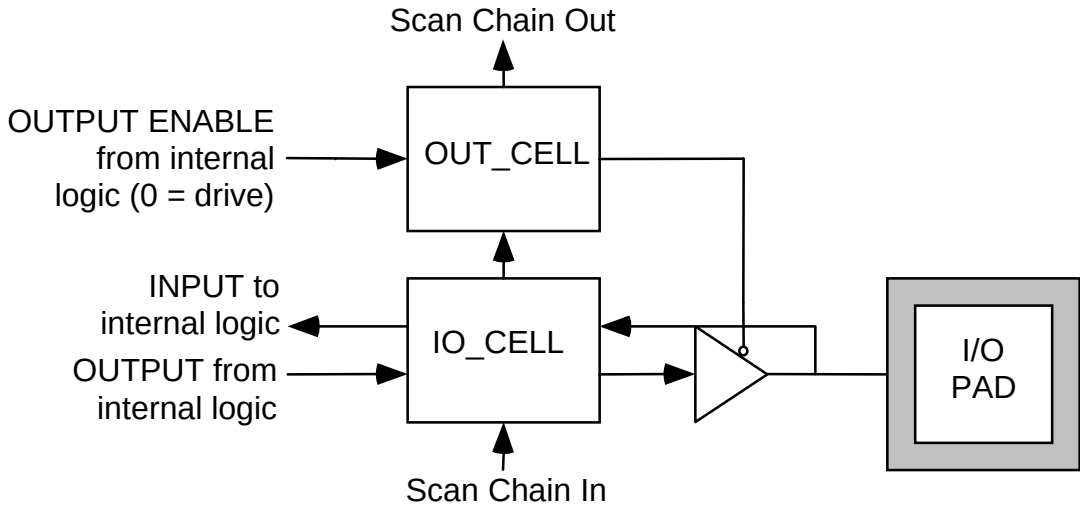


Figure 13 - I/O Cell (I/O with OE pair)



12 FUNCTIONAL TIMING

The timing of the TUPP-PLUS input signals is illustrated in Figure 14. This diagram shows a simple STS-3 case that outlines the function of the various input signals. Data on ID[7:0] is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the IPL signal being set high. The IC1J1 signal pulses high while IPL is low to mark the position of the first C1 byte in the STS-3 transport envelope. The IC1J1 signal is set high for three SCLK periods while IPL is also set high to mark the J1 bytes of each STS-1 SPE. The ITMF signal is selectable to mark the third byte after J1 of the first tributary in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the last H4 byte of the tributary multiframe in STS-1 #1 and STS-1 #3. The H4 byte in STS-1 #2, as shown, is not last in the tributary multiframe. In this simple example, all STS-1 SPEs are aligned to the STS-3 transport envelope such that the J1 bytes directly follow the C1 bytes and no STS-1 pointer justification events are occurring.

This same diagram applies for the AU3 mode as it is equivalent to the STS-1 mode, except for nomenclature.

Figure 14 - Input Bus Timing - Simple STS-1/AU3 Case

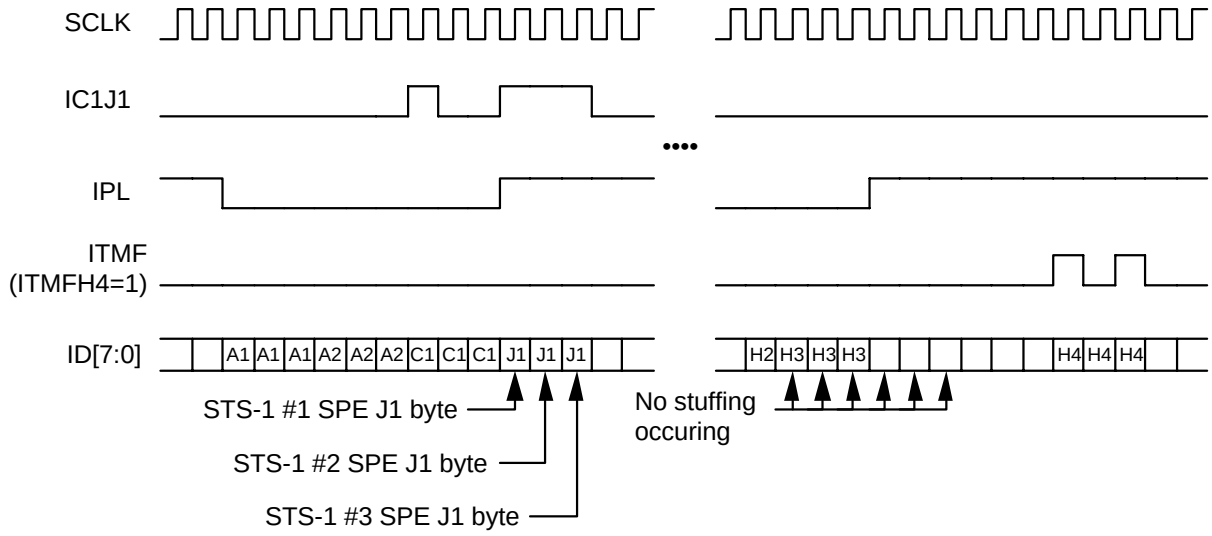


Figure 15 shows a more complex STS-3 case that illustrates the flexibility provided by the various input signals. Data on ID[7:0] is sampled on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the IPL signal being set high. This example shows a negative stuff event occurring on STS-1 #2 and a positive stuff event occurring on STS-1 #3. The IC1J1 signal pulses high while IPL is low to mark the position of the C1 byte of STS-1 #1. The IC1J1 signal pulses high again to mark the J1 byte of each of the three STS-1 SPEs. The ITMF signal is selectable to mark the third byte after J1 in an STS-1 SPE or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the V1 byte of the first tributary multiframe in STS-1 #2. The three STS-1 SPEs are shown to have different alignments to the STS-3 transport envelope and the alignment is changing for two of the STS-1 SPEs (STS-1 #1 and #2) due to the pointer justification events shown.

Again, this same diagram would apply for AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

Figure 15 - Input Bus Timing - Complex STS-1 / AU3 Case

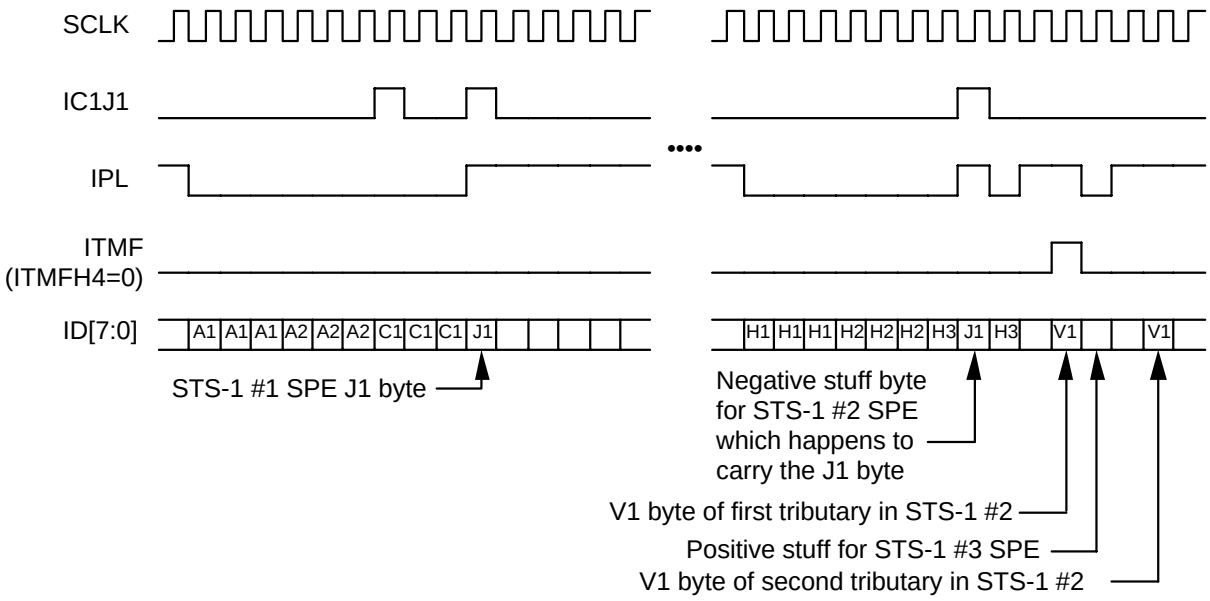
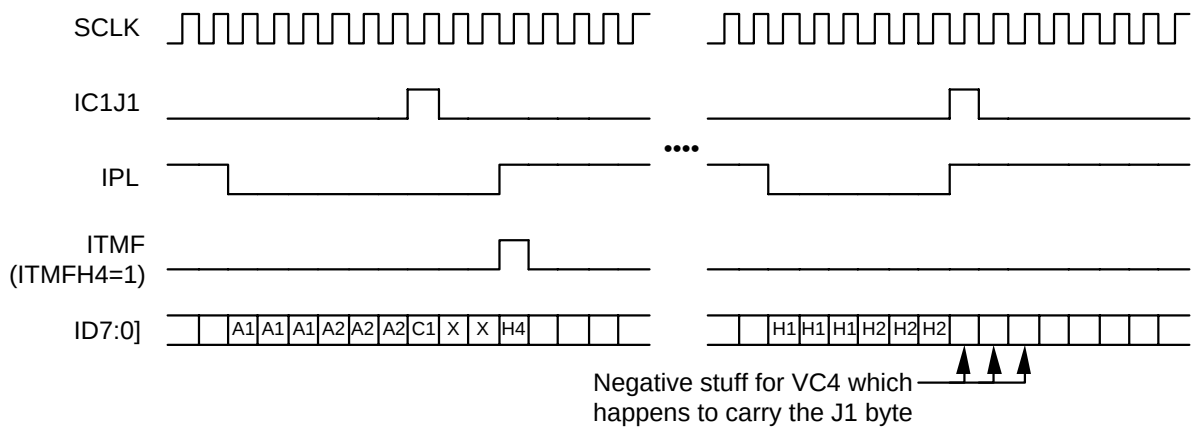


Figure 16 shows timing relationships of the various input signals in the AU4 mode. Data on ID[7:0] is sampled on the rising edge of SCLK. The bytes forming the AU4 virtual container are identified by the IPL signal being set high. This example shows a negative stuff occurring for the VC4. The IC1J1 signal

pulses high while IPL is set low to mark the position of the single C1 byte in the STM-1 transport envelope. The ITMF signal is selectable to mark the third byte after J1, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, ITMF is shown to be marking the final H4 byte of the tributary multiframe. The IC1J1 signal pulses high to mark the single J1 byte of the VC4.

This diagram applies when the TUPP-PLUS is in AU4 mode, regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode.

Figure 16 - Input Bus Timing - AU4 Case



The timing of the TUPP-PLUS output bus is illustrated in Figure 17. This diagram shows the relationships of the output signals in locked STS-1 mode. Data on OD[7:0] is updated on the rising edge of SCLK, and the OPL input must be logic 0. The OC1J1 signal pulses high to mark the position of the C1 byte of the first STS-1 stream in every frame of the STS-3 transport envelope. In locked STS-1 mode, the position of the J1 bytes and the STS-1 SPEs is implicitly defined by the C1 byte position. All three STS-1 SPEs are defined to be aligned to the STS-3 transport envelope such that the J1 bytes immediately follow the C1 bytes and no STS-1 pointer justification events are possible. This fixed implicit alignment is reflected in the locked mode control signals LC1J1V1 and LPL. LC1J1V1 pulses high to mark the first C1 byte, all three J1 bytes and the third byte after J1 of the first tributary in each STS-1 stream. LPL identifies the SPE bytes on OD[7:0]. The OTMF input marks the frame containing V1 bytes. It is sampled only at the first V1 byte position of the first STS-1 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing

tributary. The TPOH signal marks the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributary.

This same diagram would apply for AU3 mode as it is equivalent to STS-1 mode, except for nomenclature.

Figure 17 - Output Bus Timing - Locked STS-1 SPEs / AU3 VCs Case

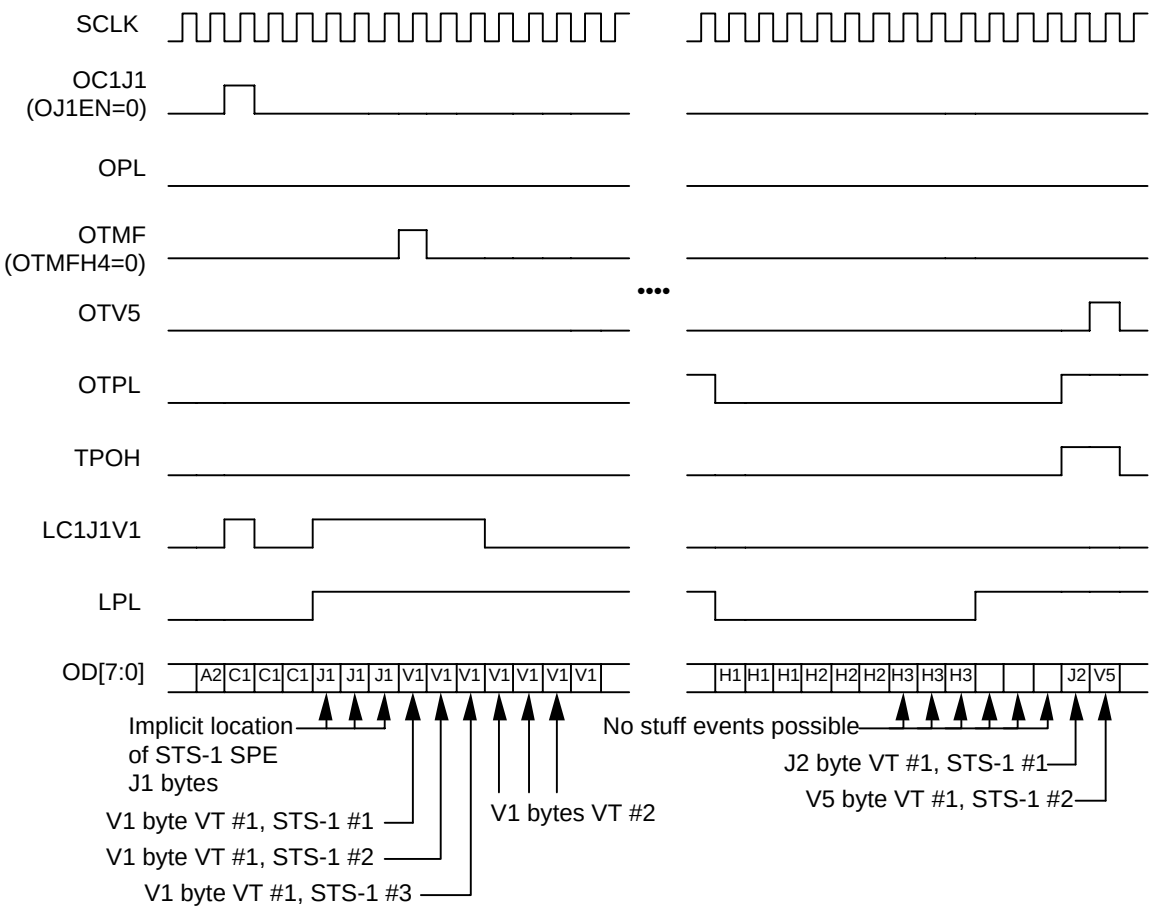
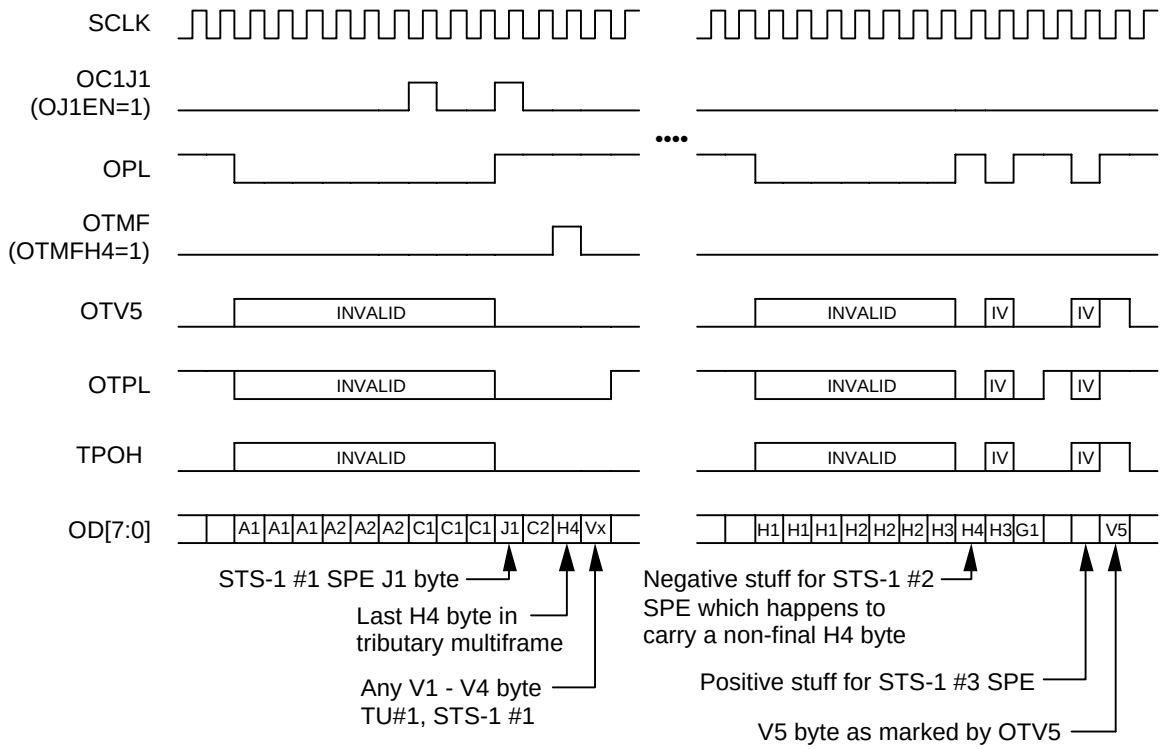


Figure 18 shows the function of the various output signals in floating STS-1 mode and AU3 mode. Data on OD[7:0] is updated on the rising edge of SCLK. The bytes forming the three STS-1 synchronous payload envelopes are identified by the setting the OPL signal high. In this diagram, a negative stuff event is shown occurring on STS-1 #2 and a positive stuff event on STS-1 #3. The OC1J1 signal pulses high, while OPL is set low, to mark the C1 byte of the first STS-1 in every frame of the STS-3 transport envelope. The OC1J1 signal is set

high to mark every J1 byte of each of the three STS-1 SPEs. The OTMF input is selectable to mark the third byte after J1 in each STS-1 SPE, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, OTMF is shown to be marking the last H4 byte of the tributary multiframe in STS-1 #1. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributaries. The TPOH signal pulses high to mark the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributaries. OTPL, OTV5 and TPOH are invalid when OPL is set low. The three STS-1 SPEs each have different alignments to the STS-3 transport envelope and the alignment is changing for two of the STS-1 SPEs (STS-1 #2 and #3) due to the pointer justification events shown. In floating mode, LC1J1V1 and LPL are held low and are not shown in Figure 18.

Figure 18 - Output Bus Timing - Floating STS-1 SPEs / AU3 VCs Case



The timing of the TUPP-PLUS output signals in locked and floating AU4 modes is illustrated in Figure 19 and Figure 20, respectively. The operation of the various signals is analogous to the locked and floating STS-1 modes, except that there is only a single J1 byte and all pointer justification events must involve a group of

three stuff bytes. These diagrams apply when the TUPP-PLUS is in AU4 mode, regardless of whether individual tributary payload processors are configured for TUG3 or TU3 mode.

Figure 19 shows the case of the TUPP-PLUS operating in locked AU4 mode. Data on OD[7:0] is updated on the rising edge of SCLK, and the OPL input must be logic 0. The OC1J1 signal pulses high to mark the position of the single C1 byte in every frame of the AU4 transport envelope. In locked AU4 mode, the position of the single J1 byte and the VC4 is implicitly defined by the C1 byte position. The VC4 is defined to be aligned to the AU4 transport envelope such that the J1 byte occupies the first available payload byte after the C1 byte, and no pointer justification events are possible. This fixed implicit alignment is reflected in the locked mode control signals LC1J1V1 and LPL. LC1J1V1 pulses high to mark the first C1 byte, the J1 byte and the third byte after J1 of the first tributary in the AU4 stream. LPL identifies the payload bytes on OD[7:0]. The OTMF input marks the frame containing V1 bytes. It is sampled only at the J1 plus one byte position of the first TUG3 stream. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL signal being set high. The OTV5 signal pulses high to mark the V5 bytes of each outgoing tributary. The TPOH signal pulses high to mark the tributary path overhead bytes (V5, J2, Z6 and Z7) of each outgoing tributary.

Figure 19 - Output Bus Timing - Locked AU4 VC Case

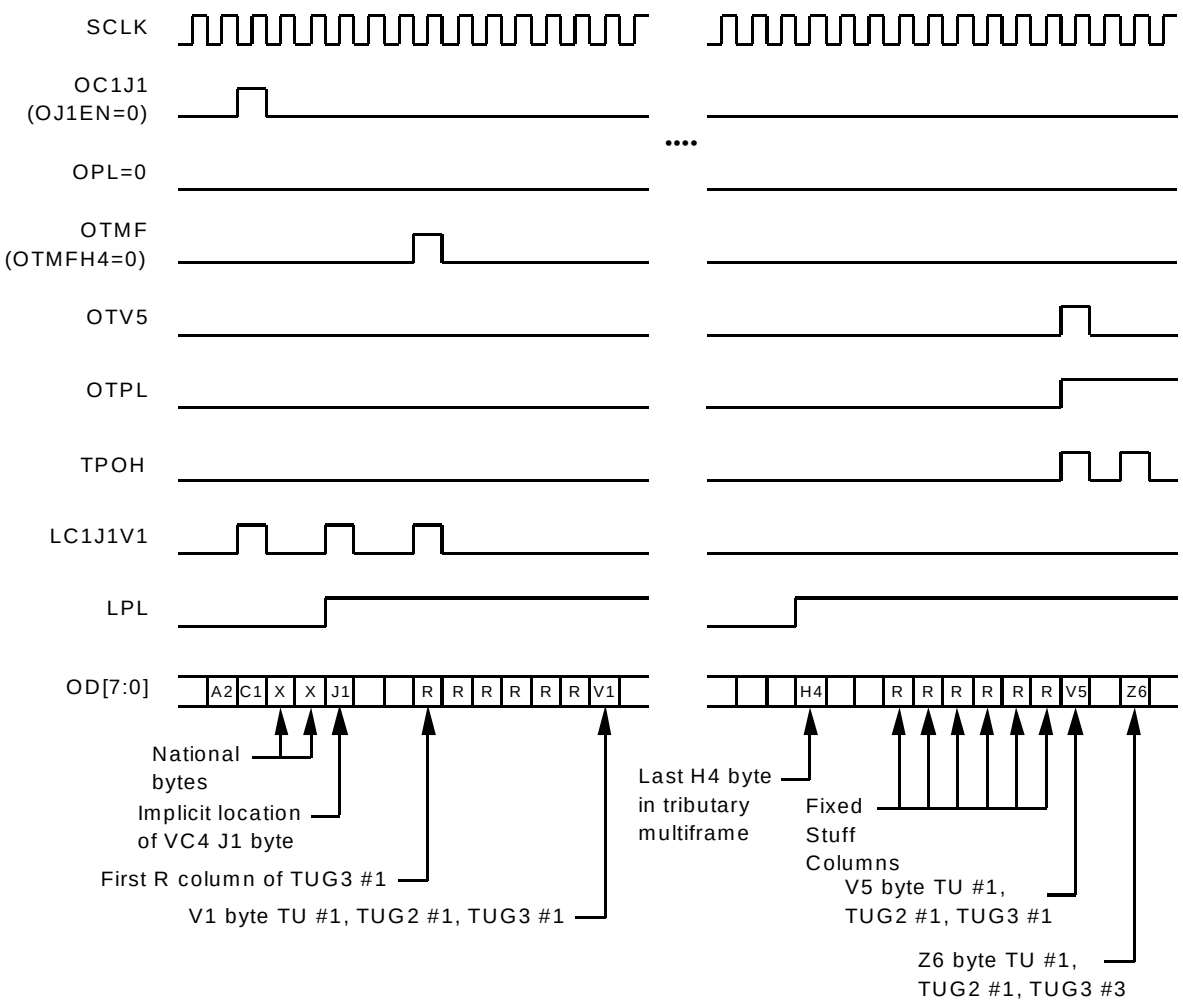
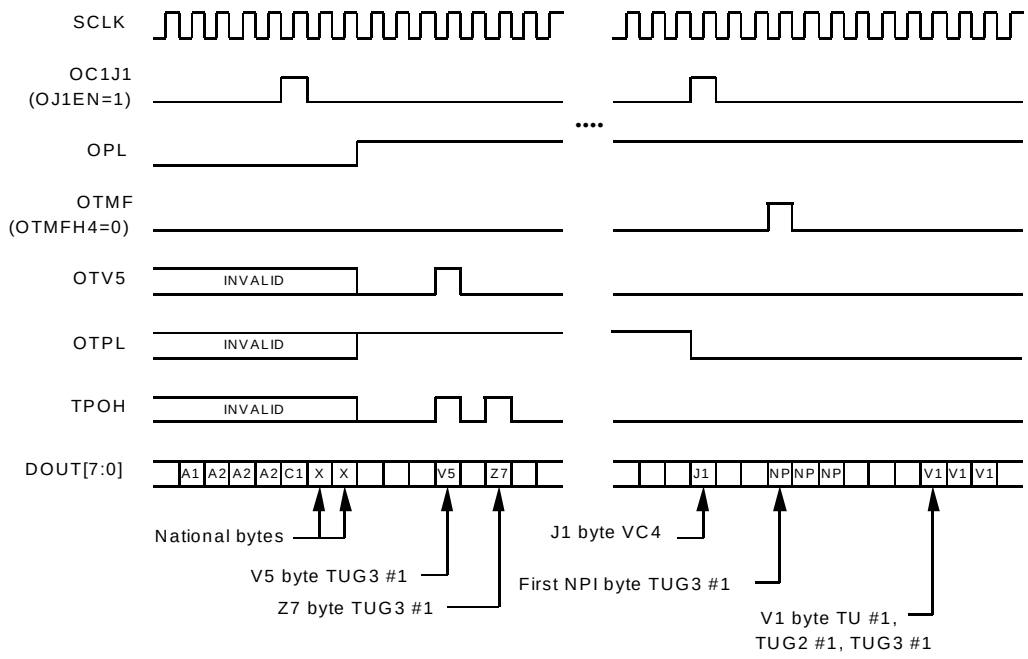


Figure 20 shows the function of the various output signals in floating AU4 mode. Data on OD[7:0] is updated on the rising edge of SCLK. The bytes forming the VC4 virtual container are identified by the setting the OPL signal high. The OC1J1 signal pulses high, while OPL is set low, to mark the single C1 byte in every frame of the AU4 transport envelope. The OC1J1 signal is set high again with OPL high to mark the J1 byte of the VC4. The OTMF input is selectable to mark the third byte after J1 in the VC4, or the H4 byte in the last (fourth) frame of a tributary multiframe. In this diagram, OTMF is shown to be marking the first V1 byte. The bytes forming the various tributary synchronous payload envelopes are identified by the OTPL signal being set high. The OTV5 signal pulses high to

mark the V5 bytes of each outgoing tributaries. The TOPH signal pulses high to mark the tributary overhead bytes of each outgoing tributaries.

Figure 20 - Output Bus Timing - Floating AU4 VC Case



The three tributary payload processor may be individually disabled. Incoming data destined to a disabled processor is re-transmitted unchanged to the outgoing data after some delay. The amount of delay is dependent on the relative phase of the incoming frame pulse (IC1J1) and the outgoing frame pulse (OC1J1). Figure 21 shows the delay for the three possible alignments of IC1J1 in relation to OC1J1 in byte interface mode. The delay from the rising edge of SCLK where TUPP-PLUS samples ID[7:0] to the rising edge of SCLK where a downstream device samples OD[7:0] is 5, 6, or 7 cycles. Figure 22 shows the alignment of the data to the frame pulses IC1J1 and OC1J1 in nibble interface mode. The more significant nibble on ID[3:0] and OD[3:0] is transmitted first and is marked by the C1 and J1 pulses. The possible delay values ranges from 11 to 16 NSCLK cycles. The minimum and maximum delay scenarios are shown in Figure 22.

Figure 21 - Byte Interface, By-passed Mode Functional Timing

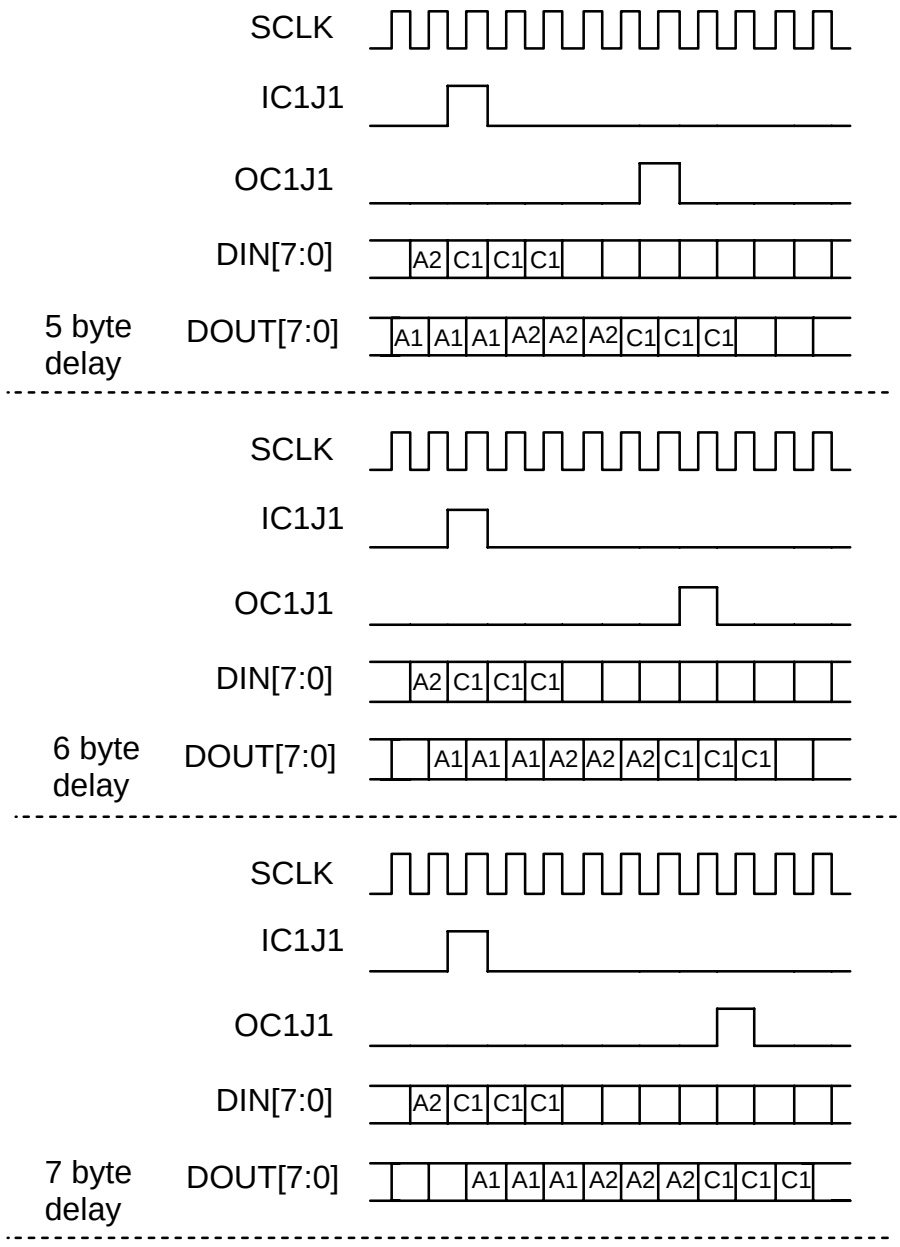
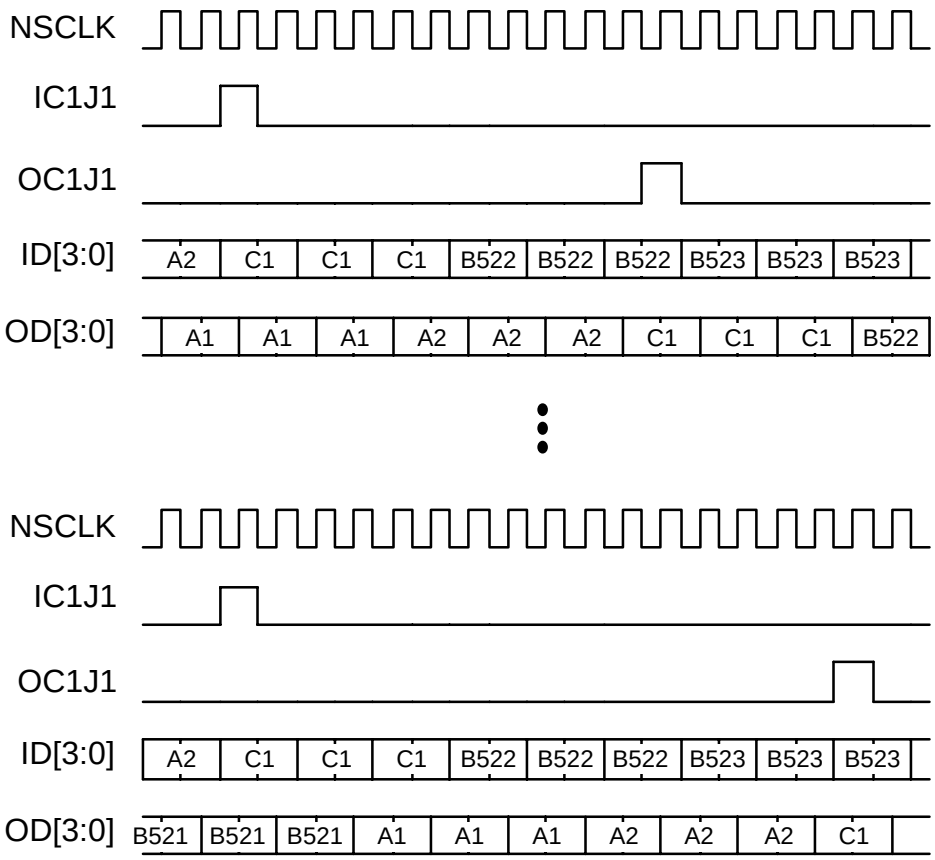


Figure 22 - Nibble Interface, By-passed Mode Functional Timing



The tributary overhead serial interface is shown in Figure 23. The tributary path overhead bytes in each of the STS-1 (AU3) or TUG3 streams on ID[7:0] are individually serialized on POH[3:1]. The most significant bit of the V5 byte of the first tributary (TU#1, TUG2 #1) of each STS-1 stream is identified by a logic high value on the corresponding POHEN[3:1] output. All four tributary path overhead bytes (V5, J2, Z6, Z7) are shifted out once per payload frame. Since the nominal arrival rate of overhead is once per multiframe, each overhead byte is presented on POH an average of four times. To distinguish the first presentation of an overhead byte from subsequent repeat presentations, the corresponding POHEN[3:1] output is set high to mark a fresh byte and set low to mark a stale byte. POHCK provides timing for the POH[3:1], POHFP[3:1] and POHEN[3:1] outputs. POHCK[3:1] are 9.72 MHz clocks and run continuously.

Tributaries on POH are arranged in the order of transmission as in the incoming data stream ID[7:0]. I.e., TU #1 of TUG2 #1, TU#1 of TUG2 #2, ... TU #1 of

TUG2 #7, TU #2 of TUG2 #1, ... TU #2 of TUG2 #7, TU #3 of TUG2 #1, ... TU #4 of TUG2 #7. Timeslot assignment on POH is unrelated to the configuration of the tributary group. Timeslots for four tributaries are always reserved for any tributary group even if it is configured for TU12, VT3 or TU2. At timeslots devoted to non-existent tributaries, for example, tributary 2, 3 and 4 of a TUG2 configured for TU2, POH and POHEN will be set low. The path overhead frame pulse, POHFP, identifies the most significant bit of the first tributary (TU #1 of TUG2 #1) on POH.

In TU3 mode, the POH stream carry the nine path overhead bytes. The bytes are shifted out twice per payload frame. The assignment of TU3 POH bytes to lower order tributary overhead timeslots shown in Figure 13 are:

TU3, J1 -> TU #1, TUG2 #1, V5 and TU #3, TUG2 #1, V5

TU3, B3 -> TU #1, TUG2 #1, J2 and TU #3, TUG2 #1, J2

TU3, C2 -> TU #1, TUG2 #1, Z6 and TU #3, TUG2 #1, Z6

TU3, G1 -> TU #1, TUG2 #1, Z7 and TU #3, TUG2 #1, Z7

TU3, F2 -> TU #1, TUG2 #2, V5 and TU #3, TUG2 #2, V5

TU3, H4 -> TU #1, TUG2 #2, J2 and TU #3, TUG2 #2, J2

TU3, Z3 -> TU #1, TUG2 #2, Z6 and TU #3, TUG2 #2, Z6

TU3, Z4 -> TU #1, TUG2 #2, Z7 and TU #3, TUG2 #2, Z7

TU3, Z5 -> TU #1, TUG2 #3, V5 and TU #1, TUG2 #3, V5

Figure 23 - Tributary Path Overhead Serialization Functional Timing

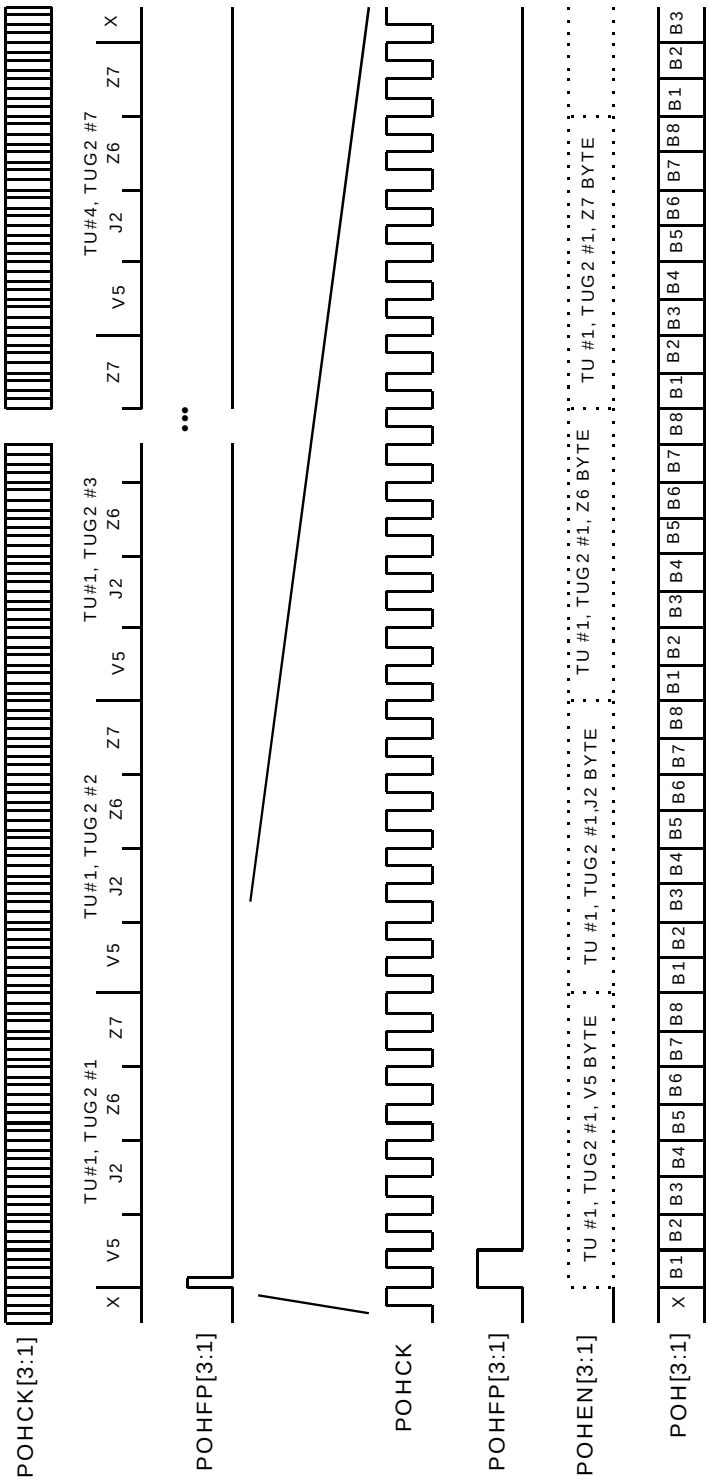


Figure 24 shows the timing of the receive alarm port. Timing is provided by the POHCK[1] output which is a continuous 9.72 MHz clock. The BIP-2, RDI, auxiliary RDI, PDI and LOM indications of all the tributaries in the incoming stream are combined and reported on the RAD output. The bits labeled B1 and B2 reports the number of BIP-2 errors. If the number of BIP-2 errors is one, only one of B1 is set high. Both B1 and B2 are set high when two BIP-2 errors are detected. The bit labeled R and AR reports the remote defect indication (RDI) and auxiliary remote defect indication (ARDI) status of the associated tributary. They are set high due to incoming AIS, LOP, PLSM, PSLU, TIM, TIU and LOM. The bit labeled P report the path defect indication (PDI-P) due to tributary path defect indication PDI-V, AIS, LOP and UNEQ states. The PDI-P indications allow a downstream device where the tributaries are aggregated into an SPE to form a C2 byte containing the count of tributaries in alarm state. The bit labeled L reports the loss of multiframe state. Tributaries timeslots on RAD are arranged in the order of transmission as in the incoming data stream ID[7:0]. I.e., TU #1 of TUG2 #1 TUG3 #1, TU #1 of TUG2 #1 TUG3 #2, TU #1 of TUG2 #1 TUG3 #3, TU#1 of TUG2 #2 TUG3 #2, ... TU #1 of TUG2 #7 TUG3 #3, TU #2 of TUG2 #1 TUG3 #1, ..., TU #2 of TUG2 #7 TUG3 #3, ..., TU #4 of TUG2 #7 TUG3 #3. Timeslot assignment on RAD is unrelated to the configuration of the tributary group. Timeslots for four tributaries are always reserved for any tributary group even if it is configured for TU12, VT3 or TU2. At timeslots devoted to non-existent tributaries, for example, tributary 2, 3 and 4 of a TUG2 configured for TU2, RAD will be set low. The path overhead frame pulse, POHFP[1], identifies the BIP-2 error indication for the odd-numbered bits of the first tributary (TU #1 of TUG2 #1 STS-1 #1) on RAD.

When a TUG3 stream is configured in TU3 mode, the segregation of RAD, for that TUG3, into tributary timeslots are dissolved. Any bit normally carrying tributary BIP-2 indications may carry a TU3 BIP-8 error indication. All remaining bits will report the associated state of the TU3 stream simultaneously.

When a TUG3 is bypassed by setting corresponding TUGEN bit in the VTPP Configuration register low, no performance monitoring is performed on that TUG3 stream. Consequently, the timeslots associated with the bypassed stream on the RAD stream are invalid.

Figure 24 - Receive Alarm Port Functional Timing

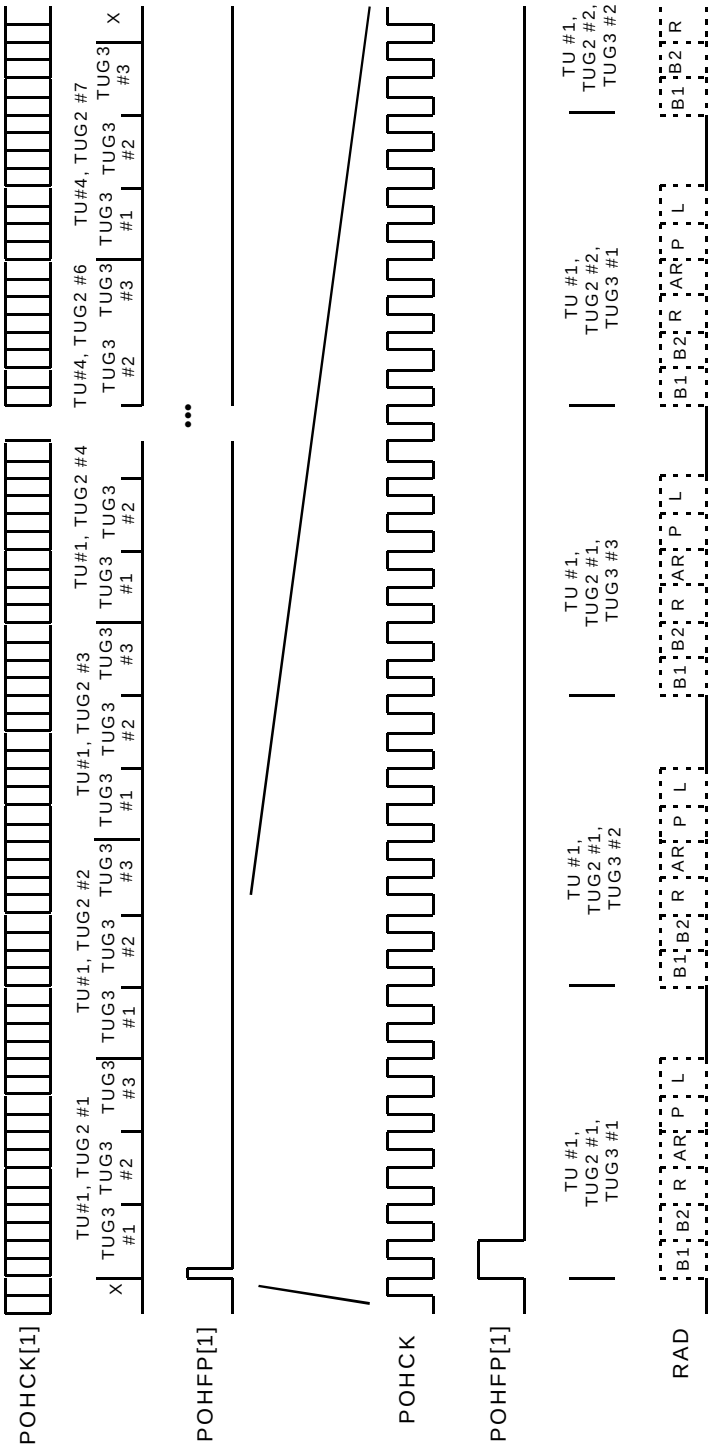
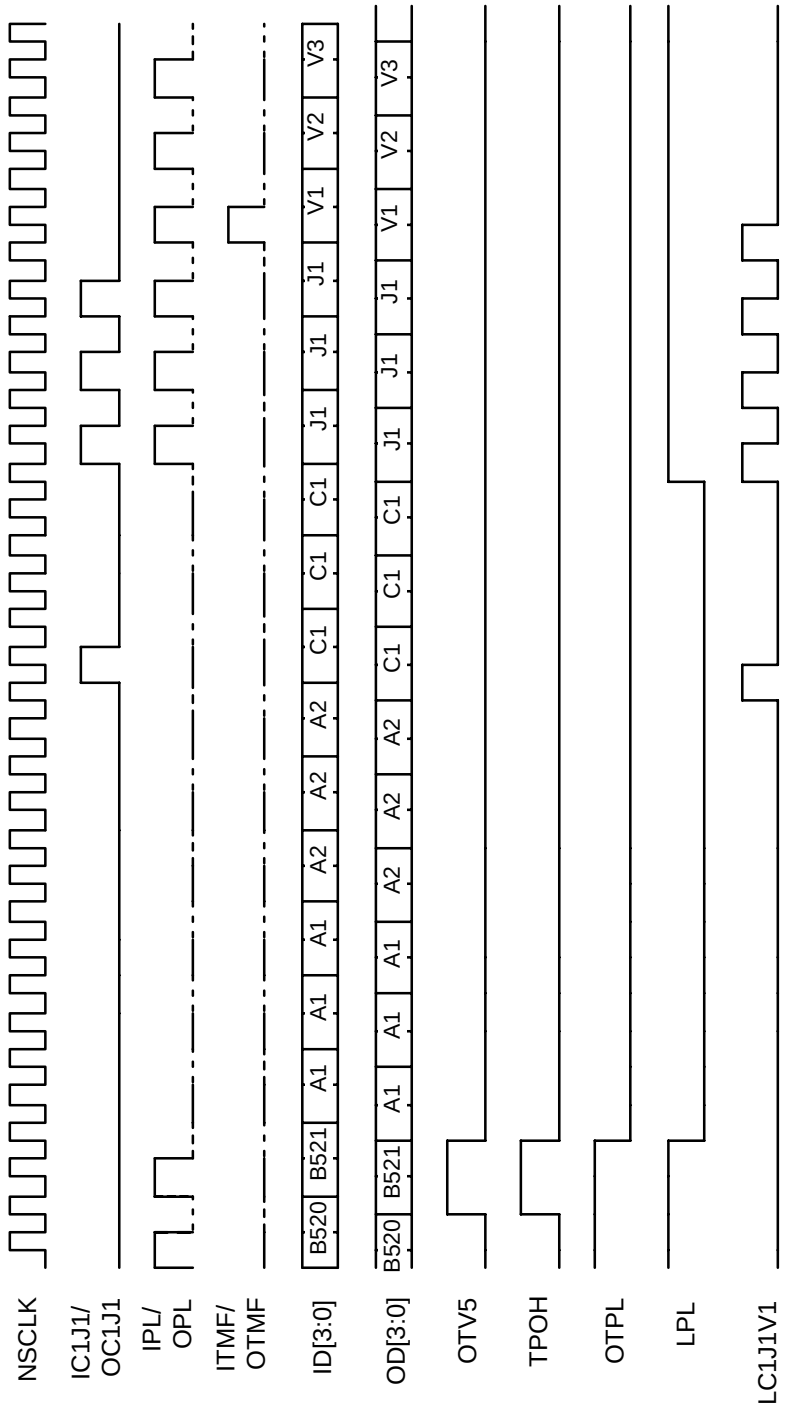


Figure 25 illustrates the input and output timing in nibble interface mode. For each byte on the incoming data stream ID[3:0], the more significant nibble is transmitted first, followed by the less significant nibble. The more significant nibble of the C1 byte on ID[3:0] is marked by a high pulse on IC1J1 while IPL is set low. IC1J1 is always set low at the less significant nibble of any byte. Similarly, the more significant nibble of the J1 byte(s) is (are) marked by a high pulse on IC1J1 while IPL is set high. IPL is only meaningful during the more significant nibble of each incoming data byte and is ignored during the less significant nibble. The first frame of each incoming tributary multiframe is marked by a pulse on ITMF. ITMF is only meaningful during the more significant nibble and is ignored during the less significant nibble.

The outgoing data stream OD[3:0] behaves similarly to the incoming data stream. The more significant nibble of each byte is transmitted first, followed by the less significant nibble. The more significant nibble of the C1 byte on OD[3:0] is marked by a high pulse on OC1J1 while OPL is set low. OC1J1 is always set low at the less significant nibble of any byte. Similarly, the more significant nibble of the J1 byte(s) is (are) marked by a high pulse on OC1J1 while OPL is set high. OPL is only meaningful during the more significant nibble of each incoming data byte and is ignored during the less significant nibble. The first frame of each incoming tributary multiframe is marked by a pulse on OTMF. OTMF is only meaningful during the more significant nibble and is ignored during the less significant nibble. The OTV5 output identifies both nibbles of the V5 bytes on the outgoing stream while OTPL identifies both nibbles of tributary payload bytes. All tributary path overhead bytes are identified by the TPOH signal. The LC1J1V1 output marks the transport frame, payload frame and tributary multiframe boundaries on OD[3:0] when the TUPP-PLUS is operating in locked mode. It will only pulse high during the more significant nibble of the identified bytes and will be set low during the less significant nibble of any byte. The LPL output identifies payload bytes on OD[3:0]. LPL is set to the same value on both the more and less significant nibbles.

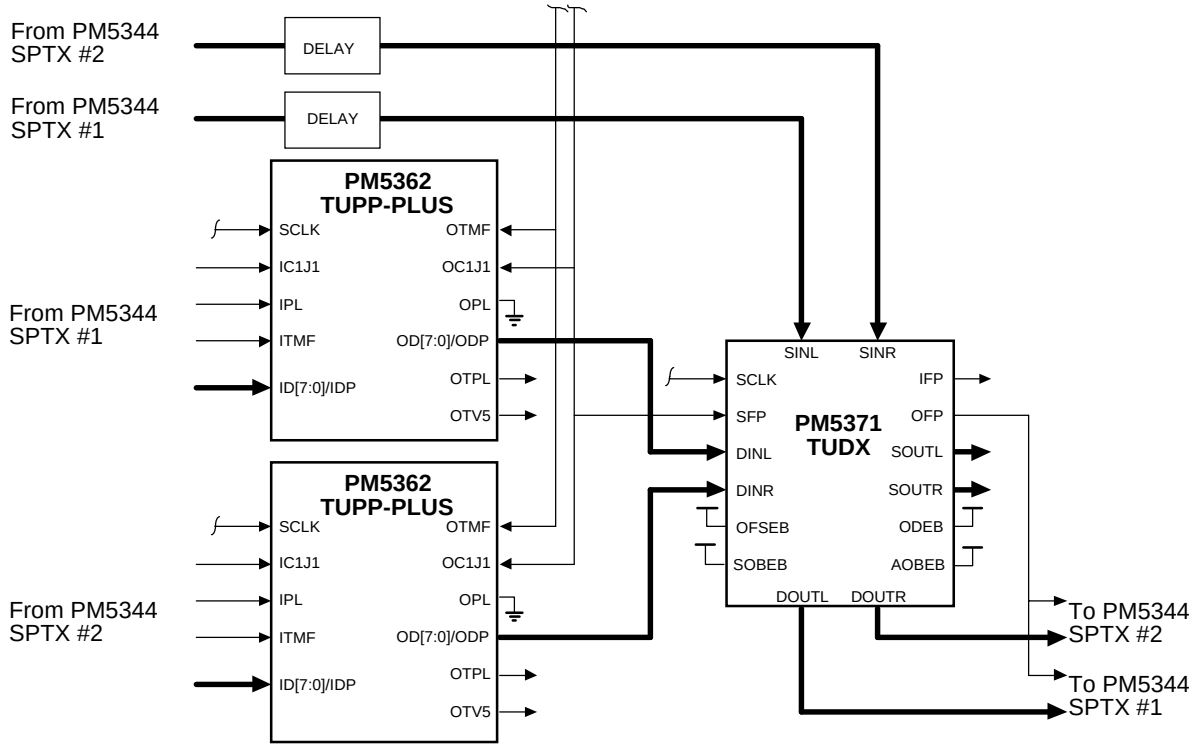
Figure 25 - Nibble Interface Mode Input/Output Functional Timing



13 APPLICATION EXAMPLES

The TUPP-PLUS is typically used as part of a SONET/SDH tributary cross-connect. The TUPP-PLUS can be used to transfer the payloads of incoming tributaries into outgoing tributaries that are aligned to facilitate switching. A typical example is illustrated in Figure 26. This example shows the tributaries extracted from an STS-1 or AU3 path terminating device, such as the PM5344 SPTX SONET/SDH Path Terminating Transceiver, being routed through TUPP-PLUS so as to be aligned for cross-connection using the PM5371 TUDX SONET/SDH Tributary Unit Cross-Connect. The TUPP-PLUS (and SPTX) can be bypassed by switching through whole STS-1s or AU3s that are output by the SPTX through a delay that matches the delay between the C1 pulse on IC1J1 and the C1 pulse on OC1J1. Note that in this application example, the TUPP-PLUS is operating in locked output mode (i.e. their OJ1EN bits are low) to allow convenient interfacing to the TUDX.

Figure 26 - SONET/SDH Tributary Cross-Connect Application



14 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

Table 5 - TUPP-PLUS Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+220°C
Absolute Maximum Junction Temperature	+150°C
Power Dissipation	1.5 W

15 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 6 - TUPP-PLUS D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage			0.4	Volts	I_{OL} = -8 mA for INTB, D[7:0], POHCK and GSCLK[1] I_{OL} = -4 mA for all others Note 3
V_{OH}	Output or Bidirectional High Voltage	VDD-1.0			Volts	I_{OH} = 8 mA for INTB, D[7:0], POHCK and GSCLK[1] I_{OH} = 4 mA for all others Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	
I_{ILPU}	Input Low Current (Pull-ups)	+100	+350	+525	µA	V_{IL} = GND, Notes 1, 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IHPU}	Input High Current (Pull-ups)	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP1}	Operating Current Processing Tributaries			185	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Processing Tributaries
I_{DDOP2}	Operating Current Tributary Processing Disabled			80	mA	V_{DD} = 5.5 V, Outputs Unloaded, SCLK = 19.44 MHz, Alternating Data, Tributary Processors Bypassed

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.

2. Input pin or bidirectional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. Input pin or bidirectional pin with internal pull-down resistor.

16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 7 - Microprocessor Interface Read Access (Figure 27, Figure 28)

Symbol	Parameter	Min	Typ	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25			ns
tH_{AR}	Address to Valid Read Hold Time	25			ns
tS_{RWB}	RWB to Valid Read Set-up Time	25			ns
tH_{RWB}	RWB to Valid Read Hold Time		10		ns
tS_{ALR}	Address to Latch Set-up Time	20			ns
tH_{ALR}	Address to Latch Hold Time	20			ns
tV_{L}	Valid Latch Pulse Width	20			ns
tS_{LR}	Latch to Read Set-up	0			ns
tH_{LR}	Latch to Read Hold	20			ns
tP_{RD}	Valid Read to D[7:0] Valid			80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state			20	ns
tZ_{INTH}	Valid Read Negated to INTB High			70	ns

Figure 27 - Microprocessor Interface Read Timing (Intel Mode)

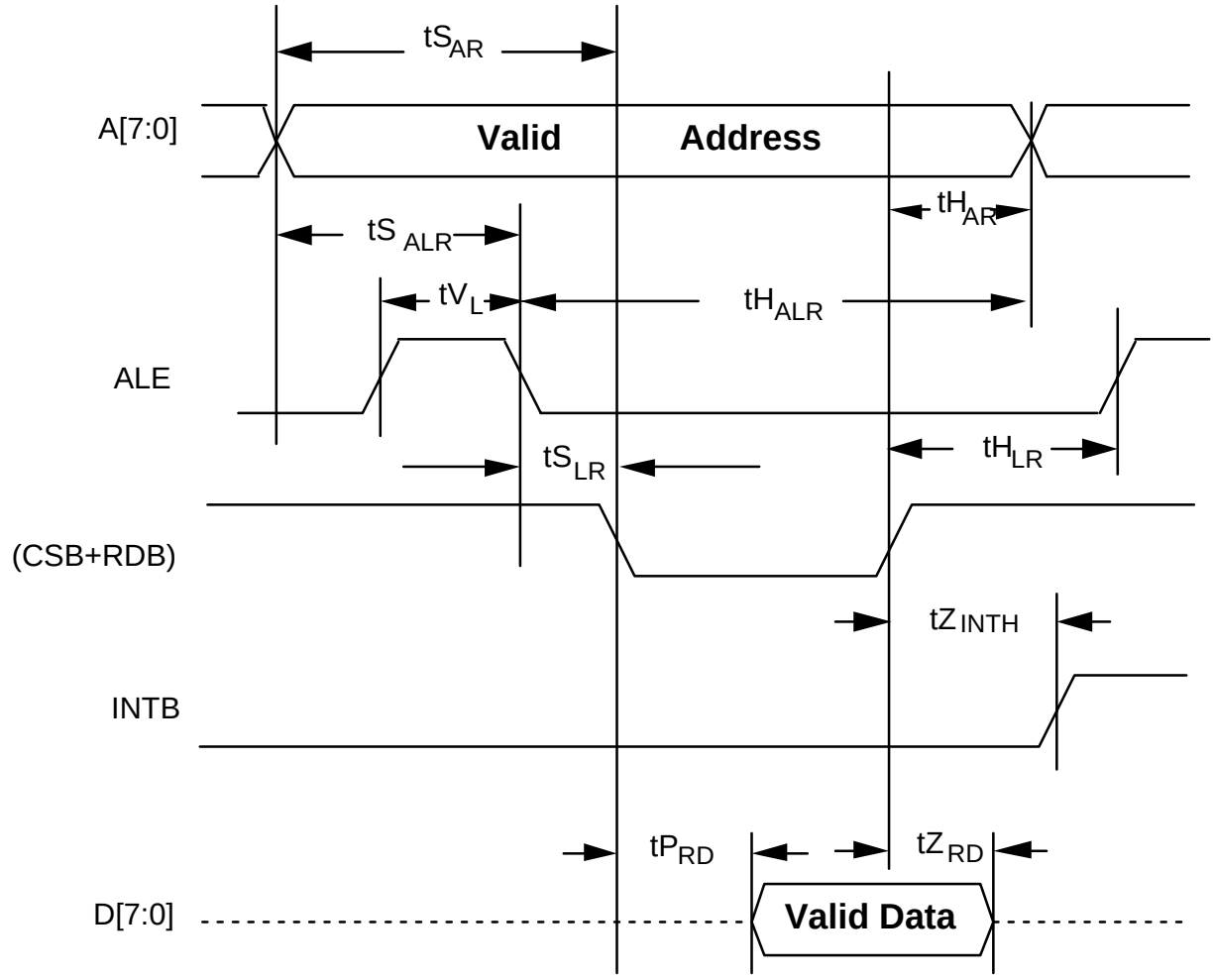
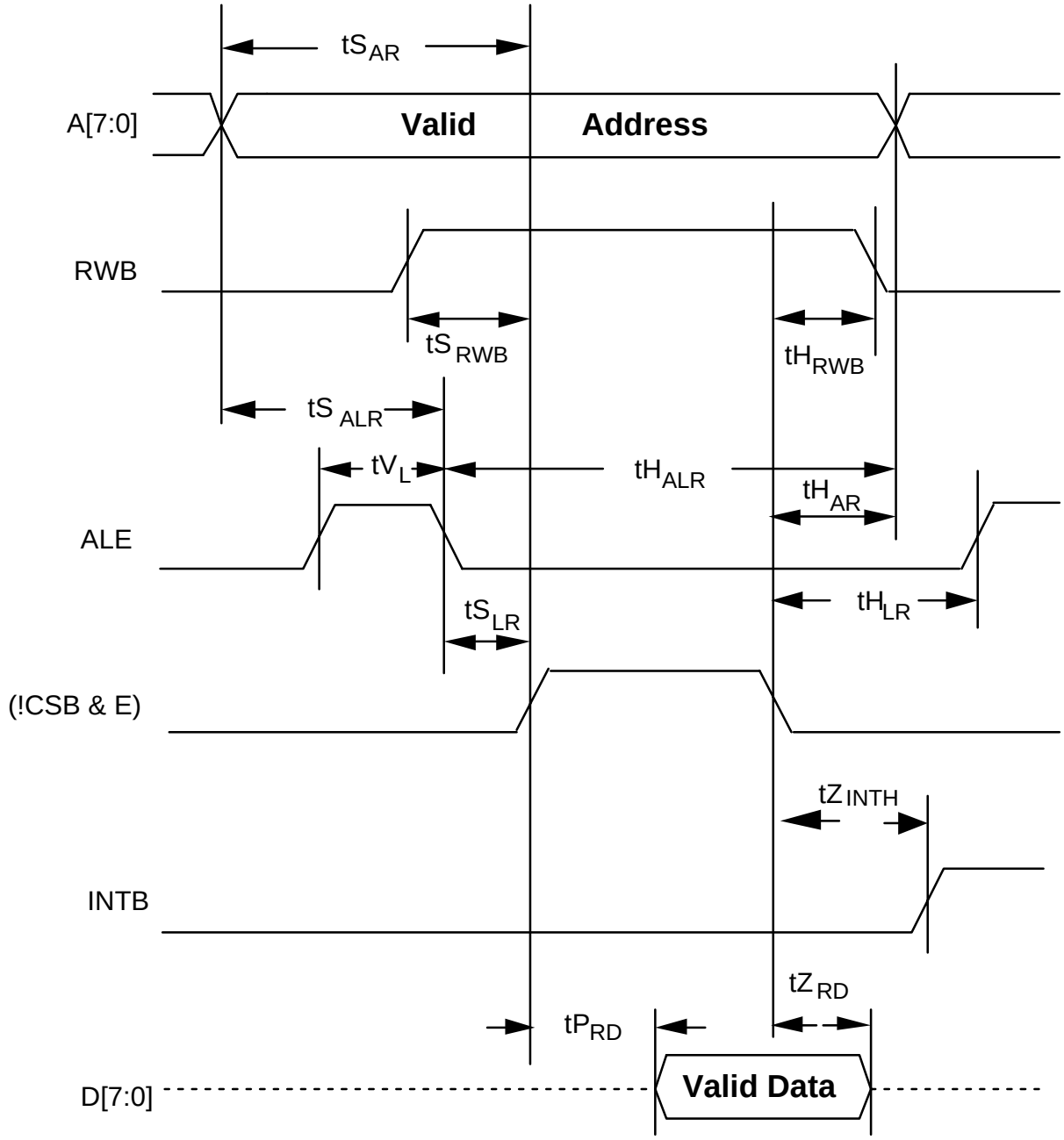


Figure 28 - Microprocessor Interface Read Timing (Motorola Mode)



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. a. In Intel mode, a valid read enable bar is defined as a logical OR of the CSB and the RDB signals.

   b. In Motorola mode, a valid read enable is defined as a logical AND of the E signal, the RWB signal, and the inverted CSB signal.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameters tH_{AR} and tS_{AR} are not applicable if address latching is used.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

9. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the ±300mV of the termination voltage on the output. The test load is 50Ω to 1.4V in parallel with 10pF to GND.

Table 8 - Microprocessor Interface Write Access (Figure 29, Figure 30)

Symbol	Parameter	Min	Typ	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25			ns
tS_{DW}	Data to Valid Write Set-up Time	20			ns
tS_{ALW}	Address to Latch Set-up Time	20			ns
tH_{ALW}	Address to Latch Hold Time	20			ns
tV_{L}	Valid Latch Pulse Width	20			ns
tS_{LW}	Latch to Write Set-up	0			ns
tH_{LW}	Latch to Write Hold	20			ns
tH_{DW}	Data to Valid Write Hold Time	20			ns
tH_{AW}	Address to Valid Write Hold Time	25			ns
tV_{WR}	Valid Write Pulse Width	40			ns
tS_{RWB}	RWB to Write Set-up Time	25			ns
tH_{RWB}	RWB to Write Hold Time		10		ns

Figure 29 - Microprocessor Interface Write Timing (Intel Mode)

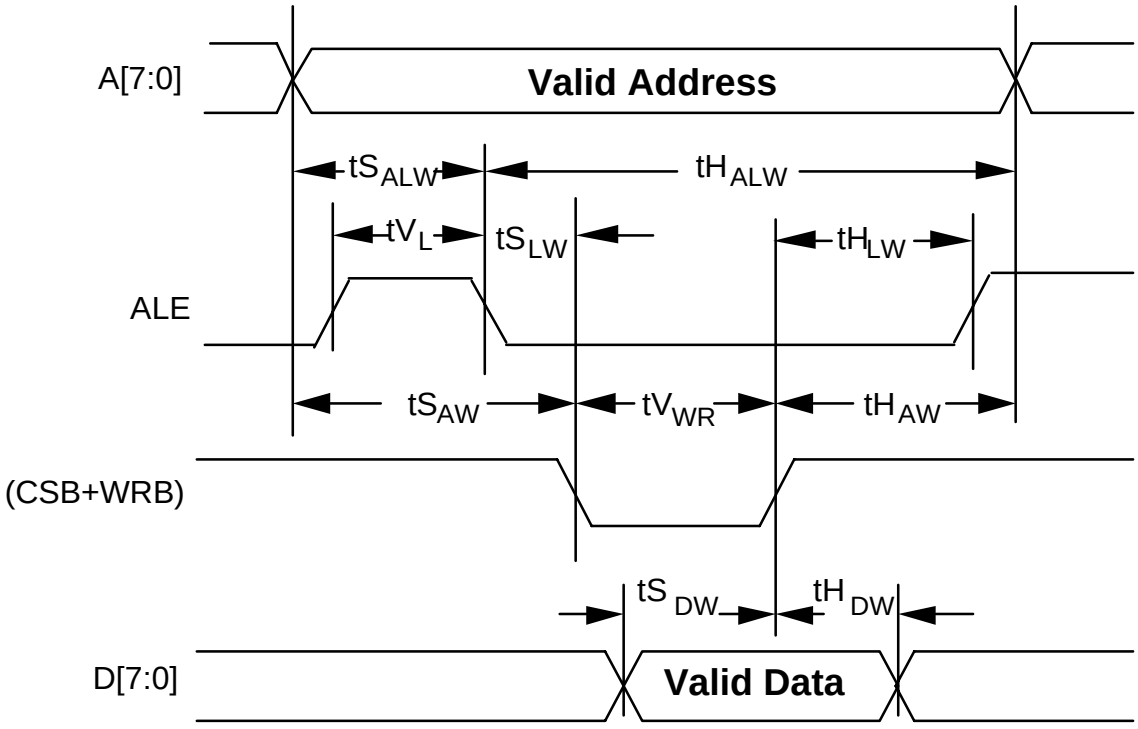
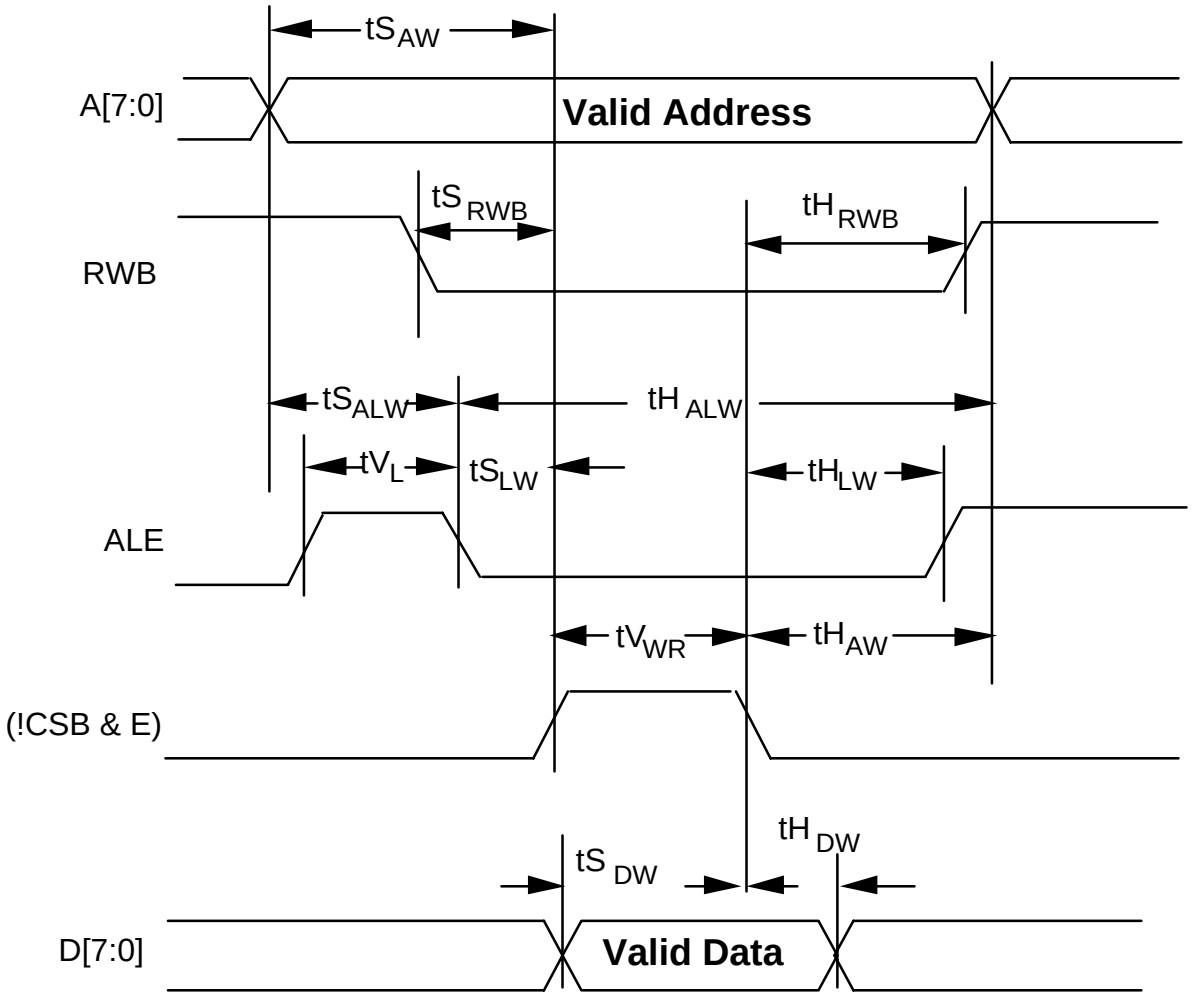


Figure 30 - Microprocessor Interface Write Timing (Motorola Mode)



Notes on Microprocessor Interface Write Timing:

1. a. In Intel mode, a valid write strobe bar is defined as a logical OR of the CSB and the WRB signals.

   b. In Motorola mode, a valid write strobe is defined as a logical AND of the E signal, the inverted RWB signal, and the inverted CSB signal.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

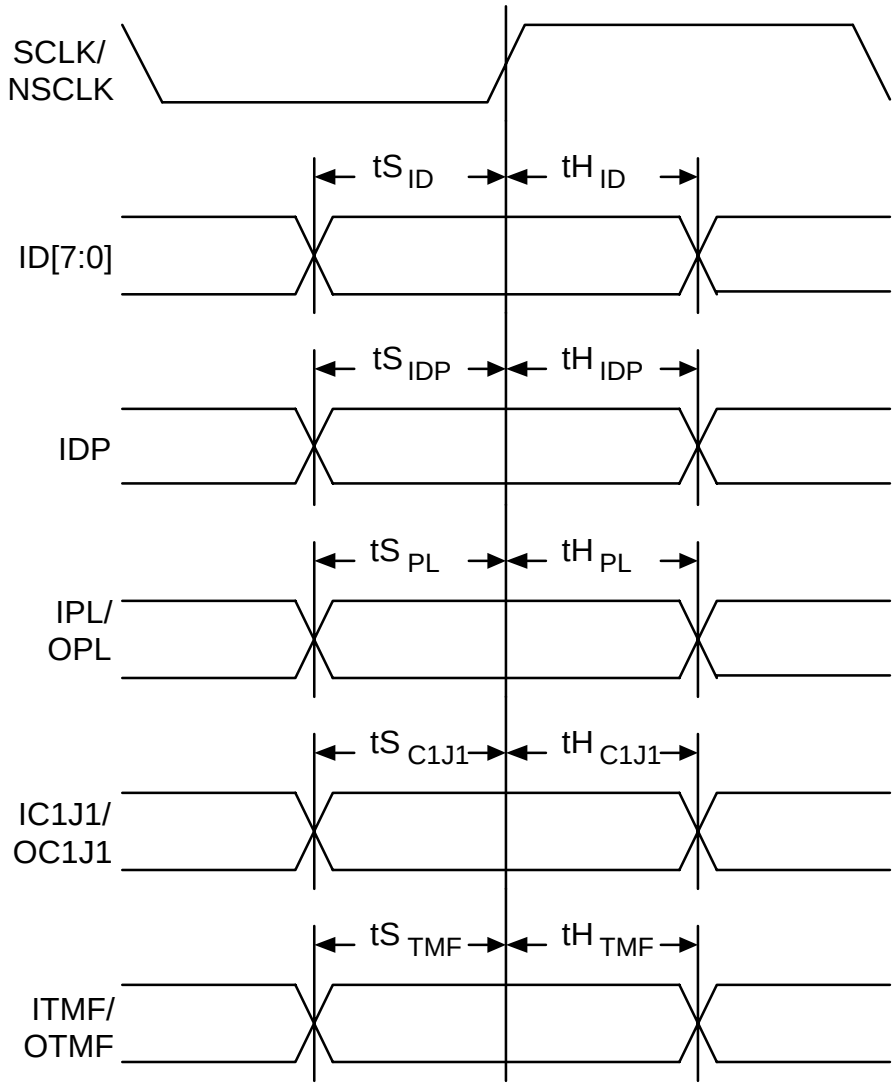
17 TUPP-PLUS TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Table 9 - TUPP-PLUS Input (Figure 31)

Symbol	Description	Min	Max	Units
	SCLK Frequency (nominally 19.44 MHz)		20	MHz
	SCLK Duty Cycle	40	60	%
	NSCLK Frequency (nominally 38.88 MHz)		40	MHz
	NSCLK Duty Cycle	40	60	%
tS_{ID}	ID[7:0] Set-up Time	5		ns
tH_{ID}	ID[7:0] Hold Time	3		ns
tS_{IDP}	IDP Set-up Time	5		ns
tH_{IDP}	IDP Hold Time	3		ns
tS_{PL}	IPL and OPL Set-Up Time	5		ns
tH_{PL}	IPL and OPL Hold Time	3		ns
tS_{C1J1}	IC1J1 and OC1J1 Set-Up Time	5		ns
tH_{C1J1}	IC1J1 and OC1J1 Hold Time	3		ns
tS_{TMF}	ITMF and OTMF Set-Up Time	5		ns
tH_{TMF}	ITMF and OTMF Hold Time	3		ns

Figure 31 - Input Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 10 - TUPP-PLUS Stream Output (Figure 32)

Symbol	Description	Min	Max	Units
tP_{OD}	SCLK High to OD[7:0] Valid	4	25	ns
tP_{ODP}	SCLK High to ODP Valid	4	25	ns
tP_{TPL}	SCLK High to OTPL Valid	4	25	ns
tP_{TV5}	SCLK High to OTV5 Valid	4	25	ns
tP_{TPOH}	SCLK High to TPOH Valid	4	25	ns
tP_{AIS}	SCLK High to AIS Valid	4	25	ns
tP_{IDLE}	SCLK High to IDLE Valid	4	25	ns
tP_{LC1}	SCLK High to LC1J1V1 Valid	4	25	ns
tP_{LPL}	SCLK High to LPL Valid	4	25	ns
tP_{LOM}	SCLK High to LOM Valid	4	25	ns
tP_{OD}	NSCLK High to OD[3:0] Valid	3	20	ns
tP_{ODP}	NSCLK High to ODP Valid	3	20	ns
tP_{TPL}	NSCLK High to OTPL Valid	3	20	ns
tP_{TV5}	NSCLK High to OTV5 Valid	3	20	ns
tP_{TPOH}	NSCLK High to TPOH Valid	3	20	ns
tP_{AIS}	NSCLK High to AIS Valid	3	20	ns
tP_{IDLE}	NSCLK High to IDLE Valid	3	20	ns
tP_{LC1}	NSCLK High to LC1J1V1 Valid	3	20	ns
tP_{LPL}	NSCLK High to LPL Valid	3	20	ns

Figure 32 - Stream Output Timing

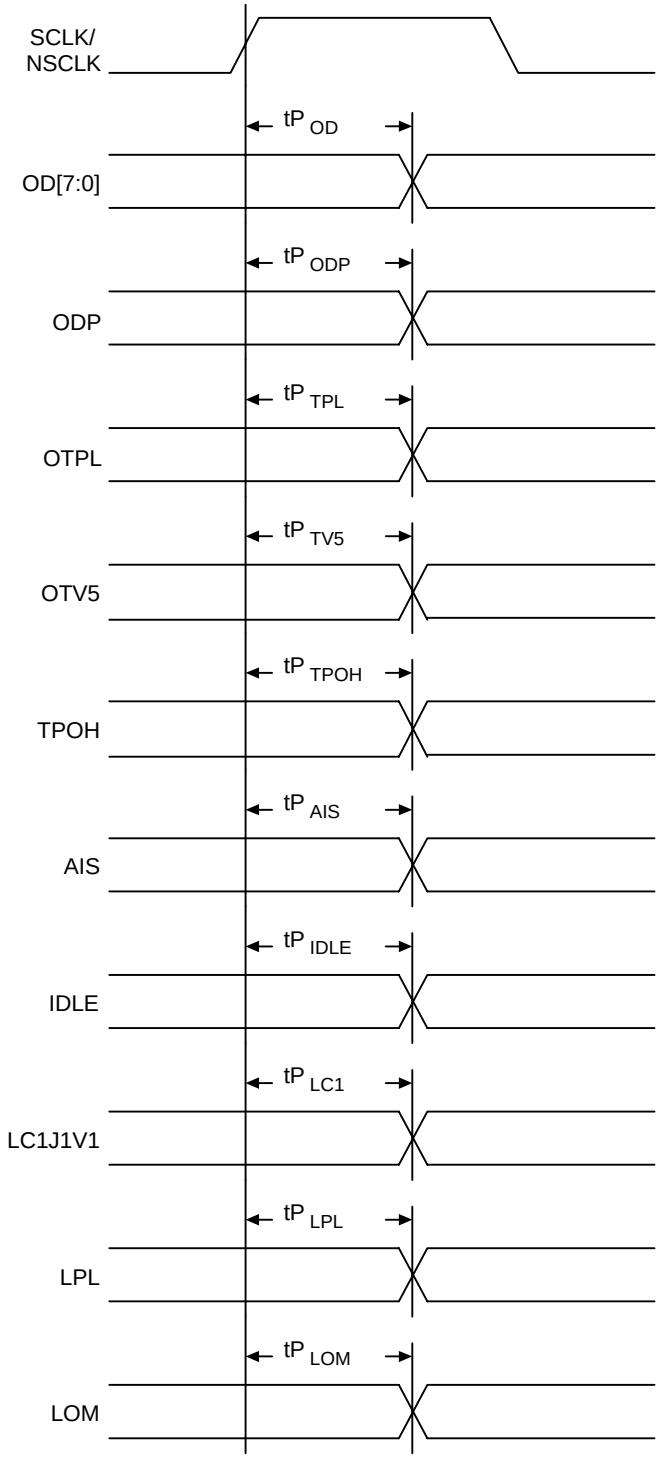


Table 11 - TUPP-PLUS Path Overhead Output (Figure 33)

Symbol	Description	Min	Max	Units
tP_{POH}	POHCK Low to POH[3:1] Valid	-5	25	ns
tP_{POHFP}	POHCK Low to POHFP[3:1] Valid	-5	25	ns
tP_{POHEN}	POHCK Low to POHEN[3:1] Valid	-5	25	ns
tP_{RAD}	POHCK Low to RAD Valid	-5	25	ns

Figure 33 - Path Overhead Output Timing

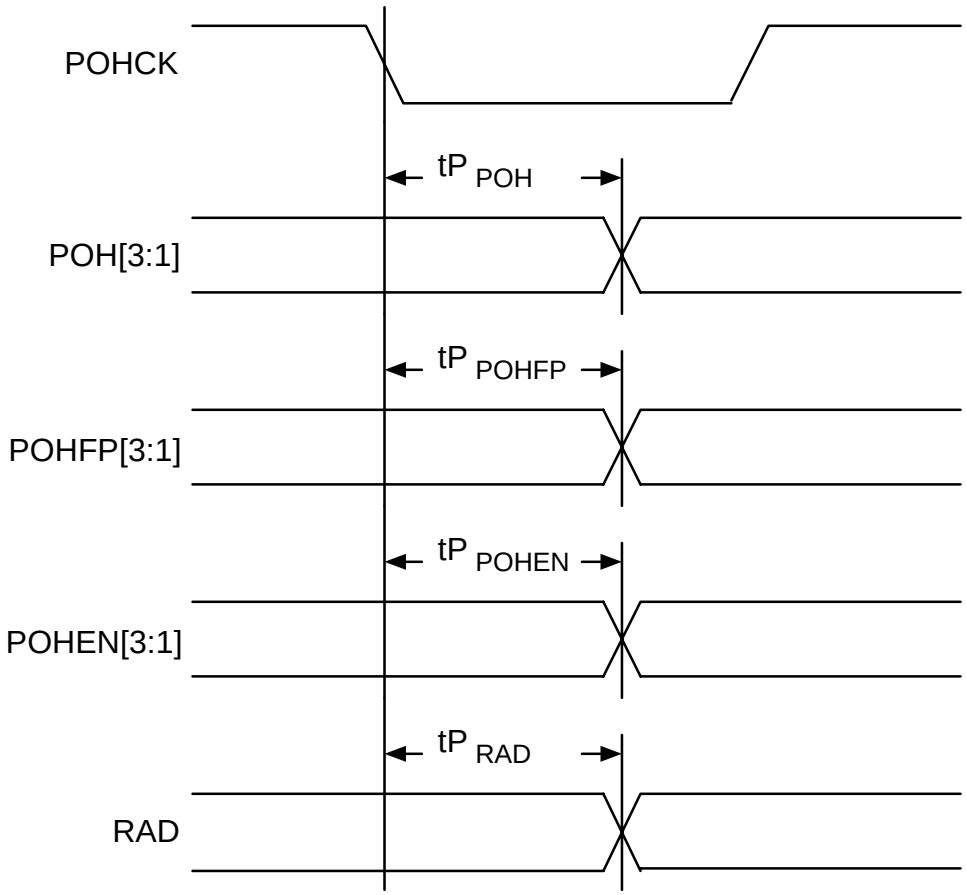
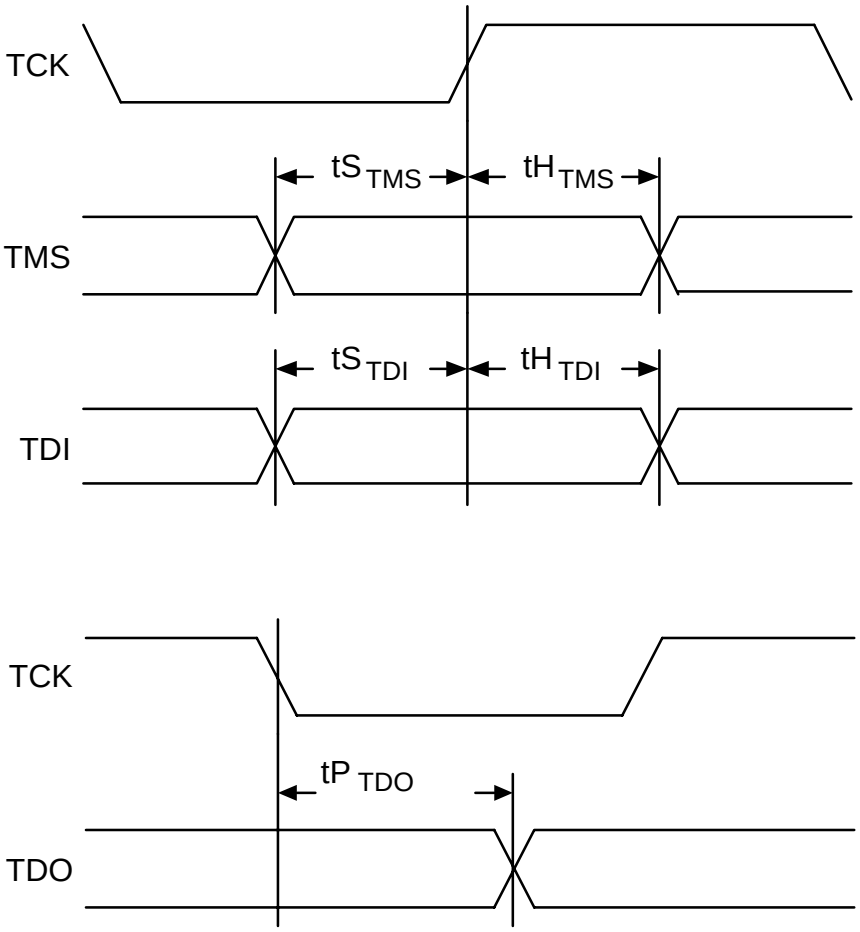


Table 12 - JTAG Port Interface (Figure 34)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 34 - JTAG Port Interface Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Output propagation delays are measured with a 50 pF load on the outputs.

3. Output propagation delays of signal outputs that are specified in relation to a reference output are measured with a 50 pF load on both the signal output and the reference output.

18 ORDERING AND THERMAL INFORMATION

Table 13 - TUPP-PLUS Ordering Information

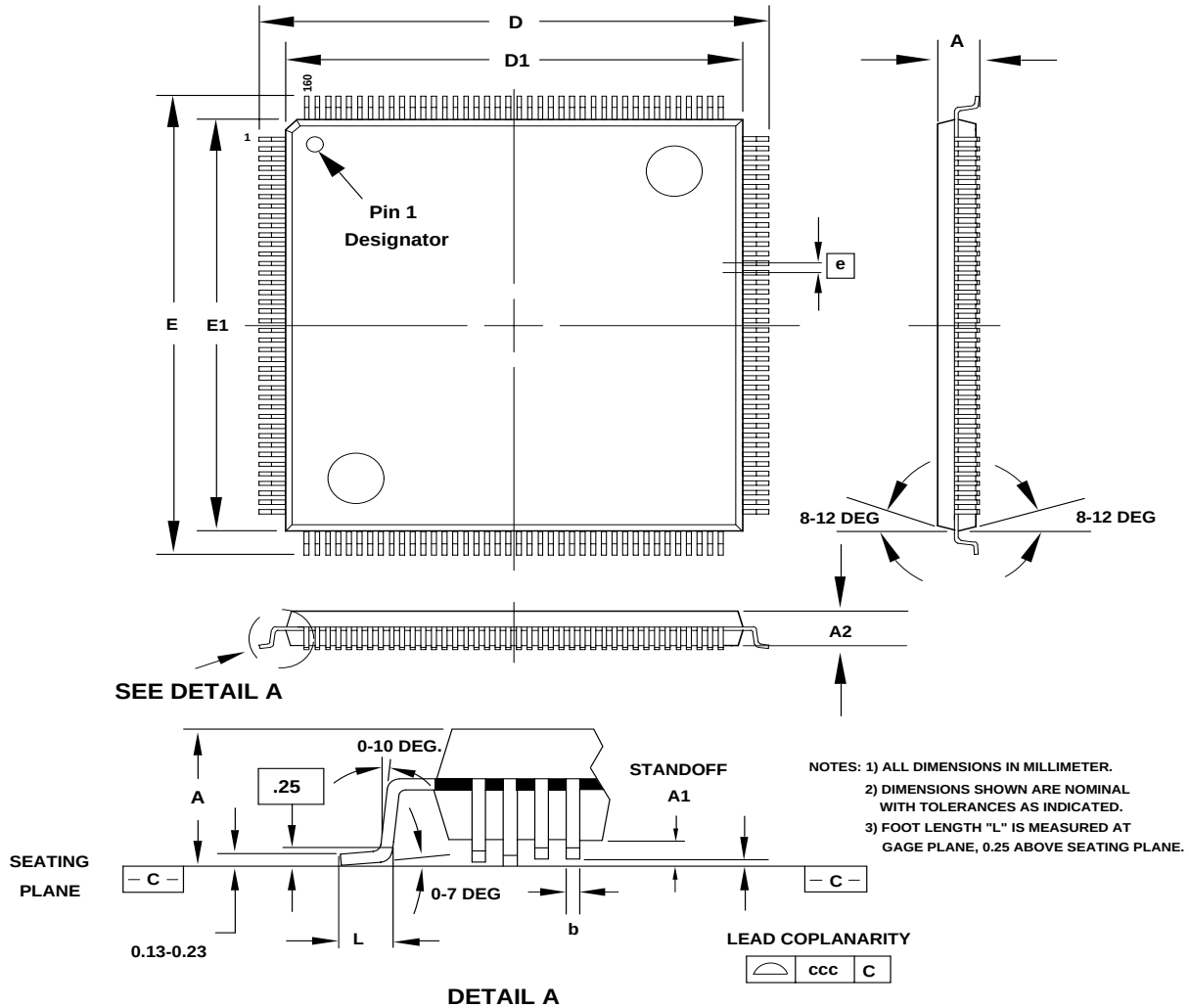
PART NO.	DESCRIPTION
PM5362-RI	160 Metric Plastic Quad Flat Pack (MQFP)

Table 14 - TUPP-PLUS Thermal Information

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM5362-RI	-40°C to 85°C	35°C/W	9°C/W

19 MECHANICAL INFORMATION

Figure 35 - METRIC PLASTIC QUAD FLATPACK - MQFP (BODY 28x28x3.49MM) 160 PIN MQFP - (R SUFFIX)



PACKAGE TYPE: 160 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 28 x 28 x 3.49 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	3.42	0.25	3.17	30.95	27.85	30.95	27.85	0.73		0.22	
Nom.			3.42	31.20	28.00	31.20	28.00	0.88	0.65		
Max.	4.07	0.39	3.68	31.45	28.10	31.45	28.10	1.03		0.38	0.10

NOTES

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-951010 (P6) ref PMC-940528 (P9) Issue date: March 1998