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VFD Driver/Controller IC **PT6315**

DESCRIPTION

PT6315 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/12 duty factor. Sixteen segment output lines, 4 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6315 via a three-line serial interface. It is housed in a 44-pin, SSOP and LQFP Package.

FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (16 x 2 matrix)
- Multiple Display Modes: (16 segments, 12 digits to 24 segments, 4 digits)
- 8-Step Dimming Circuitry
- LED Ports Provided (4 channels, 20 mA max.)
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 44-pin, SSOP and LQFP Package

APPLICATION

- Microcomputer Peripheral Device

BLOCK DIAGRAM

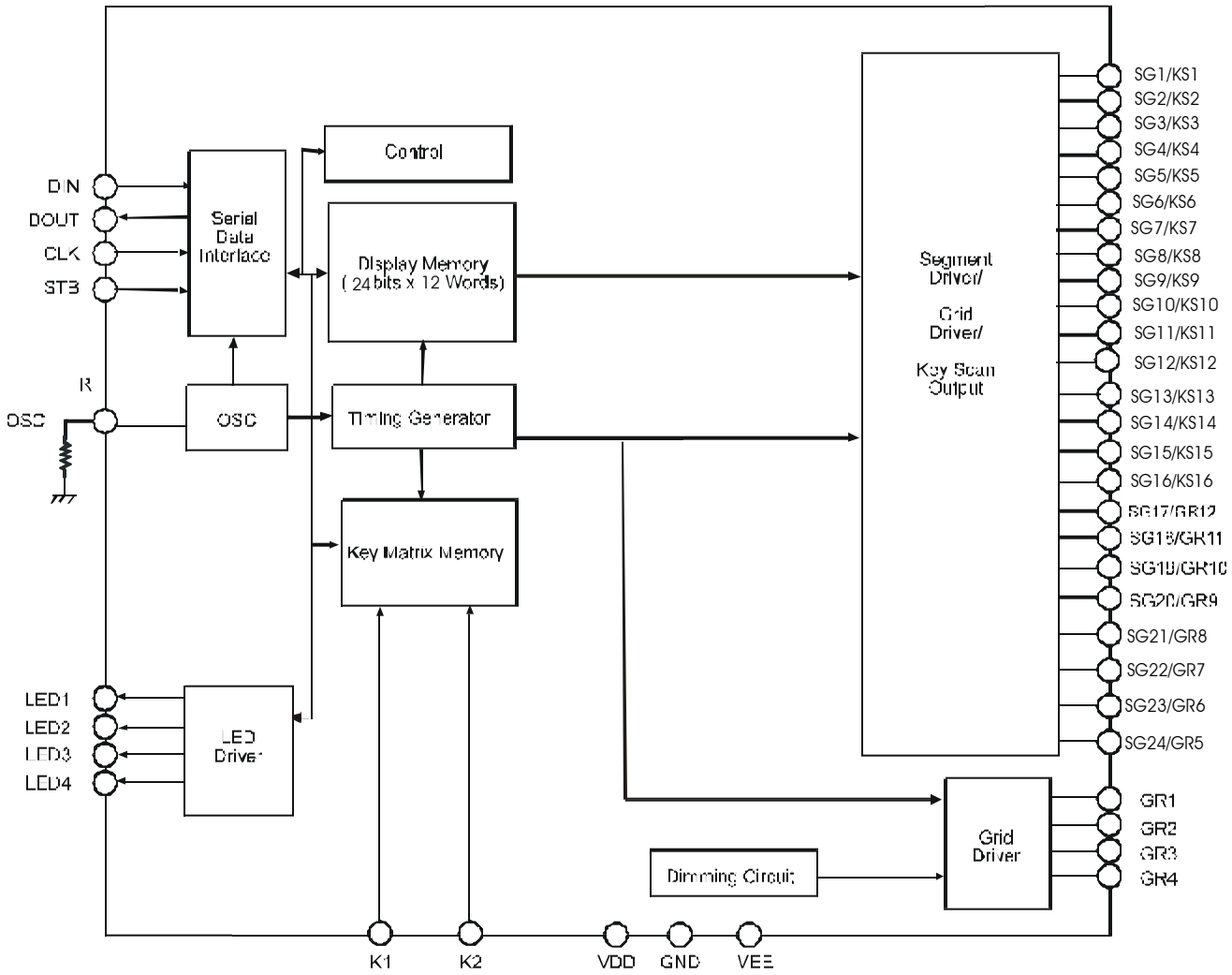


Figure 1: PT6315 Internal Block Diagram

PIN CONFIGURATION 44PIN LQFP

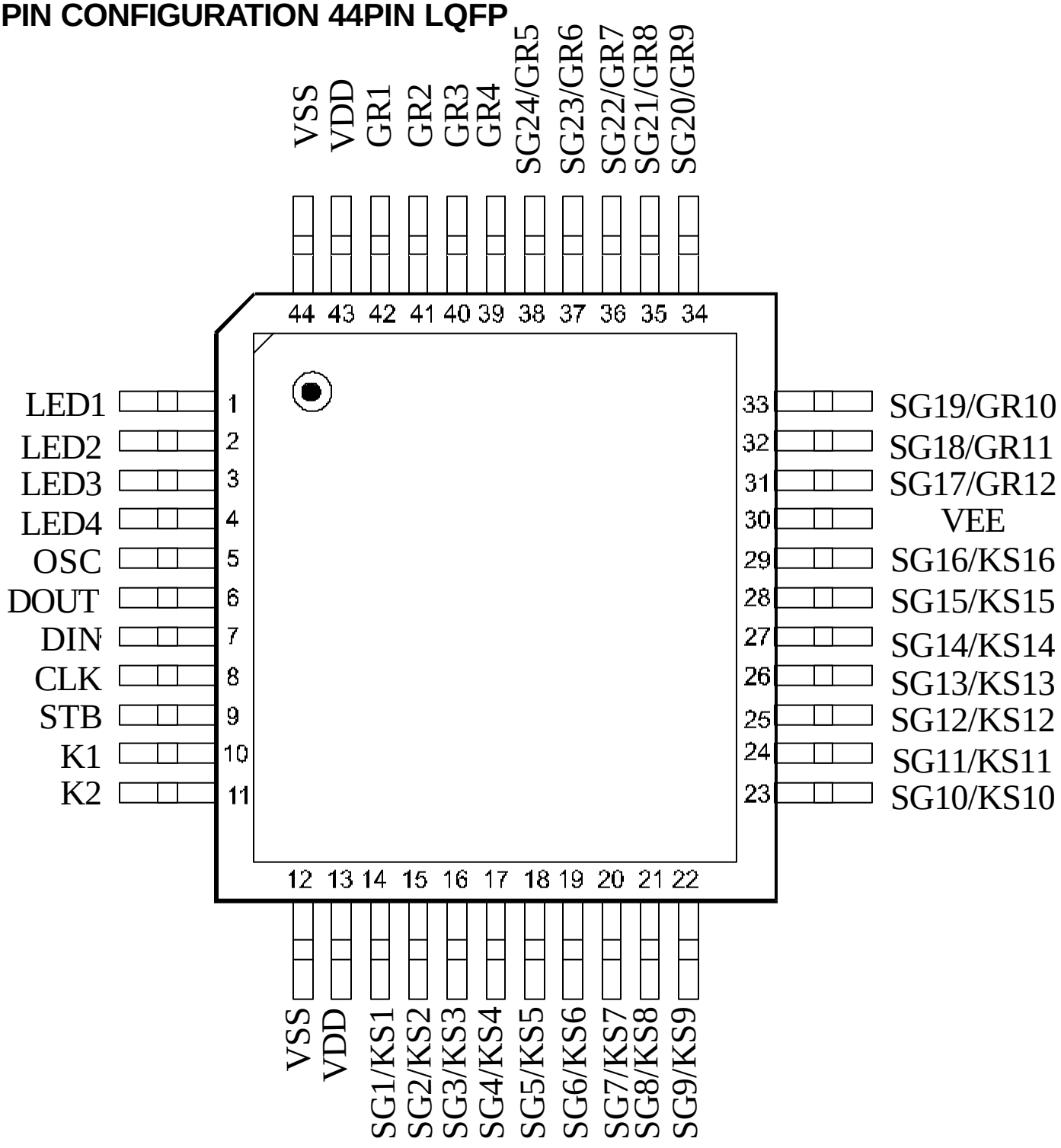


Figure 2: PT6315 LQFP Pin Configuration

PIN CONFIGURATION 44PIN SSOP

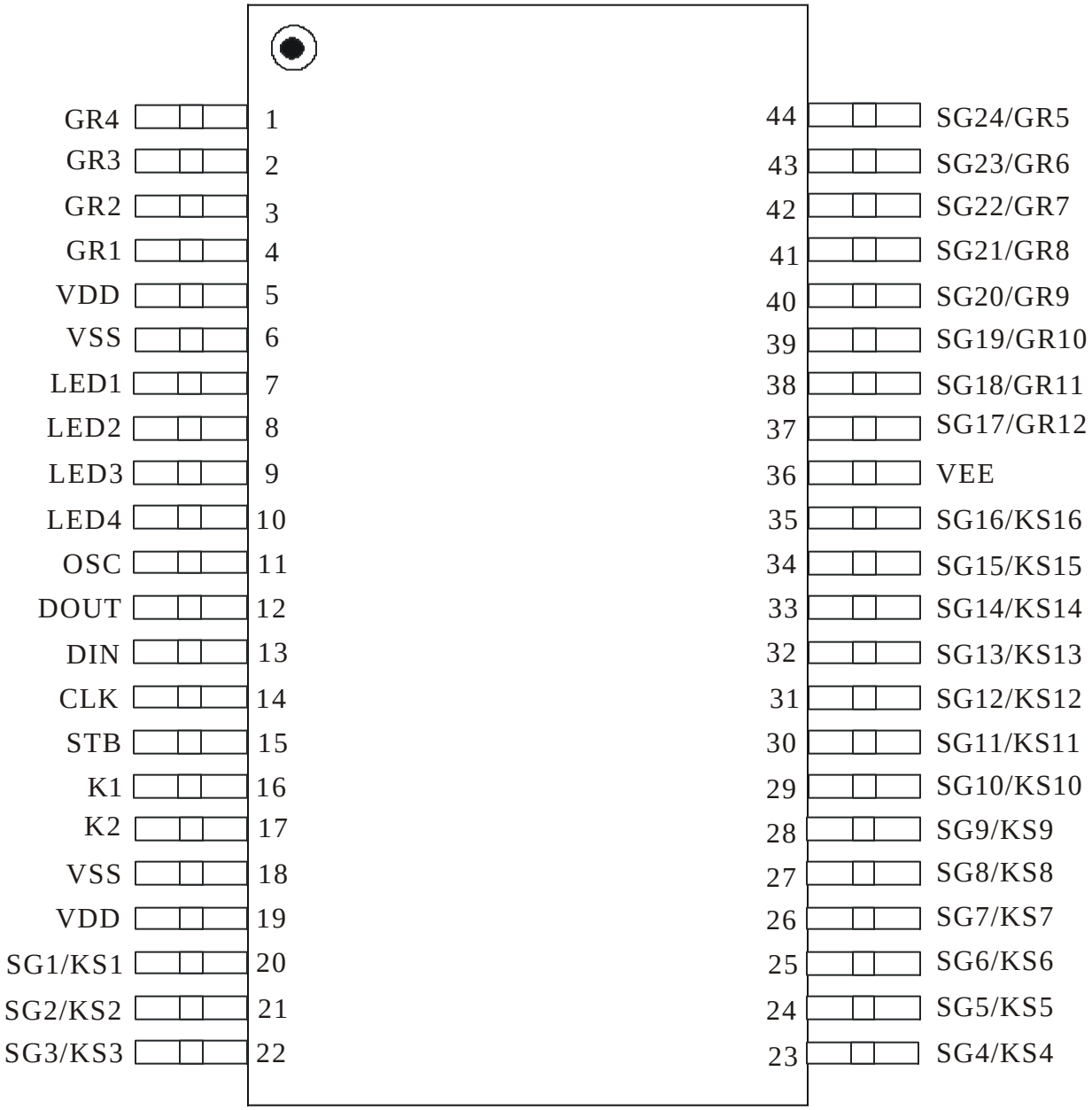


Figure 3: PT6315 SSOP Pin Configuration

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
LED1 to LED4	O	LED Output Pin	1 to 4
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	5
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	6
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	7
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	9
K1 to K2	I	Key Data Input Pins The data inputted to these pins are latched at the end of the display cycle.	10 ,11
VSS	-	Logic Ground Pin	12,44
VDD	-	Logic Power Supply	13,43
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source	14 to 29
VEE	-	Pull-Down Level	30
SG17/GR12 to SG24/GR5	O	High Voltage Segment/Grid Output Pins	31 to 38
GR4 to GR1	O	High-Voltage Grid Output Pins	39 to 42

FUNCTIONAL DESCRIPTION

Commands

Commands determine the display mode and status of PT6315. A command is the first byte (b0 to b7) inputted to PT6315 via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6315 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6315 via the DIN Pin when STB is "LOW". However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/12 duty, 16 to 24 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned "ON", the 12-digit , 16-segment modes is selected.

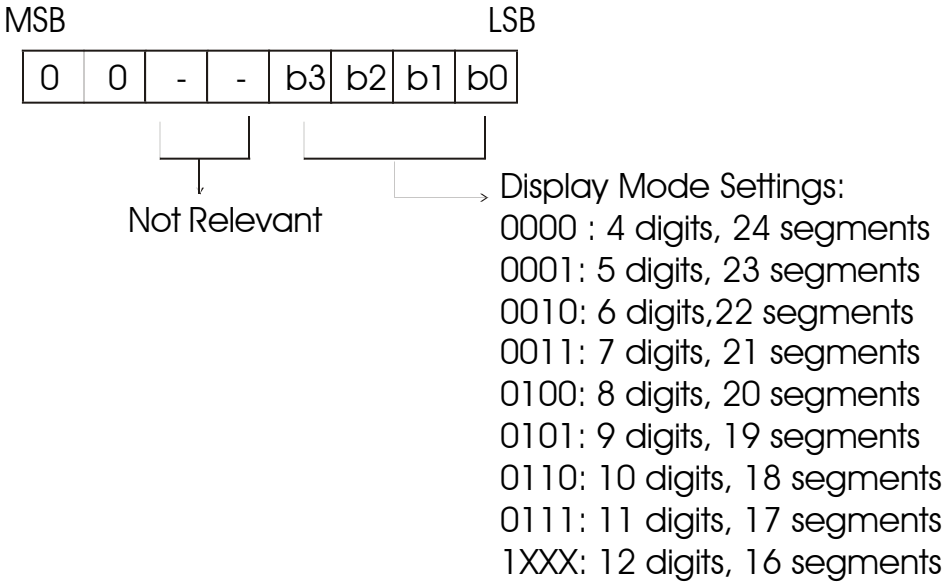


Figure 3: Display Mode Settings

Display Mode and RAM Address

Data transmitted from an external device to PT6315 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6315 are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	SG16	SG17	SG20	SG21	SG24	
00H L	00H U	01H L	01H U	02H L	02H U							DIG1
03H L	03H U	04H L	04H U	05H L	05H U							DIG2
06H L	06H U	07H L	07H U	08H L	08H U							DIG3
09H L	09H U	0AH L	0AH U	0BH L	0BH U							DIG4
0CH L	0CH U	0DH L	0DH U	0EH L	0EH U							DIG5
0FH L	0FH U	10H L	10H U	11H L	11H U							DIG6
12H L	12H U	13H L	13H U	14H L	14H U							DIG7
15H L	15H U	16H L	16H U	17H L	17H U							DIG8
18H L	18H U	19H L	19H U	1AH L	1AH U							DIG9
1BH L	1BH U	1CH L	1CH U	1DH L	1DH U							DIG10
1EH L	1EH U	1FH L	1FH U	20H L	20H U							DIG11
21H L	21H U	22H L	22H U	23H L	23H U							DIG12

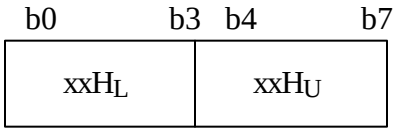


Figure 4: PT6315 RAM Address

COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6315. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of "0".

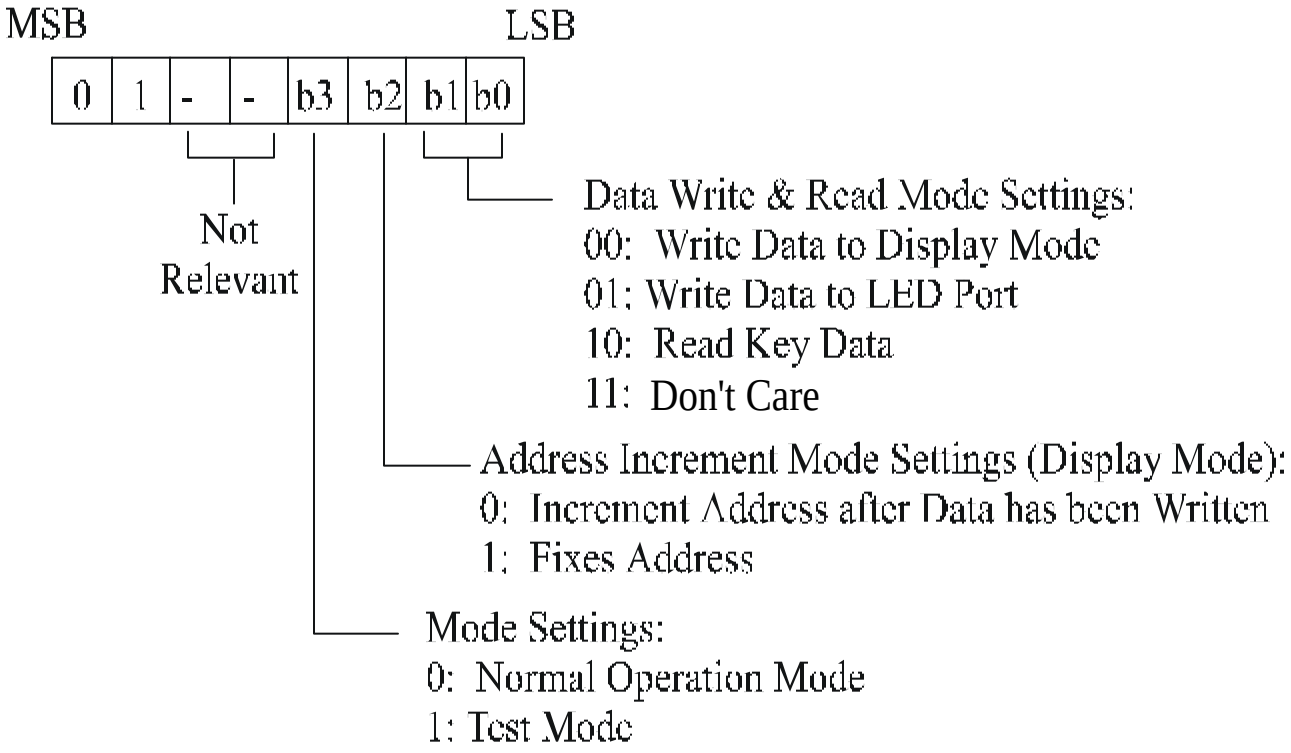


Figure 5: Data Settings

PT6315 Key Matrix & Key Input Data Storage RAM

PT6315 Key Matrix consists of 16 x 2 array as shown below:

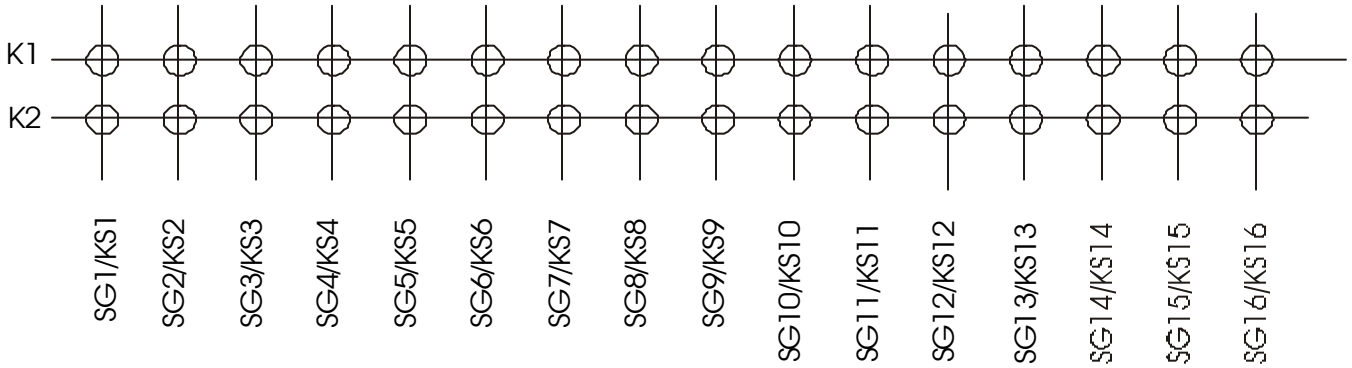


Figure 6: PT6315 Key Matrix

Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG1, b0) has been read, the least significant bit of the next data (SG16, b7) is read.

K1 ..... K2	K1 ..... K2	K1 ..... K2	K1 ..... K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	SG11/KS11	SG12/KS12
SG11/KS11	SG14/KS14	SG15/KS15	SG16/KS16
b0 .....b1	**b2 .....b3**	**b4 .....b5**	**b6.....b7**

READING SEQUENCE

Figure 7: PT6315 Key Input Data Storage

LED Display

PT6315 provides 4 LED Display Terminals, namely LED1 to LED4. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 4 LED display terminals, bits 5 to 8 (b4 ~ b7) are not used and therefore ignored. This means that b4 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

When a bit (b0 ~ b3) in the LED Port is "1", the corresponding LED is OFF. Conversely, when the bit is "0", the LED Display is turned ON. For example, Bit 1 (as designated by b0) has the value of "1", then this means that LED1 is OFF. **It must be noted that when power is turned ON, bit 1 to bit 4 (bo to b3) are given the value of "0" (all LEDs are turned ON)**. Please refer to the diagrams below.

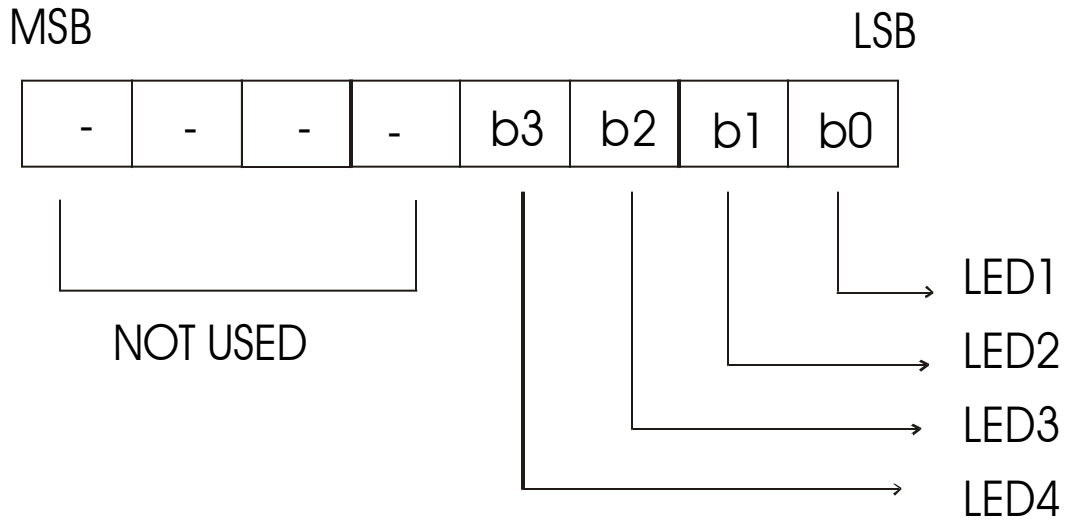


Figure 8: PT6315 LED Display Designation

COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "23H". If the address is set to 24H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".

Please refer to the diagram below.

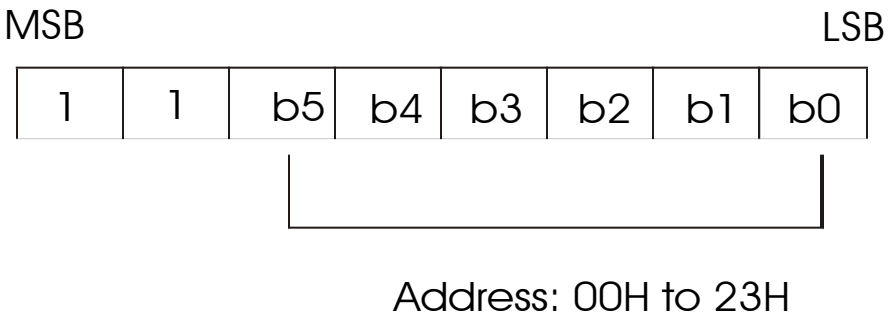


Figure 10: Address Settings

COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).

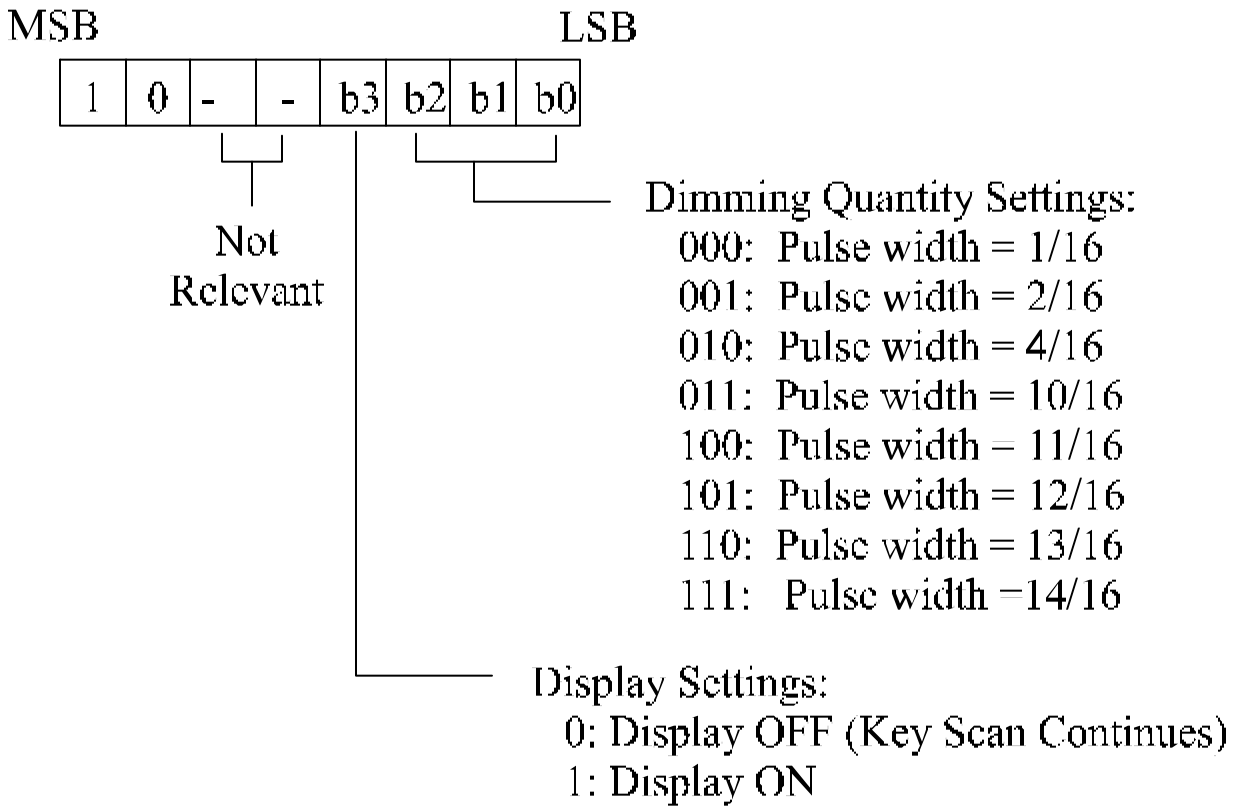


Figure 11: Display Control Settings

SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 16 x 2 matrix is stored in the RAM.
Internal Operating Frequency (fosc) = 224/T

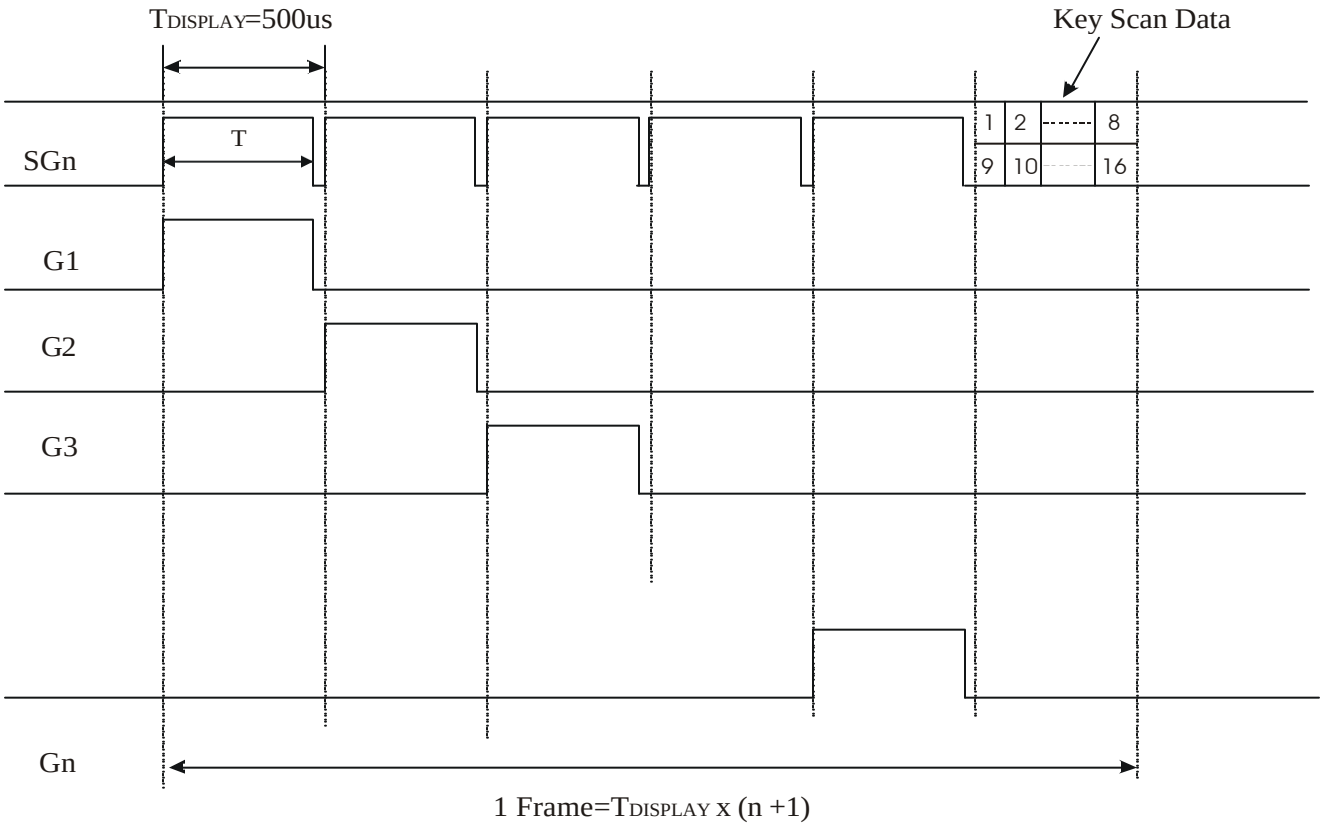


Figure 12: PT6315 Scanning & Display Timing Diagram

Note: T is the width of Segment only

SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6315 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KOhms to 10 KOhms) must be connected to DOUT.

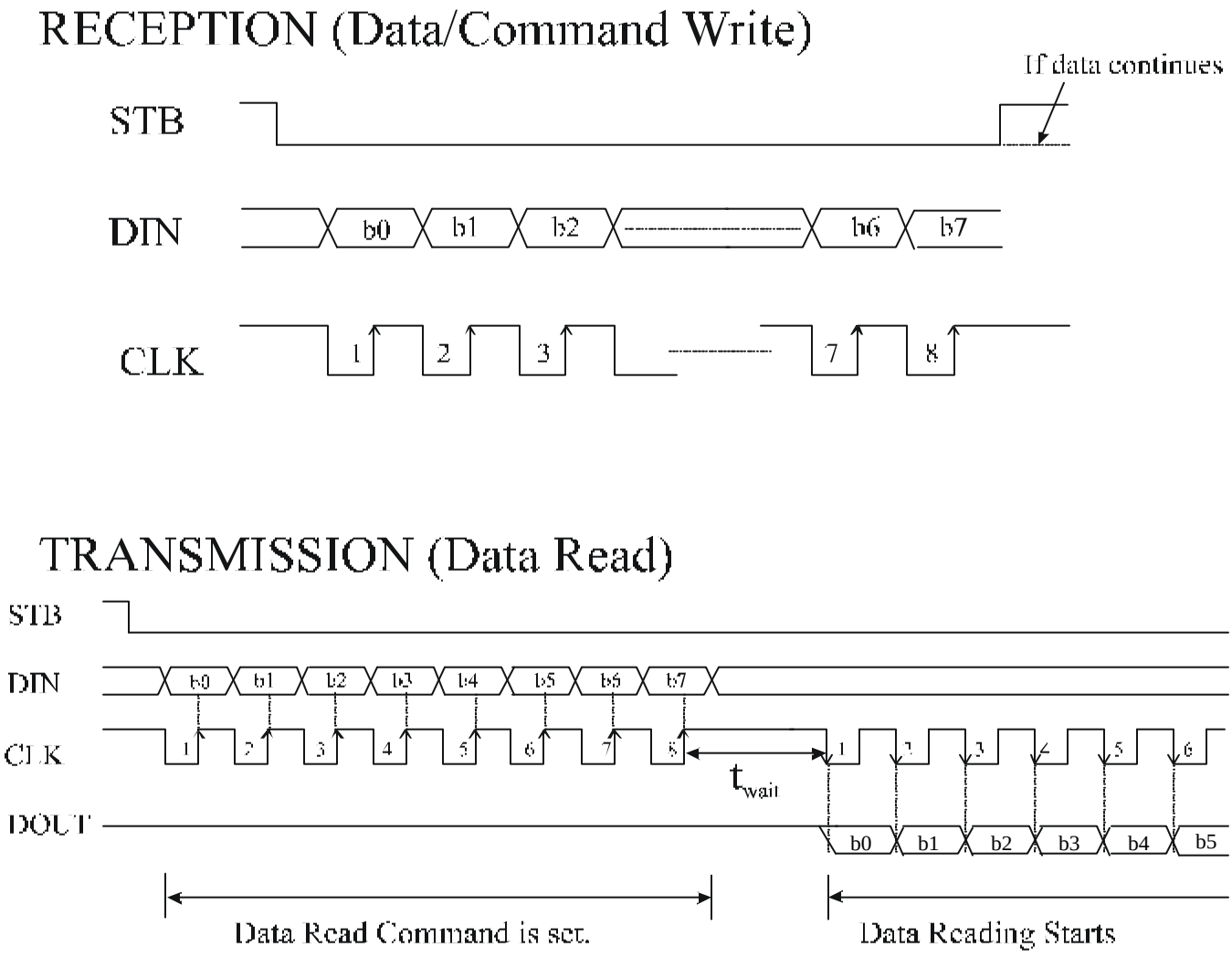


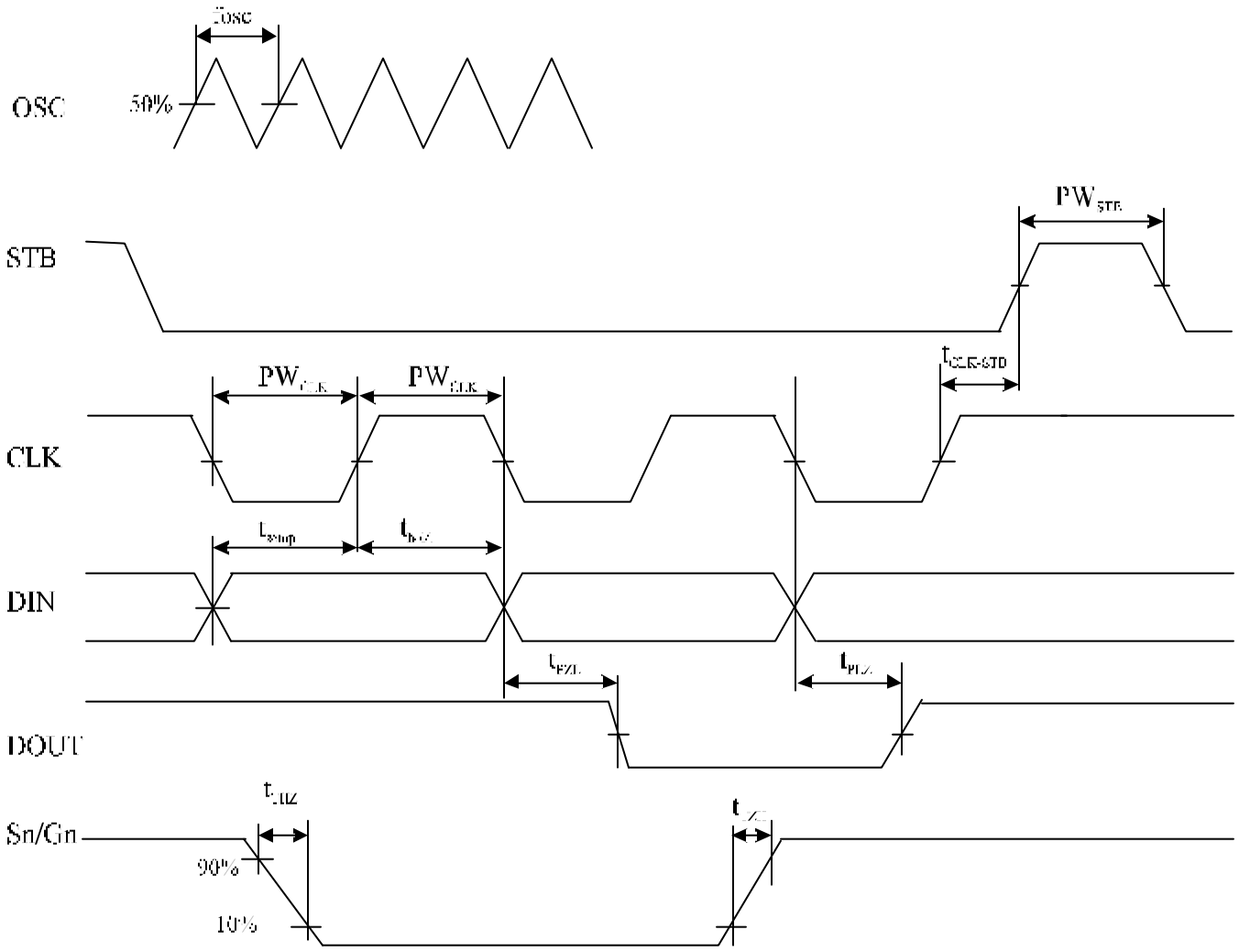
Figure 13: PT6315 Serial Communication Format

where: t_{wait} (waiting time) $\geq$ 1us

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1µs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6315 Switching Characteristics Waveform is given below.

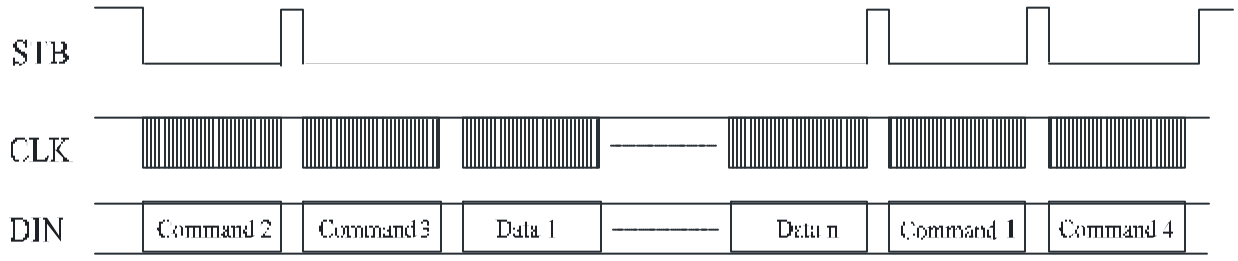


where: PW_{CLK} (Clock Pulse Width)≥400ns
t setup (Data Setup Time) ≥100ns
$t_{CLK-STB}$ (Clock - Strobe Time)≥1us
t_{TZH2} (Grid Rise Time)≤0.5us (at VDD=5V)
t_{TZH2} (Grid Rise Time)≤1.0us (at VDD=3.3V)
t_{TZH1} (Segment Rise Time)≤2.0us (at VDD=5V)
t_{TZH1} (Segment Rise Time)≤3.0us (at VDD=3.3V)
PW_{STB} (Strobe Pulse Width)≥1us
t_{hold} (Data Hold Time)≥100ns
t_{THZ} (Fall Time)≤150us
t_{PZL} (Propagation Delay Time)≤100ns
t_{PLZ} (Propagation Delay Time)≤400ns
fosc = Oscillation Frequency

Figure 14: PT6315 Switching Characteristic Waveform

APPLICATIONS

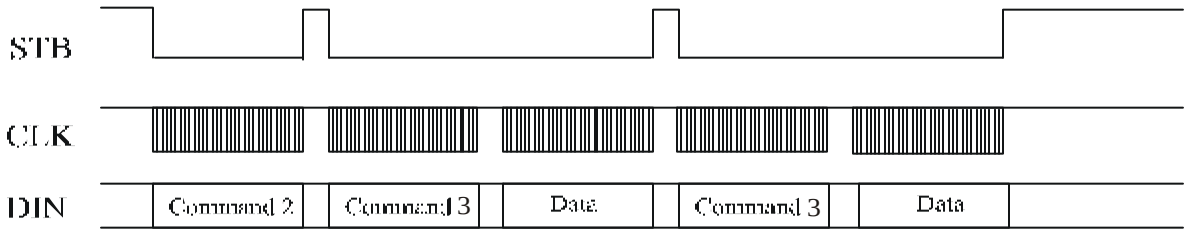
Display memory are updated by incrementing addresses. Please refer to the following diagram.



where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (36 Bytes max.)
Command 4: Display Control Command

Figure 15: Display Memory Updated by Address Increments

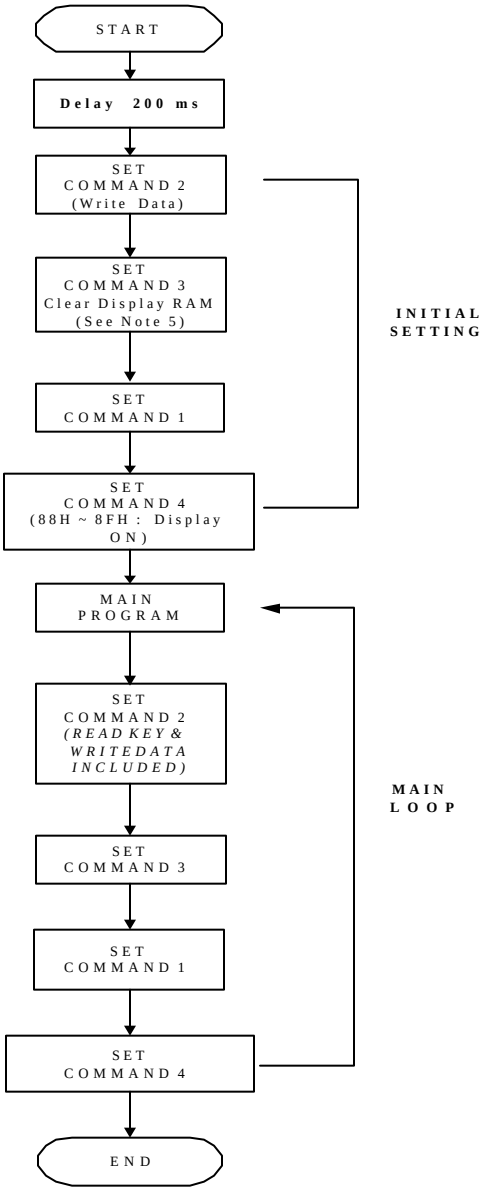
The following diagram shows the waveforms when updating specific addresses.



where: Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

Figure 16: Address Update

RECOMMENDED SOFTWARE FLOWCHART



Note: 1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3 : Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

Figure 17: Recommended Software Flowchart

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD}	-0.5 to +7	Volts
Driver Supply Voltage	V_{EE}	V_{DD}+0.5 to V_{DD}- 40	Volts
Logic Input Voltage	V_I	-0.5 to V_{DD}+0.5	Volts
VFD Driver Output Voltage	Vo	V_{EE}-0.5 to V_{DD}+0.5	Volts
LED Driver Output Current	I_{OLED}	±20	mA
VFD Driver Output Current	I_{OVFD}	-40 (Grid) -15 (Segment)	mA

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-20 to +70°C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	3.0	5	5.5	V
High-Level Input Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	-	$0.3V_{DD}$	V
Driver Supply Voltage	V_{EE}	V_{DD}-35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD}=5V, GND=0V, V_{EE}=V_{DD}-35 V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED=-12mA LED1 to LED4	V_{DD}-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED=+15mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	Vo=VDD-2V SG1/KS1 to SG16/KS16	-3	-	-	mA
High-Level Output Current	IOHGR	Vo=VDD-2V GR1 to GR8, SG17/GR12 to SG24/GR5	-15	-	-	mA
Oscillation Frequency	fosc	R=82 Kohms (see Note)	350	500	650	KHz
Schmitt-Trigger Transfer Voltage (+)	VT+	VDD=5V (DIN, CLK, STB)	2.7	3	3.3	V
Schmitt-Trigger Transfer Voltage (-)	VT-	VDD=5V (DIN, CLK, STB)	0.7	1.0	1.3	V
Hysteresis Voltage	Vhys	VDD=5V (DIN, CLK, STB)	1.4	2.0	-	V
Input Current	I_I	V_I = V_{DD} or V_{SS}	-	-	±1	uA
Dynamic Current Consumption	I_{DDdyn}	Under no load Display OFF	-	-	5	mA

Note: The frequency value is for PTC test condition. fosc=224/T

If you want to know details data, please see page 13.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD}=3.3V, GND=0V, V_{EE}=V_{DD}-35 V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOHLED	IOHLED=-6mA LED1 to LED4	V_{DD}-1	-	-	V
Low-Level Output Voltage	VOLLED	IOLLED=+15mA LED1 to LED4	-	-	1	V
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	Vo=VDD-2V SG1/KS1 to SG16/KS16	-1.5	-	-	mA
High-Level Output Current	IOHGR	Vo=VDD-2V GR1 to GR8, SG17/GR12 to SG24/GR5	-6	-	-	mA
Oscillation Frequency	fosc	R=100 Kohms (see Note)	350	500	650	KHz
Schmitt-Trigger Transfer Voltage (+)	VT+	VDD=3.3V (DIN, CLK, STB)	1.8	2.0	2.2	V
Schmitt-Trigger Transfer Voltage (-)	VT-	VDD=3.3V (DIN, CLK, STB)	0.2	0.4	0.6	V
Hysteresis Voltage	Vhys	VDD=3.3V (DIN, CLK, STB)	1.0	1.6	-	V
Input current	I_I	V_I = V_{DD} or V_{SS}	-	-	±1	uA
Dynamic Current Consumption	I_{DDdyn}	Under no load Display OFF	-	-	3	mA

Note: The frequency value is for PTC test condition. fosc=224/T

If you want to know details data, please see page 13.

APPLICATION CIRCUIT 1
44 PIN LQFP

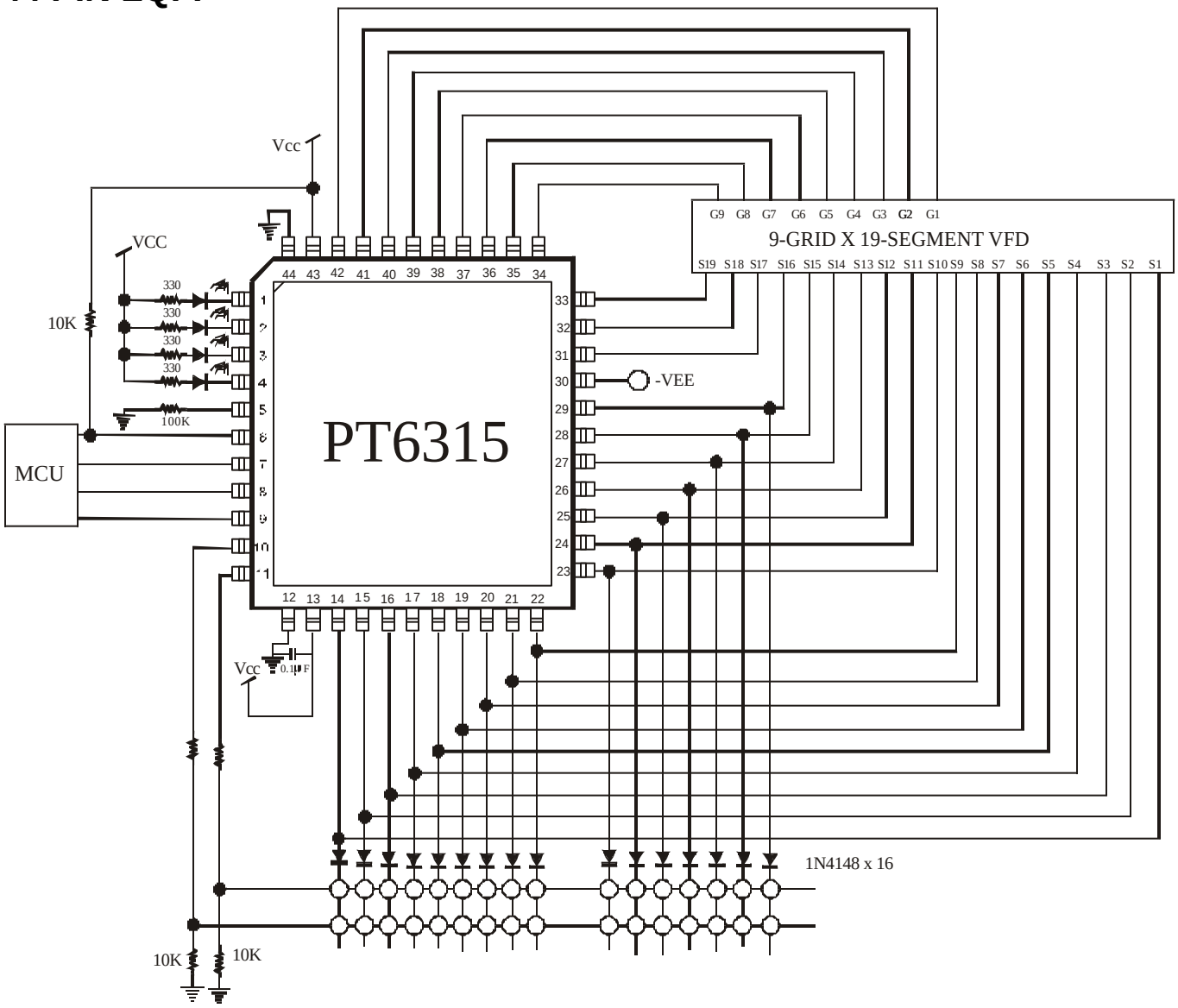


Figure 18: PT6315 LQFP Applicaiton Circuit

Note: The capacitor (0.1uF) connected between the GND and the VDD pins must be located as close as possible to the PT6315 chip.

APPLICATION CIRCUIT 2
44 PIN SSOP

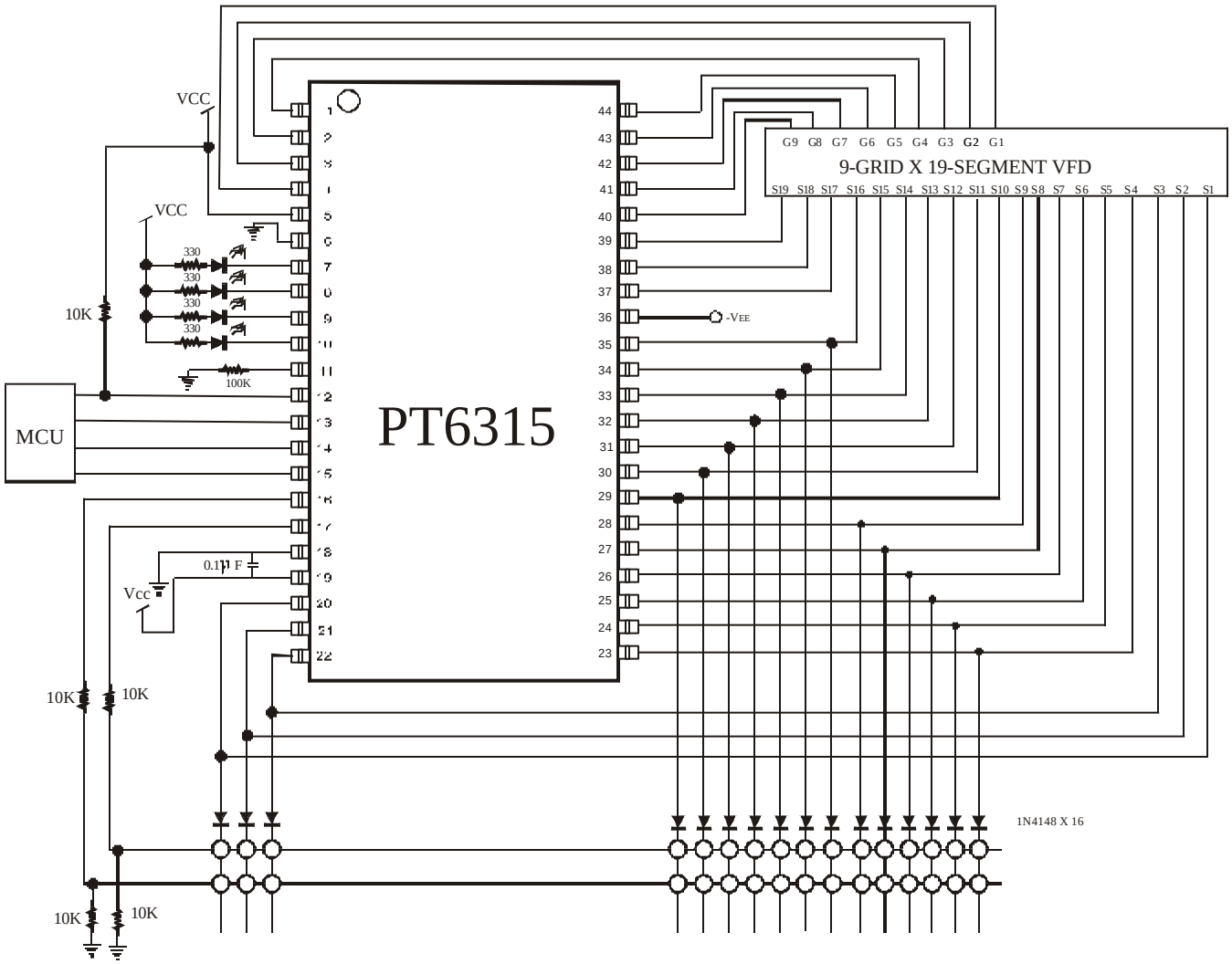


Figure 19: PT6315 SSOP Applicaiton Circuit

Note: The capacitor (0.1uF) connected between the GND and the VDD pins must be located as close as possible to the PT6315 chip.

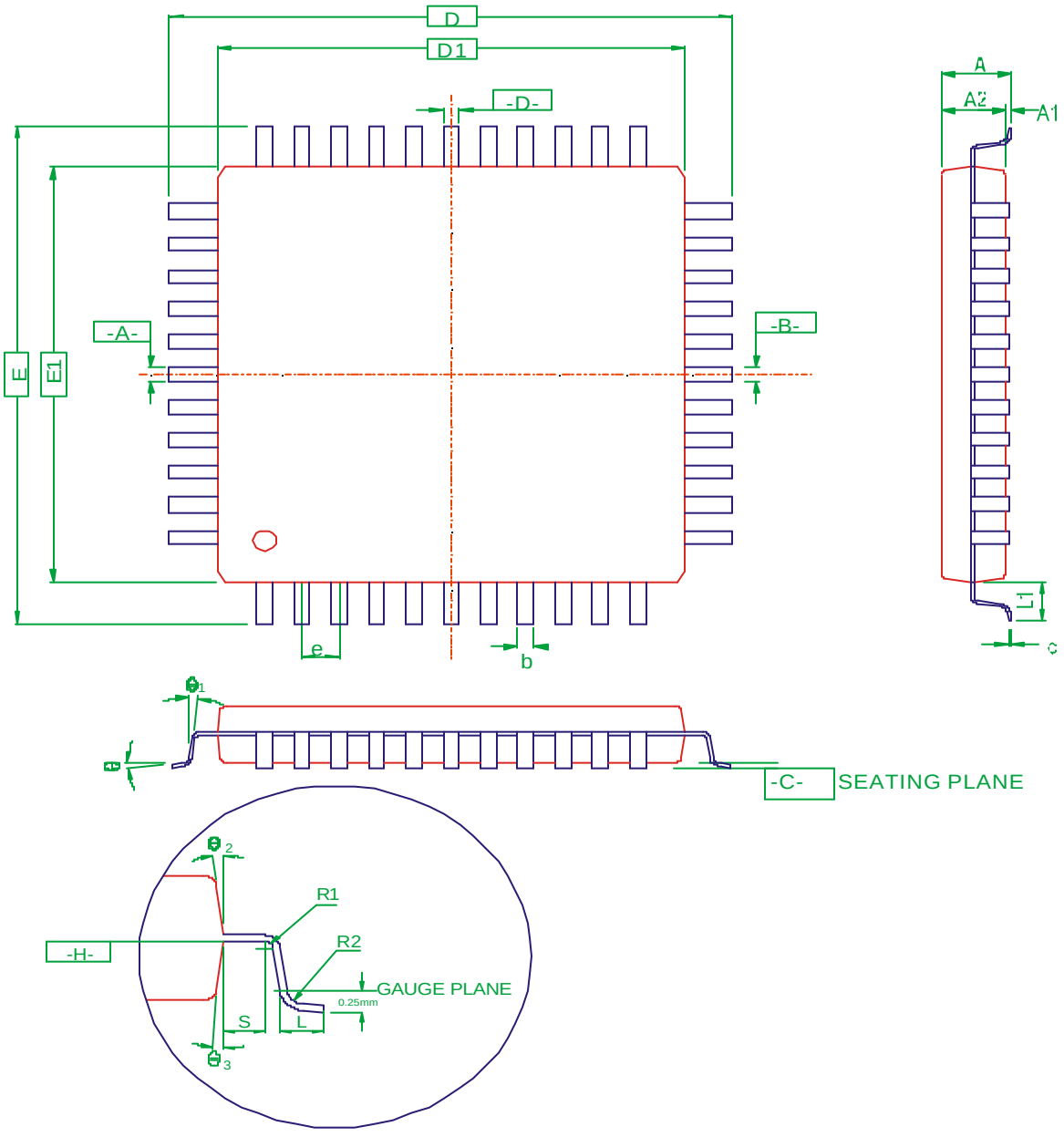
ORDER INFORMATION

Order Part Number	Package Type	Top Code
PT6315	44 pin LQFP Package	PT6315
PT6315-S	44 pin SOP Package	PT6315-S
PT6315 Ⓛ or "L"in circle	44 pin LQFP Package	PT6315
PT6315-S Ⓛ or "L"in circle	44 pin SOP Package	PT6315-S

Note: 1. Ⓛ = Lead Free
2. The Lead Free mark is put in front of the date code.

PACKAGE DIMENSION

44-Pin LQFP Package (Body Size: 10mm x 10mm; Pitch: 0.80mm; THK Body: 1.40mm)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
-	-		
D	12.00 BSC		
D1	10.00 BSC		
e	0.80 BSC		
E	12.00 BSC		
E1	10.00 BSC		
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
C	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

Notes:
1. Controlling Dimensions are in millimeters .
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. The top packge body size may be smaller than the bottom package size by as much as 0.15mm.
4. Datums A-B and D to be determined at datum plane H.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin1 identifier are optional but must be located within the zone indicated.
7. Dimension b does not include dambar protrusion. Alowable dambar protrusion shall not cause the lead to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Refer to JEDEC STD MS-026 Variation BCB

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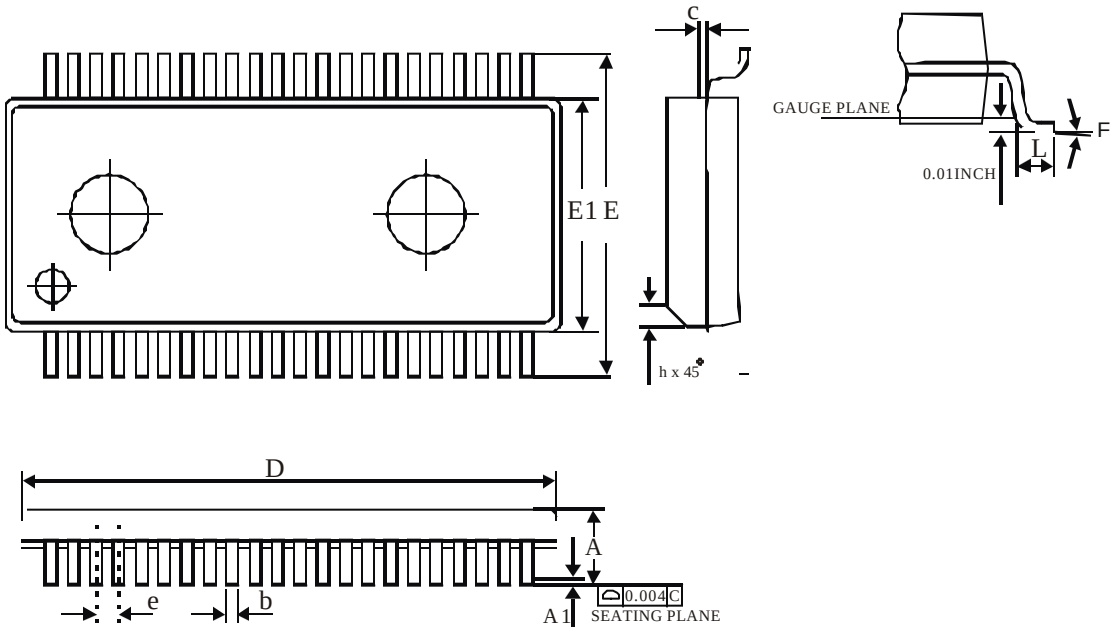
44-Pin SSOP Package



Symbol	Min	Typ	Max
A	0.095	0.102	0.110
A1	0.008	0.012	0.016
b	0.012		0.018
c	0.005		0.010
e		0.032 Basic	
E	0.395		0.420
E1	0.291	0.295	0.299
h	0.015		0.025
L	0.020		0.040
θ	0		8
D	0.720	0.725	0.730

Notes:
1. Dimension D do not include mold flash, protrusions or gate burrs.
2. Mold flash, protrusions or gate burrs shall not exceed 0.006 inch (0.152 mm) per side