1 PRODUCT OVERVIEW

S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Among the major CPU features are:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Idle and Stop power-down mode release by interrupt
— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of four CPU clocks) can be assigned to specific interrupt levels.

S3C8248/C8245/P8245/C8247/C8249/P8249 MICROCONTROLLER

The S3C8248/C8245/P8245/C8247/C8249/P8249 single-chip CMOS microcontroller are fabricated using the highly advanced CMOS process, based on Samsung's newest CPU architecture.

The S3C8248, S3C8245, S3C8247, S3C8249 are a microcontroller with a 8K-byte, 16K-byte, 24K-byte. 32K-byte mask-programmable ROM embedded respectively.

The S3P8245 is a microcontroller with a 16K-byte one-time-programmable ROM embedded.
The S3P8249 is a microcontroller with a 32K-byte one-time-programmable ROM embedded.

Using a proven modular design approach, Samsung engineers have successfully developed the S3C8248/C8245/P8245/C8247/C8249/P8249 by integrating the following peripheral modules with the powerful SAM8 core:

— Six programmable I/O ports, including five 8-bit ports and one 5-bit port, for a total of 45 pins.
— Eight bit-programmable pins for external interrupts.
— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
— Two 8-bit timer/counter and two 16-bit timer/counter with selectable operating modes.
— Watch timer for real time.
— 8-input A/D converter
— Serial I/O interface

The S3C8248/C8245/P8245/C8247/C8249/P8249 is versatile microcontroller for camera, LCD and ADC application, etc. They are currently available in 80-pin TQFP and 80-pin QFP package

OTP

The S3P8245/P8249 are OTP (One Time Programmable) version of the S3C8245/C8249 microcontroller. The S3P8245 microcontroller has an on-chip 16K-byte one-time-programmable EPROM instead of a masked ROM. The S3P8249 microcontroller has an on-chip 32K-byte one-time-programmable EPROM instead of a masked ROM. The S3P8245 is comparable to the S3P8245, both in function and in pin configuration.
The S3P8249 is comparable to the S3P8249, both in function and in pin configuration.

FEATURES

Memory

- ROM: 32K-byte (S3C8249/P8249)
- ROM: 16K-byte (S3C8245/P8245)
- RAM: 1056-Byte (S3C8249/P8249, S3C8247)
- RAM: 544-Byte (S3C8245/P8245, S3C8248)
- Data memory mapped I/O

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency 1-10 MHz (3 MHz at 1.8 V, 10 MHz at 2.7 V)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (1/1, 1/2, 1/8, 1/16)

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (System clock stops)

Interrupts

- 6 level 8 vector 8 internal interrupt
- 2 level 8 vector 8 external interrupt

Watch Timer

- Real-time and interval time measurement
- Clock generation for LCD
- Four frequency outputs for buzzer sound

LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- Display modes: static, 1/2 duty (1/2 bias)
- 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

A/D Converter

- Eight analog input channels
- 50 µs conversion speed at 1 MHz f_{ADC} clock
- 10-bit conversion resolution

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first/MSB-first transmission selectable
- Internal/external clock source

Voltage Booster

- LCD display voltage supply
- S/W control en/disable
- 3.0 V drive

45 I/O Pins

- 45 configurable I/O pins

Basic Timer

- Overflow signal makes a system reset.
- Watchdog function

8-Bit Timer/Counter A

- Programmable 8-bit timer
- Interval, capture, PWM mode
- Match/capture, overflow interrupt

8-Bit Timer/Counter B

- Programmable 8-bit timer
- Carrier frequency generator

16-Bit Timer/Counter 0

- Programmable 16-bit timer
- Match interrupt generates

16-Bit Timer/Counter 1

- Programmable 16-bit timer
- Interval, capture, PWM mode
- Match/capture, overflow interrupt

Voltage Detector

- Programmable detection voltage (2.2 V, 2.4 V, 3.0 V, 4.0 V)
- En/Disable S/W selectable

Instruction Execution Times

- 400 ns at 10 MHz (main)
- 122 us at 32.768 kHz (subsystem)

Operating Temperature Range

- -40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 80-pin QFP
- 80-pin TQFP

S3C8249's ROM version device

- S3C8247 (ROM 24K-byte)

S3C8245's ROM version device

- S3C8248 (ROM 8K-byte)

BLOCK DIAGRAM

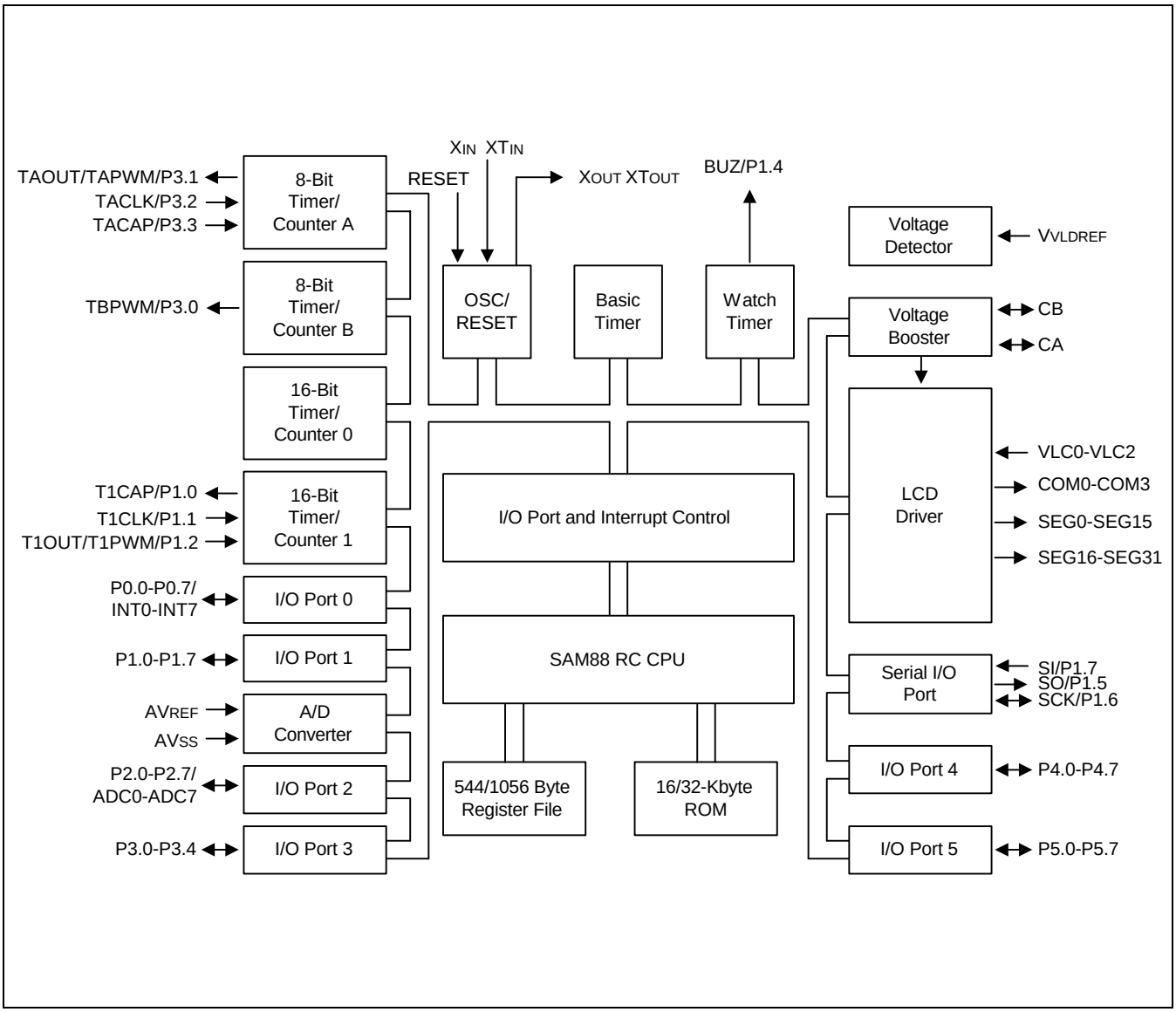


Figure 1-1. Block Diagram

PIN ASSIGNMENT

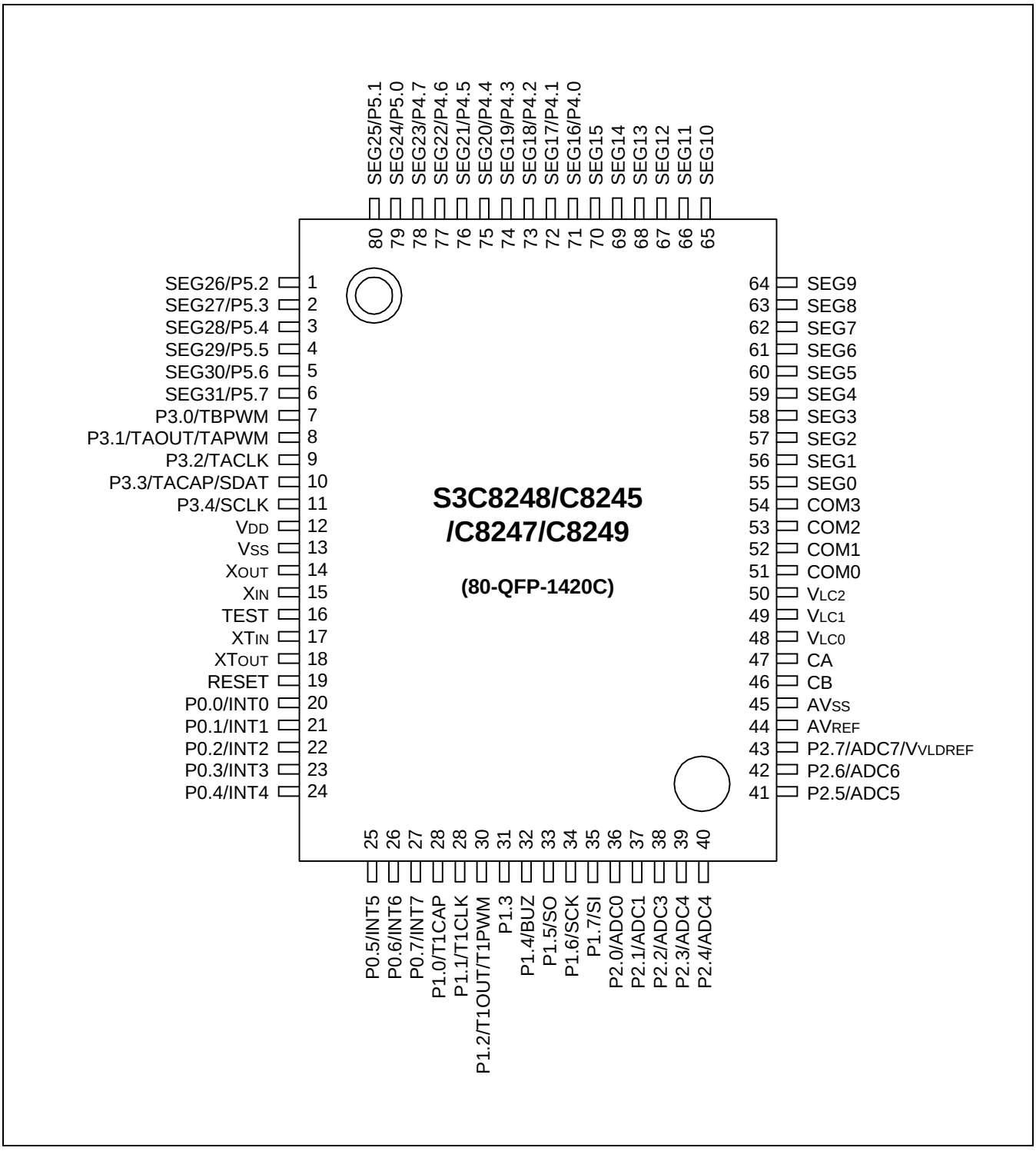


Figure 1-2. S3C8248/C8245/C8247/C8249 Pin Assignments (80-QFP)

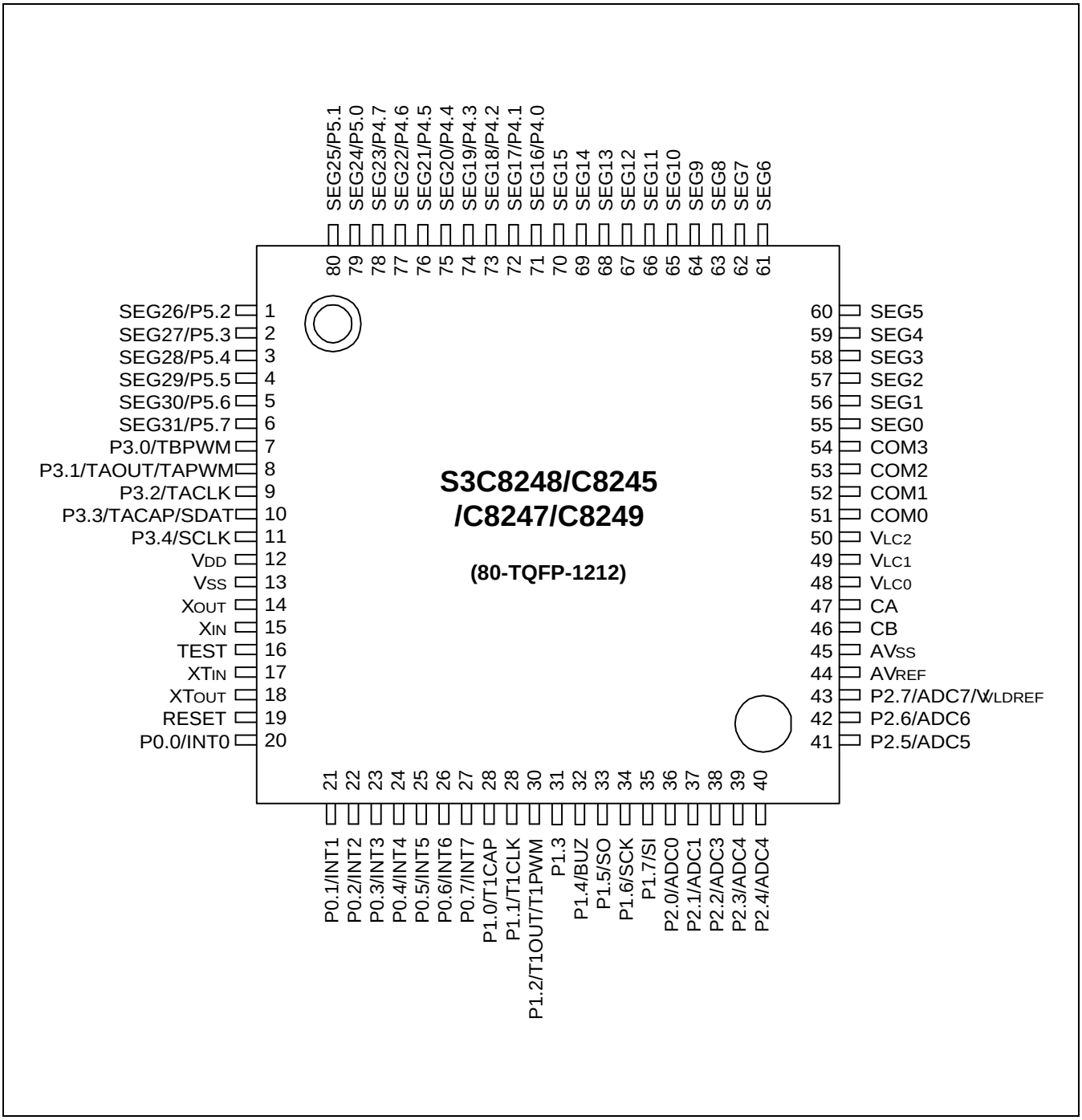


Figure 1-3. S3C8248/C8245/C8247/C8249 Pin Assignments (80-TQFP)

PIN DESCRIPTIONS

Table 1-1. S3C8248/C8245/C8247/C8249 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers (note)	Share Pins
P0.0–P0.7	I/O	I/O port with bit programmable pins; Schmitt trigger input or output mode selected by software; software assignable pull-up. P0.0–P0.7 can be used as inputs for external interrupts INT0–INT7 (with noise filter and interrupt control).	D–4	20–27	INT0–INT7
P1.0–1.7	I/O	I/O port with bit programmable pins; Input or output mode selected by software; Open-drain output mode can be selected by software; software assignable pull-up. Alternately P1.0–P1.7 can be used as SI, SO, SCK, BUZ, T1CAP, T1CLK, T1OUT, T1PWM	E–2	28-35	SI, SO, SCK, BUZ, T1CAP T1CLK T1OUT T1PWM
P2.0–P2.7	I/O	I/O port with bit programmable pins; normal input and AD input or output mode selected by software; software assignable pull-up.	F–10 F–18	36–42, 43	ADC0–ADC6 V_{VLDREF} (ADC7)
P3.0–P3.4	I/O	I/O port with bit programmable pins. Input or push-pull output with software assignable pull-up. Alternately P3.0–P3.3 can be used as TACAP, TACLK, TAOUT, TAPWM, TBPWM	D–2	7–11	TACAP TACLK TAOUT TAPWM TBPWM
P4.0–P4.7	I/O	I/O port with bit programmable pins. Push-pull or open drain output and input with software assignable pull-up. P4.0–P4.7 can alternately be used as outputs for LCD SEG	H–14	71–78	SEG16–SEG23
P5.0–P5.7	I/O	Have the same characteristic as port 4	H–14	79–6	SEG24–SEG31

Table 1-1. S3C8248/C8245/C8247/C8249 Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers (note)	Share Pins
ADC0–ADC6 ADC7	I	A/D converter analog input channels	F–10 F–18	36–42 43	P2.0–P2.6 P2.7
AV_{REF}	–	A/D converter reference voltage	–	44	–
AV_{SS}	–	A/D converter ground	–	45	–
INT0–INT7	I	External interrupt input pins	D–4	20–27	P0.0–P0.7
RESET	I	System reset pin (pull-up resistor: 250 kΩ)	B	19	–
TEST	I	0 V: Normal MCU operating 5 V: Test mode 12 V: for OTP writing	–	16	–
SDAT, SCLK	O	Serial OTP interface pins; serial data and clock	D–2	10, 11	P3.3, P3.4
V_{DD}, V_{SS}	–	Power input pins for CPU operation (internal) and Power input for OTP Writing	–	12, 13	–
X_{OUT}, X_{IN}	–	Main oscillator pins	–	14, 15	–
SCK, SO, SI	I/O	Serial I/O interface clock signal	E–2	33–35	P1.5–P1.7
V_{VLDREF}	I	Voltage detector reference voltage input	F–18	43	P2.7
TACAP	I	Timer A Capture input	D–2	10	P3.3
TACLK	I	Timer A External clock input	D–2	9	P3.2
TAOUT/TAPWM	O	Timer A output and PWM output	D–2	8	P3.1
TBPWM	O	Timer B PWM output	D–2	7	P3.0
T1CAP	I	Timer 1 Capture input	E–2	28	P1.0
T1CLK	I	Timer 1 External clock input	E–2	29	P1.1
T1OUT/T1PWM	O	Timer 1 output and PWM output	E–2	30	P1.2
COM0–COM3	O	LCD common signal output	H	51–54	–
SEG0–SEG15	O	LCD segment output	H	55–70	–
SEG16–SEG23	O	LCD segment output	H–14	71–78	P4.0–P4.7
SEG24–SEG31	O	LCD Segment output	H–14	79–6	P5.0–P5.7
V_{LC0}–V_{LC2}	O	LCD power supply	–	48–50	–
BUZ	O	0.5, 1, 2 or 4 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32768 Hz subsystem clock	E–2	32	P1.4
CA, CB	–	Capacitor terminal for voltage booster	–	46–47	–

PIN CIRCUITS

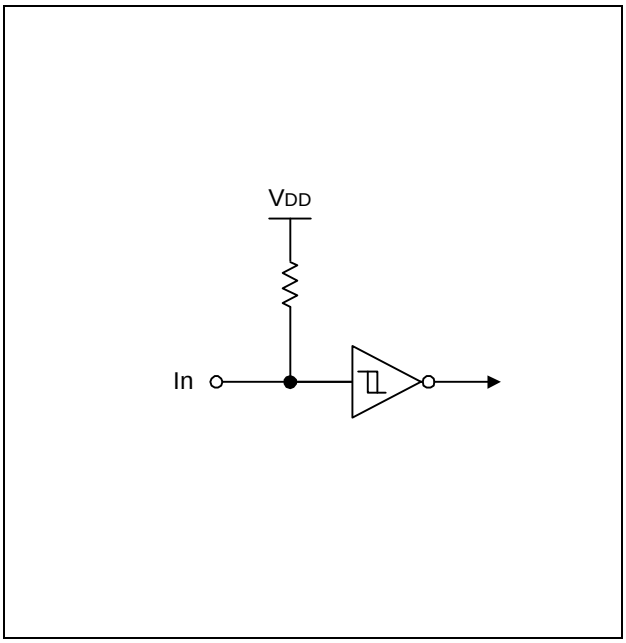


Figure 1-4. Pin Circuit Type B (RESET)

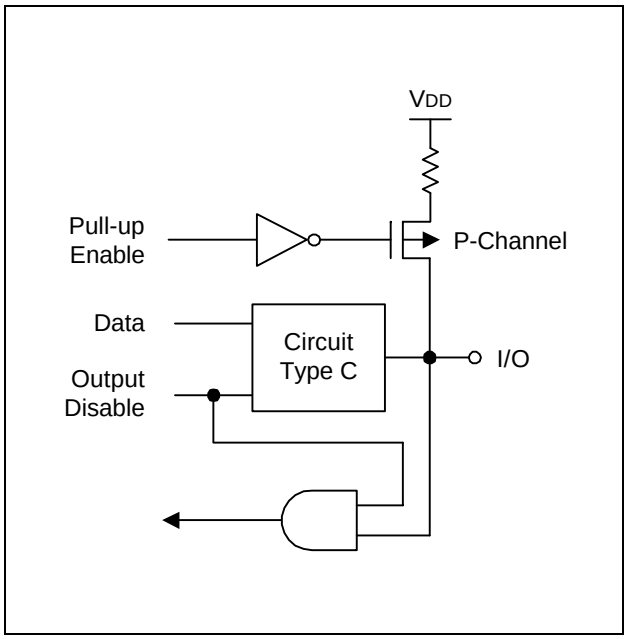


Figure 1-6. Pin Circuit Type D-2 (P3)

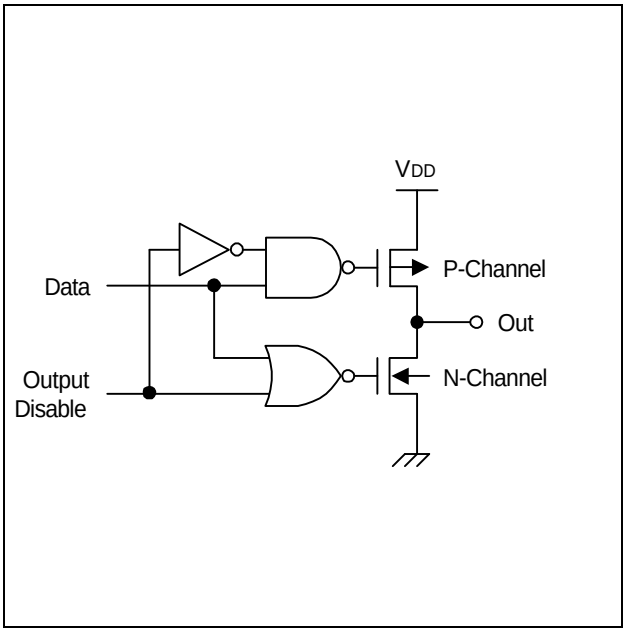


Figure 1-5. Pin Circuit Type C

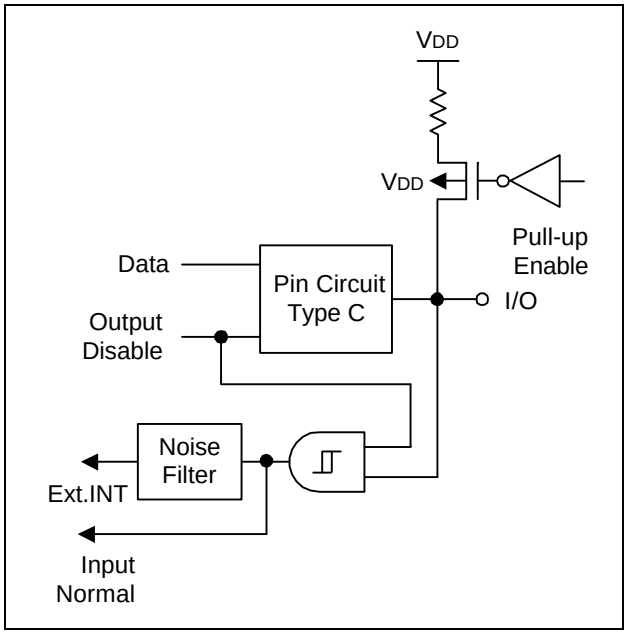


Figure 1-7. Pin Circuit Type D-4 (P0)

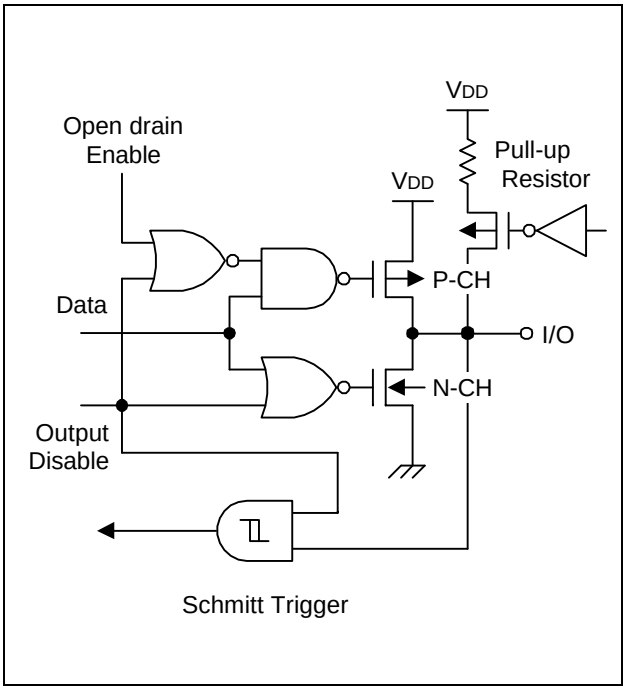


Figure 1-8. Pin Circuit Type E-2 (P1)

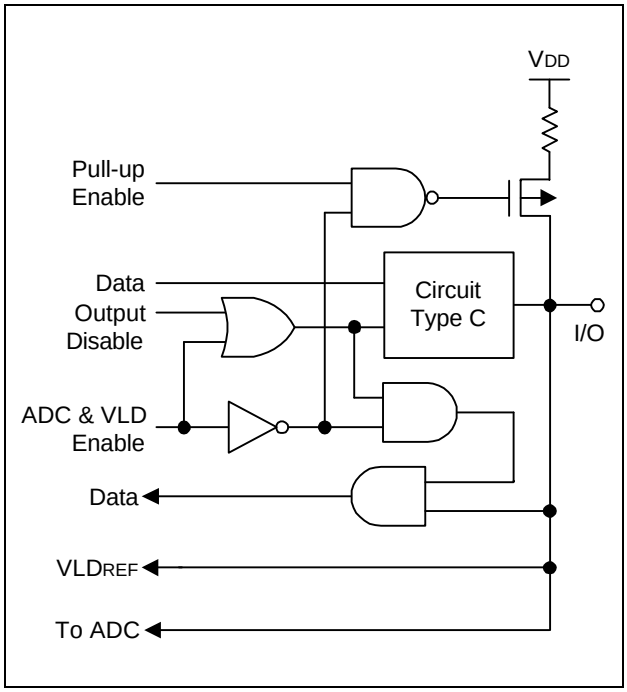


Figure 1-10. Pin Circuit Type F-18 (P2.7/VLD_{REF})

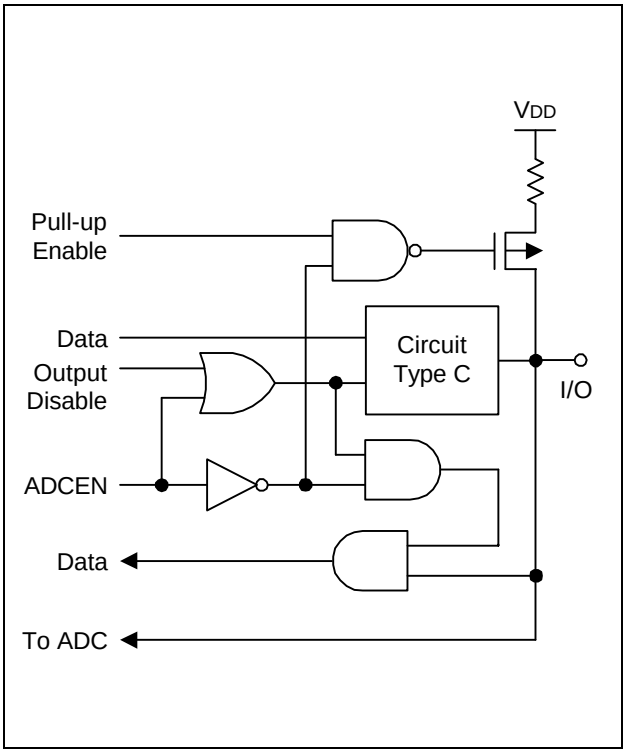


Figure 1-9. Pin Circuit Type F-10 (P2.0–P2.6)

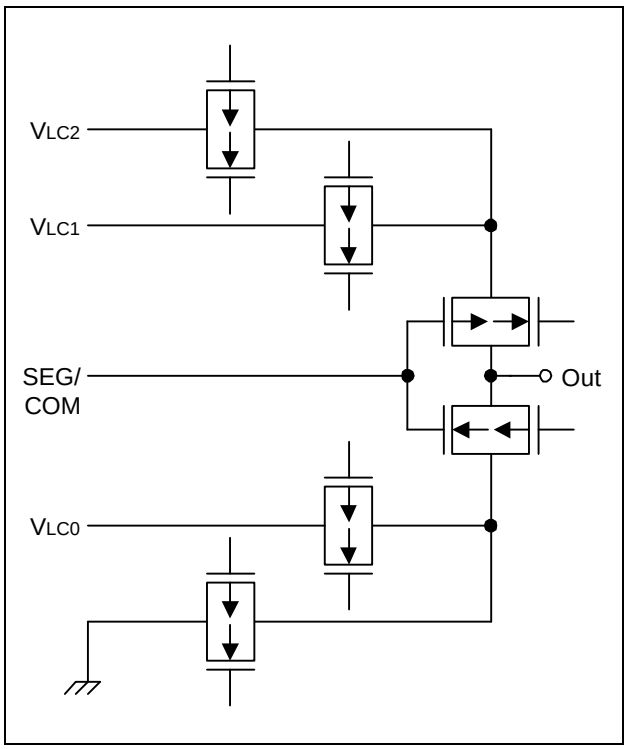


Figure 1-11. Pin Circuit Type H (SEG/COM)

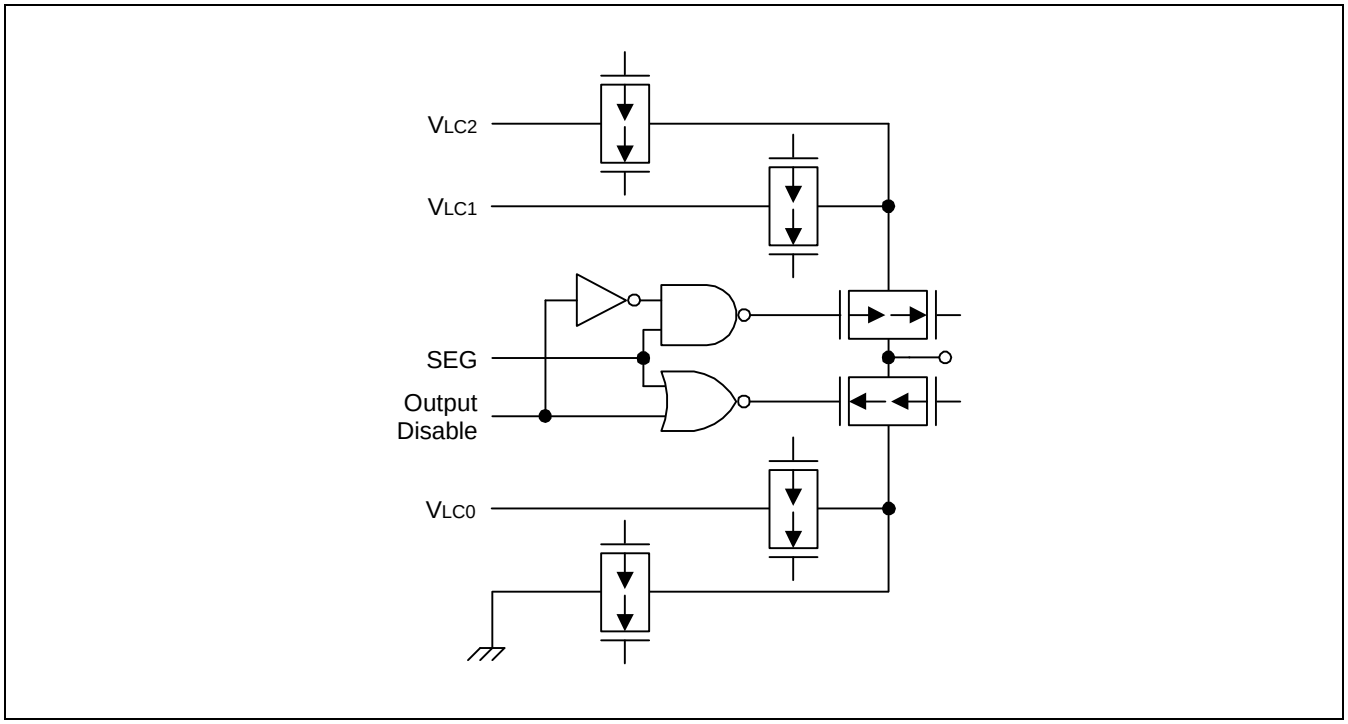


Figure 1-12. Pin Circuit Type H-4

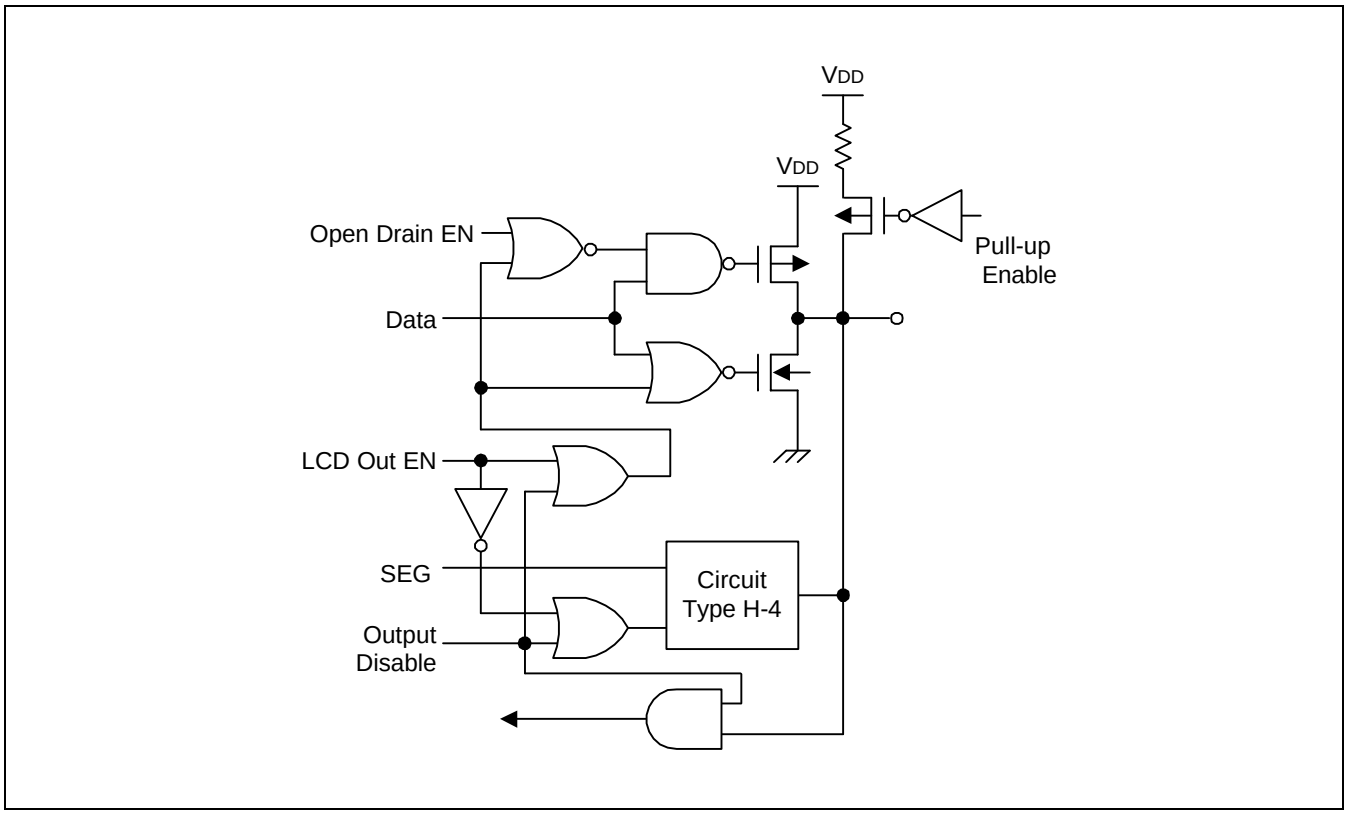


Figure 1-13. Pin Circuit Type H-14 (P4, P5)

19 ELECTRICAL DATA

OVERVIEW

In this chapter, S3C8248/C8245/C8247/C8249 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— Input/output capacitance
— D.C. electrical characteristics
— A.C. electrical characteristics
— Oscillation characteristics
— Oscillation stabilization time
— Data retention supply voltage in stop mode
— Serial I/O timing characteristics
— A/D converter electrical characteristics

Table 19-1. Absolute Maximum Ratings

(T_A= 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		– 0.3 to +6.5	V
Input voltage	V_I		– 0.3 to V_{DD} + 0.3	
Output voltage	V_O		– 0.3 to V_{DD} + 0.3	
Output current high	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current low	I_{OL}	One I/O pin active	+ 30	
		Total pin current for port	+ 100	
Operating temperature	T_A		– 40 to + 85	°C
Storage temperature	T_{STG}		– 65 to + 150	

Table 19-2. D.C. Electrical Characteristics

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	f_{CPU} = 10 MHz	2.7	–	5.5	V
		f_{CPU} = 3 MHz	1.8	–	5.5	
Input high voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	
	V_{IH2}	X_{IN}, XT_{IN}	V_{DD}-0.1	–		
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	
	V_{IL2}	X_{IN}, XT_{IN}			0.1	

Table 19-2. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH}	V_{DD} = 5 V; I_{OH} = -1 mA All output pins	V_{DD}–1.0	–	–	V
Output low voltage	V_{OL}	V_{DD} = 5 V; I_{OL} = 2 mA All output pins	–	–	0.4	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	3	uA
	I_{LIH2}	V_{IN} = V_{DD}, X_{IN}, XT_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except I_{LIL2}	–	–	-3	
	I_{LIL2}	V_{IN} = 0 V, X_{IN}, XT_{IN}, RESET			-20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	–	–	3	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and output pins	–	–	-3	
Oscillator feed back resistors	R_{osc1}	V_{DD} = 5.0 V T_A = 25 °C X_{IN} = V_{DD}, X_{OUT} = 0 V	800	1000	1200	kΩ
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ±10 % Port 0,1,2,3,4,5 T_A = 25°C	25	50	100	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ±10% T_A=25 °C, RESET only	110	210	310	
V_{LC0} out voltage (Booster run mode)	V_{LC0}	T_A = 25 °C, (1/3 bias mode)	0.9	1.0	1.1	V
		T_A = 25 °C, (1/2 bias mode)	1.4	1.5	1.7	
V_{LC1} out voltage (Booster run mode)	V_{LC1}	T_A = 25 °C (1/2 and 1/3 bias mode)	$2V_{LC0}$ - 0.1	–	$2V_{LC0}$ + 0.1	
V_{LC2} out voltage (Booster run mode)	V_{LC2}	T_A = 25 °C (1/3 bias mode)	$3V_{LC0}$ - 0.1	–	$3V_{LC0}$ + 0.1	
COM output voltage deviation	V_{DC}	V_{DD} = V_{LC2} = 3 V (V_{LCD}-COMi) IO = ± 15 µA (i = 0-3)	–	± 60	± 120	mV
SEG output voltage deviation	V_{Ds}	V_{DD} = V_{LC2} = 3 V (V_{LCD}-SEGi) IO = ± 15 µA (i = 0-31)	–	± 60	± 120	

Table 19-2. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10 % 10 MHz crystal oscillator	–	12	25	mA
		3 MHz crystal oscillator		4	10	
		V_{DD} = 3 V ± 10 % 10 MHz crystal oscillator		3	8	
		3 MHz crystal oscillator		1	5	
	I_{DD2}	Idle mode: V_{DD} = 5 V ± 10 % 10 MHz crystal oscillator	–	3	10	
		3 MHz crystal oscillator		1.5	4	
		Idle mode: V_{DD} = 3 V± 10 % 10 MHz crystal oscillator		1.2	3	
		3 MHz crystal oscillator		0.5	1.5	
	I_{DD3}	Sub operating: main-osc stop V_{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	–	20	40	uA
	I_{DD4}	Sub idle mode: main-osc stop V_{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	–	7	14	
	I_{DD5}	Main stop mode : sub-osc stop V_{DD} = 5 V ± 10 %	–	1	3	
		V_{DD} = 3 V ± 10 %		0.5	2	

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. I_{DD1} and I_{DD2} include a power consumption of subsystem oscillator.
3. I_{DD3} and I_{DD4} are the current when the main system clock oscillation stop and the subsystem clock is used. And does not include the LCD and Voltage booster and voltage level detector
4. I_{DD5} is the current when the main and subsystem clock oscillation stop.
5. Voltage booster's operating voltage range is 2.0 V to 5.5 V. The range of 1.8 V to 2.0 V could be referenced in page 17-4.

In case of S3C8248/C8245, the characteristic of V_{OH} and V_{OL} is differ with the characteristic of S3C8247/C8249 like as following. Other characteristics are same each other.

Table 19-3. D.C Electrical Characteristics of S3C8248/C8245

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH1}	V_{DD} = 5 V; I_{OH} = -1 mA All output pins except V_{OH2}	V_{DD}-1.0	–	–	V
	V_{OH2}	V_{DD} = 5 V; I_{OH} = -6 mA Port 3.0 only in S3C8248/C8245	V_{DD}-0.7			
Output low voltage	V_{OL1}	V_{DD} = 5 V; I_{OL} = 2 mA All output pins except V_{OL2}	–	–	0.4	
	V_{OL2}	V_{DD} = 5 V; I_{OH} = 12 mA Port 3.0 only in S3C8248/C8245			0.7	

Table 19-4. A.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width (P0.0–P0.7)	tINTH, tINTL	P0.0–P0.7, V_{DD} = 5 V	200	–		ns
RESET input low width	tRSL	V_{DD} = 5 V	1	–	–	us

NOTE: User must keep more large value then min value.

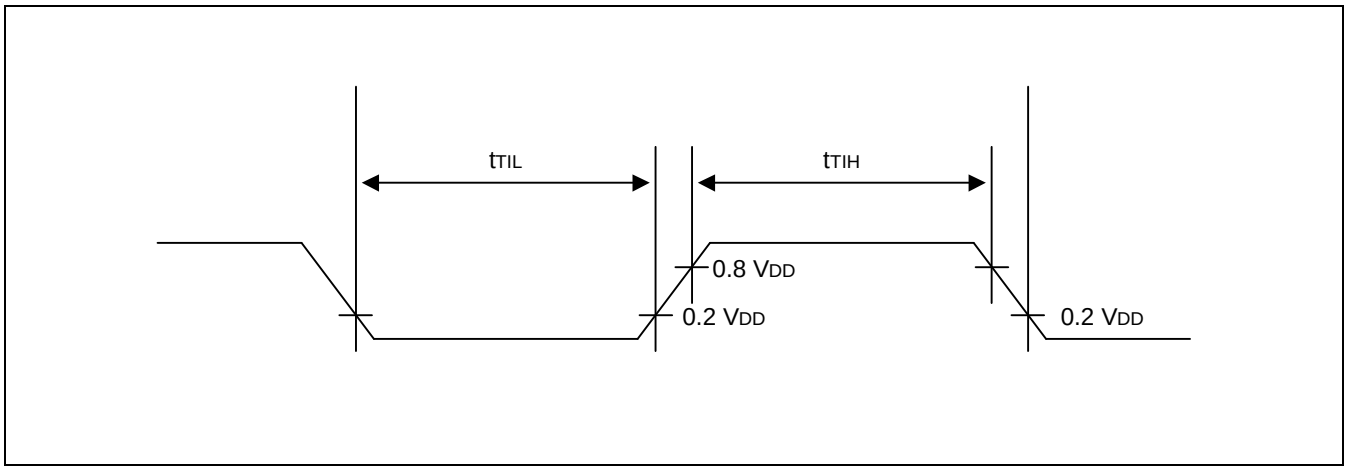


Figure 19-1. Input Timing for External Interrupts (Ports 0)

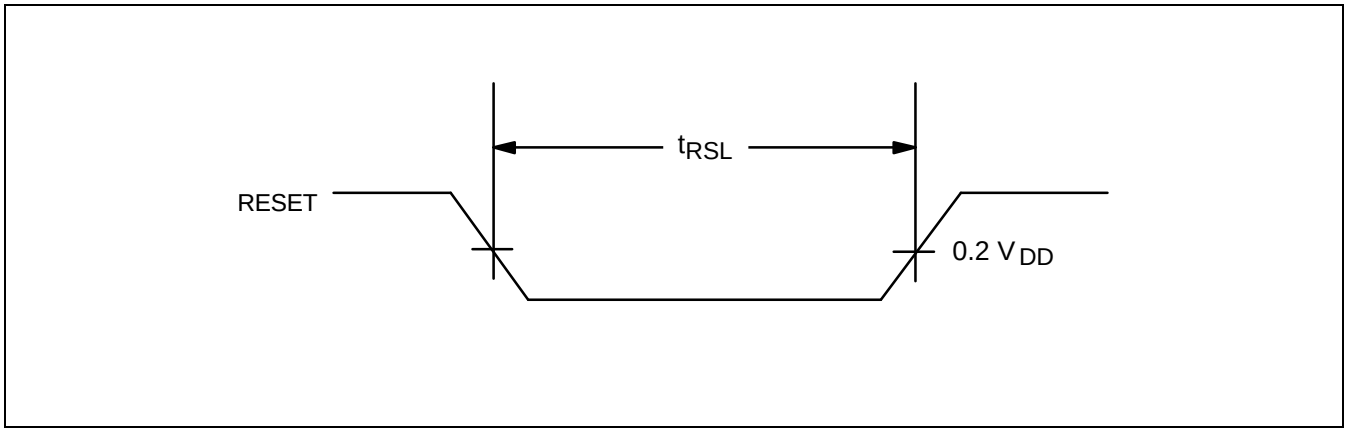


Figure 19-2. Input Timing for RESET

Table 19-5. Input/Output Capacitance

(T_A = -40 °C to +85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are returned to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 19-6. Data Retention Supply Voltage in Stop Mode

(T_A = -40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2 V	–	–	3	uA

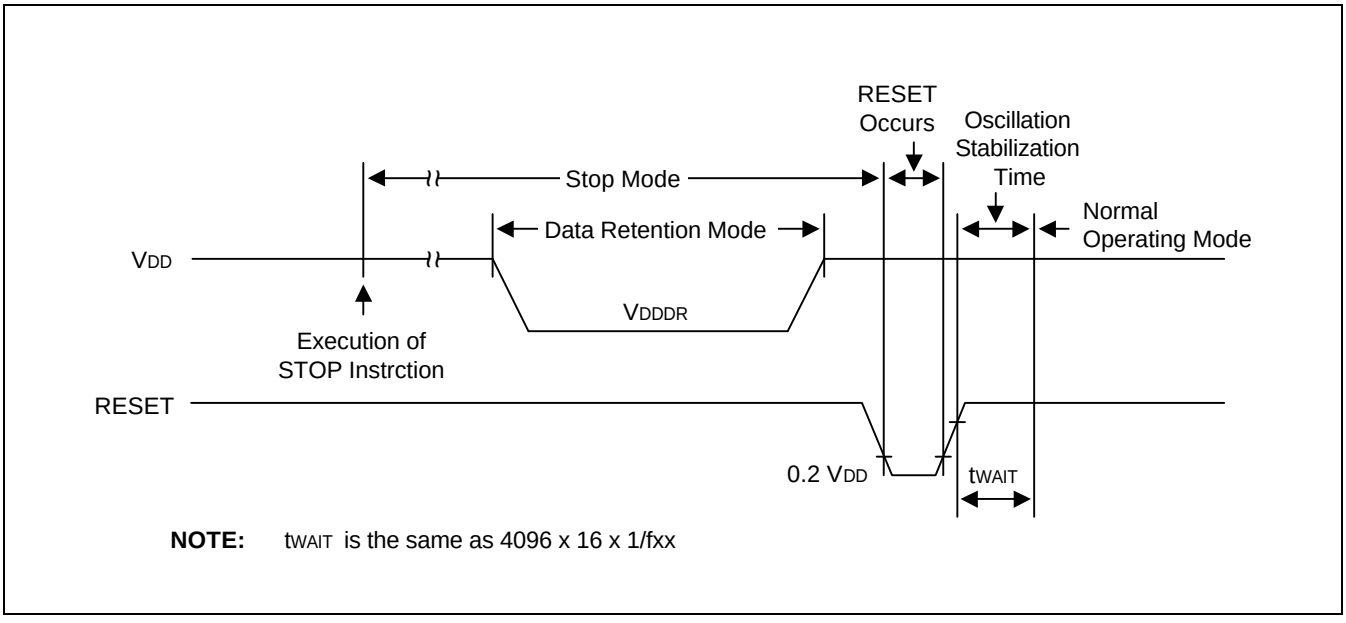
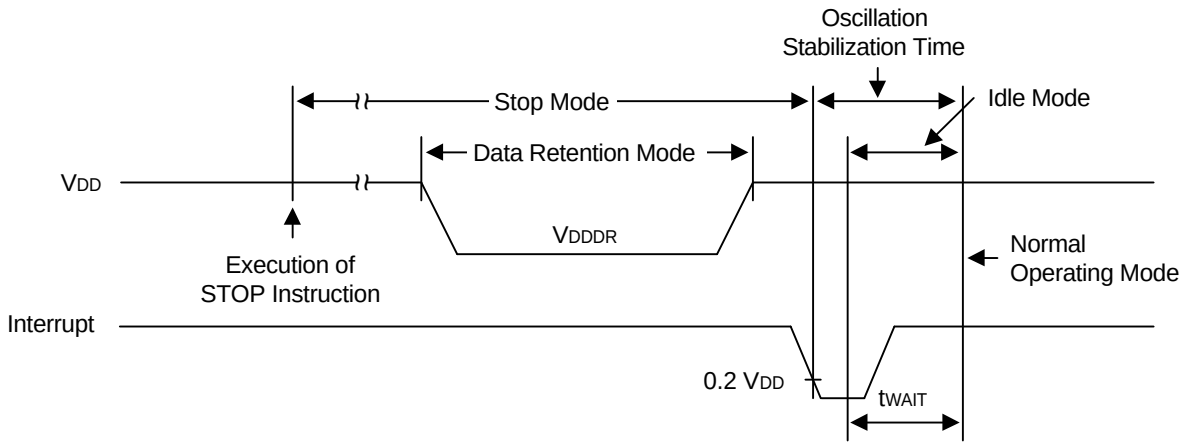
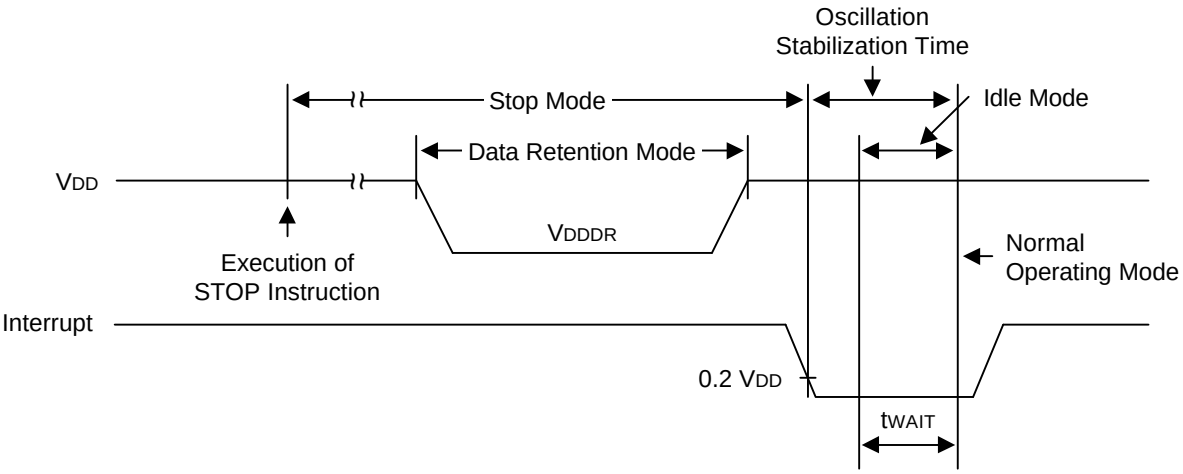


Figure 19-3. Stop Mode Release Timing Initiated by RESET



NOTE: tWAIT is the same as 4096 x 16 x BT clock

Figure 19-4. Stop Mode (Main) Release Timing Initiated by Interrupts



NOTE: When the case of select the fxx/128 for basic timer input clock before enter the stop mode.
tWAIT = 128 x 16 x (1/32768) = 62.5 ms

Figure 19-5. Stop Mode (Sub) Release Timing Initiated by Interrupts

Table 19-7. A/D Converter Electrical Characteristics

(T_A = - 40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	10	–	bit
Total accuracy		V_{DD} = 5 V AV_{REF} = 5 V AV_{SS} = 0 V	–	–	±3	LSB
Integral Linearity Error	ILE			–	±2	
Differential Linearity Error	DLE			–	±1	
Offset Error of Top	EOT			±1	±3	
Offset Error of Bottom	EOB			±0.5	±2	
Conversion time (1)	t_{CON}	–	–	40	–	fxx
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	1000	–	Mohm
Analog reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
Analog ground	AV_{SS}	–	V_{SS}	–	V_{SS} + 0.3	
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5 V	–	–	10	uA
Analog block current (2)	I_{ADC}	AV_{REF} = V_{DD} = 5 V	–	1	3	mA
		AV_{REF} = V_{DD} = 3 V		0.5	1.5	
		AV_{REF} = V_{DD} = 5 V When power down mode		100	500	nA

NOTES:
1. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is an operating current during A/D conversion.

Table 19-8. Synchronous SIO Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, fxx = 10 MHz oscillator)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK Cycle time	t_{CYC}	–	200	–	–	ns
Serial Clock High Width	t_{SCKH}	–	60	–	–	
Serial Clock Low Width	t_{SCKL}	–	60	–	–	
Serial Output data delay time	t_{OD}	–	–	–	50	
Serial Input data setup time	t_{ID}	–	40	–	–	
Serial Input data Hold time	t_{IH}	–	100	–	–	

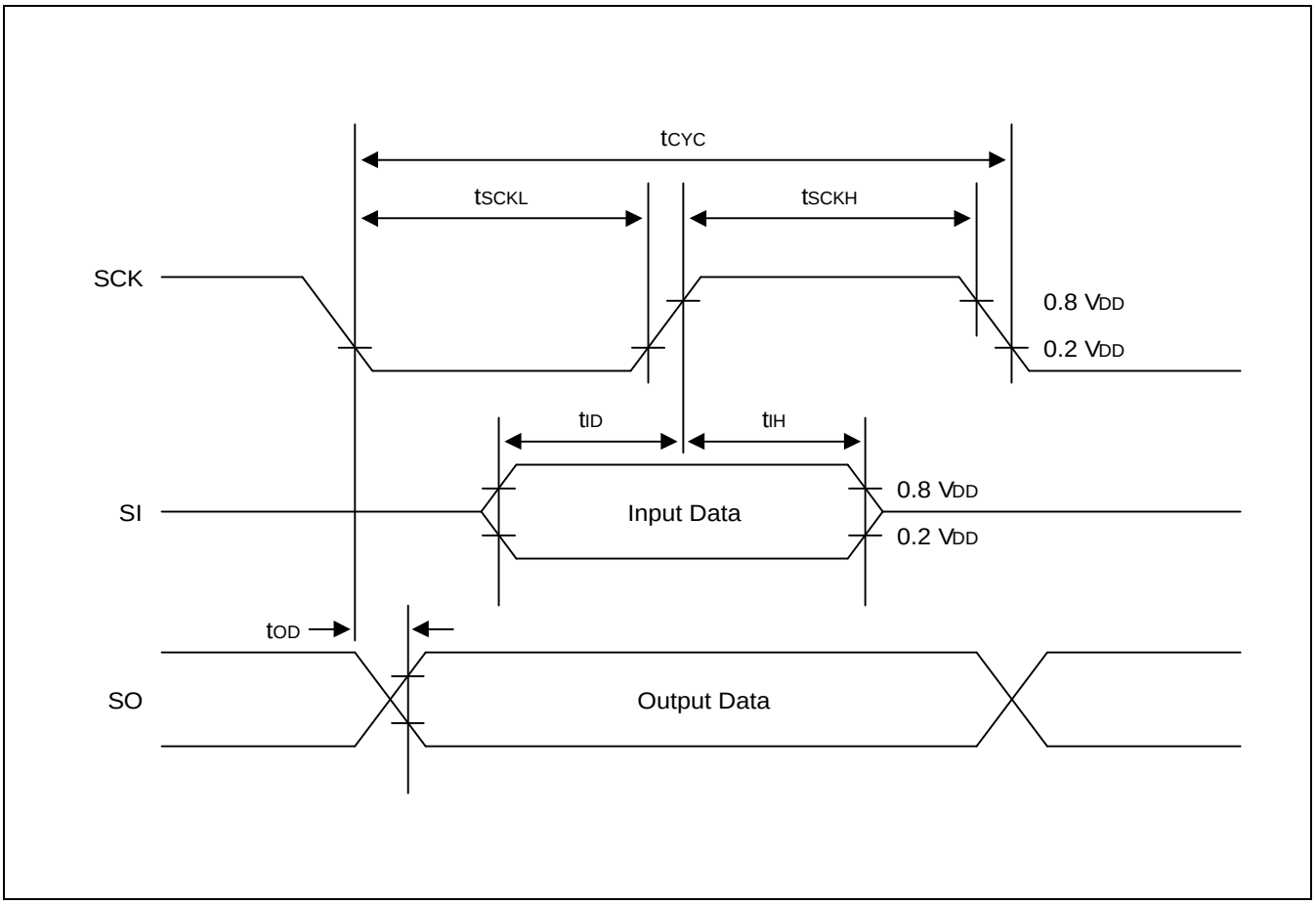


Figure 19-6. Serial Data Transfer Timing

Table 19-9. Main Oscillator Frequency (f_{OSC1})

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

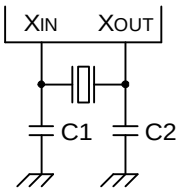
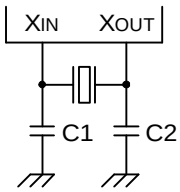
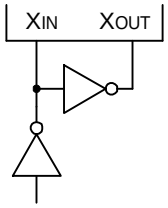
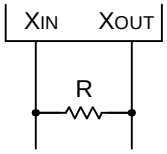
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		Crystal oscillation frequency	1	–	10	MHz
Ceramic		Ceramic oscillation frequency	1	–	10	MHz
External clock		X_{IN} input frequency	1	–	10	MHz
RC		r = 35 kΩ, V_{DD} = 5 V		2		MHz

Table 19-10. Main Oscillator Clock Stabilization Time (t_{ST1})

(T_A = -40 °C to +85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	50	–	–	ns

NOTE: Oscillation stabilization time (t_{ST1}) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is ended by a RESET signal. The RESET should therefore be held at low level until the t_{ST1} time has elapsed

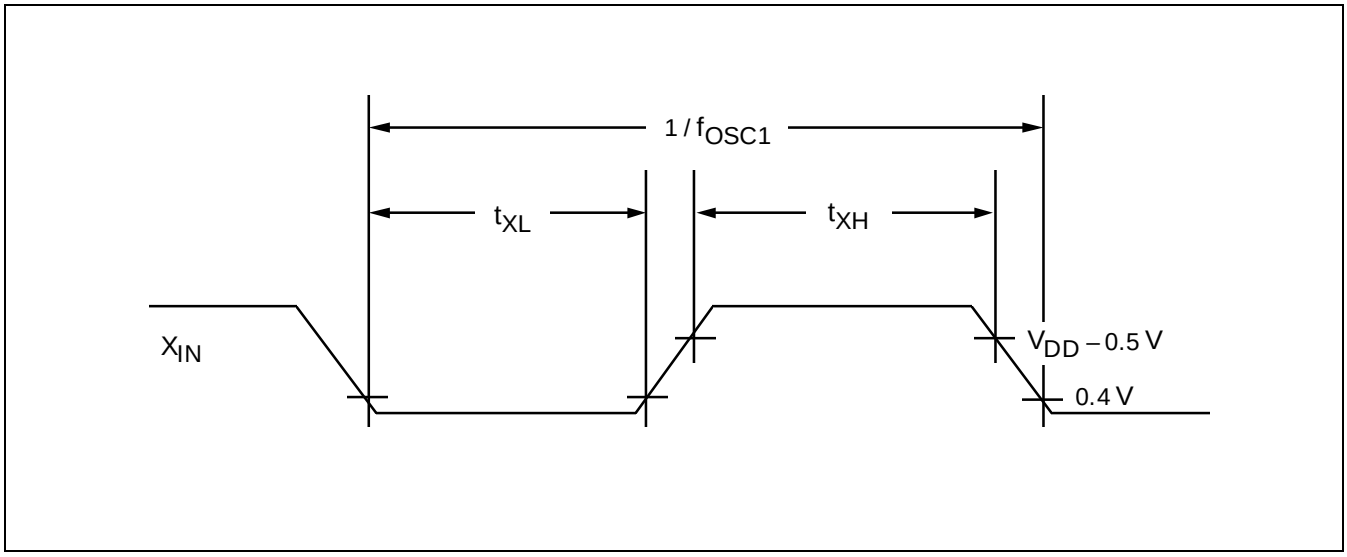


Figure 19-7. Clock Timing Measurement at X_{IN}

Table 19-11. Sub Oscillator Frequency (f_{OSC2})

(T_A = -40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

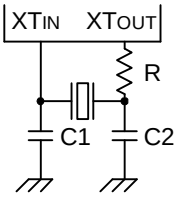
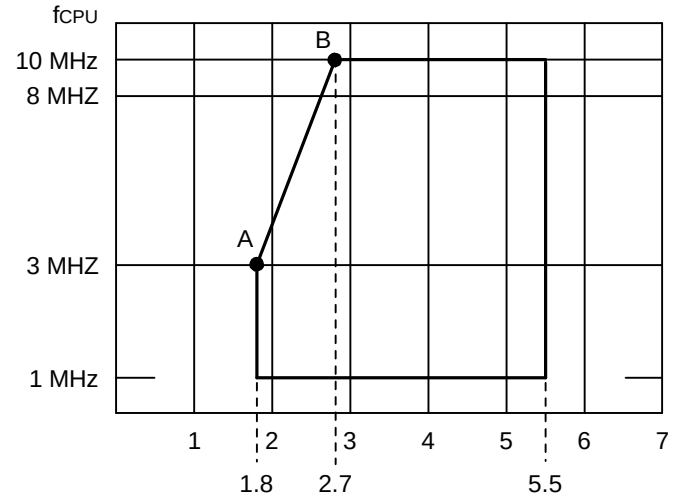
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		Crystal oscillation frequency C1 = 22 pF, C2 = 33 pF R = 39 KΩ XT_{IN} and XT_{OUT} are connected with R and C by soldering.	32	32.768	35	kHz

Table 19-12. Sub Oscillator(crystal) Stabilization Time (t_{ST2})

(T_A = 25 °C)

Oscillator	Test Condition	Min	Typ	Max	Unit
normal mode	V_{DD} = 4.5 V to 5.5 V	–	250	500	ms
	V_{DD} = 1.8 V to 3.0 V	–	–	2	s
strong mode	V_{DD} = 4.5 V to 5.5 V	–	–	2	s
	V_{DD} = 1.8 V to 3.0 V	–	250	500	ms

NOTE: Oscillation stabilization time (t_{ST2}) is the time required for the oscillator to it's normal oscillation when stop mode is released by interrupts. The value Typ and Max are measured by buzzer output signal after stop release.
For example in voltage range of 4.5 V to 5.5 V of normal mode, we can see the buzzer output signal within 400 ms at our test condition.



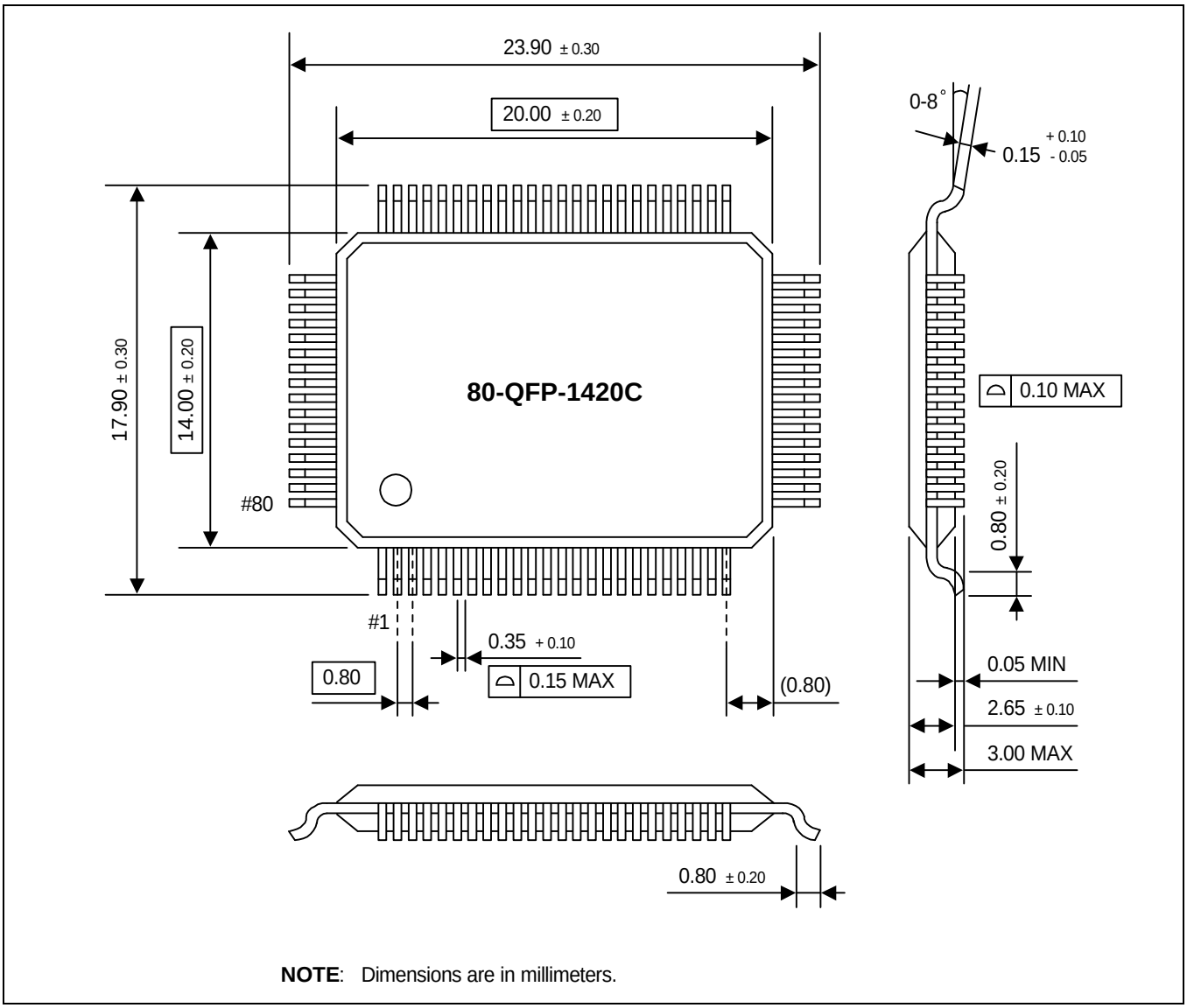
Minimum instruction clock = 1/4 x oscillator frequency

Figure 19-8. Operating Voltage Range

20 MECHANICAL DATA

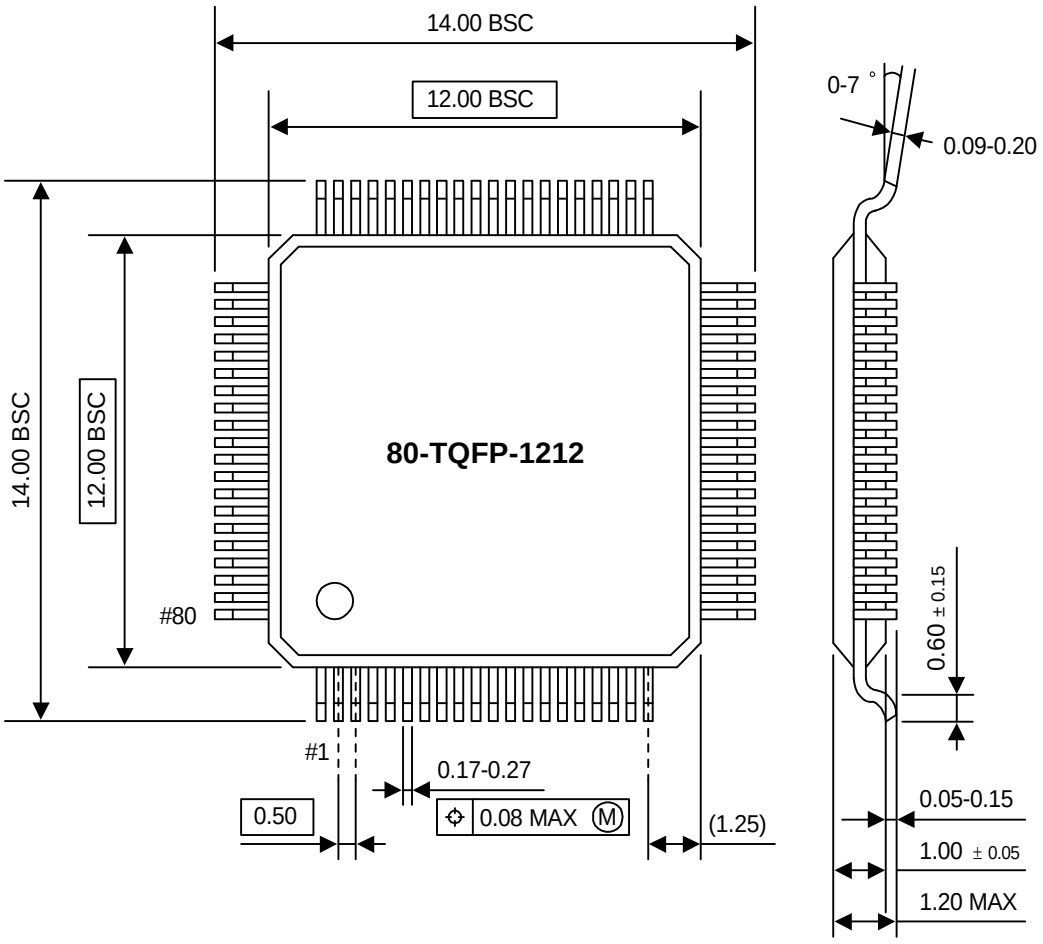
OVERVIEW

The S3C8248/C8245/C8247/C8249 microcontroller is currently available in 80-pin-QFP/TQFP package.



NOTE: Dimensions are in millimeters.

Figure 20-1. Package Dimensions (80-QFP-1420C)



NOTE: Dimensions are in millimeters.

Figure 20-2. Package Dimensions (80-TQFP-1212)

21 S3P8245/P8249 OTP

OVERVIEW

The S3P8245/P8249 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8248/C8245/C8247/C8249 microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P8245/P8249 is fully compatible with the S3C8248/C8245/C8247/C8249, both in function and in pin configuration. Because of its simple programming requirements, the S3P8245/P8249 is ideal as an evaluation chip for the S3C8248/C8245/C8247/C8249.

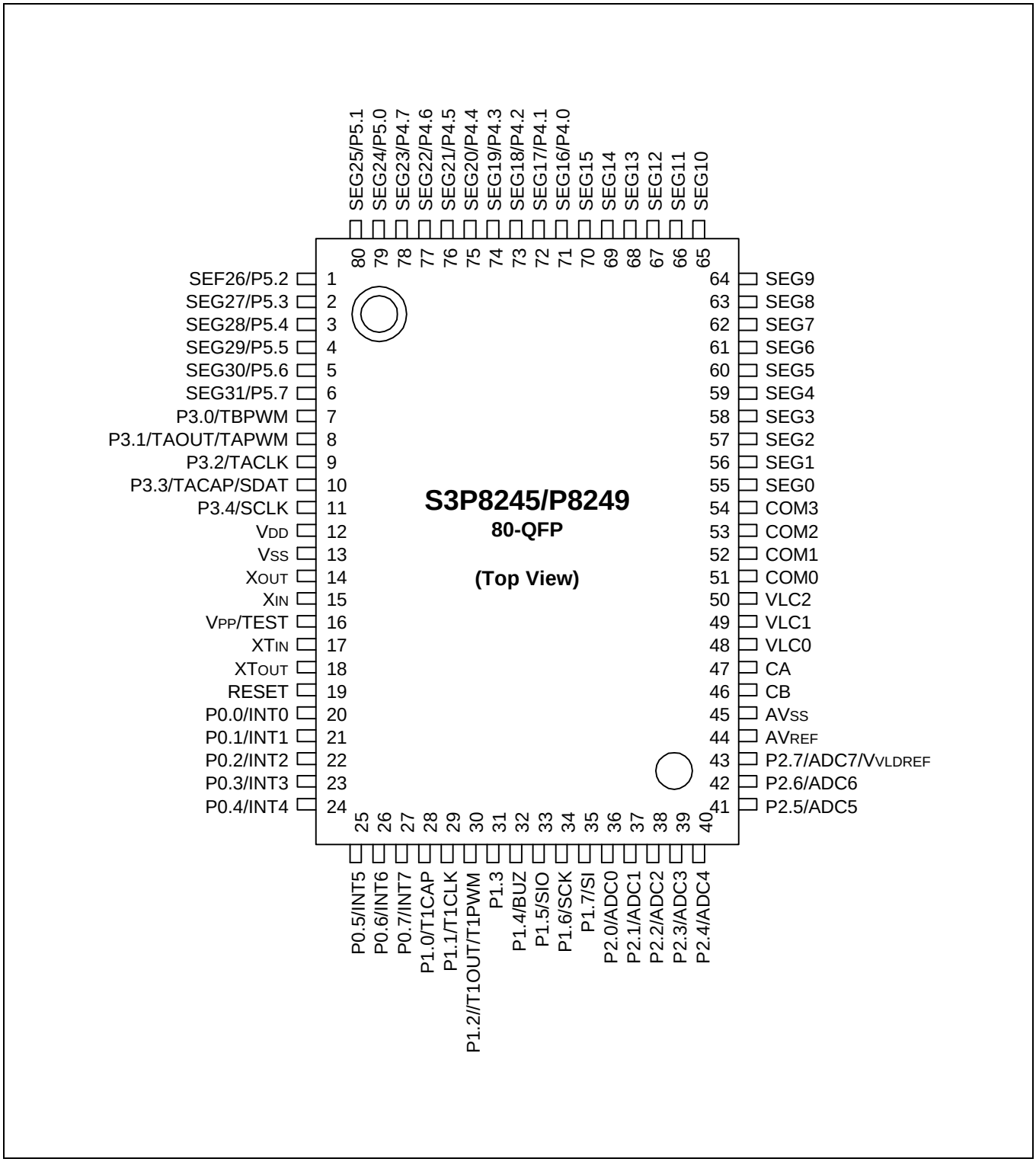


Figure 21-1. Pin Assignments (80-QFP)

Table 21-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P2.0	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P2.1	SCLK	11	I	Serial clock pin. Input only pin.
V_{PP}	TEST	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	19	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	12/13	–	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

Table 21-2. Comparison of S3P8245/P8249 and S3C8248/C8245/C8247/C8249 Features

Characteristic	S3P8245/P8249	S3C8248/C8245/C8247/C8249
Program Memory	16K/32K-byte EPROM	16K/32K-byte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	
Pin Configuration	80-QFP/80-TQFP	80-QFP/80-TQFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P8245/P8249, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 21-3 below.

Table 21-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/MEM	Address(A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 21-4. D.C Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	f_{CPU} = 10 MHz	2.7	–	5.5	V
		All input pins except $V_{IH2, 3}$	1.8	–	5.5	
Input high voltage	V_{IH1}	Port 4,5 $V_{LCD2} \geq V_{DD}$	0.8 V_{DD}	–	V_{DD}	
	V_{IH2}	X_{IN}, XT_{IN}	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	All input pins except V_{IL2}	V_{DD}- 0.1	–	V_{DD}	
Input low voltage	V_{IL1}	X_{IN}, XT_{IN}	–	–	0.2 V_{DD}	
	V_{IL2}	V_{DD} = 5 V; I_{OH} = -1 mA All output pins			0.1	
Output high voltage	V_{OH}	V_{DD} = 5 V; I_{OL} = 2 mA All output pins	V_{DD} -1.0	–	–	
Output low voltage	V_{OL}		–	–	0.4	

Table 21-4. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	3	uA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, XT_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except I_{LIL2}	–	–	-3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, XT_{IN}, RESET			-20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and Output pins	–	–	3	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and Output pins	–	–	-3	
Oscillator feed back resistors	R_{osc1}	V_{DD} = 5.0 V T_A = 25 °C X_{IN} = V_{DD}, X_{OUT} = 0 V	800	1000	1200	kΩ
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ±10 % Port 0,1,2,3,4,5 T_A = 25°C	25	50	100	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ±10% T_A=25 °C, RESET only	110	210	310	
V_{LC0} out voltage (Booster run mode)	V_{LC0}	T_A = 25 °C (1/3 bias mode)	0.9	1.0	1.1	V
		T_A = 25 °C (1/2 bias mode)	1.4	1.5	1.7	
V_{LC1} out voltage (Booster run mode)	V_{LC1}	T_A = 25 °C	$2V_{LC0}$ - 0.1	–	$2V_{LC0}$ + 0.1	
V_{LC2} out voltage (Booster run mode)	V_{LC2}	T_A = 25 °C	$3V_{LC0}$ - 0.1	–	$3V_{LC0}$ + 0.1	
COM output voltage deviation	V_{DC}	V_{DD} = V_{LC2} = 3 V (V_{LC}-COMi) IO = ± 15 µA (1 = 0–3)	–	± 60	± 120	mV
SEG output voltage deviation	V_{Ds}	V_{DD} = V_{LC2} = 3 V (V_{LC}-COMi) IO = ± 15 µA (1 = 0–3)	–	± 60	± 120	

Table 21-4. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10 % 10 MHz crystal oscillator	–	12	25	mA
		3 MHz crystal oscillator		4	10	
		V_{DD} = 3 V ± 10 % 10 MHz crystal oscillator		3	8	
		3 MHz crystal oscillator		1	5	
	I_{DD2}	Idle mode: V_{DD} = 5 V ± 10 % 10 MHz crystal oscillator		3	10	
		3 MHz crystal oscillator		1.5	4	
		Idle mode: V_{DD} = 3 V± 10 % 10 MHz crystal oscillator		1.2	3	
		3 MHz crystal oscillator		0.5	1.5	
	I_{DD3}	Sub operating: main-osc stop V_{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	–	20	40	uA
	I_{DD4}	Sub idle mode: main-osc stop V_{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	–	7	14	
	I_{DD5}	Main stop mode : sub-osc stop V_{DD} = 5 V ± 10 %	–	1	3	
		V_{DD} = 3 V ± 10 %		0.5	2	

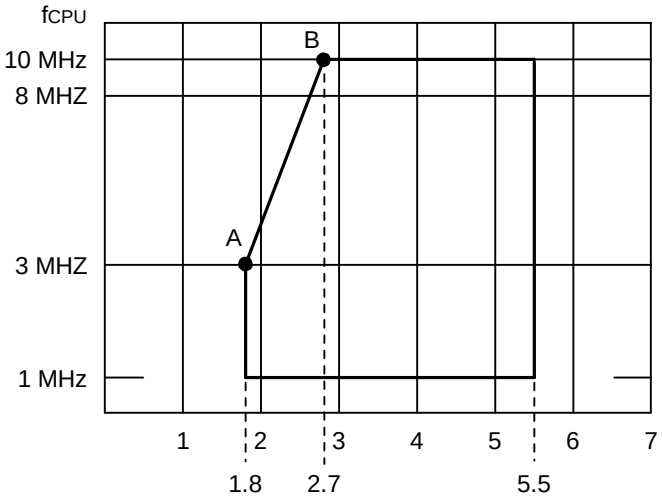
NOTES:
1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. I_{DD} and I_{DD2} include a power consumption of subsystem oscillator.
3. I_{DD3} and I_{DD4} are the current when the main system clock oscillation stop and the subsystem clock is used.
4. I_{DD5} is the current when the main and subsystem clock oscillation stop.

case of S3P8245, the characteristic of V_{OH} and V_{OL} is differ with the characteristic of S3P8249 like as bellow. Other characteristics are same each other.

Table 21-5. D.C Electrical Characteristics of S3C8248/C8245

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH1}	V_{DD} = 5 V; I_{OH} = -1 mA All output pins except V_{OH2}	V_{DD}-1.0	–	–	V
	V_{OH2}	V_{DD} = 5 V; I_{OH} = -6 mA Port 3.0 only in S3P8245	V_{DD}-0.7			
Output low voltage	V_{OL1}	V_{DD} = 5 V; I_{OL} = 2 Ma All output pins except V_{OL2}	–	–	0.4	
	V_{OL2}	V_{DD} = 5 V; I_{OH} = 12 mA Port 3.0 only in S3P8245			0.7	



Minimum instruction clock = 1/4 x oscillator frequency

Figure 21-2. Operating Voltage Range