# TMS470R1B1M
# 16/32-Bit RISC Flash Microcontroller

SPNS109–SEPTEMBER 2005

## FEATURES

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 60-MHz System Clock (Pipeline Mode)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
- Integrated Memory
  - 1M-Byte Program Flash
    - Two Banks With 16 Contiguous Sectors
  - 64K-Byte Static RAM (SRAM)
  - Memory Security Module (MSM)
  - JTAG Security Module
- Operating Features
  - Low-Power Modes: STANDBY and HALT
  - Industrial Temperature Range
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory/Peripherals
  - Digital Watchdog (DWD) Timer
  - Analog Watchdog (AWD) Timer
  - Enhanced Real-Time Interrupt (RTI)
  - Interrupt Expansion Module (IEM)
  - System Integrity and Failure Detection
  - ICE Breaker
- Direct Memory Access (DMA) Controller
  - 32 Control Packets and 16 Channels
- Zero-Pin Phase-Locked Loop (ZPLL)-Based Clock Module With Prescaler
  - Multiply-by-4 or -8 Internal ZPLL Option
  - ZPLL Bypass Mode
- Twelve Communication Interfaces:
  - Two Serial Peripheral Interfaces (SPIs)
  - 255 Programmable Baud Rates
  - Three Serial Communication Interfaces (SCIs)
    - $2^{24}$ Selectable Baud Rates
    - Asynchronous/Isosynchronous Modes
  - Two High-End CAN Controllers (HECC)
    - 32-Mailbox Capacity
    - Fully Compliant With CAN Protocol, Version 2.0B
  - Five Inter-Integrated Circuit (I2C) Modules
    - Multi-Master and Slave Interfaces
    - Up to 400 Kbps (Fast Mode)
    - 7- and 10-Bit Address Capability
- High-End Timer Lite (HET)
  - 12 Programmable I/O Channels:
    - 12 High-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 64-Instruction Capacity
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)
- 12-Channel, 10-Bit Multi-Buffered ADC (MibADC)
  - 64-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 µs Minimum Sample and Conversion Time
  - Calibration Mode and Self-Test Features
- Flexible Interrupt Handling
- Expansion Bus Module (EBM)
  - Supports 8- and 16-Bit Expansion Bus Memory Interface Mappings
  - 42 I/O Expansion Bus Pins
- 46 Dedicated General-Purpose I/O (GIO) Pins and 47 Additional Peripheral I/Os
- Sixteen External Interrupts
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1(1) (JTAG) Test-Access Port
- 144-Pin Plastic Low-Profile Quad Flatpack (PGE Suffix)

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(1) The test-access port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

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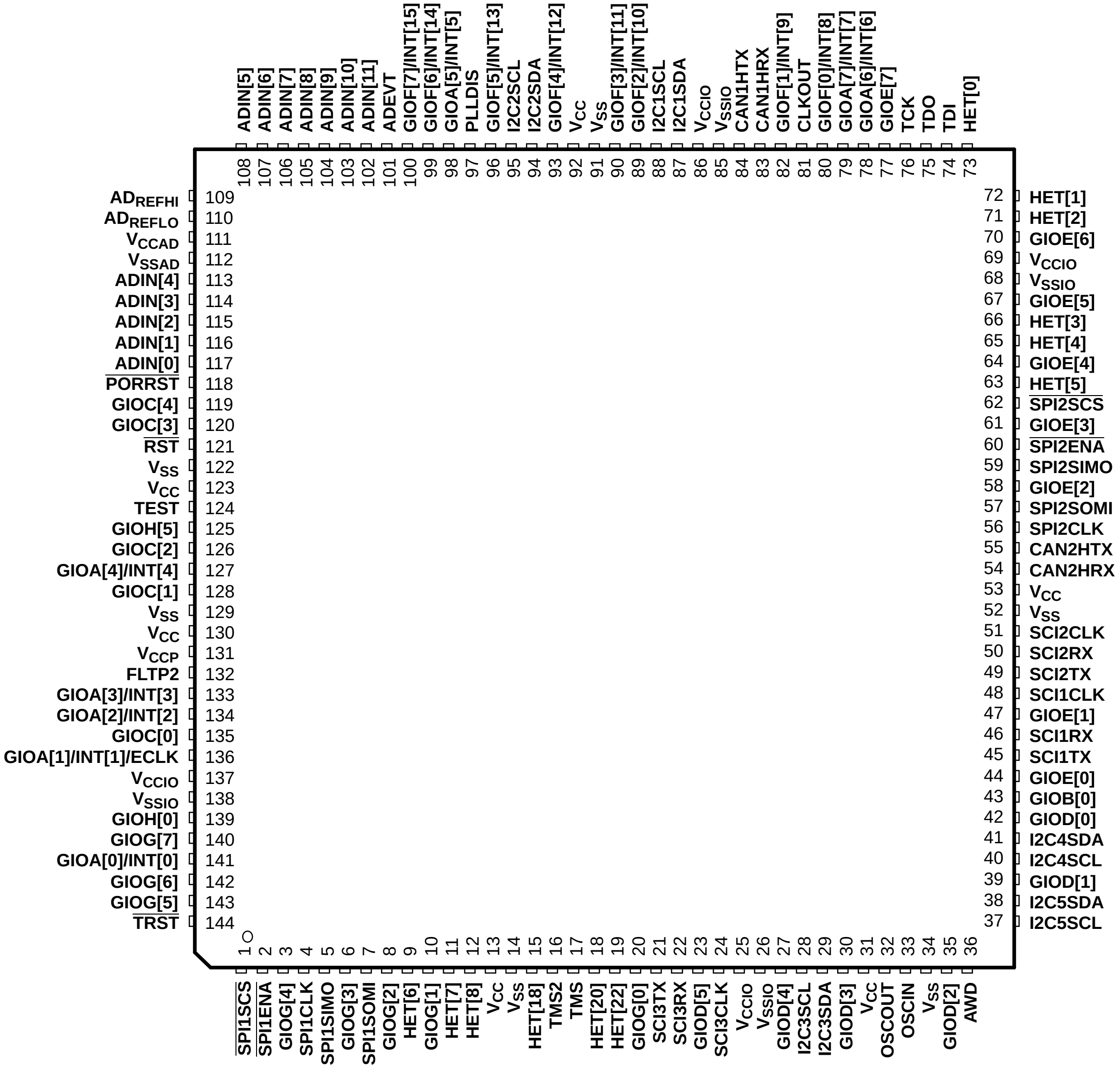
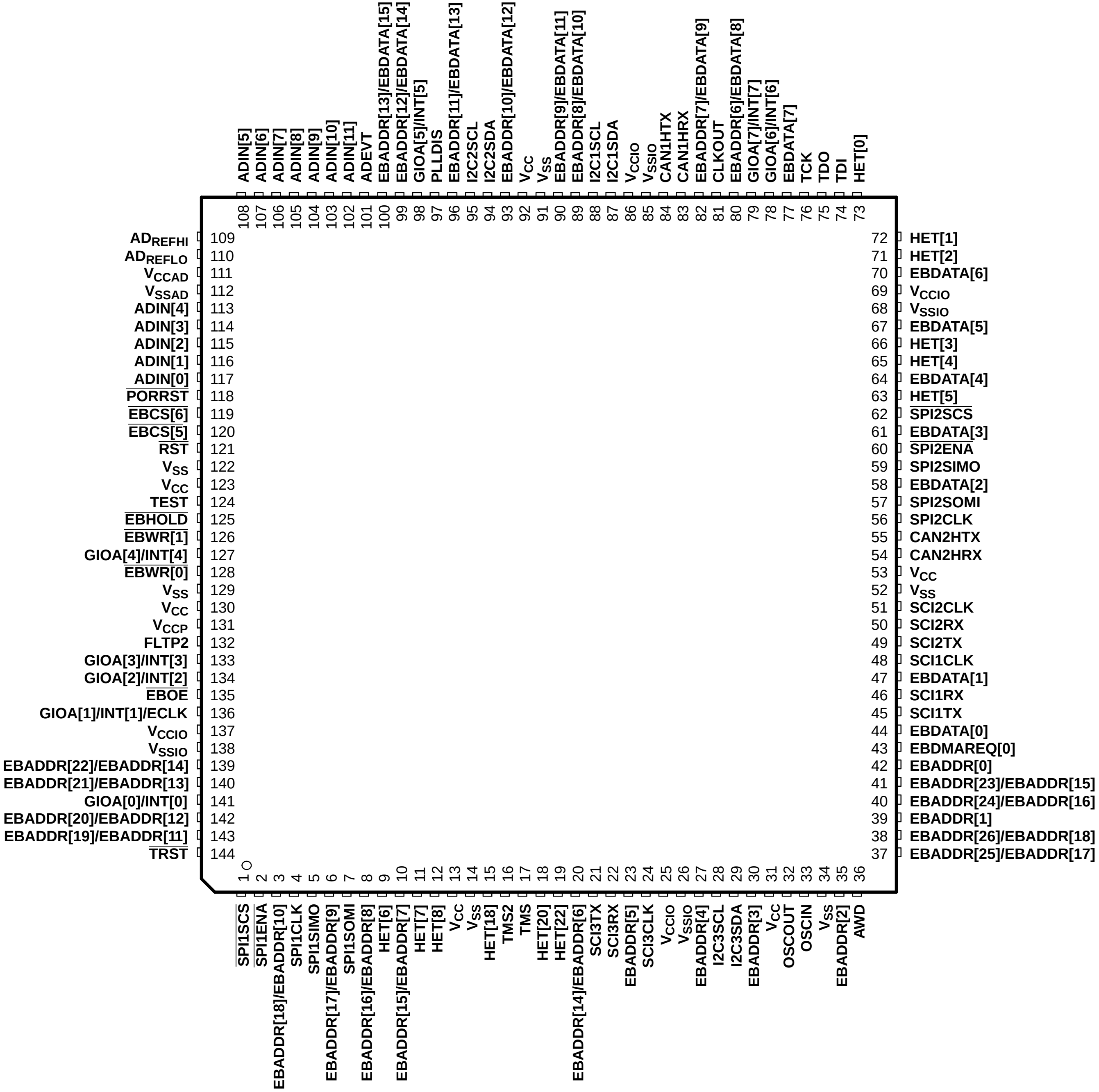
**TMS470R1B1M 144-Pin PGE Package Without Expansion Bus (Top View)**



**TMS470R1B1M 144-Pin PGE Package With Expansion Bus (Top View)**



## DESCRIPTION

The TMS470R1B1M[1] devices are members of the Texas Instruments TMS470R1x family of general-purpose 16/32-bit reduced instruction set computer (RISC) microcontrollers. The B1M microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The TMS470R1B1M utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The B1M RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The B1M devices contain the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 1M-byte flash
- 64K-byte SRAM
- Zero-pin phase-locked loop (ZPLL) clock module
- Digital watchdog (DWD) timer
- Analog watchdog (AWD) timer
- Enhanced real-time interrupt ( RTI) module
- Interrupt expansion module (IEM)
- Memory security module (MSM)
- JTAG security module
- Two serial peripheral interface (SPI) modules
- Three serial communications interface (SCI) modules
- Two high-end CAN controllers (HECC)
- Five inter-integrated circuit (I2C) modules
- 10-bit multi-buffered analog-to-digital converter (MibADC), with 12 input channels
- High-end timer lite (HET) controlling 12 I/Os
- External clock prescale (ECP)
- Expansion bus module (EBM)
- Up to 93 I/O pins

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Prioritization for all internal interrupt sources
- Device clock control
- Parallel signature analysis (PSA)

The enhanced real-time interrupt (RTI) module on the B1M has the option to be driven by the oscillator clock. The digital watchdog (DWD) is a 25-bit resettable decrementing counter that provides a system reset when the watchdog counter expires. This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The B1M memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

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(1) Throughout the remainder of this document, the TMS470R1B1M will be referred to as either the full device name or as B1M.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The flash operates with a system clock frequency of up to 24 MHz or 30 MHz, depending on the input voltage. When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz or 60 MHz, depending on the input voltage. For more detailed information on the flash, see the *F05 Flash* section of this data sheet.

The memory security module (MSM) and the JTAG security module prevent unauthorized access and visibility to on-chip memory, thereby preventing reverse engineering or manipulation of proprietary code.

The B1M device has twelve communication interfaces: two SPIs, three SCIs, two HECCs, and five I2Cs. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The HECC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). These CAN peripherals are ideal for applications operating in noisy and harsh environments (e.g., industrial fields) that require reliable serial communication or multiplexed wiring. The I2C module is a multi-master communication module providing an interface between the B1M microcontroller and an I2C-compatible device via the I2C serial bus. The I2C supports both 100 Kbps and 400 Kbps speeds. For more detailed functional information on the SPI, SCI, and CAN peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197). For more detailed functional information on the I2C, see the *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223).

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. The HET used in this device is the high-end timer lite. It has fewer I/Os than the usual 32 in a standard HET. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The B1M HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high-resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The B1M device has one 10-bit-resolution, sample-and-hold MibADC. Each of the MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other B1M device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

**NOTE:**

> ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The expansion bus module (EBM) is a standalone module that supports the multiplexing of the GIO functions and the expansion bus interface. For more information on the EBM, see the *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222).

The B1M device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

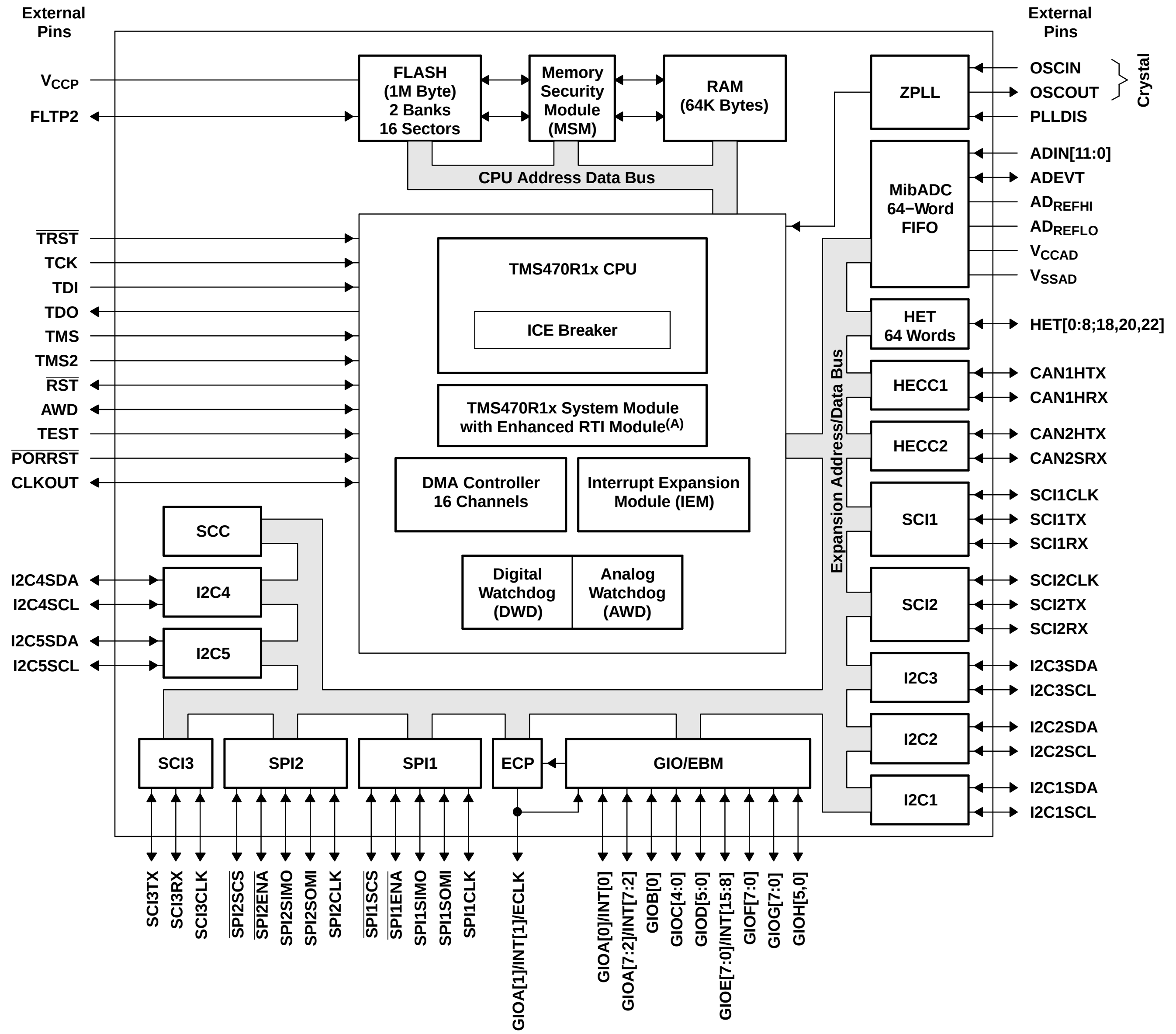
## Device Characteristics

Table 1 identifies all the characteristics of the B1M device except the SYSTEM and CPU, which are generic.

### Table 1. Device Characteristics

| CHARACTERISTICS | DEVICE DESCRIPTION TMS470R1B1M | COMMENTS |
|---|---|---|
| **MEMORY** | | |
| For the number of memory selects on this device, see Table 3, *TMS470R1B1M Memory Selection Assignment*. | | |
| INTERNAL MEMORY | Pipeline/Non-Pipeline<br>1M-Byte flash<br>64K-Byte SRAM<br>Memory Security Module (MSM)<br>JTAG Security Module | Flash is pipeline-capable.<br>The B1M RAM is implemented in one 64K array selected by two memory-select signals (see Table 3, *TMS470R1B1M Memory Selection Assignment* ). |
| **PERIPHERALS** | | |
| For the device-specific interrupt priority configurations, see Table 6, *Interrupt Priority*. And for the 1K peripheral address ranges and their peripheral selects, see Table 4, *B1M Peripherals, System Module, and Flash Base Addresses*. | | |
| CLOCK | ZPLL | Zero-pin PLL has no external loop filter pins. |
| Expansion Bus | EBM | Expansion bus module with 42 pins. Supports 8- and 16-bit memories. See Table 7 for details. |
| GENERAL-PURPOSE I/Os | 46 I/O | Port A has 8 external pins; Port B has only 1 external pin; Port C has 5 external pins; Port D has 6 external pins; Ports E, F, and G each have 8 external pins; and Port H has 2 external pins. |
| ECP | YES | |
| SCI | 3 (3-pin) | |
| CAN (HECC and/or SCC) | 2 HECC | Two high-end CAN controllers |
| SPI (5-pin, 4-pin or 3-pin) | 2 (5-pin) | |
| I2C | 5 | |
| HET with XOR Share | 12 I/O | The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199). |
| HET RAM | 64-Instruction Capacity | |
| MibADC | 10-bit, 12-channel<br>64-word FIFO | Both the logic and registers for a full 16-channel MibADC are present. |
| CORE VOLTAGE | 1.8 V | |
| I/O VOLTAGE | 3.3 V | |
| PINS | 144 | |
| PACKAGES | PGE | |

## Functional Block Diagram



A. The enhanced RTI module is the system module with two extra bits to disable the ZPLL while in STANDBY mode.

### Table 2. Terminal Functions

| **TERMINAL** | | **TYPE** [1][2] | | **INTERNAL PULLUP/ PULLDOWN** [3] | **DESCRIPTION** |
|---|---|---|---|---|---|
| **NAME** | **NO.** | | | | |
| **HIGH-END TIMER (HET)** | | | | | |
| HET[0] | 73 | 3.3-V | 2mA -z | IPD (20 µA) | Timer input capture or output compare. The HET[8:0,18,20,22] applicable pins can be programmed as general-purpose input/output (GIO) pins. All are high-resolution pins.<br>The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199). |
| HET[1] | 72 | | | | |
| HET[2] | 71 | | | | |
| HET[3] | 66 | | | | |
| HET[4] | 65 | | | | |
| HET[5] | 63 | | | | |
| HET[6] | 9 | | | | |
| HET[7] | 11 | | | | |
| HET[8] | 12 | | | | |
| HET[18] | 15 | | | | |
| HET[20] | 18 | | | | |
| HET[22] | 19 | | | | |
| **HIGH-END CAN CONTROLLER (HECC)** | | | | | |
| CAN1HRX | 83 | 5V tolerant | 4mA | | HECC1 receive pin or GIO pin |
| CAN1HTX | 84 | 3.3-V | 2mA -z | IPU (20 µA) | HECC1 transmit pin or GIO pin |
| CAN2HRX | 54 | 5V tolerant | 4mA | | HECC2 receive pin or GIO pin |
| CAN2HTX | 55 | 3.3-V | 2mA -z | IPU (20 µA) | HECC2 transmit pin or GIO pin |
| **STANDARD CAN CONTROLLER (SCC)** | | | | | |
| CANSRX | - | 5V tolerant | 4mA | | SCC receive pin.The CANSRX signal is only connected to the pad and not to a package pin. **For reduced power consumption in low power mode, CANSRX should be driven output LOW.** |
| CANSTX | - | 3.3-V | 2mA -z | IPU (20 µA) | SCC transmit pin. The CANSTX signal is only connected to the pad and not to a package pin. **For reduced power consumption in low power mode, CANSTX should be driven output LOW.** |
| **GENERAL-PURPOSE I/O (GIO)** | | | | | |
| GIOA[0]/INT[0] | 141 | 5V tolerant | 4mA | | General-purpose input/output pins. GIOA[7:0]/INT[7:0] are interrupt-capable pins.<br>GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module. |
| GIOA[1]/INT[1]/ECLK | 136 | | | | |
| GIOA[2]/INT[2] | 134 | | | | |
| GIOA[3]/INT[3] | 133 | | | | |
| GIOA[4]/INT[4] | 127 | | | | |
| GIOA[5]/INT[5] | 98 | | | | |
| GIOA[6]/INT[6] | 78 | | | | |
| GIOA[7]/INT[7] | 79 | | | | |
| GIOB[0]/EBDMAREQ0 | 43 | 3.3-V | 2mA -z | IPD (20 µA) | GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], and GIOH[5,0] are multiplexed with the expansion bus module.<br>See Table 7. |
| GIOC[0]/$\overline{\text{EBOE}}$ | 135 | | | | |
| GIOC[1]/$\overline{\text{EBWR[0]}}$ | 128 | | | | |
| GIOC[2]/$\overline{\text{EBWR[1]}}$ | 126 | | | | |
| GIOC[3]/$\overline{\text{EBCS[5]}}$ | 120 | | | | |
| GIOC[4]/$\overline{\text{EBCS[6]}}$ | 119 | | | | |

(1) PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$ , are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

### Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE[1][2] | | INTERNAL PULLUP/ PULLDOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| GIOD[0]/EBADDR[0] | 42 | 3.3-V | 2mA -z | IPD (20 µA) | GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], and GIOH[5,0] are multiplexed with the expansion bus module.<br>GIOF[7:0]/INT[15:8] are interrupt-capable pins.<br>See Table 7. |
| GIOD[1]/EBADDR[1] | 39 | | | | |
| GIOD[2]/EBADDR[2] | 35 | | | | |
| GIOD[3]/EBADDR[3] | 30 | | | | |
| GIOD[4]/EBADDR[4] | 27 | | | | |
| GIOD[5]/EBADDR[5] | 23 | | | | |
| GIOE[0]/EBDATA[0] | 44 | | | | |
| GIOE[1]/EBDATA[1] | 47 | | | | |
| GIOE[2]/EBDATA[2] | 58 | | | | |
| GIOE[3]/EBDATA[3] | 61 | | | | |
| GIOE[4]/EBDATA[4] | 64 | | | | |
| GIOE[5]/EBDATA[5] | 67 | | | | |
| GIOE[6]/EBDATA[6] | 70 | | | | |
| GIOE[7]/EBDATA[7] | 77 | | | | |
| GIOF[0]/INT[8]/ EBADDR[6]/EBDATA[8] | 80 | | | | |
| GIOF[1]/INT[9]/ EBADDR[7]/EBDATA[9] | 82 | | | | |
| GIOF[2]/INT[10]/ EBADDR[8]/EBDATA[10] | 89 | | | | |
| GIOF[3]/INT[11]/ EBADDR[9]/EBDATA[11] | 90 | | | | |
| GIOF[4]/INT[12]/ EBADDR[10]/EBDATA[12] | 93 | | | | |
| GIOF[5]/INT[13]/ EBADDR[11]/EBDATA[13] | 96 | | | | |
| GIOF[6]/INT[14]/ EBADDR[12]/EBDATA[14] | 99 | | | | |
| GIOF[7]/INT[15]/ EBADDR[13]/EBDATA[15] | 100 | | | | |
| GIOG[0]/EBADDR[14]/ EBADDR[6] | 20 | | | | |
| GIOG[1]/EBADDR[15]/ EBADDR[7] | 10 | | | | |
| GIOG[2]/EBADDR[16]/ EBADDR[8] | 8 | | | | |
| GIOG[3]/EBADDR[17]/ EBADDR[9] | 6 | | | | |
| GIOG[4]/EBADDR[18]/ EBADDR[10] | 3 | | | | |
| GIOG[5]/EBADDR[19]/ EBADDR[11] | 143 | | | | |
| GIOG[6]/EBADDR[20]/EB ADDR[12] | 142 | | | | |
| GIOG[7]/EBADDR[21]/ EBADDR[13] | 140 | | | | |
| GIOH[0]/EBADDR[22]/ EBADDR[14] | 139 | | | | |
| GIOH[5]/$\overline{\text{EBHOLD}}$ | 125 | | | | |

### Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE (1) (2) | | INTERNAL PULLUP/ PULLDOWN (3) | DESCRIPTION |
|---|---|---|---|---|---|
| **NAME** | **NO.** | | | | |
| | | **MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)** | | | |
| ADEVT | 101 | 3.3-V | 2mA -z | IPD (20 µA) | MibADC event input. Can be programmed as a GIO pin. |
| ADIN[0] | 117 | | | | MibADC analog input pins |
| ADIN[1] | 116 | | | | |
| ADIN[2] | 115 | | | | |
| ADIN[3] | 114 | | | | |
| ADIN[4] | 113 | | | | |
| ADIN[5] | 108 | | | | |
| ADIN[6] | 107 | | | | |
| ADIN[7] | 106 | | | | |
| ADIN[8] | 105 | | | | |
| ADIN[9] | 104 | | | | |
| ADIN[10] | 103 | | | | |
| ADIN[11] | 102 | | | | |
| AD$_{REFHI}$ | 109 | 3.3-V REF | | | MibADC module high-voltage reference input |
| AD$_{REFLO}$ | 110 | GND REF | | | MibADC module low-voltage reference input |
| V$_{CCAD}$ | 111 | 3.3-V PWR | | | MibADC analog supply voltage |
| V$_{SSAD}$ | 112 | GND | | | MibADC analog ground reference |
| | | **SERIAL PERIPHERAL INTERFACE 1 (SPI1)** | | | |
| SPI1CLK | 4 | 5V tolerant | 4mA | | SPI1 clock. SPI1CLK can be programmed as a GIO pin. |
| $\overline{\text{SPI1ENA}}$ | 2 | | | | SPI1 chip enable. Can be programmed as a GIO pin. |
| $\overline{\text{SPI1SCS}}$ | 1 | | | | SPI1 slave chip select. Can be programmed as a GIO pin. |
| SPI1SIMO | 5 | | | | SPI1 data stream. Slave in/master out. Can be programmed as a GIO pin. |
| SPI1SOMI | 7 | | | | SPI1 data stream. Slave out/master in. Can be programmed as a GIO pin. |
| | | **SERIAL PERIPHERAL INTERFACE 2 (SPI2)** | | | |
| SPI2CLK | 56 | 5V tolerant | 4mA | | SPI2 clock. Can be programmed as a GIO pin. |
| $\overline{\text{SPI2ENA}}$ | 60 | | | | SPI2 chip enable. Can be programmed as a GIO pin. |
| $\overline{\text{SPI2SCS}}$ | 62 | | | | SPI2 slave chip select. Can be programmed as a GIO pin. |
| SPI2SIMO | 59 | | | | SPI2 data stream. Slave in/master out. Can be programmed as a GIO pin. |
| SPI2SOMI | 57 | | | | SPI2 data stream. Slave out/master in. Can be programmed as a GIO pin. |
| | | **INTER-INTEGRATED CIRCUIT 1 (I2C1)** | | | |
| I2C1SDA | 87 | 5V tolerant | 4mA | | I2C1 serial data pin or GIO pin |
| I2C1SCL | 88 | | | | I2C1 serial clock pin or GIO pin |
| | | **INTER-INTEGRATED CIRCUIT 2 (I2C2)** | | | |
| I2C2SDA | 94 | 5V tolerant | 4mA | | I2C2 serial data pin or GIO pin |
| I2C2SCL | 95 | | | | I2C2 serial clock pin or GIO pin |

## Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE[1][2] | | INTERNAL PULLUP/ PULLDOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **INTER-INTEGRATED CIRCUIT 3 (I2C3)** | | | | | |
| I2C3SDA | 29 | 5V tolerant | 4mA | | I2C3 serial data pin or GIO pin |
| I2C3SCL | 28 | | | | I2C3 serial clock pin or GIO pin |
| **INTER-INTEGRATED CIRCUIT 4 (I2C4)** | | | | | |
| I2C4SDA | 41 | 5V tolerant | 4mA | | I2C4 serial data pin or GIO pin |
| I2C4SCL | 40 | | | | I2C4 serial clock pin or GIO pin |
| **INTER-INTEGRATED CIRCUIT 5 (I2C5)** | | | | | |
| I2C5SDA | 38 | 5V tolerant | 4mA | | I2C5 serial data pin or GIO pin |
| I2C5SCL | 37 | | | | I2C5 serial clock pin or GIO pin |
| **ZERO-PIN PHASE-LOCKED LOOP (ZPLL)** | | | | | |
| OSCIN | 33 | 1.8-V | | | Crystal connection pin or external clock input |
| OSCOUT | 32 | | 2mA | | External crystal connection pin |
| PLLDIS | 97 | 3.3-V | | IPD (20 µA) | Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock. If not in bypass mode, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. |
| **SERIAL COMMUNICATIONS INTERFACE 1 (SCI1)** | | | | | |
| SCI1CLK | 48 | 3.3-V | 2mA -z | IPD (20 µA) | SCI1 clock. SCI1CLK can be programmed as a GIO pin. |
| SCI1RX | 46 | 5V tolerant | 4mA | | SCI1 data receive. SCI1RX can be programmed as a GIO pin. |
| SCI1TX | 45 | 3.3-V | 2mA -z | IPU (20 µA) | SCI1 data transmit. SCI1TX can be programmed as a GIO pin. |
| **SERIAL COMMUNICATIONS INTERFACE 2 (SCI2)** | | | | | |
| SCI2CLK | 51 | 3.3-V | 2mA -z | IPD (20 µA) | SCI2 clock. SCI2CLK can be programmed as a GIO pin. |
| SCI2RX | 50 | 5V tolerant | 4mA | | SCI2 data receive. SCI2RX can be programmed as a GIO pin. |
| SCI2TX | 49 | 3.3-V | 2mA -z | IPU (20 µA) | SCI2 data transmit. SCI2TX can be programmed as a GIO pin. |
| **SERIAL COMMUNICATIONS INTERFACE 3 (SCI3)** | | | | | |
| SCI3CLK | 24 | 3.3-V | 2mA -z | IPD (20 µA) | SCI3 clock. SCI3CLK can be programmed as a GIO pin. |
| SCI3RX | 22 | 5V tolerant | 4mA | | SCI3 data receive. SCI3RX can be programmed as a GIO pin. |
| SCI3TX | 21 | 3.3-V | 2mA -z | IPU (20 µA) | SCI3 data transmit. SCI3TX can be programmed as a GIO pin. |
| **SYSTEM MODULE (SYS)** | | | | | |
| CLKOUT | 81 | 3.3-V | 8mA | | Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK. |
| $\overline{\text{PORRST}}$ | 118 | 3.3-V | | IPD (20 µA) | Input master chip power-up reset. External $V_{CC}$ monitor circuitry must assert a power-on reset. |
| $\overline{\text{RST}}$ | 121 | 3.3-V | 4mA | IPU (20 µA) | Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset.<br>On this pin, the output buffer is implemented as an open drain (drives low only).<br>To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin. |

### Table 2. Terminal Functions (continued)

| TERMINAL | | TYPE[1][2] | | INTERNAL PULLUP/ PULLDOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)** | | | | | |
| AWD | 36 | 3.3-V | 8mA | | Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.<br>For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189). |
| **TEST/DEBUG (T/D)** | | | | | |
| TCK | 76 | 3.3-V | | IPD (20 µA) | Test clock. TCK controls the test hardware (JTAG). |
| TDI | 74 | | 8mA | IPU (20 µA) | Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG). |
| TDO | 75 | | 8mA | IPD (20 µA) | Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG). |
| TEST | 124 | 3.3-V | | IPD (20 µA) | Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. |
| TMS | 17 | | 8mA | IPU (20 µA) | Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG). |
| TMS2 | 16 | | 8mA | IPU (20 µA) | Serial input for controlling the second TAP. TI recommends that this pin be connected to $V_{CCIO}$ or pulled up to $V_{CCIO}$ by an external resistor. |
| $\overline{\text{TRST}}$ | 144 | | | IPD (20 µA) | Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that this pin be pulled down to ground by an external resistor. |
| **FLASH** | | | | | |
| FLTP2 | 132 | NC | NC | | Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].** |
| $V_{CCP}$ | 131 | 3.3-V PWR | | | Flash external pump voltage (3.3 V) |
| **SUPPLY VOLTAGE CORE (1.8 V)** | | | | | |
| $V_{CC}$ | 13 | 1.8-V PWR | | | Core logic supply voltage |
| | 31 | | | | |
| | 53 | | | | |
| | 92 | | | | |
| | 123 | | | | |
| | 130 | | | | |
| **SUPPLY VOLTAGE DIGITAL I/O (3.3 V)** | | | | | |
| $V_{CCIO}$ | 25 | 3.3-V PWR | | | Digital I/O supply voltage |
| | 69 | | | | |
| | 86 | | | | |
| | 137 | | | | |

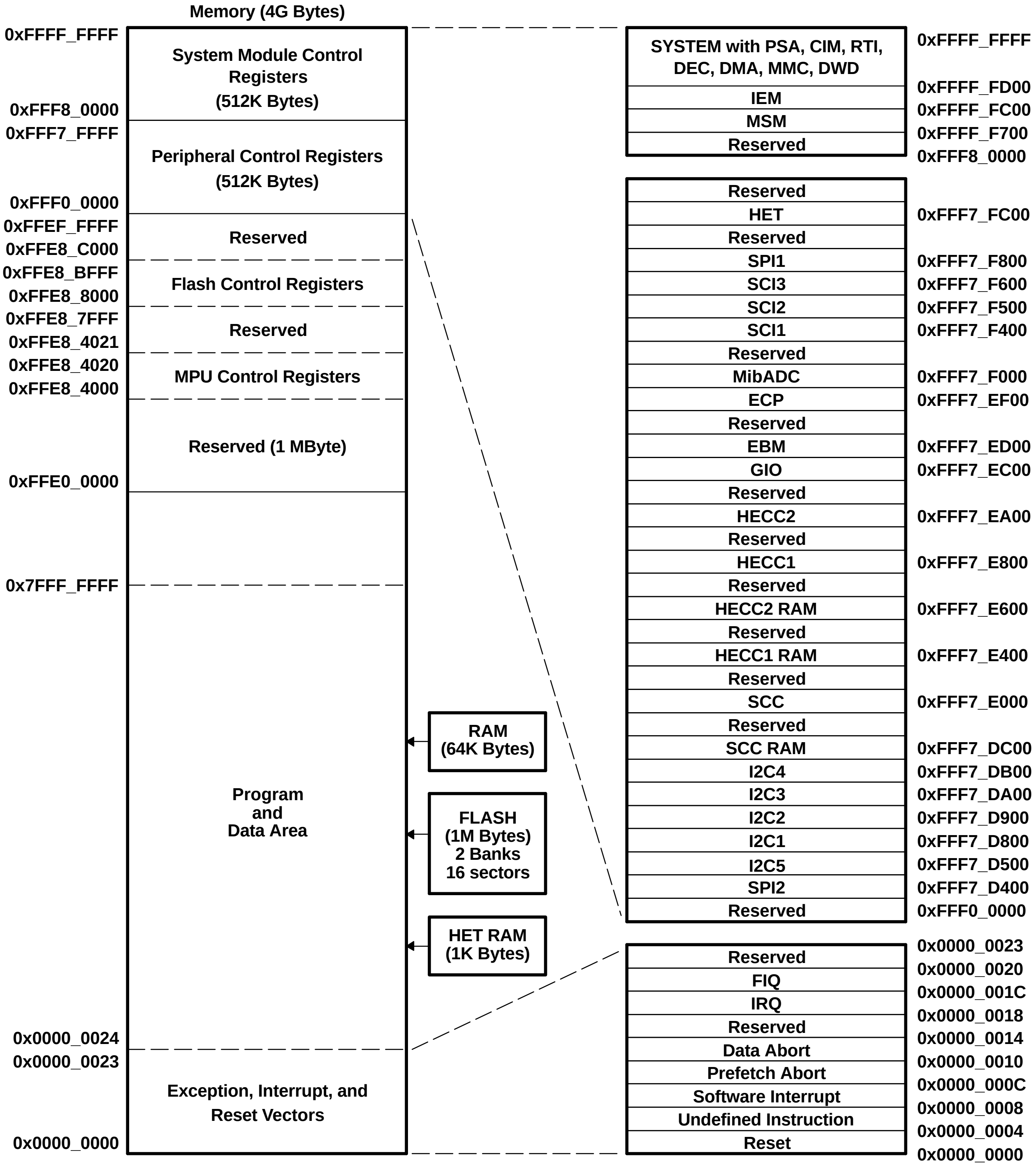
### Table 2. Terminal Functions (continued)

| TERMINAL |  | TYPE(1)(2) |  | INTERNAL PULLUP/ PULLDOWN(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. |  |  |  |  |
| **SUPPLY GROUND CORE** |  |  |  |  |  |
| $V_{SS}$ | 14<br>34<br>52<br>91<br>122<br>129 | GND |  |  | Core supply ground reference |
| **SUPPLY GROUND DIGITAL I/O** |  |  |  |  |  |
| $V_{SSIO}$ | 26<br>68<br>85<br>138 | GND |  |  | Digital I/O supply ground reference |

## B1M Device-Specific Information

### Memory

Figure 1 shows the memory map of the B1M device.



A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.

B. The CPU registers are not part of the memory map.

**Figure 1. TMS470R1B1M Memory Map**

## memory selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 3.

**Table 3. TMS470R1B1M Memory Selection Assignment**

| MEMORY SELECT | MEMORY SELECTED (ALL INTERNAL) | MEMORY SIZE(1) | MPU | MSM | MEMORY BASE ADDRESS REGISTER | STATIC MEM CTL REGISTER |
|---|---|---|---|---|---|---|
| 0 (fine) | FLASH/ROM | 1M | NO | YES | MFBAHR0 and MFBALR0 | |
| 1 (fine) | FLASH/ROM | | NO | YES | MFBAHR1 and MFBALR1 | |
| 2 (fine) | RAM | 64K(2) | YES | YES | MFBAHR2 and MFBALR2 | |
| 3 (fine) | RAM | | YES | YES | MFBAHR3 and MFBALR3 | |
| 4 (fine) | HET RAM | 1K | NO | NO | MFBAHR4 and MFBALR4 | SMCR1 |
| 5 (coarse) | $\overline{\text{CS[5]}}$/GIOC[3] | 128MB (x8)<br>512K (x16) | NO | NO | MCBAHR2 and MCBALR2 | SMCR5 |
| 6 (coarse) | $\overline{\text{CS[6]}}$/GIOC[4] | 128MB (x8)<br>512K (x16) | NO | NO | MCBAHR3 and MCBALR3 | SMCR6 |

(1) x8 refers to size of memory in 8-bits; x16 refers to size of memory in 16-bits.
(2) The starting addresses for both RAM memory-select signals cannot be offset from each other by a multiple of the user-defined block size in the memory-base address register.

### *JTAG security module*

The B1M device includes a JTAG security module to provide maximum security to the memory contents. The visible unlock code can be in the OTP sector or in the first bank of the user-programmable memory. For the B1M, the visible unlock code is in the OTP sector at address 0x0000_01F8.

### *memory security module*

The B1M device also includes a memory security module (MSM) to provide additional security and flexibility to the memory contents' protection. The password for unlocking the MSM is located in the four words just before the flash protection keys.

### *RAM*

The B1M device contains 64K-bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This B1M RAM is implemented in one 64K-byte array selected by two memory-select signals. This B1M configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects cannot be offset from each other by the multiples of the size of the physical RAM (i.e., 64K bytes for the B1M device). The B1M RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

### *F05 Flash*

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the *Flash read* and *Flash program and erase* sections.

### flash protection keys

The B1M device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the B1M are located in the last 4 words of the first 64K sector.

### flash read

The B1M flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

**NOTE:**

The flash external pump voltage ($V_{CCP}$) is required for all operations (program, erase, and read).

### flash pipeline mode

When in pipeline mode, the flash operates with a system clock frequency of up to 60 MHz (versus a system clock frequency of 30 MHz in normal mode). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also, in pipeline mode the flash can be read with no wait states when memory addresses are contiguous (after the initial 1- or 2-wait-state reads).

**NOTE:**

After a system reset, pipeline mode is disabled (ENPIPE bit [FMREGOPT.0] is a 0). In other words, the B1M device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GBLCTRL.4) will override pipeline mode.

**flash program and erase**

The B1M device flash contains two 512K-byte memory arrays (or banks), for a total of 1M-byte of flash, and consists of sixteen sectors. These sixteen sectors are sized as follows:

| SECTOR NO. | SEGMENT | LOW ADDRESS | HIGH ADDRESS | MEMORY ARRAYS (OR BANKS) |
|---|---|---|---|---|
| OTP | 2K Bytes | 0x0000_0000 | 0x0000_007FF | BANK0<br>(512K Bytes) |
| 0 | 64K Bytes | 0x0000_0000 | 0x0000_FFFF | |
| 1 | 64K Bytes | 0x0001_0000 | 0x0001_FFFF | |
| 2 | 64K Bytes | 0x0002_0000 | 0x0002_FFFF | |
| 3 | 64K Bytes | 0x0003_0000 | 0x0003_FFFF | |
| 4 | 64K Bytes | 0x0004_0000 | 0x0004_FFFF | |
| 5 | 64K Bytes | 0x0005_0000 | 0x0005_FFFF | |
| 6 | 64K Bytes | 0x0006_0000 | 0x0006_FFFF | |
| 7 | 64K Bytes | 0x0007_0000 | 0x0007_FFFF | |
| 0 | 64K Bytes | 0x0008_0000 | 0x0008_FFFF | BANK1<br>(512K Bytes) |
| 1 | 64K Bytes | 0x0009_0000 | 0x0009_FFFF | |
| 2 | 64K Bytes | 0x000A_0000 | 0x000A_FFFF | |
| 3 | 64K Bytes | 0x000B_0000 | 0x000B_FFFF | |
| 4 | 64K Bytes | 0x000C_0000 | 0x000C_FFFF | |
| 5 | 64K Bytes | 0x000D_0000 | 0x000D_FFFF | |
| 6 | 64K Bytes | 0x000E_0000 | 0x000E_FFFF | |
| 7 | 64K Bytes | 0x000F_0000 | 0x000F_FFFF | |

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

**NOTE:**

> The flash external pump voltage ($V_{CCP}$) is required for all operations (program, erase, and read).

Execution can occur from one bank while programming/erasing any or all sectors of another bank. However, execution cannot occur from any sector within a bank that is being programmed or erased.

**NOTE:**

> When the OTP sector is enabled, the rest of flash memory is disabled. The OTP memory can only be read or programmed from code executed out of RAM.

### *HET RAM*

The B1M device contains HET RAM. The HET RAM has a 64-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

## peripheral selects and base addresses

The B1M device uses 10 of the 16 peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 4.

**Table 4. B1M Peripherals, System Module, and Flash Base Addresses**

| CONNECTING MODULE | ADDRESS RANGE | | PERIPHERAL SELECTS |
|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | |
| SYSTEM | 0 x FFFF_FFCC | 0 x FFFF_FFFF | N/A |
| RESERVED | 0 x FFFF_FF70 | 0 x FFFF_FFCB | N/A |
| DWD | 0xFFFF_FF60 | 0 x FFFF_FF6F | N/A |
| PSA | 0 x FFFF_FF40 | 0 x FFFF_FF5F | N/A |
| CIM | 0 x FFFF_FF20 | 0 x FFFF_FF3F | N/A |
| RTI | 0 x FFFF_FF00 | 0 x FFFF_FF1F | N/A |
| DMA | 0 x FFFF_FE80 | 0 x FFFF_FEFF | N/A |
| DEC | 0 x FFFF_FE00 | 0 x FFFF_FE7F | N/A |
| RESERVED | 0xFFFF_FD80 | 0xFFFF_FDFF | N/A |
| MMC | 0 x FFFF_FD00 | 0 x FFFF_FD7F | N/A |
| IEM | 0 x FFFF_FC00 | 0 x FFFF_FCFF | N/A |
| RESERVED | 0 x FFFF_Fb00 | 0 x FFFF_FBFF | N/A |
| RESERVED | 0 x FFFF_Fa00 | 0 x FFFF_FAFF | N/A |
| DMA CMD BUFFER | 0 x FFFF_F800 | 0 x FFFF_F9FF | N/A |
| MSM | 0xFFFF_F700 | 0xFFFF_F7FF | N/A |
| RESERVED | 0xFFF8_0000 | 0xFFFF_F6FF | N/A |
| RESERVED | 0 x FFF7_FD00 | 0xFFF7_FFFF | PS[0] |
| HET | 0xFFF7_FC00 | 0xFFF7_FCFF | |
| RESERVED | 0xFFF7_F900 | 0xFFF7_FBFF | PS[1] |
| SPI1 | 0xFFF7_F800 | 0xFFF7_F8FF | |
| RESERVED | 0xFFF7_F700 | 0xFFF7_F7FF | PS[2] |
| SCI3 | 0xFFF7_F600 | 0xFFF7_F6FF | |
| SCI2 | 0XFFF7_F500 | 0XFFF7_F5FF | |
| SCI1 | 0xFFF7_F400 | 0xFFF7_F4FF | |
| RESERVED | 0xFFF7_F100 | 0xFFF7_F3FF | PS[3] |
| MibADC | 0xFFF7_F000 | 0xFFF7_F0FF | |
| ECP | 0xFFF7_EF00 | 0xFFF7_EFFF | PS[4] |
| RESERVED | 0xFFF7_EE00 | 0xFFF7_EEFF | |
| EBM | 0xFFF7_ED00 | 0xFFF7_EDFF | |
| GIO | 0xFFF7_EC00 | 0xFFF7_ECFF | |
| HECC2 | 0xFFF7_EB00 | 0xFFF7_EBFF | PS[5] |
| | 0xFFF7_EA00 | 0xFFF7_EAFF | |
| HECC1 | 0xFFF7_E900 | 0xFFF7_E9FF | |
| | 0xFFF7_E800 | 0xFFF7_E8FF | |
| HECC2 RAM | 0xFFF7_E700 | 0xFFF7_E7FF | PS[6] |
| | 0xFFF7_E600 | 0xFFF7_E6FF | |
| HECC1 RAM | 0xFFF7_E500 | 0xFFF7_E5FF | |
| | 0xFFF7_E400 | 0xFFF7_E4FF | |
| RESERVED | 0xFFF7_E100 | 0xFFF7_E3FF | PS[7] |
| SCC | 0xFFF7_E000 | 0xFFF7_E0FF | |

### Table 4. B1M Peripherals, System Module, and Flash Base Addresses (continued)

| CONNECTING MODULE | ADDRESS RANGE | | PERIPHERAL SELECTS |
|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | |
| RESERVED | 0xFFF7_DD00 | 0xFFF7_DFFF | PS[8] |
| SCC RAM | 0xFFF7_DC00 | 0xFFF7_DCFF | |
| I2C4 | 0xFFF7_DB00 | 0xFFF7_DBFF | PS[9] |
| I2C3 | 0xFFF7_DA00 | 0xFFF7_DAFF | |
| I2C2 | 0xFFF7_D900 | 0xFFF7_D9FF | |
| I2C1 | 0xFFF7_D800 | 0xFFF7_D8FF | |
| RESERVED | 0xFFF7_D600 | 0xFFF7_D7FF | PS[10] |
| I2C5 | 0xFFF7_D500 | 0xFFF7_D5FF | |
| SPI2 | 0xFFF7_D400 | 0xFFF7_D4FF | |
| RESERVED | 0xFFF7_CC00 | 0xFFF7_D3FF | PS[11] – PS[12] |
| RESERVED | 0xFFF7_C800 | 0xFFF7_CBFF | PS[13] |
| RESERVED | 0xFFF7_C000 | 0xFFF7_C7FF | PS[14] – PS[15] |
| RESERVED | 0xFFF0_0000 | 0xFFF7_BFFF | N/A |
| FLASH CONTROL REGISTERS | 0xFFE8_8000 | 0xFFE8_BFFF | N/A |
| RESERVED | 0xFFF8_4024 | 0xFFF8_7FFF | N/A |
| MPU CONTROL REGISTERS | 0xFFE8_4000 | 0xFFE8_4023 | N/A |
| RESERVED | 0xFFF8_0000 | 0xFFF8_3FFF | N/A |

### direct-memory access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the B1M memory map (except for restricted memory locations like the system control registers area). The DMA manages up to 16 channels, and supports data transfer for both on-chip and off-chip memories and peripherals. The DMA controller is connected to both the CPU and peripheral buses, enabling these data transfers to occur in parallel with CPU activity and thus maximizing overall system performance.

Although the DMA controller has two possible configurations, for the B1M device, the DMA controller configuration is 32 control packets and 16 channels.

For the B1M DMA request hardwired configuration, see Table 5.

**Table 5. DMA Request Lines Connections**(1)

| MODULES | DMA REQUEST INTERRUPT SOURCES | | DMA CHANNEL |
|---|---|---|---|
| EBM | Expansion Bus DMA request | EBDMAREQ[0] | DMAREQ[0] |
| SPI1/I2C4 | SPI1 end-receive/I2C4 read | SPI1DMA0/I2C4DMA0 | DMAREQ[1] |
| SPI1/I2C4 | SPI1 end-transmit/I2C4 write | SPI1DMA1/I2C4DMA1 | DMAREQ[2] |
| MibADC/I2C1 | ADC EV/I2C1 read | MibADCDMA0/I2C1DMA0 | DMAREQ[3] |
| MibADC/SCI1/I2C5 | ADC G1/SCI1 end-receive/I2C5 read | MibADCDMA1/SCI1DMA0/I2C5DMA0 | DMAREQ[4] |
| MibADC/SCI1/I2C5 | ADC G2/SCI1 end-transmit/I2C5 write | MibADCDMA2/SCI1DMA1/I2C5DMA1 | DMAREQ[5] |
| I2C1 | I2C1 write | I2C1DMA1 | DMAREQ[6] |
| SCI3/SPI2 | SCI3 end-receive/SPI2 end-receive | SCI3DMA0/SPI2DMA0 | DMAREQ[7] |
| SCI3/SPI2 | SCI3 end-transmit/SPI2 end-transmit | SCI3DMA01SPI2DMA1 | DMAREQ[8] |
| I2C2 | I2C2 read end-receive | I2C2DMA0 | DMAREQ[9] |
| I2C2 | I2C2 write end-transmit | I2C2DMA1 | DMAREQ[10] |
| I2C3 | I2C3 read | I2C3DMA0 | DMAREQ[11] |
| I2C3 | I2C3 write | I2C3DMA1 | DMAREQ[12] |
| Reserved | | | DMAREQ[13] |
| SCI2 | SCI2 end-receive | SCI2DMA0 | DMAREQ[14] |
| SCI2 | SCI2 end-transmit | SCI2DMA1 | DMAREQ[15] |

(1) For DMA channels with more than one assigned request source, *only one* of the sources listed can be the DMA request generator in a given application. The device has software control to ensure that there are no conflicts between requesting modules.

Each channel has two control packets attached to it, allowing the DMA to continuously load RAM and generate periodic interrupts so that the data can be read by the CPU. The control packets allow for the interrupt enable, and the channels determine the priority level of the interrupt.

DMA transfers occur in one of two modes:

- Non-request mode (used when transferring from memory to memory)
- Request mode (used when transferring from memory to peripheral)

For more detailed functional information on the DMA controller, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

### interrupt priority (IEM to CIM)

Interrupt requests originating from the B1M peripheral modules (i.e., SPI1 or SPI2; SCI1 or SCI2; RTI; etc.) are assigned to channels within the 48-channel interrupt expansion module (IEM) where, via programmable register mapping, these channels are then mapped to the 32-channel central interrupt manager (CIM) portion of the SYS module.

Programming multiple interrupt sources in the IEM to the same CIM channel effectively shares the CIM channel between sources.

The CIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The CIM prioritizes interrupts. The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For IEM-to-CIM default mapping, channel priorities, and their associated modules, see Table 6.

**Table 6. Interrupt Priority (IEM and CIM)**

| MODULES | INTERRUPT SOURCES | DEFAULT CIM INTERRUPT LEVEL/CHANNEL | IEM CHANNEL |
|---|---|---|---|
| SPI1 | SPI1 end-transfer/overrun | 0 | 0 |
| RTI | COMP2 interrupt | 1 | 1 |
| RTI | COMP1 interrupt | 2 | 2 |
| RTI | TAP interrupt | 3 | 3 |
| SPI2 | SPI2 end-transfer/overrun | 4 | 4 |
| GIO | GIO interrupt A | 5 | 5 |
| Reserved | | 6 | 6 |
| HET | HET interrupt 1 | 7 | 7 |
| I2C1 | I2C1 interrupt | 8 | 8 |
| SCI1/SCI2 | SCI1 or SCI2 error interrupt | 9 | 9 |
| SCI1 | SCI1 receive interrupt | 10 | 10 |
| Reserved | | 11 | 11 |
| I2C2 | I2C2 interrupt | 12 | 12 |
| HECC1 | HECC1 interrupt A | 13 | 13 |
| SCC | SCC interrupt A | 14 | 14 |
| Reserved | | 15 | 15 |
| MibADC | MibADC end event conversion | 16 | 16 |
| SCI2 | SCI2 receive interrupt | 17 | 17 |
| DMA | DMA interrupt 0 | 18 | 18 |
| I2C3 | I2C3 interrupt | 19 | 19 |
| SCI1 | SCI1 transmit interrupt | 20 | 20 |
| System | SW interrupt (SSI) | 21 | 21 |
| Reserved | | 22 | 22 |
| HET | HET interrupt 2 | 23 | 23 |
| HECC1 | HECC1 interrupt B | 24 | 24 |
| SCC | SCC interrupt B | 25 | 25 |
| SCI2 | SCI2 transmit interrupt | 26 | 26 |
| MibADC | MibADC end Group 1 conversion | 27 | 27 |
| DMA | DMA Interrupt 1 | 28 | 28 |
| GIO | GIO interrupt B | 29 | 29 |
| MibADC | MibADC end Group 2 conversion | 30 | 30 |
| SCI3 | SCI3 error interrupt | 31 | 31 |

### Table 6. Interrupt Priority (IEM and CIM) (continued)

| MODULES | INTERRUPT SOURCES | DEFAULT CIM INTERRUPT LEVEL/CHANNEL | IEM CHANNEL |
|---|---|---|---|
| Reserved | | 31 | 32–37 |
| HECC2 | HECC2 interrupt A | 31 | 38 |
| HECC2 | HECC2 interrupt B | 31 | 39 |
| SCI3 | SCI3 receive interrupt | 31 | 40 |
| SCI3 | SCI3 transmit interrupt | 31 | 41 |
| I2C4 | I2C4 interrupt | 31 | 42 |
| I2C5 | I2C5 interrupt | 31 | 43 |
| Reserved | | 31 | 44–47 |

For more detailed functional information on the IEM, see the *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211). For more detailed functional information on the CIM, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

## expansion bus module (EBM)

The expansion bus module (EBM) is a standalone module used to bond out both general-purpose input/output pins and expansion bus interface pins. This module supports the multiplexing of the GIO and the expansion bus interface functions. The module also supports 8- and 16- bit expansion bus memory interface mappings as well as mapping of the following expansion bus signals:

- 27-bit address bus (EBADDR[26:0] for x8, 19-bit address bus (EBADDR[18:0] for x16
- 8- or 16-bit data bus (EBDATA[7:0] or EBDATA[15:0])
- 2 write strobes (EBWR[1:0])
- 2 memory chip selects (EBCS[6:5])
- 1 output enable (EBOE)
- 1 external hold signal for interfacing to slow memories (EBHOLD)
- 1 DMA request line (EBDMAREQ[0])

Table 7 shows the multiplexing of I/O signals with the expansion bus interface signals. The mapping of these pins varies depending on the memory mode.

**Table 7. Expansion Bus Mux Mapping(1)**

| GIO | EXPANSION BUS MODULE PINS | |
|---|---|---|
| | **x8(2)** | **x16(2)** |
| GIOB[0] | EBDMAREQ[0] | EBDMAREQ[0] |
| GIOC[0] | $\overline{\text{EBOE}}$ | $\overline{\text{EBOE}}$ |
| GIOC[2:1] | $\overline{\text{EBWR[1:0]}}$ | $\overline{\text{EBWR[1:0]}}$ |
| GIOC[4:3] | $\overline{\text{EBCS[6:5]}}$ | $\overline{\text{EBCS[6:5]}}$ |
| GIOD[5:0] | EBADDR[5:0] | EBADDR[5:0] |
| GIOE[7:0] | EBDATA[7:0] | EBDATA[7:0] |
| GIOF[7:0] | EBADDR[13:6] | EBDATA[15:8] |
| GIOG[7:0] | EBADDR[21:14] | EBADDR[13:6] |
| GIOH[5] | $\overline{\text{EBHOLD}}$ | $\overline{\text{EBHOLD}}$ |
| I2C5SDA | EBADDR[26] | EBADDR[18] |
| I2C5SCL | EBADDR[25] | EBADDR[17] |
| I2C4SCL | EBADDR[24] | EBADDR[16] |
| I2C4SDA | EBADDR[23] | EBADDR[15] |
| GIOH[0] | EBADDR[22] | EBADDR[14] |

(1) For more detailed information, see the*TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222) and the *TMS470R1x General Purpose Input/Output Reference Guide* (literature number SPNU192).
(2) X8 refers to size of memory in 8-bits; X16 refers to size of memory in 16-bits.

Table 8 lists the names of the expansion bus interface signals and their functions.

**Table 8. Expansion Bus Pins**

| PIN | DESCRIPTION |
|---|---|
| EBDMAREQ | Expansion bus DMA request |
| $\overline{\text{EBOE}}$ | Expansion bus pin enable |
| $\overline{\text{EBWR}}$ | Expansion bus write strobe EBWR[1] controls EBDATA[15:8] and EBWR[0] controls EBDATA[7:0] |
| $\overline{\text{EBCS}}$ | Expansion bus chip select |
| EBADDR | Expansion bus address pins |
| EBDATA | Expansion bus data pins |
| $\overline{\text{EBHOLD}}$ | Expansion bus hold: An external device may assert this signal to add wait states to an expansion bus transaction. |

## MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The B1M MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group [event, group1 (G1), and group2 (G2)]. In buffered mode, the MibADC buffers can be serviced by interrupts or by the DMA.

### *MibADC event trigger enhancements*

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group 1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group1 and the event group from the options identified in Table 9.

**Table 9. MibADC Event Hookup Configuration**

| EVENT # | SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] OR EVSRC[1:0]) | SIGNAL PIN NAME |
|---|---|---|
| EVENT1 | 00 | ADEVT |
| EVENT2 | 01 | HET18 |
| EVENT3 | 10 | Reserved |
| EVENT4 | 11 | Reserved |

For group1, these event-triggered selections are configured via the group 1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

### JTAG Interface

There are two main test access ports (TAPs) on the device:

- TMS470R1x CPU TAP
- Device TAP for factory test

Some of the JTAG pins are shared among these two TAPs. The hookup is illustrated in Figure 2.

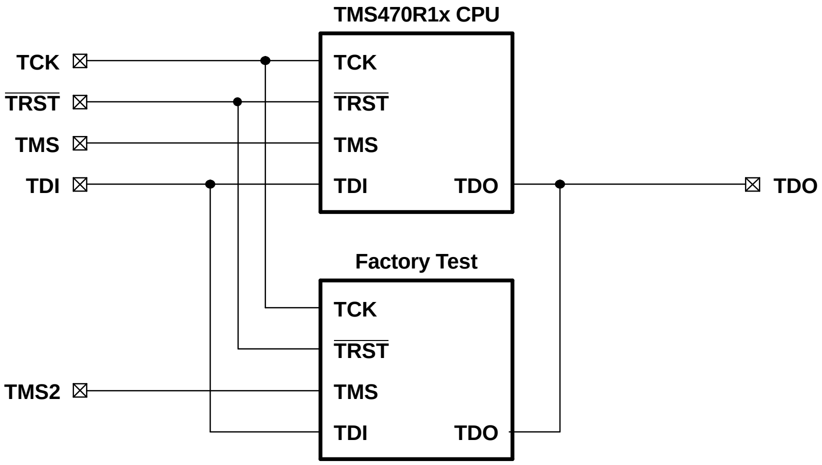


Figure 2. JTAG Interface

### documentation support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include data sheets with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- Bulletin
  - *TMS470 Microcontroller Family Product Bulletin* (literature number SPNB086)
- User's Guides
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x General Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
  - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x MultiBuffered Analog to Digital (MibADC) Reference Guide* (literature number SPNU206)
  - *TMS470R1x Zero Pin Phase Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212)
  - *TMS470R1x Digital Watchdog Timer Reference Guide* (literature number SPNU244)
  - *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Class II Serial Interface A (C2SIa) Reference Guide* (literature number SPNU218)
  - *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222)
  - *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223)
  - *TMS470R1x JTAG Security Module (JSM) Reference Guide* (literature number SPNU245)
  - *TMS470R1x Memory Security Module (MSM) Reference Guide* (literature number SPNU246)
  - *TMS470 Peripherals Overview Reference Guide* (literature number SPNU248)
- Errata Sheet
  - *TMS470R1B1M TMS470 Microcontrollers Silicon Errata* (literature number SPNZ139)

## Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**470R1B1M). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

| | |
|---|---|
| **TMX** | Experimental device that is not necessarily representative of the final device's electrical specifications |
| **TMP** | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification |
| **TMS** | Fully qualified production device |

Support tool development evolutionary flow:

| | |
|---|---|
| **TMDX** | Development-support product that has not yet completed Texas Instruments internal qualification testing. |
| **TMDS** | Fully qualified development-support product |

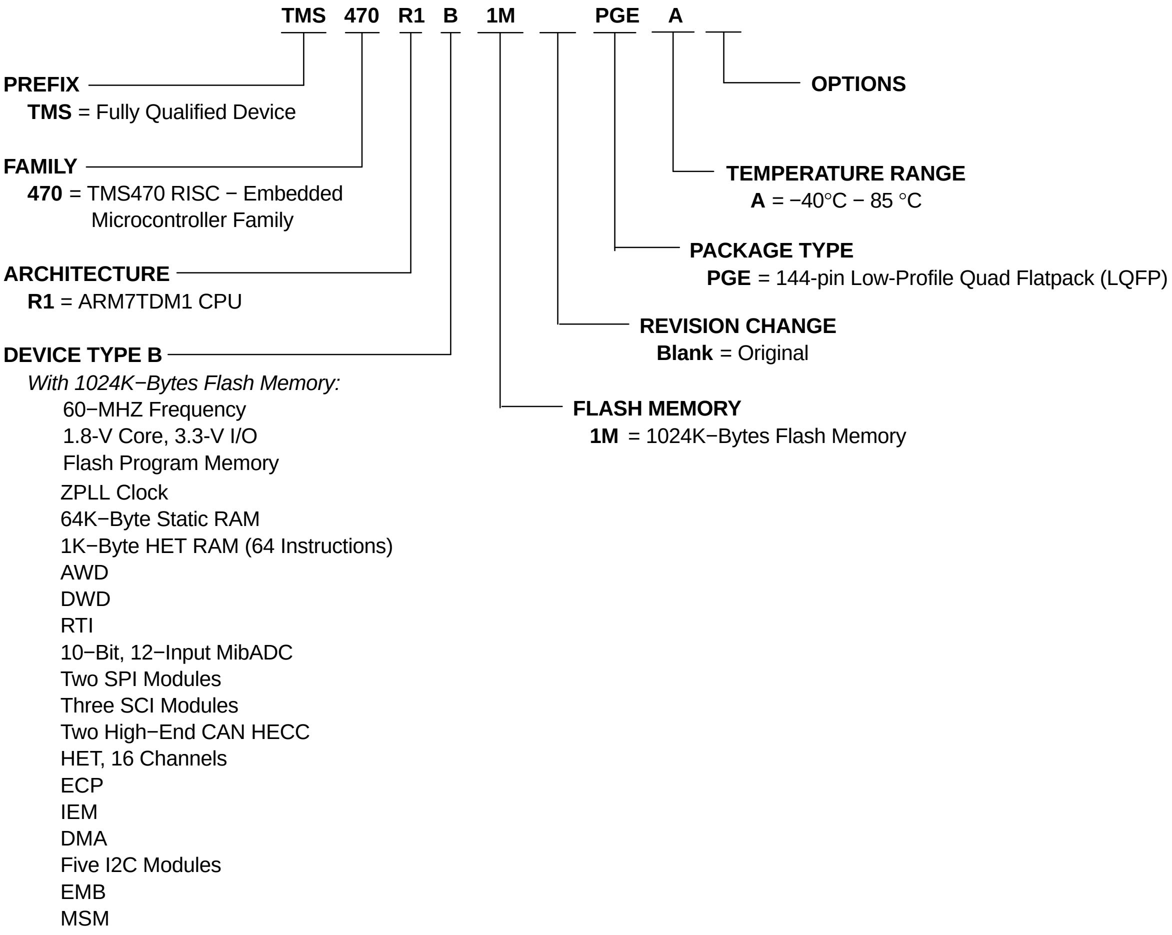
TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Figure 3 illustrates the numbering and symbol nomenclature for the TMS470R1x family.



**TMS 470 R1 B 1M PGE A**

**PREFIX**
**TMS** = Fully Qualified Device

**FAMILY**
**470** = TMS470 RISC − Embedded Microcontroller Family

**ARCHITECTURE**
**R1** = ARM7TDM1 CPU

**DEVICE TYPE B**
*With 1024K−Bytes Flash Memory:*
60−MHZ Frequency
1.8-V Core, 3.3-V I/O
Flash Program Memory
ZPLL Clock
64K−Byte Static RAM
1K−Byte HET RAM (64 Instructions)
AWD
DWD
RTI
10−Bit, 12−Input MibADC
Two SPI Modules
Three SCI Modules
Two High−End CAN HECC
HET, 16 Channels
ECP
IEM
DMA
Five I2C Modules
EMB
MSM

**OPTIONS**

**TEMPERATURE RANGE**
**A** = −40°C − 85 °C

**PACKAGE TYPE**
**PGE** = 144-pin Low-Profile Quad Flatpack (LQFP)

**REVISION CHANGE**
**Blank** = Original

**FLASH MEMORY**
**1M** = 1024K−Bytes Flash Memory

**Figure 3. TMS470R1x Family Nomenclature**

### device identification code register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Table 10). The B1M device identification code register value is 0xnA5F.

**Figure 4. TMS470 Device ID Bit Allocation Register [offset = 0xFFFF_FFF0h]**

<table>
<tr><td>31</td><td>16</td></tr>
<tr><td colspan="2">Reserved</td></tr>
</table>

<table>
<tr><td>15</td><td>12</td><td>11</td><td>10</td><td>9</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VERSION</td><td>TF</td><td>R/F</td><td colspan="2">PART NUMBER</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="2">R-K</td><td>R-K</td><td>R-K</td><td colspan="2">R-K</td><td>R-1</td><td>R-1</td><td>R-1</td></tr>
</table>

LEGEND:
For bits 3-15: R = Read only, -K = Value constant after $\overline{\text{RESET}}$.
For bits 0-2: R = Read only, -1 = Value after $\overline{\text{RESET}}$.

**Table 10. TMS470 Device ID Bit Allocation Register Field Descriptions**

| Bit | Field | Value | Description |
|---|---|---|---|
| 31-16 | Reserved | | Reads are undefined and writes have no effect. |
| 15-12 | VERSION | | Silicon version (revision) bits<br>These bits identify the silicon version of the device. |
| 11 | TF | | Technology family bit<br>This bit distinguishes the technology family core power supply: |
| | | 0 | 3.3 V for F10/C10 devices |
| | | 1 | 1.8 V for F05/C05 devices |
| 10 | R/F | | ROM/flash bit<br>This bit distinguishes between ROM and flash devices: |
| | | 0 | Flash device |
| | | 1 | ROM device |
| 9-3 | PART NUMBER | | Device-specific part number bits<br>These bits identify the assigned device-specific part number. The assigned device-specific part number for the B1M device is 1001011. |
| 2-0 | 1 | | Mandatory High<br>Bits 2, 1, and 0 are tied high by default. |

## DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

### Absolute Maximum Ratings

over operating free-air temperature range, A version (unless otherwise noted)(1)

| | | |
|---|---|---|
| Supply voltage ranges: | $V_{CC}$ (2) | -0.3 V to 2.5 V |
| Supply voltage ranges: | $V_{CCIO}$, $V_{CCAD}$, $V_{CCP}$ (flash pump)(2) | -0.3 V to 4.1 V |
| Input voltage range: | All 5 V tolerant input pins | -0.3 V to 6.0 V |
| | All other input pins | -0.3 V to 4.1 V |
| Input clamp current: | $I_{IK}$ ($V_I < 0$ or $V_I > V_{CCIO}$)<br>All pins except ADIN[0:11], $\overline{\text{PORRST}}$, $\overline{\text{TRST}}$ , TEST, and TCK | ±20 mA |
| | $I_{IK}$ ($V_I < 0$ or $V_I > V_{CCAD}$)<br>ADIN[0:11] | ±10 mA |
| Operating free-air temperature ranges, $T_A$: | A version | -40°C to 85°C |
| Operating junction temperature range, $T_J$: | | -40°C to 150°C |
| Storage temperature range, $T_{stg}$: | | -40°C to 150°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.

### Device Recommended Operating Conditions(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Digital logic supply voltage (Core) | SYSCLK = 48 MHz (pipeline mode enabled) | 1.71 | | 2.05 | V |
| | | SYSCLK = 60 MHz (pipeline mode enabled) | 1.81 | | 2.05 | |
| $V_{CCIO}$ | Digital logic supply voltage (I/O) | | 3 | | 3.6 | V |
| $V_{CCAD}$ | ADC supply voltage | | 3 | | 3.6 | V |
| $V_{CCP}$ | Flash pump supply voltage | | 3 | | 3.6 | V |
| $V_{SS}$ | Digital logic supply ground | | | 0 | | V |
| $V_{SSAD}$ | ADC supply ground(1) | | -0.1 | | 0.1 | V |
| $T_A$ | Operating free-air temperature | A version | -40 | | 85 | ° C |
| $T_J$ | Operating junction temperature | | -40 | | 150 | ° C |

(1) All voltages are with respect to $V_{SS}$, except $V_{CCAD}$, which is with respect to $V_{SSAD}$.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range(1)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Input hysteresis | | | 0.15 | | | V |
| $V_{IL}$ | Low-level input voltage | All inputs(3) | | -0 .3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | All inputs | | 2 | | $V_{CCIO}$ + 0. 3 | V |
| $V_{IH}$ | Input threshold voltage | AWD only(4) | | 1.35 | | 1.8 | V |
| $V_{OL}$ | Low-level output voltage(5) | | $I_{OL} = I_{OL}$ MAX | | | 0.2 $V_{CCIO}$ | V |
| | | | $I_{OL}$ = 50 µA | | | 0.2 | |
| $V_{OH}$ | High-level output voltage(5) | | $I_{OH} = I_{OH}$ MIN | 0.8 $V_{CCIO}$ | | | V |
| | | | $I_{OH}$ = 50 µA | $V_{CCIO}$ - 0.2 | | | |
| $I_{IC}$ | Input clamp current (I/O pins)(6) | | $V_I < V_{SSIO}$ - 0. 3 or $V_I > V_{CCIO}$ + 0. 3 | -2 | | 2 | mA |
| $I_I$ | Input current (3.3 V input pins) | $I_{IL}$ Pulldown | $V_I = V_{SS}$ | -1 | | 1 | µ A |
| | | $I_{IH}$ Pulldown | $V_I = V_{CCIO}$ | 5 | | 40 | |
| | | $I_{IL}$ Pullup | $V_I = V_{SS}$ | -40 | | -5 | |
| | | $I_{IH}$ Pullup | $V_I = V_{CCIO}$ | -1 | | 1 | |
| | | All other pins | No pullup or pulldown | -1 | | 1 | |
| | Input current (5 V tolerant input pins) | | $V_I = V_{SS}$ | -1 | | 1 | µ A |
| | | | $V_I = V_{CCIO}$ | 1 | | 5 | |
| | | | $V_I$ = 5 V | 5 | | 25 | |
| | | | $V_I$ = 5.5 V | 25 | | 50 | |
| $I_{OL}$ | Low-level output current | CLKOUT, AWD, TDI, TDO, TMS, TMS2 | $V_{OL} = V_{OL}$ MAX | | | 8 | mA |
| | | $\overline{RST}$ | | | | 4 | |
| | | All other 3.3 V I/O(7) | | | | 2 | |
| | | 5 V tolerant | | | | 4 | |
| $I_{OH}$ | High-level output current | CLKOUT, TDI, TDO, TMS, TMS2 | $V_{OH} = V_{OH}$ MIN | -8 | | | mA |
| | | $\overline{RST}$ | | -4 | | | |
| | | All other 3.3 V I/O(7) | | -2 | | | |
| | | 5 V tolerant | | -4 | | | |
| $I_{CC}$ | $V_{CC}$ Digital supply current (operating mode) | | SYSCLK = 48 MHz,<br>ICLK = 24 MHz, $V_{CC}$ = 2.05 V | | | 110 | mA |
| | | | SYSCLK = 60 MHz,<br>ICLK = 30 MHz, $V_{CC}$ = 2.05 V | | | 125 | mA |
| | $V_{CC}$ Digital supply current (standby mode)(8)(9) | | OSCIN = 5 MHz, $V_{CC}$ = 2.05 V | | | 1.30 | mA |
| | $V_{CC}$ Digital supply current (halt mode)(8)(9) | | All frequencies, $V_{CC}$ = 2.05 V | | | 700 | µA |

---

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) The typical values indicated in this table are the expected values during operation under normal operating conditions: nominal $V_{CC}$, $V_{CCIO}$, or $V_{CCAD}$, room temperature.
(3) This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the *$\overline{RST}$ and $\overline{PORRST}$ Timings* section.
(4) These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
(5) $V_{OL}$ and $V_{OH}$ are linear with respect to the amount of load current ($I_{OL}/I_{OH}$) applied.
(6) Parameter does not apply to input-only or output-only pins.
(7) Some of the 2 mA buffers on this device are zero-dominant buffers, as indicated by a -z in the Output Current column of the Terminal Functions table. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.
(8) For flash banks/pumps in sleep mode.
(9) For reduced power consumption in low power mode, CANSRX and CANSTX should be driven output LOW.

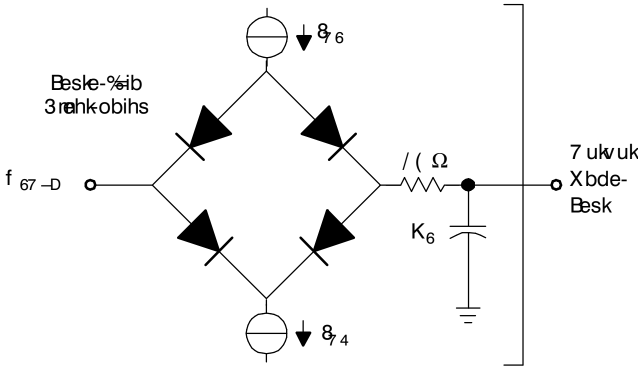
## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CCIO}$ | $V_{CCIO}$ Digital supply current (operating mode) | No DC load, $V_{CCIO}$ = 3.6 V[10] | | | 15 | mA |
| | $V_{CCIO}$ Digital supply current (standby mode)[9] | No DC load, $V_{CCIO}$ = 3.6 V[10] | | | 10 | µA |
| | $V_{CCIO}$ Digital supply current (halt mode)[9] | No DC load, $V_{CCIO}$ = 3.6 V[10] | | | 10 | µ A |
| $I_{CCAD}$ | $V_{CCAD}$ supply current (operating mode) | All frequencies, $V_{CCAD}$ = 3.6 V | | | 15 | mA |
| | $V_{CCAD}$ supply current (standby mode) | All frequencies, $V_{CCAD}$ = 3.6 V | | | 10 | µA |
| | $V_{CCAD}$ supply current (halt mode) | All frequencies, $V_{CCAD}$ = 3.6 V | | | 10 | µA |
| $I_{CCP}$ | $V_{CCP}$ pump supply current | SYSCLK = 48 MHz, $V_{CCP}$ = 3.6 V read operation | | | 45 | mA |
| | | SYSCLK = 60 MHz, $V_{CCP}$ = 3.6 V read operation | | | 55 | mA |
| | | $V_{CCP}$ = 3.6 V program and erase | | | 70 | mA |
| | | $V_{CCP}$ = 3.6 V standby mode operation[8] | | | 10 | µA |
| | | $V_{CCP}$ = 3.6 V halt mode operation[8] | | | 10 | µA |
| $C_I$ | Input capacitance | | | 2 | | pF |
| $C_O$ | Output capacitance | | | 3 | | pF |

(10) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ $V_{CCIO}$ - 0.2 V.

## Parameter Measurement Information



Where: $I_{OL}$ = $I_{OL}$ MAX for the respective pin (A)
$I_{OH}$ = $I_{OH}$ MIN for the respective pin(A)
$V_{LOAD}$ = 1.5 V
$C_L$ = 150-pF typical load-circuit capacitance(B)

A. For these values, see the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.

B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 5. Test Load Circuit

## Timing Parameter Symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| | | | |
|---|---|---|---|
| CM | Compaction, CMPCT | RD | Read |
| CO | CLKOUT | RST | Reset, $\overline{\text{RST}}$ |
| ER | Erase | RX | SCInRX |
| ICLK | Interface clock | S | Slave mode |
| M | Master mode | SCC | SCInCLK |
| OSC, OSCI | OSCIN | SIMO | SPInSIMO |
| OSCO | OSCOUT | SOMI | SPInSOMI |
| P | Program, PROG | SPC | SPInCLK |
| R | Ready | SYS | System clock |
| R0 | Read margin 0, RDMRGN0 | TX | SCInTX |
| R1 | Read margin 1, RDMRGN1 | | |

Lowercase subscripts and their meanings are:

| | | | |
|---|---|---|---|
| a | access time | r | rise time |
| c | cycle time (period) | su | setup time |
| d | delay time | t | transition time |
| f | fall time | v | valid time |
| h | hold time | w | pulse duration (width) |

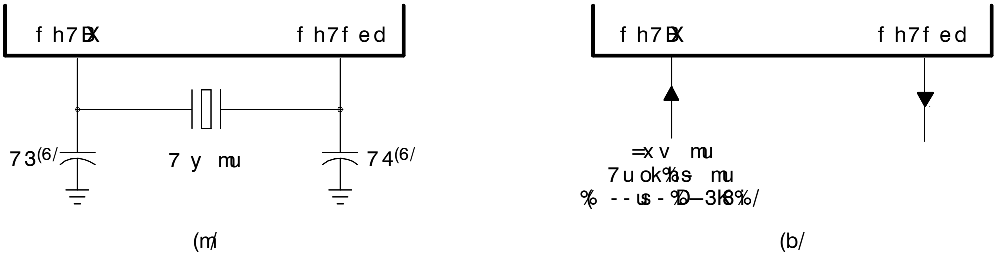
The following additional letters are used with these meanings:

| | | | |
|---|---|---|---|
| H | High | X | Unknown, changing, or don't care level |
| L | Low | Z | High impedance |
| V | Valid | | |

## External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 4–10 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 6a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 6b.



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 6. Crystal/Clock Connection

## ZPLL AND CLOCK SPECIFICATIONS

### Timing Requirements for ZPLL Circuits Enabled or Disabled

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(OSC)}$ | Input clock frequency | 4 | | 10 | MHz |
| $t_{c(OSC)}$ | Cycle time, OSCIN | 100 | | | ns |
| $t_{w(OSCIL)}$ | Pulse duration, OSCIN low | 15 | | | ns |
| $t_{w(OSCIH)}$ | Pulse duration, OSCIN high | 15 | | | ns |
| $f_{(OSCRST)}$ | OSC FAIL frequency(1) | | 53 | | kHz |

(1) Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

### Switching Characteristics over Recommended Operating Conditions for Clocks(1)(2)(3)

| PARAMETER | | TEST CONDITIONS(4) | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(SYS)}$ | System clock frequency(5) | Pipeline mode enabled | | 60(6) | MHz |
| | | Pipeline mode disabled | | 24 | MHz |
| $f_{(CONFIG)}$ | System clock frequency - flash config mode | | | 24 | MHz |
| $f_{(ICLK)}$ | Interface clock frequency | Pipeline mode enabled | | 30 | MHz |
| | | Pipeline mode disabled | | 24 | MHz |
| $f_{(ECLK)}$ | External clock output frequency for ECP module | Pipeline mode enabled | | 30 | MHz |
| | | Pipeline mode disabled | | 24 | MHz |
| $t_{c(SYS)}$ | Cycle time, system clock | Pipeline mode enabled | 16.7 | | ns |
| | | Pipeline mode disabled | 41.6 | | ns |
| $t_{c(CONFIG)}$ | Cycle time, system clock - flash config mode | | 41.6 | | ns |
| $t_{c(ICLK)}$ | Cycle time, interface clock | Pipeline mode enabled | 33.3 | | ns |
| | | Pipeline mode disabled | 41.6 | | ns |
| $t_{c(ECLK)}$ | Cycle time, ECP module external clock output | Pipeline mode enabled | 33.3 | | ns |
| | | Pipeline mode disabled | 41.6 | | ns |

(1) $f_{(SYS)} = M \times f_{(OSC)} / R$, where M = {8}, R = {1,2,3,4,5,6,7,8} when PLLDIS = 0. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL[2:0]) and M is the PLL multiplier determined by the MULT4 bit also in the GLBCTRL register (GLBCTRL.3).
$f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8} when PLLDIS = 1.
$f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.

(2) $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.

(3) Only ZPLL mode is available. FM mode must not be turned on.

(4) Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).

(5) Flash Vread must be set to 5V to achieve maximum system clock frequency.

(6) Operating $V_{CC}$ range for this system clock frequency is 1.81 to 2.05 V.

## Switching Characteristics over Recommended Operating Conditions for External Clocks(1)(2)(3)

(see Figure 7 and Figure 8)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(COL)}$ | Pulse duration, CLKOUT low | SYSCLK or MCLK(4) | $0.5t_{c(SYS)} - t_f$ | | ns |
| | | ICLK: X is even or 1(5) | $0.5t_{c(ICLK)} - t_f$ | | |
| | | ICLK: X is odd and not 1(5) | $0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$ | | |
| $t_{w(COH)}$ | Pulse duration, CLKOUT high | SYSCLK or MCLK(4) | $0.5t_{c(SYS)} - t_r$ | | ns |
| | | ICLK: X is even or 1(5) | $0.5t_{c(ICLK)} - t_r$ | | |
| | | ICLK: X is odd and not 1(5) | $0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$ | | |
| $t_{w(EOL)}$ | Pulse duration, ECLK low | N is even and X is even or odd | $0.5t_{c(ECLK)} - t_f$ | | ns |
| | | N is odd and X is even | $0.5t_{c(ECLK)} - t_f$ | | |
| | | N is odd and X is odd and not 1 | $0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$ | | |
| $t_{w(EOH)}$ | Pulse duration, ECLK high | N is even and X is even or odd | $0.5t_{c(ECLK)} - t_r$ | | ns |
| | | N is odd and X is even | $0.5t_{c(ECLK)} - t_r$ | | |
| | | N is odd and X is odd and not 1 | $0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$ | | |

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
(4) Clock source bits are selected as either SYSCLK (CLKCNTL[6:5] = 11 binary) or MCLK (CLKCNTL[6:5] = 10 binary).
(5) Clock source bits are selected as ICLK (CLKCNTL[6:5] = 01 binary).

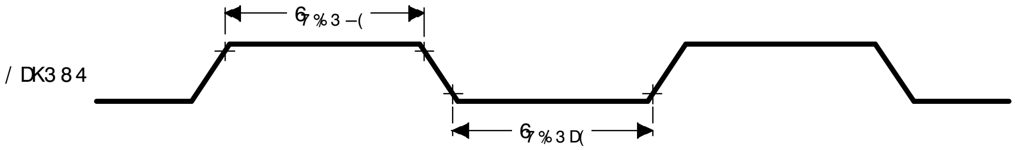


Figure 7. CLKOUT Timing Diagram

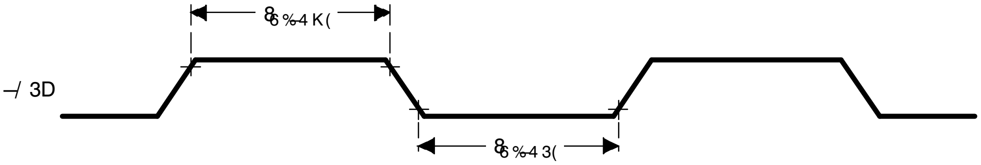


Figure 8. ECLK Timing Diagram

## $\overline{\text{RST}}$ AND $\overline{\text{PORRST}}$ TIMINGS

### Timing Requirements for $\overline{\text{PORRST}}$

(see Figure 9)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CCPORL}$ | $V_{CC}$ low supply level when $\overline{\text{PORRST}}$ must be active during power up | | 0.6 | V |
| $V_{CCPORH}$ | $V_{CC}$ high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down | 1.5 | | V |
| $V_{CCIOPORL}$ | $V_{CCIO}$ low supply level when $\overline{\text{PORRST}}$ must be active during power up | | 1.1 | V |
| $V_{CCIOPORH}$ | $V_{CCIO}$ high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down | 2.75 | | V |
| $V_{IL}$ | Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$ | | 0.2 $V_{CCIO}$ | V |
| $V_{IL(PORRST)}$ | Low-level input voltage of $\overline{\text{PORRST}}$ before V CCIO > $V_{CCIOPORL}$ | | 0.5 | V |
| $t_{su(PORRST)r}$ | Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up | 0 | | ms |
| $t_{su(VCCIO)r}$ | Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$ | 0 | | ms |
| $t_{h(PORRST)r}$ | Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$ | 1 | | ms |
| $t_{su(PORRST)f}$ | Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down | 8 | | µs |
| $t_{h(PORRST)rio}$ | Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCIOPORH}$ | 1 | | ms |
| $t_{h(PORRST)d}$ | Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$ | 0 | | ms |
| $t_{su(PORRST)fio}$ | Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCIOPORH}$ during power down | 0 | | ns |
| $t_{su(VCCIO)f}$ | Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$ | 0 | | ns |

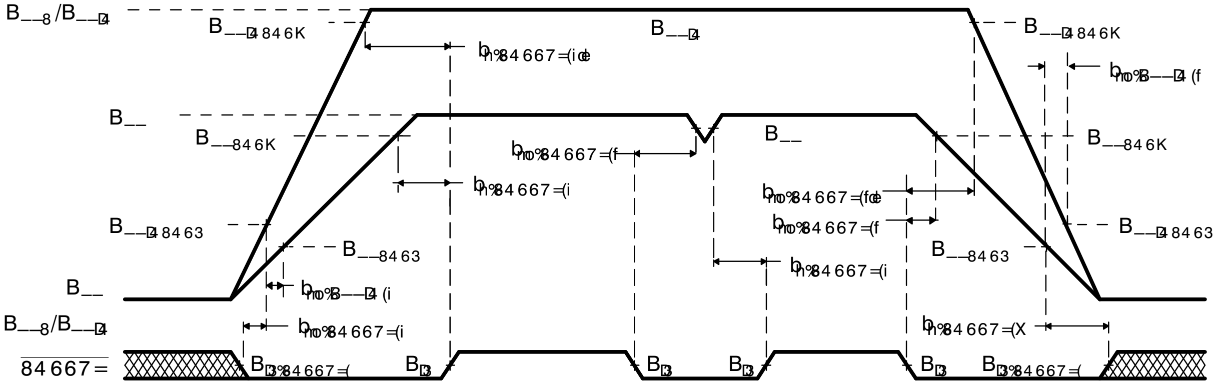


Figure 9. $\overline{\text{PORRST}}$ Timing Diagram

### Switching Characteristics over Recommended Operating Conditions for $\overline{\text{RST}}$[(1)]

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{v(RST)}$ | Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive | $4112t_{c(OSC)}$ | | ns |
| | Valid time, $\overline{\text{RST}}$ active (all others) | $8t_{c(SYS)}$ | | |
| $t_{fsu}$ | Flash start up time, from $\overline{\text{RST}}$ inactive to fetch of first instruction from flash (flash pump stabilization time) | $836t_{c(OSC)}$ | | ns |

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

## JTAG SCAN INTERFACE TIMING (JTAG CLOCK SPECIFICATION 10-MHz AND 50-pF LOAD ON TDO OUTPUT)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(JTAG)}$ | Cycle time, JTAG low and high period | 50 | | ns |
| $t_{su(TDI/TMS - TCKr)}$ | Setup time, TDI, TMS before TCK rise (TCKr) | 15 | | ns |
| $t_{h(TCKr -TDI/TMS)}$ | Hold time, TDI, TMS after TCKr | 15 | | ns |
| $t_{h(TCKf -TDO)}$ | Hold time, TDO after TCKf | 10 | | ns |
| $t_{d(TCKf -TDO)}$ | Delay time, TDO valid after TCK fall (TCKf) | | 45 | ns |

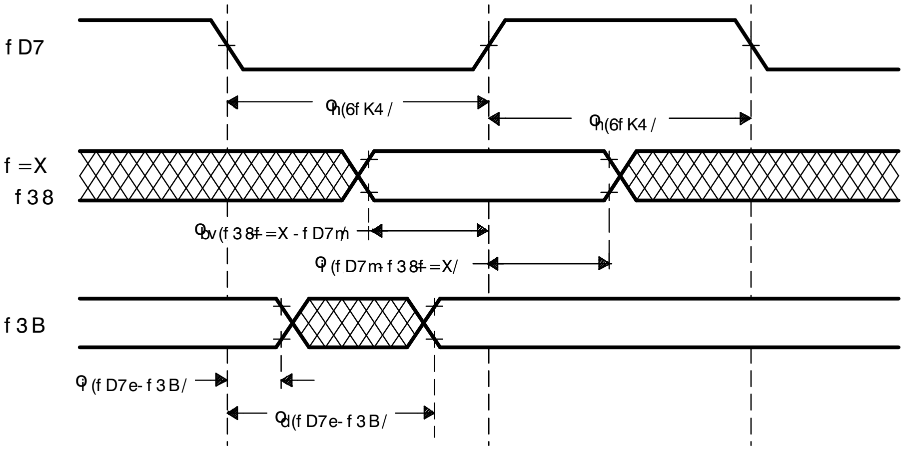


Figure 10. JTAG Scan Timings

## OUTPUT TIMINGS

### Switching Characteristics for Output Timings versus Load Capacitance ($C_L$)

(see Figure 11)

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_r$ | Rise time, AWD, CLKOUT, $\overline{\text{TDI, TDO, TMS, TMS2}}$ | $C_L$ = 15 pF | 0.5 | 2.5 | ns |
| | | $C_L$ = 50 pF | 1.5 | 5.0 | |
| | | $C_L$ = 100 pF | 3.0 | 9.0 | |
| | | $C_L$ = 150 pF | 4.5 | 12.5 | |
| $t_f$ | Fall time, AWD, CLKOUT, $\overline{\text{TDI, TDO, TMS, TMS2}}$ | $C_L$ = 15 pF | 0.5 | 2.5 | ns |
| | | $C_L$ = 50 pF | 1.5 | 5.0 | |
| | | $C_L$ = 100 pF | 3.0 | 9.0 | |
| | | $C_L$ = 150 pF | 4.5 | 12.5 | |
| $t_r$ | Rise time, $\overline{\text{RST}}$ | $C_L$ = 15 pF | 2.5 | 8 | ns |
| | | $C_L$ = 50 pF | 5 | 14 | |
| | | $C_L$ = 100 pF | 9 | 23 | |
| | | $C_L$ = 150 pF | 13 | 32 | |
| $t_r$ | Rise time, 4mA, 5 V tolerant pins | $C_L$ = 15 pF | 3 | 10 | ns |
| | | $C_L$ = 50 pF | 3.5 | 12 | |
| | | $C_L$ = 100 pF | 7 | 21 | |
| | | $C_L$ = 150 pF | 9 | 28 | |
| | | $C_L$ = 400 pF | 18 | 40 | |
| $t_f$ | Fall time, 4mA, 5 V tolerant pins | $C_L$ = 15 pF | 2 | 8 | ns |
| | | $C_L$ = 50 pF | 2.5 | 9 | |
| | | $C_L$ = 100 pF | 8 | 25 | |
| | | $C_L$ = 150 pF | 11 | 35 | |
| | | $C_L$ = 400 pF | 20 | 45 | |
| $t_r$ | Rise time, all other output pins | $C_L$ = 15 pF | 2.5 | 10 | ns |
| | | $C_L$ = 50 pF | 6.0 | 25 | |
| | | $C_L$ = 100 pF | 12 | 45 | |
| | | $C_L$ = 150 pF | 18 | 65 | |
| $t_f$ | Fall time, all other output pins | $C_L$ = 15 pF | 3 | 10 | ns |
| | | $C_L$ = 50 pF | 8.5 | 25 | |
| | | $C_L$ = 100 pF | 16 | 45 | |
| | | $C_L$ = 150 pF | 23 | 65 | |

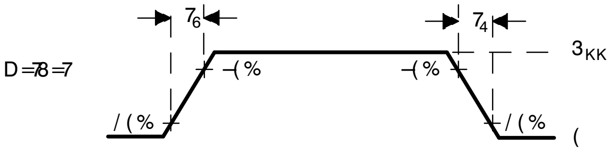


Figure 11. CMOS-Level Outputs

## INPUT TIMINGS

### Timing Requirements for Input Timings[1]

(see Figure 12)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{pw}$ | Input minimum pulse width | $t_{c(ICLK)}$ + 10 | | ns |

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$

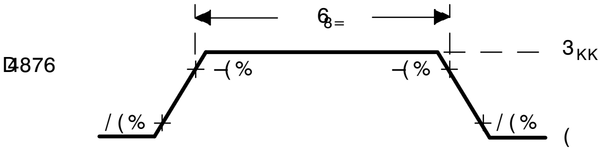


Figure 12. CMOS-Level Inputs

## FLASH TIMINGS

### Timing Requirements for Program Flash[1]

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{prog(16\text{-}bit)}$ | Half word (16-bit) programming time | 4 | 16 | 200 | µs |
| $t_{prog(Total)}$ | 1M-byte programming time[2] | | 8 | 32 | s |
| $t_{erase(sector)}$ | Sector erase time | | 7 | | s |
| $t_{wec}$ | Write/erase cycles at $T_A$ = 85°C | 100 | 1000 | | cycles |
| $t_{fp(\overline{RST})}$ | Flash pump settling time from $\overline{\text{RST}}$ to SLEEP | | $167t_{c(SYS)}$ | | ns |
| $t_{fp(SLEEP)}$ | Initial flash pump settling time from SLEEP to STANDBY | | $167t_{c(SYS)}$ | | ns |
| $t_{fp(STANDBY)}$ | Initial flash pump settling time from STANDBY to ACTIVE | | $84t_{c(SYS)}$ | | ns |

(1) For more detailed information on the flash core sectors, see the *flash program and erase* section of this data sheet.
(2) The 1M-byte programming time includes overhead of state machine.

## SPIn MASTER MODE TIMING PARAMETERS

### SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)[1][2][3] (see Figure 13)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK[4] | 100 | $256t_{c(ICLK)}$ | ns |
| 2[5] | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3[5] | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4[5] | $t_{d(SPCH-SIMO)M}$ | Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0) | | 10 | |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1) | | 10 | |
| 5[5] | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | $t_{c(SPC)M} - 5 - t_f$ | | |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | $t_{c(SPC)M} - 5 - t_r$ | | |
| 6[5] | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 0) | 6 | | |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 1) | 6 | | |
| 7[5] | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0) | 4 | | |
| | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1) | 4 | | |

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

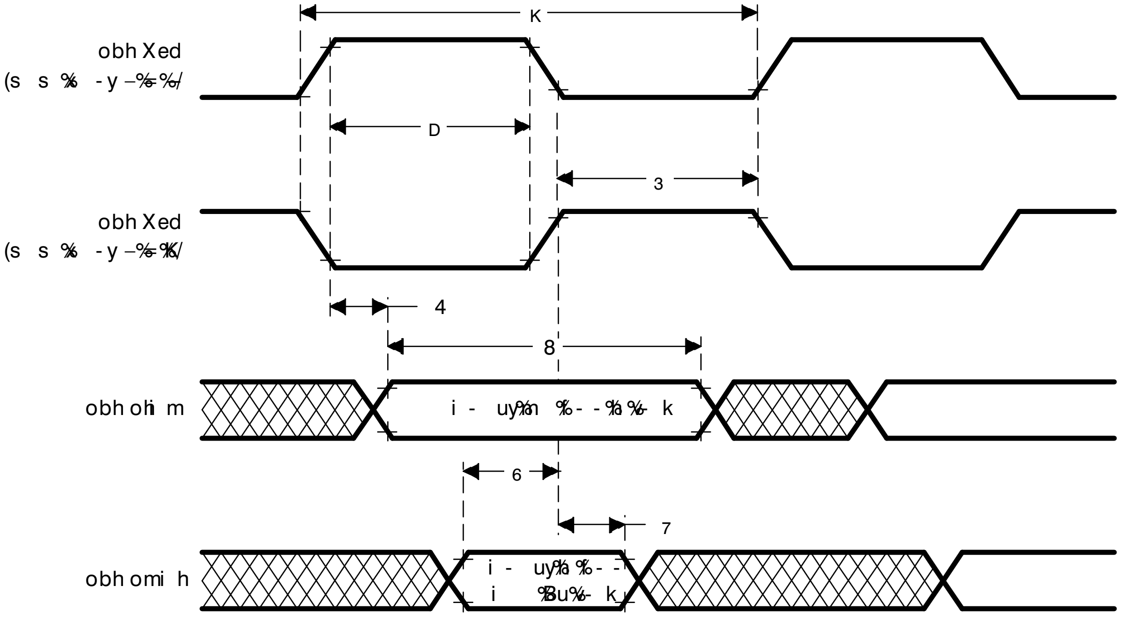


Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 0)

## SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 14)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK(4) | 100 | $256t_{c(ICLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4(5) | $t_{v(SIMO-SPCH)M}$ | Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | |
| | $t_{v(SIMO-SPCL)M}$ | Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | |
| 5(5) | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 5 - t_r$ | | |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 5 - t_f$ | | |
| 6(5) | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 1) | 6 | | |
| 7(5) | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | 4 | | |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | 4 | | |

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

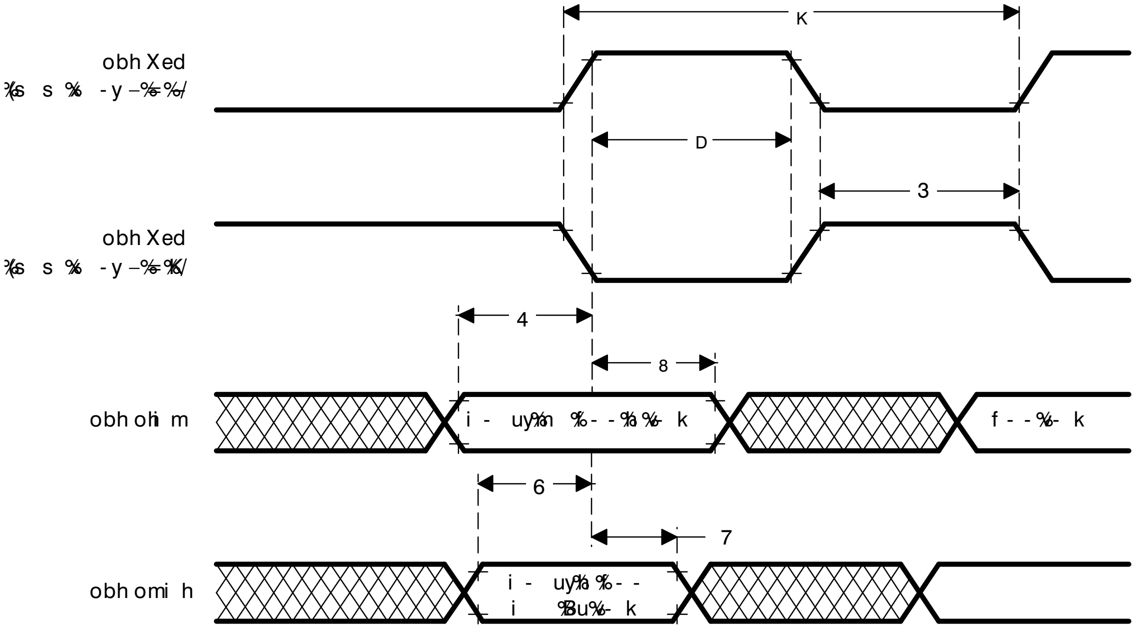


Figure 14. SPIn Master Mode External Timing (CLOCK PHASE = 1)

## SPIn SLAVE MODE TIMING PARAMETERS

### SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 15)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPInCLK(5) | 100 | $256t_{c(ICLK)}$ | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| 4(6) | $t_{d(SPCH-SOMI)S}$ | Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0) | | $6 + t_r$ | |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1) | | $6 + t_f$ | |
| 5(6) | $t_{v(SPCH-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $t_{c(SPC)S} - 6 - t_r$ | | |
| | $t_{v(SPCL-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $t_{c(SPC)S} - 6 - t_f$ | | |
| 6(6) | $t_{su(SIMO-SPCL)S}$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 0) | 6 | | |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 1) | 6 | | |
| 7(6) | $t_{v(SPCL-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | 6 | | |
| | $t_{v(SPCH-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | 6 | | |

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\, t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1) t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

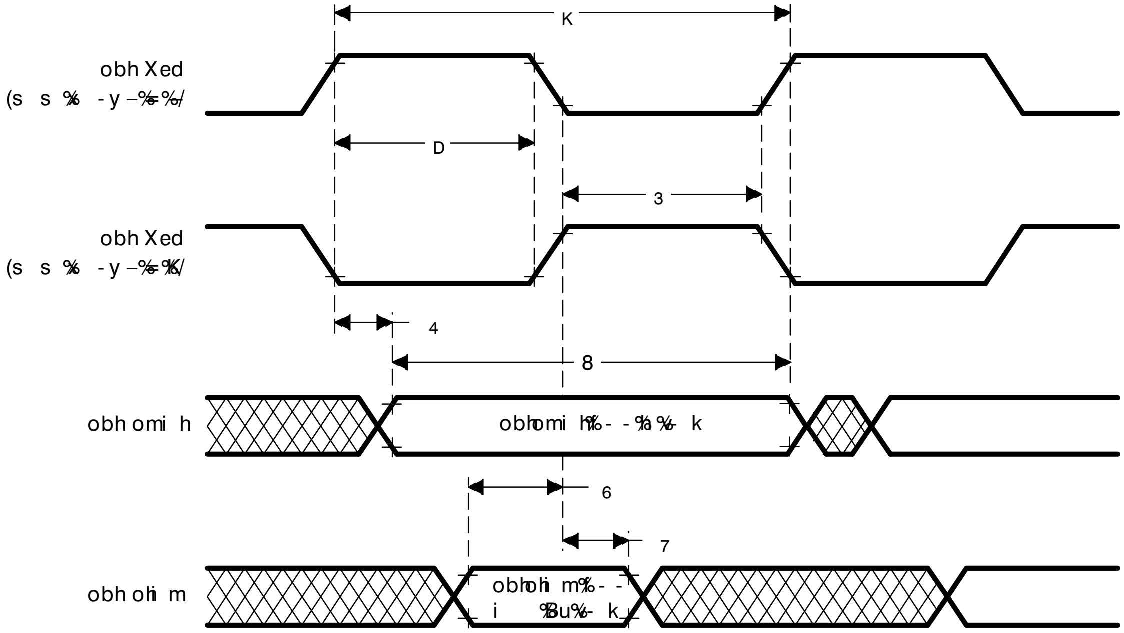


**Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 0)**

## SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 16)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPInCLK(5) | 100 | $256t_{c(ICLK)}$ | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$ | |
| 4(6) | $t_{v(SOMI\text{-}SPCH)S}$ | Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0) | $0.5t_{c(SPC)S} - 6 - t_r$ | | |
| | $t_{v(SOMI\text{-}SPCL)S}$ | Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1) | $0.5t_{c(SPC)S} - 6 - t_f$ | | |
| 5(6) | $t_{v(SPCH\text{-}SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)S} - 6 - t_r$ | | |
| | $t_{v(SPCL\text{-}SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)S} - 6 - t_f$ | | |
| 6(6) | $t_{su(SIMO\text{-}SPCH)}S$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{su(SIMO\text{-}SPCL)}S$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 1) | 6 | | |
| 7(6) | $t_{v(SPCH\text{-}SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{v(SPCL\text{-}SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | 6 | | |

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2.1).

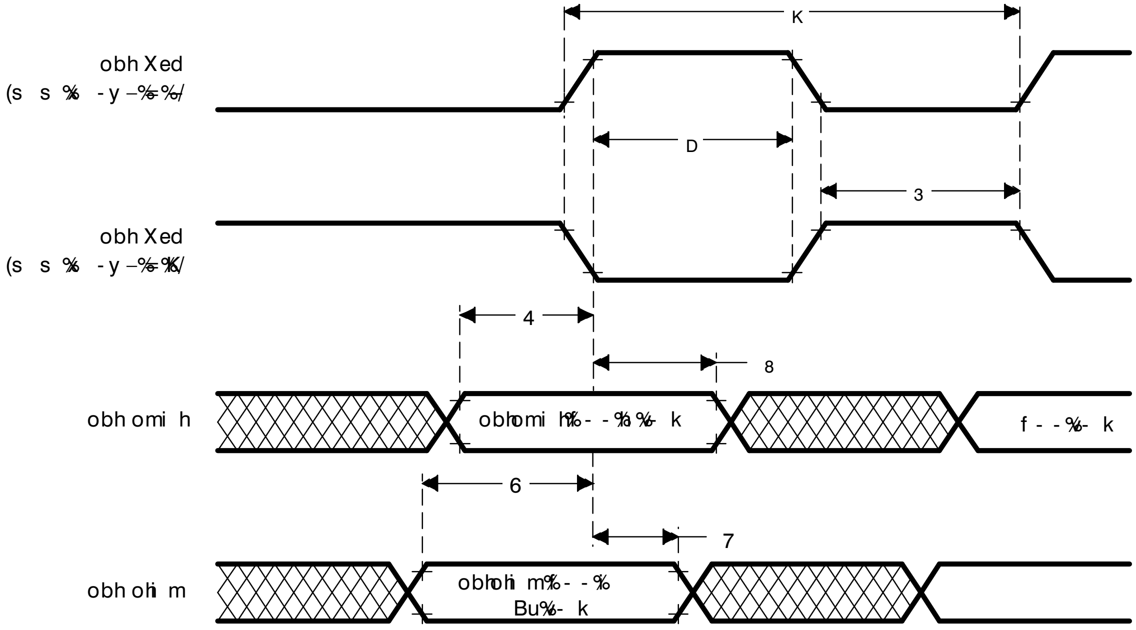


Figure 16. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

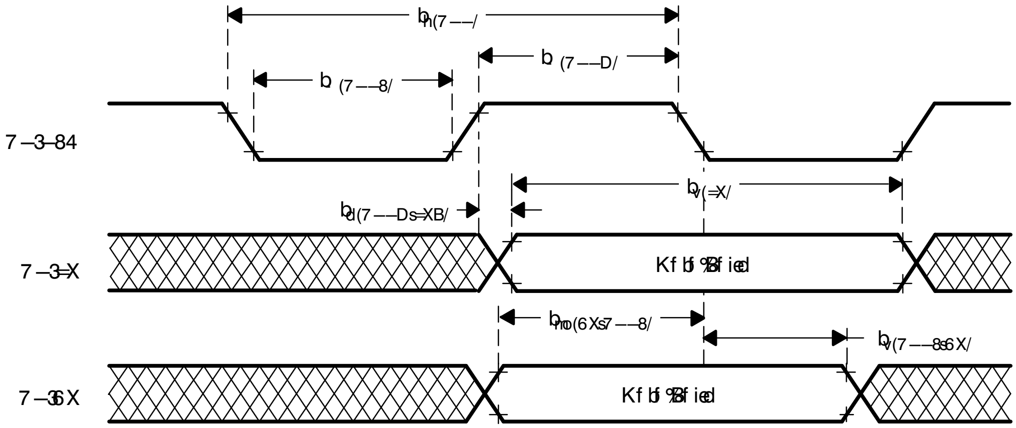
## SCIn ISOSYNCHRONOUS MODE TIMINGS - INTERNAL CLOCK

### Timing Requirements for Internal Clock SCIn Isosynchronous Mode(1)(2)(3)

(see Figure 17)

| | | (BAUD + 1) IS EVEN OR BAUD = 0 | | (BAUD + 1) IS ODD AND BAUD ≠ 0 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCC)}$ | Cycle time, SCInCLK | $2t_{c(ICLK)}$ | $2^{24}\ t_{c(ICLK)}$ | $3t_{c(ICLK)}$ | $(2^{24}\ -1)\ t_{c(ICLK)}$ | ns |
| $t_{w(SCCL)}$ | Pulse duration, SCInCLK low | $0.5t_{c(SCC)} - t_f$ | $0.5t_{c(SCC)} + 5$ | $0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$ | $0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$ | ns |
| $t_{w(SCCH)}$ | Pulse duration, SCInCLK high | $0.5t_{c(SCC)} - t_r$ | $0.5t_{c(SCC)} + 5$ | $0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$ | $0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$ | ns |
| $t_{d(SCCH-TXV)}$ | Delay time, SCInCLK high to SCInTX valid | | 10 | | 10 | ns |
| $t_{v(TX)}$ | Valid time, SCInTX data after SCInCLK low | $t_{c(SCC)} - 10$ | | $t_{c(SCC)} - 10$ | | ns |
| $t_{su(RX-SCCL)}$ | Setup time, SCInRX before SCInCLK low | $t_{c(ICLK)} + t_f + 20$ | | $t_{c(ICLK)} + t_f + 20$ | | ns |
| $t_{v(SCCL-RX)}$ | Valid time, SCInRX data after SCInCLK low | $- t_{c(ICLK)} + t_f + 20$ | | $- t_{c(ICLK)} + t_f + 20$ | | ns |

(1) BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(3) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.



A. Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

**Figure 17. SCIn Isosynchronous Mode Timing Diagram for Internal Clock**

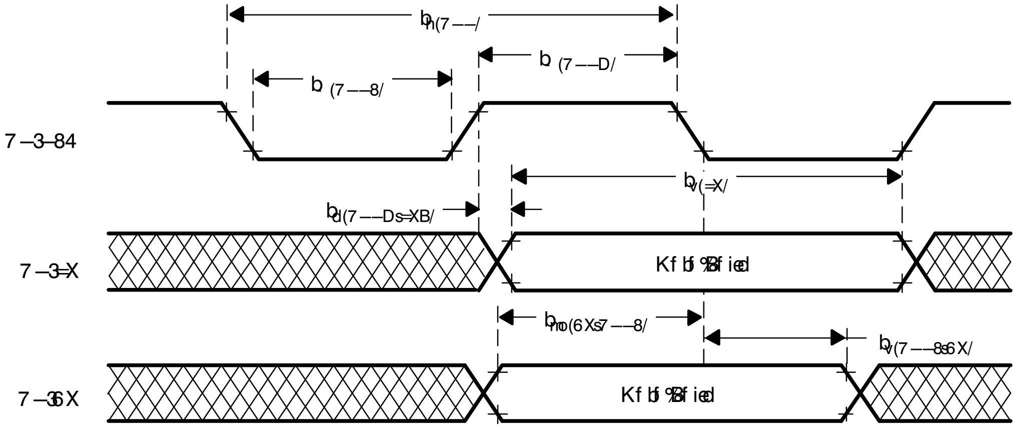
## SCIn ISOSYNCHRONOUS MODE TIMINGS - EXTERNAL CLOCK

### Timing Requirements for External Clock SCIn Isosynchronous Mode(1)(2)

(see Figure 18)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(SCC)}$ | Cycle time, SCInCLK(3) | $8t_{c(ICLK)}$ | | ns |
| $t_{w(SCCH)}$ | Pulse duration, SCInCLK high | $0.5t_{c(SCC)}$ - $0.25t_{c(ICLK)}$ | $0.5t_{c(SCC)}$ + $0.25t_{c(ICLK)}$ | ns |
| $t_{w(SCCL)}$ | Pulse duration, SCInCLK low | $0.5t_{c(SCC)}$ - $0.25t_{c(ICLK)}$ | $0.5t_{c(SCC)}$ + $0.25t_{c(ICLK)}$ | ns |
| $t_{d(SCCH-TXV)}$ | Delay time, SCInCLK high to SCInTX valid | | $2t_{c(ICLK)}$ + 12 + $t_r$ | ns |
| $t_{v(TX)}$ | Valid time, SCInTX data after SCInCLK low | $2t_{c(SCC)}$ -10 | | ns |
| $t_{su(RX-SCCL)}$ | Setup time, SCInRX before SCInCLK low | 0 | | ns |
| $t_{v(SCCL-RX)}$ | Valid time, SCInRX data after SCInCLK low | $2t_{c(ICLK)}$ + 10 | | ns |

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(2) For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
(3) When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$.



A. Data transmission / reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 18. SCIn Isosynchronous Mode Timing Diagram for External Clock

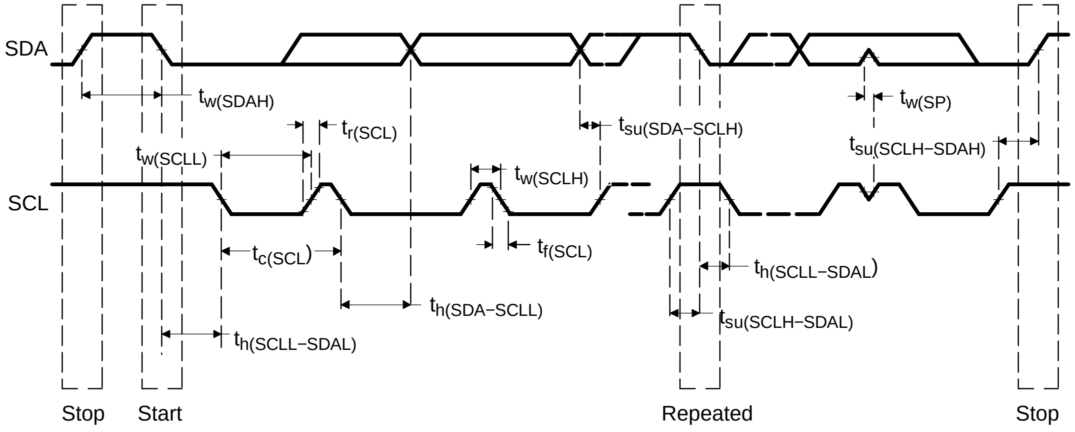
## I2C TIMING

Table 11 assumes testing over recommended operating conditions.

### I2C Signals (SDA and SCL) Switching Characteristics[(1)]

| PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(I2CCLK)}$ | Cycle time, I2C module clock | 75 | 150 | 75 | 150 | ns |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a repeated START condition) | 4 | | 0.6 | | µs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low<br>For I2C bus devices | 0 | 3.45[(2)] | 0 | 0.9 | µs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20+0.1C_b$[(3)] | 300 | ns |
| $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20+0.1C_b$[(3)] | 300 | ns |
| $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20+0.1C_b$[(3)] | 300 | ns |
| $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20+0.1C_b$[(3)] | 300 | ns |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4.0 | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b$[(3)] | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices needs to be met only if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) C $_b$ = The total capacitance of one bus line in pF. If mixed with HS=mode devices, faster fall-times are allowed.



A. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

B. The maximum $t_{h(SDA-SCLL)}$ needs only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.

C. A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$.

D. $C_b$ = total capacitance of one bus line in pF. If mixed with HS=mode devices, faster fall-times are allowed.

**Figure 19. I2C Timings**

## STANDARD CAN CONTROLLER (SCC) MODE TIMINGS

### Dynamic Characteristics for the CANSTX and CANSRX Pins

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_d$(CANSTX) | Delay time, transmit shift register to CANSTX pin[1] | | 15 | ns |
| $t_d$(CANSRX) | Delay time, CANSRX pin to receive shift register | | 5 | ns |

(1) These values do not include the rise/fall times of the output buffer.

## EXPANSION BUS MODULE TIMING

### Expansion Bus Timing Parameters, -40°C ≤ $T_J$ ≤ 150°C, 3.0 V ≤ $V_{CC}$ ≤ 3.6 V

(see Figure 20 and Figure 21)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(CO)}$ | Cycle time, CLKOUT | 20.8 | | ns |
| $t_{d(COH\text{-}EBADV)}$ | Delay time, CLKOUT high to EBADDR valid | | 21.4 | ns |
| $t_{h(COH\text{-}EBADIV)}$ | Hold time, EBADDR invalid after CLKOUT high | | 12.4 | ns |
| $t_{d(COH\text{-}EBOE)}$ | Delay time, CLKOUT high to $\overline{\text{EBOE}}$ fall | | 11.4 | ns |
| $t_{h(COH\text{-}EBOEH)}$ | Hold time, $\overline{\text{EBOE}}$ rise after CLKOUT high | | 11.4 | ns |
| $t_{d(COL\text{-}EBWR)}$ | Delay time, CLKOUT low to write strobe ($\overline{\text{EBWR}}$) low | | 11.3 | ns |
| $t_{h(COL\text{-}EBWRH)}$ | Hold time, $\overline{\text{EBWR}}$ high after CLKOUT low | | 11.6 | ns |
| $t_{su(EBRDATV\text{-}COH)}$ | Setup time, EBDATA valid before CLKOUT high (READ)(1) | 15.2 | | ns |
| $t_{h(COH\text{-}EBRDATIV)}$ | Hold time, EBDATA invalid after CLKOUT high (READ) | | (-14.7) | ns |
| $t_{d(COL\text{-}EBWDATV)}$ | Delay time, CLKOUT low to EBDATA valid (WRITE)(2) | | 16.1 | ns |
| $t_{h(COL\text{-}EBWDATIV)}$ | Hold time, EBDATA invalid after CLKOUT low (WRITE) | | 14.7 | ns |
| **SECONDARY TIMES** | | | | |
| $t_{d(COH\text{-}EBCS0)}$ | Delay, CLKOUT high to $\overline{\text{EBCS0}}$ fall | | 13.6 | ns |
| $t_{h(COH\text{-}EBCS0H)}$ | Hold, $\overline{\text{EBCS0}}$ rise after CLKOUT high | | 13.2 | ns |
| $t_{su(COH\text{-}EBHOLDL)}$ | Setup time, $\overline{\text{EBHOLD}}$ low to CLKOUT high(1) | 10.9 | | ns |
| $t_{su(COH\text{-}EBHOLDH)}$ | Setup time, $\overline{\text{EBHOLD}}$ high to CLKOUT high(1) | 10.5 | | ns |

(1) Setup time is the minimum time under worst case conditions. Data with less setup time will not work.
(2) Valid after CLKOUT goes low for write cycles.

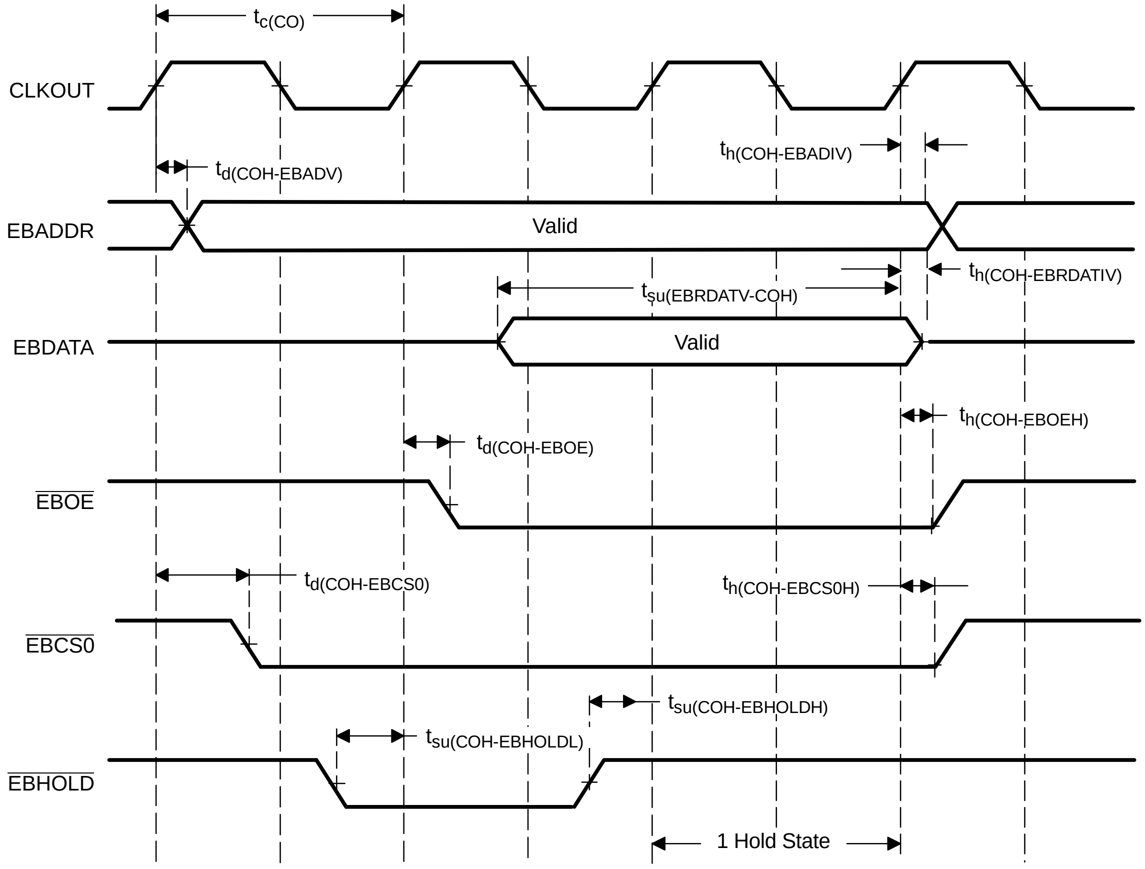


Figure 20. Expansion Memory Signal Timing - Reads

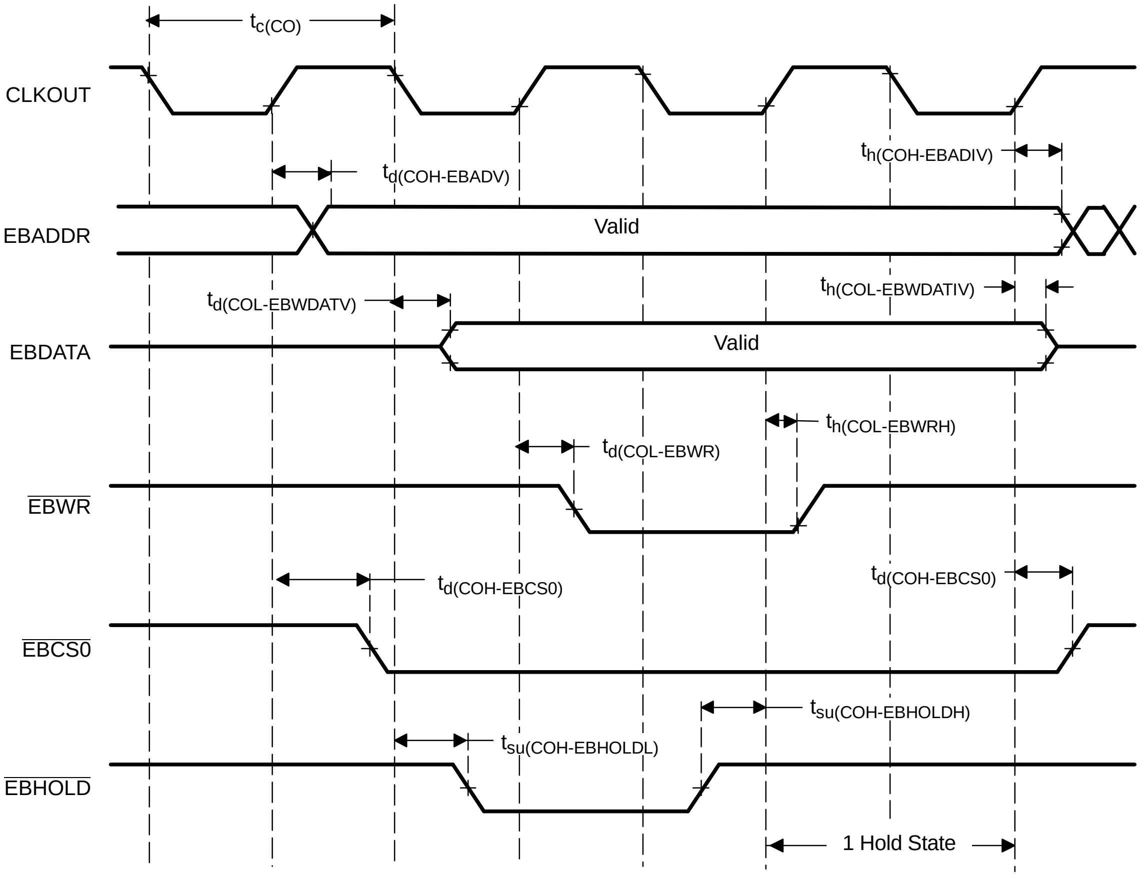


**Figure 21. Expansion Memory Signal Timing - Writes**

## HIGH-END TIMER (HET) TIMINGS

### Minimum PWM Output Pulse Width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr), which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

### Minimum Input Pulses that Can Be Captured:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

**NOTE:**

> Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

## MULTI-BUFFERED A-TO-D CONVERTER (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry, which could be present on V SS and V CC , from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD REFLO unless otherwise noted.

| | |
|---|---|
| Resolution | 10 bits (1024 values) |
| Monotonic | Assured |
| Output conversion code | 00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$ ; 3FF for $V_{AI} \geq AD_{REFHI}$ ] |

### Table 17. MibADC Recommended Operating Conditions(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $AD_{REFHI}$ | A-to-D high-voltage reference source | $V_{SSAD}$ | $V_{CCAD}$ | V |
| $AD_{REFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ | $V_{CCAD}$ | V |
| $V_{AI}$ | Analog input voltage | $V_{SSAD}$ - 0.3 | $V_{CCAD}$ + 0.3 | V |
| $I_{AIC}$ | Analog input clamp current(2)<br>($V_{AI} < V_{SSAD}$ - 0.3 or $V_{AI} > V_{CCAD}$ + 0.3) | -2 | 2 | mA |

(1) For $V_{CCAD}$ and $V_{SSAD}$ recommended operating conditions, see the "Device Recommended Operating Conditions" table.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

### Table 18. Operating Characteristics over Full Ranges of Recommended Operating Conditions(1)(2)

| PARAMETER | | DESCRIPTION/CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $R_i$ | Analog input resistance | See Figure 22. | | | 250 | 500 | Ω |
| $C_i$ | Analog input capacitance | See Figure 22. | Conversion | | | 10 | pF |
| | | | Sampling | | | 30 | pF |
| $I_{AIL}$ | Analog input leakage current | See Figure 22. | | -1 | | 1 | μA |
| $I_{ADREFHI}$ | $AD_{REFHI}$ input current | $AD_{REFHI}$ = 3.6 V, $AD_{REFLO} = V_{SSAD}$ | | | | 5 | mA |
| CR | Conversion range over which specified accuracy is maintained | $AD_{REFHI}$ - $AD_{REFLO}$ | | 3 | | 3.6 | V |
| $E_{DNL}$ | Differential nonlinearity error | Difference between the actual step width and the ideal value. See Figure 23. | | | | ± 1.5 | LSB |
| $E_{INL}$ | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. See Figure 24. | | | | ± 2 | LSB |
| $E_{TOT}$ | Total error/Absolute accuracy | Maximum value of the difference between an analog value and the ideal midstep value. See Figure 25. | | | | ± 2 | LSB |

(1) $V_{CCAD} = AD_{REFHI}$
(2) 1 LSB = $(AD_{REFHI} - AD_{REFLO})/ 2^{10}$ for the MibADC

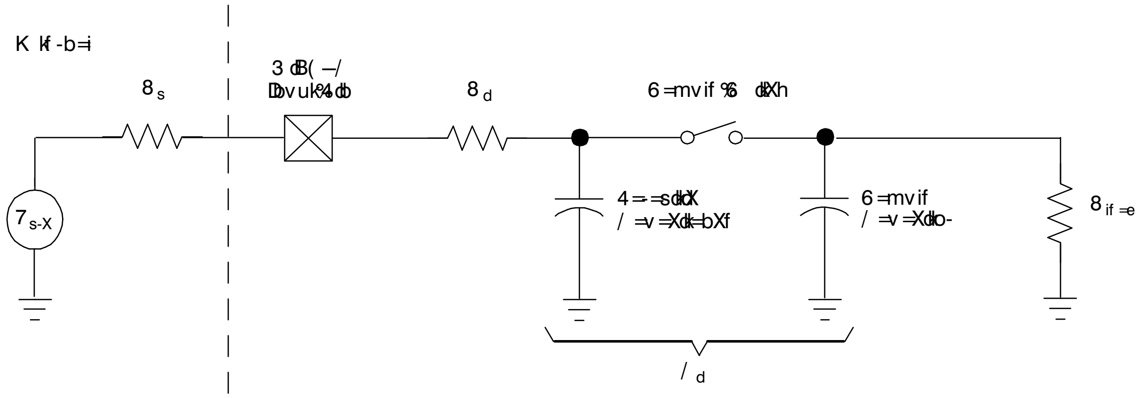


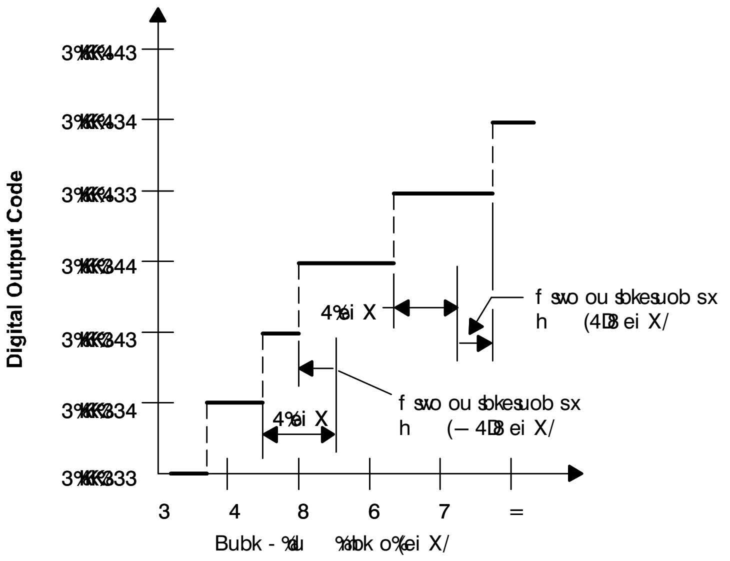
Figure 22. MibADC Input Equivalent Circuit

### Table 19. Multi-Buffer ADC Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(ADCLK)}$ | Cycle time, MibADC clock | 0.05 | | | µs |
| $t_{d(SH)}$ | Delay time, sample and hold time | 1 | | | µs |
| $t_{d(C)}$ | Delay time, conversion time | 0.55 | | | µs |
| $t_{d(SHC)}$ (1) | Delay time, total sample/hold and conversion time | 1.55 | | | µs |

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

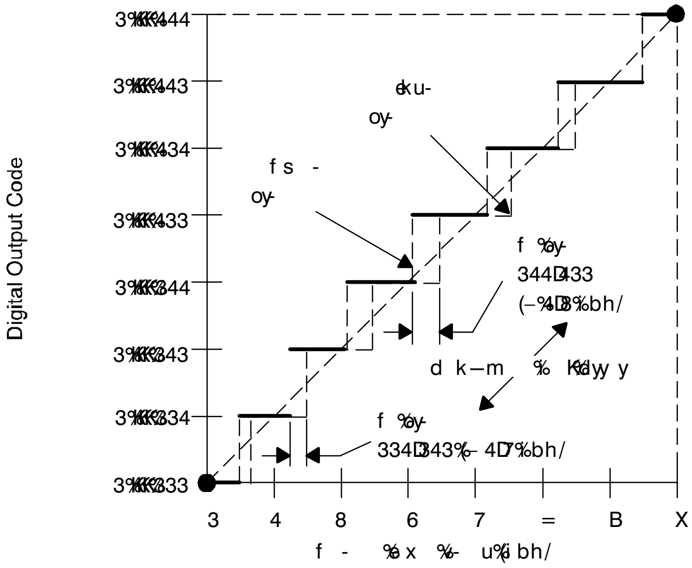
The differential nonlinearity error shown in Figure 23 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 23. Differential Nonlinearity (DNL)

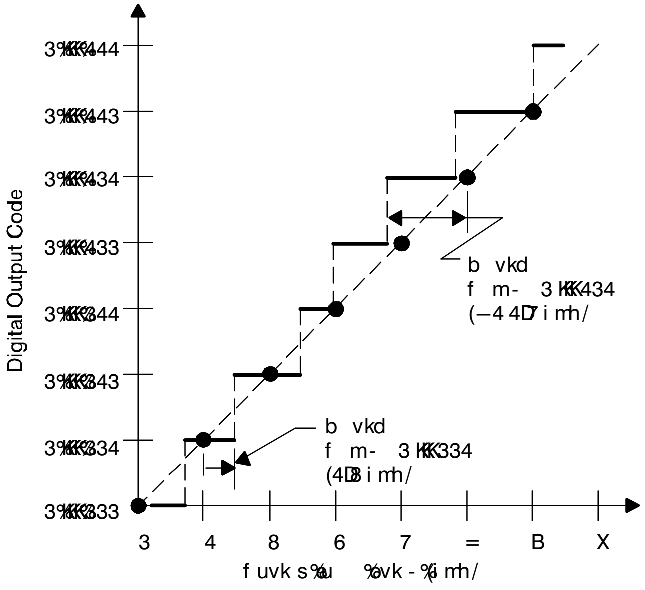
The integral nonlinearity error shown in Figure 24 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 24. Integral Nonlinearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 25 is the maximum value of the difference between an analog value and the ideal midstep value.



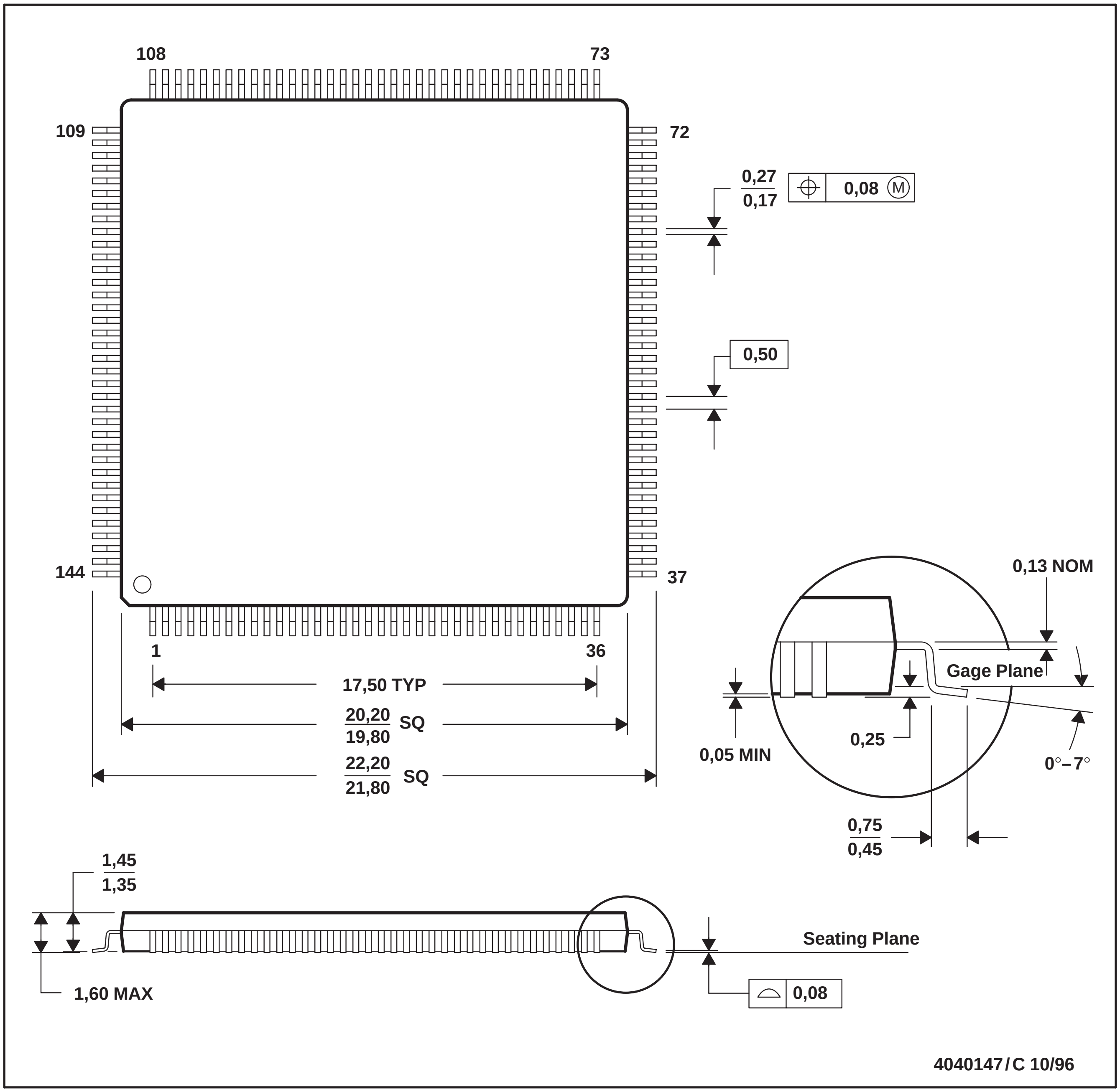
A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 25. Absolute Accuracy (Total) Error

## Thermal Resistance Characteristics

| PARAMETER | °C/W |
|---|---|
| $R_{\Theta\ JA}$ | 43 |
| $R_{\Theta\ JC}$ | 5 |

## PGE (S-PQFP-G144) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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