INTEGRATED CIRCUITS

DATA SHEET

SAA7112

Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)

Preliminary specification   1996 Jun 20

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Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)

SAA7112

FEATURES

The PELICAN SAA7112 is a video capture device for application at the image port of a VGA controller, with following feature highlights:

Video Decoder

- Six analog inputs, internal analog source selectors, (e.g. $6 \times$ CVBS or($2 \times$ YC and $2 \times$ CVBS) or ($1 \times$ YC and $4 \times$ CVBS)
- Two analog preprocessing channels, including built in analog anti-alias filters
- Fully programmable static gain for the main channels or Automatic Gain Control (AGC) for the selected CVBS/Y channel
- Two 8 bit video CMOS Analog-to-Digital Converters (ADCs)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white peak control
- On-chip line locked clock generation in accordance with CCIR-601
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources, e.g. consumer grade VTR
- Requires only one crystal (32.11 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50/60Hz field frequency, and automatic switching between standards PAL and NTSC
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance combination filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Independent Brightness Contrast Saturation (BCS) adjustment for decoder part.

Video Scaler

- Horizontal and vertical down-scaling and up-scaling to randomly sized windows
- Horizontal and vertical scaling range: 2 (zoom) to $\frac{1}{64}$ (icon); vertical zoom might be restricted
- Anti-alias- and accumulating filter for horizontal scaling

- Vertical scaling with linear phase interpolation (6-bit phase accuracy) and accumulating filter for anti-aliasing
- Horizontal phase correct up- and down-scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6-bit phase accuracy
- Two independent programming sets for scaler part, to define two 'ranges' per field or per frame
- Field-wise switching between decoder-part and expansion port input
- Brightness, contrast and saturation controls for scaled outputs.

VBI-data decoder and text slicer

- versatile VBI-data decoder, slicer, clock regeneration and byte synchronization; e.g. for WST, NABST, Close Caption, WSS, etc.

Audio clock generation

- Generation of a field locked audio master clock to support a constant number of audio clocks per video field
- Generation of an audio serial and left/right (channel) clock signal.

Digital I/O interfaces

- Real time signal port (R-port), including continuous line locked reference clock and real time status information
- Bidirectional expansion port (X-port) with half duplex functionality (D1), 8-bit YUV
  - output from decoder part, real time, or
  - input to scaler part, e.g. video from MPEG-decoder
- Video image port (I-port) configurable for 8-bit (16-bit) data in master mode (own clock), or slave mode (external clock), with auxiliary timing and hand shake signals
- 8-bit data Host port (H-port) for 16-bit extension of I-port
- Discontinuous data streams supported
- 32-word $\times$ 4 bytes FIFO register for video output data

| Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN) | SAA7112 |

- 16-word × 4 bytes FIFO register for decoded VBI output data

  Scaled 4 : 2 : 2, 4 : 1 : 1 YUV output
- Scaled 8-bit luminance only and raw data output
- Decoded VBI data output.

miscellaneous

- Power-on control
- Programming via I²C-bus, or parallel image data port (full read-back ability by an external controller)
- Chip enable function (reset for the clock generator).

APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone.

GENERAL DESCRIPTION

The PELICAN SAA7112 is a video capture device for applications at the image port of VGA controllers.

The SAA7112 is a combination of a two channel analog preprocessing circuit including source-selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multistandard decoder and a SAA7140B based scaler, including variable horizontal and vertical up and down scaling and a brightness, contrast and saturation control circuit (see Fig.1).

It is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into CCIR-601 compatible colour component values. The SAA7112 accepts as analog inputs CVBS or S-video (Y−C) from TV or VCR sources, including weak and distorted signals. An Expansion port for digital video (bidirectional half duplex, D1 compatible) is also supported to connect to MPEG or video phone CODEC. At the so called image port the SAA7112 supports 8-bit (16-bit) wide output data with auxiliary reference data for interfacing to VGA controllers

The target application for PELICAN is to capture and scale video images, to be provided as digital video stream through the image port of a VGA controller, for display via VGAs frame buffer, or for capture to system memory.

In parallel the SAA7112 incorporates also provisions for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available: to capture raw video samples and a versatile data slicer (data recovery) unit.

The SAA7112 incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of synchronization between video and audio, during capture or playback.

The circuit can be controlled via the I²C-bus or via its fast parallel programming mode of the image port interface (full write/read capability).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.0	3.6	V
V_{DDA}	analog supply voltage	3.0	3.6	V
T_{amb}	ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7112	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)
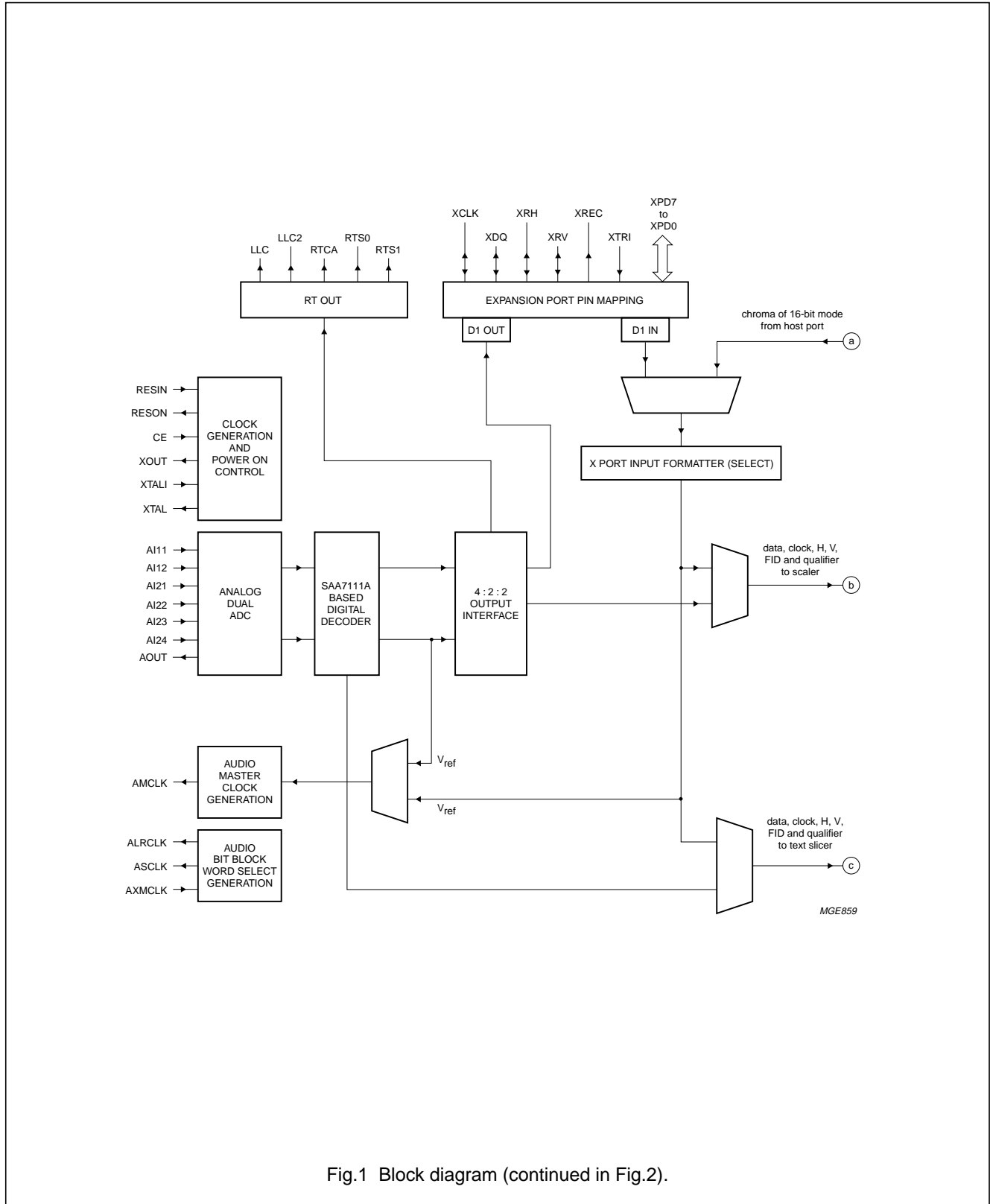
SAA7112

BLOCK DIAGRAMS

Fig.1 Block diagram (continued in Fig.2).

Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)
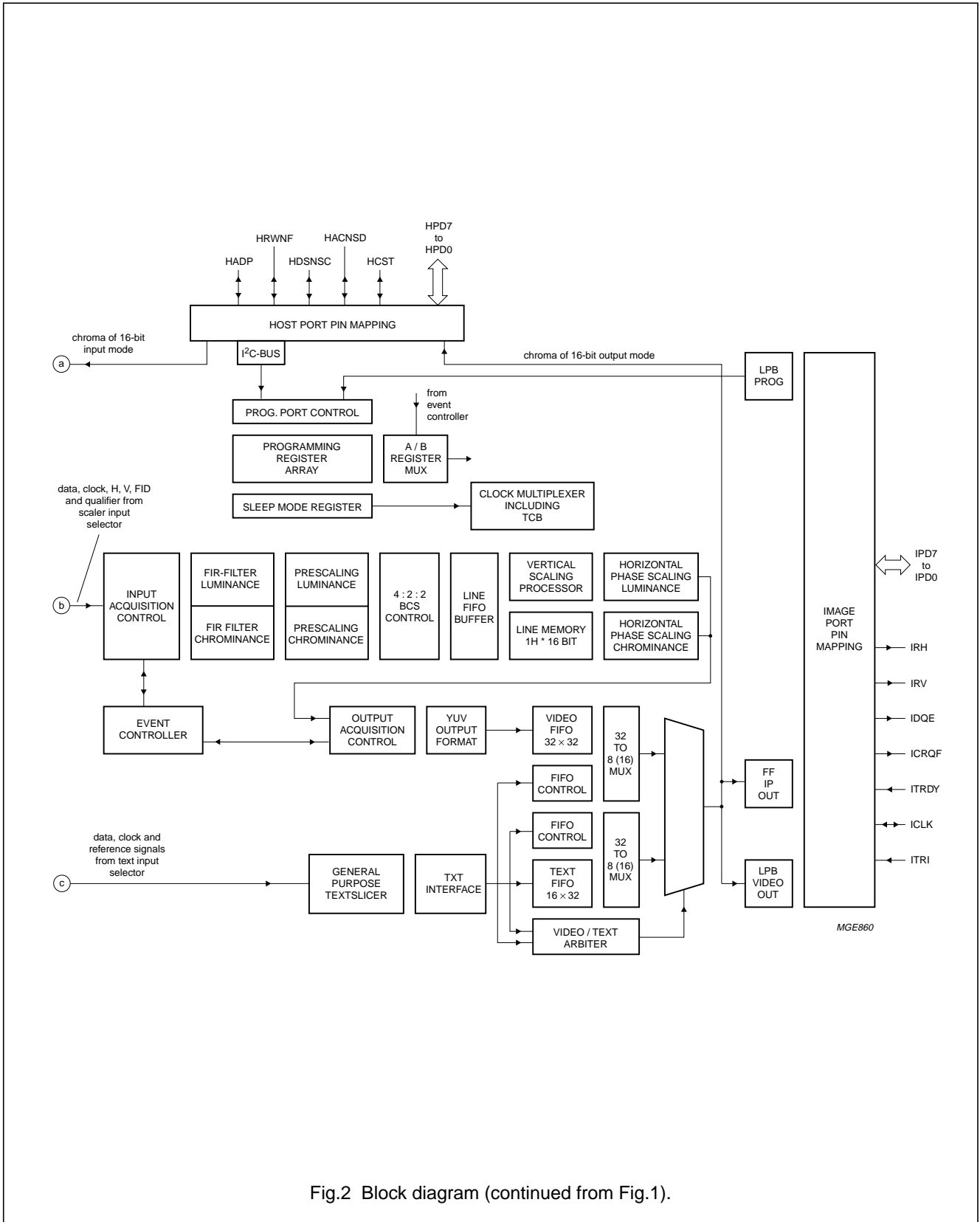
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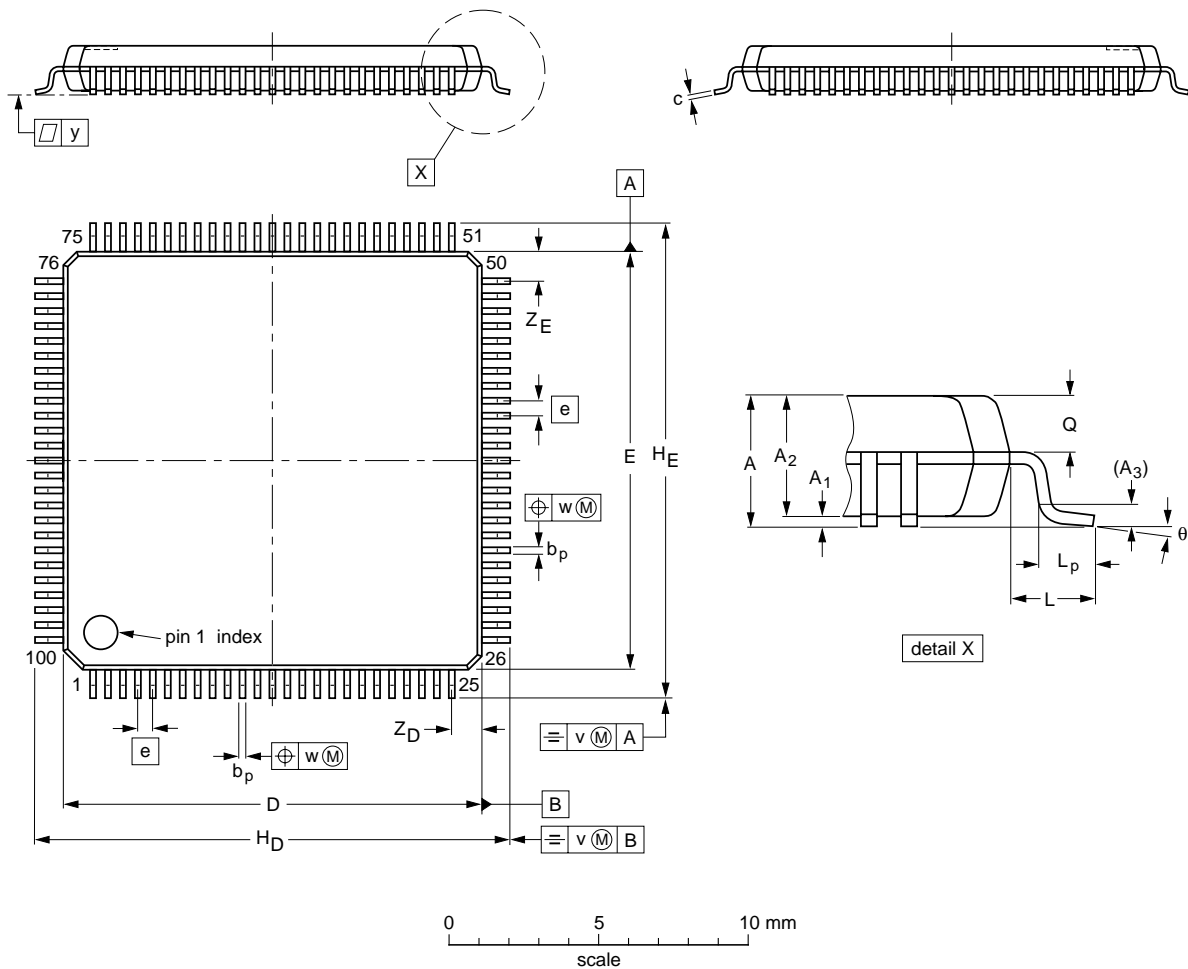

Fig.2 Block diagram (continued from Fig.1).

Decoder with High-Performance Scaler
(HPS) for Image Port (PELICAN)

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PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_D	H_E	L	Lₚ	Q	v	w	y	Z_D[1]	Z_E[1]	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						95-12-19

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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