DATA SHEET

SAA7708H
Car Radio Digital Signal Processor

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Philips
Semiconductors

PHILIPS

CONTENTS

1 GENERAL DESCRIPTION

The CDSP-chip performs all the signal functions in front of the power amplifiers and behind the AM and FM_MPX demodulation of a car radio or the tape input. These functions are: interference absorption, stereo decoding, RDS decoding, FM and AM weak signal processing (soft-mute, sliding stereo, etc.), Dolby-B tape noise reduction and the audio controls (volume, balance, fader and tone). Some functions have been implemented in hardware (stereo decoder, RDS decoding and IAC for FM_MPX) and are not freely programmable. A digital audio signals from external sources with the Philips I^2S and the LSB 16, 18 and 20 bit justified format or SPDIF format are accepted. There are four independent analog output channels..

The DSP contains a basic program which enables a set with AM/FM reception, sophisticated FM weak signal functions, MSS, Dolby-B tape noise reduction system, CD play with compressor function and separate bass and treble tone control and fader/balance control.

2 HARDWARE FEATURES

- Two 3rd order SCAD (switch cap analog to digital converters)
- D/A converters with four fold over sampling and noise shaping
- Digital stereo decoder for the FM_MPX signal
- Improved, digital IAC for FM
- RDS processing with optional 16 bit buffer via a separate channel.
- Phone input with common mode rejection. Can be mixed with DAC output of front channels or processed via an AD
- Auxiliary high CMRR analog CD input (CD-walkman, speech, economic CD-changer etc.)
- One separate full I^2S and LSB justified format and two muxable SPDIF high performance input interfaces
- Audio output short circuit protected
- I^2C bus controlled
- AM input or AM_Right and AM_Left input
- Phase Lock Loop to generate the high frequency DSP clock from common fundamental oscillator crystal
- Combined AM/FM level input
- Two analog single ended tape inputs
- -40 to +85 °C operating temperature range

3 SOFTWARE FEATURES

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation, Dolby level
- Baseband Audio processing (treble/bass/balance/fader/volume)
- Dynamic loudness or bass boost
- Audio level meter
- Music Search detection for Tape (MSS)
- Dolby-B tape noise reduction
- CD dynamics compressor
- CD De-emphasis processing
- Improved AM processing with IAC
- Soft Audio Mute

- Extended Bleep functions
- Pause detection for RDS updates
- Signal level, noise and multipath detection for AM/FM signal quality information

4 APPLICATIONS

- Car radio systems

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{d3}	Operating supply voltage 3.3 Volt analog and digital	with respect to Vss all parts	3	3.3	3.6	V
V_{d5}	Operating supply voltage 5 Volt periphery	with respect to Vss all parts	4.5	5	5.5	V
IP_3	DC supply current of the 3.3 digital core part	high activity of the DSP at 31 MHz DSP frequency	-	57.4	78	mA
IP_5	DC supply current of the 5V digital periphery part	Without external load to ground	-	5	7	mA
IP_A	DC supply current of the analog part	At zero input and output signal	-	16.5	22.6	mA
Ptot	Total power dissipation	high activity of the DSP at 31 MHz DSP frequency	-	0.273	0.423	W
ADSNR	Level AD converter SNR RMS (unweighted)	BW=0-29 kHz Max. input	48	54	-	dB
ADICL	Input voltage range level AD for full scale		0	-	VDDA1	V
AITHDM	THD FM_MPX input	1 kHz 1.1 Vrms, BW= 19 kHz, I^2C default setting	-	-70 0.03	-65 0.056	dB %
AISNRM	SNR FM_MPX input mono	1 kHz, BW=19 kHz, 0 dB ref. = 1.1 Vrms, I^2C default setting	80	83	-	dB
AISNRSS	SNR FM_MPX input stereo	1 kHz, BW=40 kHz, 0 dB ref. = 1.1 Vrms, I^2C default setting	74	77	-	dB
AITHDC	THD CD Inputs, not multiplex mode	1 kHz, 0.55Vrms, BW=20 kHz	-	-80 0.01	-76 0.016	dB %
AISNRC	SNR CD Input, not multiplex mode	1 kHz, BW=20 kHz, 0 dB ref.= 0.55 Vrms	81	84	-	dB
AITHDA	THD AM mono input, not multiplex	1 kHz, 0.55 Vrms, BW=5 kHz	- -	-80 0.01	-76 0.016	dB %
AISNRA	SNR AM mono input, not multiplex	1 kHz, BW=5 kHz, 0dB ref. = 0.55 Vrms	83	88	-	dB
AITHDT	THD Tape input, multiplex mode	1 kHz, BW = 20 kHz, 0.55 Vrms		-80 0.01	-76 0.016	dB %
AISNRT	SNR Tape input, multiplex mode	1 kHz, BW= 20 kHz, 0 dB ref. = 0.55 Vrms	70	77	-	dB
AILVL	conversion input level	THD < 1%	0.6	0.66	-	Vrms
THD&N/S	DAC total harmonic distortion + noise vs Output Signal DAC	Rload AC> 5 kΩ, f=1 kHz	-	-75	-65	dBA
DRAN	DAC Dynamic Range	f = 1 kHz, -60 dB	92	102	-	dBA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DSIL	DAC Digital Silence	f=20 Hz-17 kHz A-weighted	-102	-108	-	dBA
XTFREQ	X-tal frequency			11.2896		MHz
DSPFREQ	Clock Frequency DSP core			31.0464		MHz

6 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7708H	80	QFP	plastic	SOT318D4C

7 APPLICATION BLOCK DIAGRAM

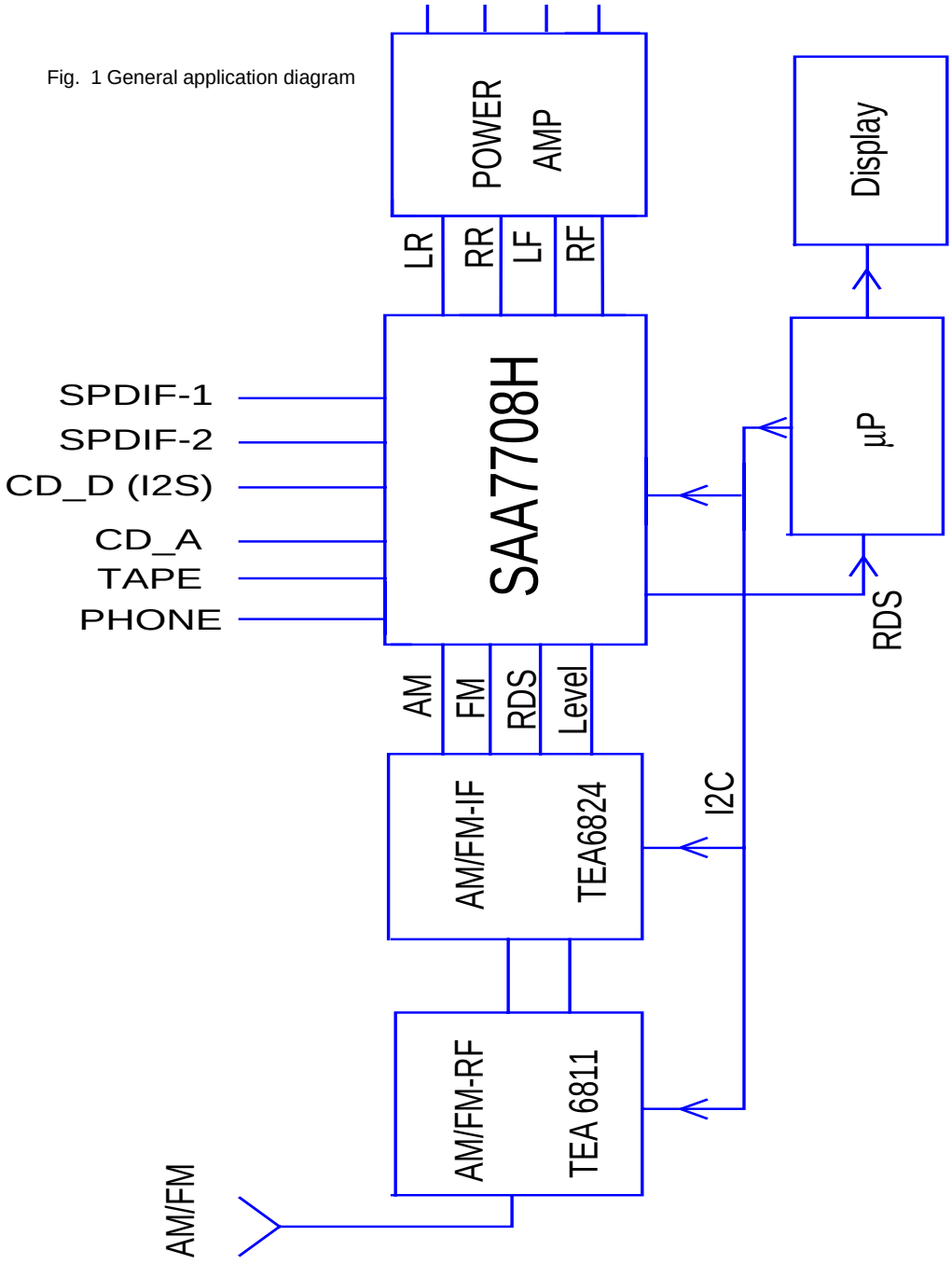


Fig. 1 General application diagram

8 BLOCK DIAGRAM

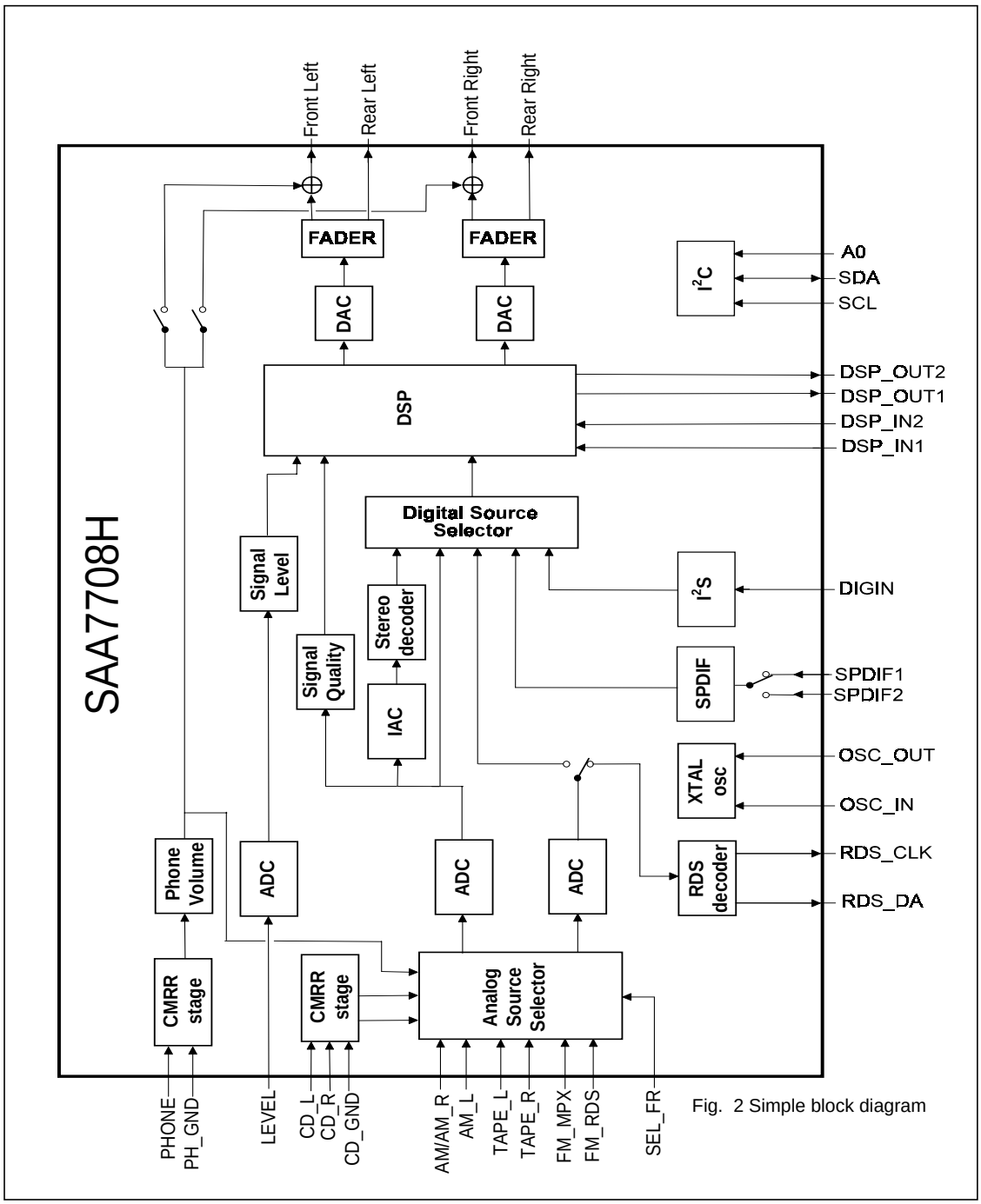


Fig. 2 Simple block diagram

9 PINNING

9.1 Pinning diagram

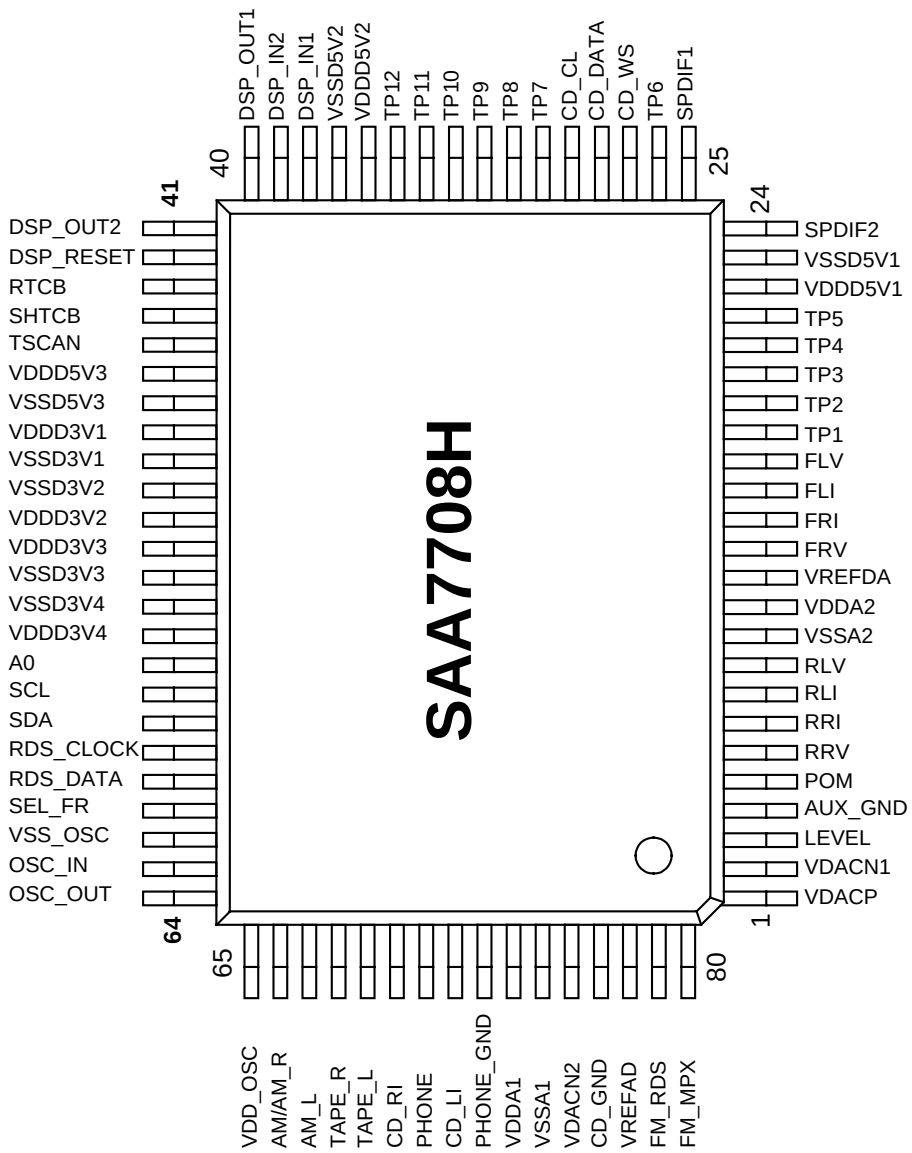


Fig. 3 Pinning diagram.

Pinning Table
Pin list SAA7708

SYMBOL	PIN	DESCRIPTION	PIN TYPE
VDACP	1	Positive reference voltage SCAD1, SCAD2 and Level AD	AP2D
VDACN1	2	Ground reference voltage 1 SCAD1, SCAD2 and Level AD	AP2D
LEVEL	3	FM/AM-level input pin. Via this pin the level of the FM signal or level of the AM signal is fed to the CDSP. The level information is used in the DSP for signal correction	AP2D
AUX_GND	4	By I2C switchable common mode reference pin to enable an arbitrary high common mode analog input.	AP2D
POM	5	Power on Mute of the FADER DAC. Timing is determined by an external capacitor.	APR2D
RRV	6	Rear Right audio voltage output of the FADER DAC	AP2D
RRI	7	Rear Right audio current output of the FADER DAC	APR2D
RLI	8	Rear Left audio current output of the FADER DAC	APR2D
RLV	9	Rear Left audio voltage output of the FADER DAC	AP2D
VSSA2	10	Ground supply analog part of the FADER DAC and SPDIF bitslicer	APVSS
VDDA2	11	3V positive supply analog part of the FADER DAC and SPDIF bitslicer	APVDD
VREFDA	12	Voltage reference of the analog part of the FADER DAC	AP2D
FRV	13	Front Right audio voltage output of the FADER DAC	AP2D
FRI	14	Front Right audio current output of the FADER DAC	APR2D
FLI	15	Front Left audio current output of the FADER DAC	APR2D
FLV	16	Front Left audio voltage output of the FADER DAC	AP2D
TP1	17	Test pin, may not be connected in the application	BT4CR
TP2	18	Test pin, may not be connected in the application	BT4CR
TP3	19	Test pin, may not be connected in the application	BT4CR
TP4	20	Test pin, may not be connected in the application	BT4CR
TP5	21	Test pin, may not be connected in the application	BD4CR
VDDD5V1	22	5V positive supply 1 peripheral cells only	VDDE5
VSSD5V1	23	Ground supply 1 of 5 volt peripheral cells only	VSSE5
SPDIF2	24	Analog bitslicer input2 for SPDIF, can be selected i.s.o. SPDIF1 via I2C bit	APR2D
SPDIF1	25	Analog bitslicer input1 for SPDIF, can be selected i.s.o. SPDIF2 via I2C bit	APR2D
TP6	26	Test pin, may not be connected in the application	SCHMITCD
CD_WS	27	I^2S or LSB justified format Word select input from a digital audio source	SCHMITCD
CD_DATA	28	I^2S or LSB justified format Left-Right Data input from a digital audio source	SCHMITCD
CD_CL	29	I^2S Clock or LSB justified format input from a digital audio source	SCHMITCD
TP7	30	Test pin, may not be connected in the application	BD4CRD
TP8	31	Test pin, may not be connected in the application	SCHMITCD
TP9	32	Test pin, may not be connected in the application	SCHMITCD

SYMBOL	PIN	DESCRIPTION	PIN TYPE
TP10	33	Test pin, may not be connected in the application	BD4CRD
TP11	34	Test pin, may not be connected in the application	BD4CRD
TP12	35	Test pin, may not be connected in the application	SCHMITCD
VDDD5V2	36	5V positive supply 2 peripheral cells only	VDDE
VSSD5V2	37	Ground supply 2 of 5 volt peripheral cells only	VSSE
DSP-IN1	38	Digital input 1 of the DSP-core (F0 of the status register). Level must always be defined externally in the application.	SCHMITC
DSP-IN2	39	Digital input 2 of the DSP-core (F1 of the status register). Level must always be defined externally in the application.	SCHMITC
DSP-OUT1	40	Digital output 1 of the DSP-core (F2 of the status register)	B4CR
DSP-OUT2	41	Digital output 2 of the DSP-core (F3 of the status register)	B4CR
DSP-RESET	42	Reset of the DSP core (active low)	IBUFU
RTCB	43	Asynchronous Reset Test Control Block active low, connect to ground	SCHMITCD
SHTCB	44	Shift Clock Test Control Block, connect to ground	SCHMITCD
TSCAN	45	Scan control active high, connect to ground	SCHMITCD
VDDD5V3	46	5V positive supply 3 peripheral cells only	VDDE5
VSSD5V3	47	Ground supply 3 of 5 volt peripheral cells only	VSSE5
VDDD3V1	48	3V positive supply 1 core only	VDDI3
VSSD3V1	49	Ground supply 1 of 3 volt core only	VSSI3
VSSD3V2	50	Ground supply 2 of 3 volt core only	VSSI
VDDD3V2	51	3V positive supply 2 core only	VDDI3
VDDD3V3	52	3V positive supply 3 core only	VDDI3
VSSD3V3	53	Ground supply 3 of 3 volt core only	VSSI3
VSSD3V4	54	Ground supply 4 of 3 volt core only	VSSI3
VDDD3V4	55	3V positive supply 4 core only	VDDI3
A0	56	Slave sub-address I^2C selection / Serial data input test control block	SCHMITCD
SCL	57	Serial clock input I^2C bus	SCHMITC
SDA	58	Serial data input / output I^2C bus	BD4SCI4
RDS_CLOCK	59	Radio Data System bit clock output / RDS external clock input	BD4CR
RDS_DATA	60	Radio Data System data output	B4CR
SEL_FR	61	AD input selection switch to enable high ohmic FM_MPX input at fast tuner search on FM_RDS input. At switch to ‘1’ the input of the FM_RDS is put through to the MPX input of the dowsample filters and FM_MPX inputs gets high ohmic. Level must always be defined externally in the application.	SCHMITC
VSS_OSC	62	Ground supply crystal oscillator circuit	APVSS
OSC_IN	63	Crystal oscillator input: crystal oscillator sense for gain control or forced input in slave mode	APR2D
OSC_OUT	64	Crystal oscillator output: Drive output to 11.2896 MHz crystal	AP2D
VDD_OSC	65	3V positive supply crystal oscillator circuit	APVDD

SYMBOL	PIN	DESCRIPTION	PIN TYPE
AM/AM_R	66	Analog input pin for AM audio frequency Right Channel or AM mono inputl	AP2D
AM_L	67	Analog input pin for AM audio frequency Left Channel	AP2D
TAPE_R	68	Input of the analog TAPE Right signal	AP2D
TAPE_L	69	Input of the analog TAPE Left signal	AP2D
CD_RI	70	Input of the analog CD Right signal	AP2D
PHONE	71	Input of common mode phone signal	AP2D
CD_LI	72	Input of the analog CD Left signal	AP2D
PHONE_GND	73	The common mode reference pin of the phone signal	AP2D
VDDA1	74	Positive supply analog SCAD1, SCAD2 and Level AD.	APVDD
VSSA1	75	Ground supply analog SCAD1, SCAD2 and Level AD.	APVSS
VDACN2	76	Ground reference voltage 2 SCAD1, SCAD2 and Level AD	AP2D
CD_GND	77	The common mode reference pin of the CD_AD LEFT and CD_AD RIGHT block	AP2D
VREFAD	78	Common mode reference voltage SCAD1, SCAD2 and Level AD	AP2D
FM_RDS	79	Analog input pin for FM RDS signal	AP2D
FM_MPX	80	Analog input pin for FM-Multiplex signal	AP2D

Table 1 Brief explanation of used pin types

PIN TYPE	EXPLANATION
AP2D	Analog IO (Input/Output)
APR2D	Analog IO with series resistor and clamp device
APVDD	Analog SUPPLY
APVSS	Analog GROUND
VDDE5	5 Volt Peripheral only supply ring
VSSE5	5 Volt Peripheral only gound connection, no connection to substrate
VDDI3	3.3 Volt SUPPLY to digital core and internal IO pads
VSSI3	3.3 Volt GROUND to digital core and internal IO pads, no substrate connection
VSSI	3.3 Volt GROUND to digital core and internal IO pads with substrate connection
SCHMITC	CMOS Schmitt trigger input
SCHMITCD	CMOS, Schmitt trigger input with active pull-down to VSSE5
IBUFD	CMOS, active pull-down to VSSE5
IBUFU	CMOS, active pull-up to VDDE5
BD4CR	Bidirectional CMOS IO buffer, 4 mA, slew rate control
BD4CRD	Bidirectional CMOS IO buffer, 4 mA, slew rate control, active pull down to VSSE5
BT4CR	4mA CMOS tristate ouput buffer, slew rate control
B4CR	4mA CMOS ouput buffer, slew rate control
BD4SCI4	CMOS IO pad with open drain output

10 FUNCTIONAL DESCRIPTION

10.1 Signal path for Level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a FM/AM Level input is implemented (pin LEVEL). In the case of radio reception the clocking of the filters and the AD is based on a 38 kHz Fs frequency. A DC input signal is converted by a bitstream first order Sigma-Delta AD converter followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to the LEVEL pin.

10.1.1 THE VREFAD PIN

Via this pin the Midref voltage of the AD's is filtered. This Midref voltage is used as reference of the LEVEL AD and half supply reference of the two third order switch capacitor ADs. External capacitors (connected to VSSA1) prevents crosstalk between the AD's. This pin must also used in the application as reference for the inputs AM/AM_R, AM_L, , TAPE_L and TAPE_R (see Fig. 21).

10.2 Signal path of the third order switched capacitor AD's.

10.2.1 THE FM MPX SIGNAL PATH

The CDSP has in total three analog audio source channels. One of the analog inputs is the FM_MPX signal. Selection of this signal is achieved according Table 3. The multiplex FM signal is converted to the digital domain in SCAD1, a bitstream third order switched capacitor AD converter. A decimation filter reduces the output of the AD to a lower sample rate. From this filter the following signals are derived and are processed in the DSP.

The outputs from this signal path to the DSP which are all running on a sample frequency of 38 kHz are:

- Pilot presence indication: Pilot-I. This one bit signal is low for a pilot frequency deviation < 3 kHz and high for a pilot frequency deviation > 3 kHz AND the FM MPX stereodecoder is locked on a pilot tone.
- 'Left' and 'Right' FM reception stereo signal: This is the 18 bit output of the stereo decoder after the matrix decoding in ISN I^2S format.This signal is fed via a muxer to a general I^2S interface block that communicates with the DSP.
- A noise level information. This signal is derived from the first MPX decimation fiter via a wide band noise filter. Detection is done with an envelope detector. This noise level is filtered in the DSP core and is used to optimize the FM weak signal processing.

Normally the FM_MPX input and the FM_RDS input have the same source. If the FM input contains a stereo radio channel, the pilot information is used to lock the clocking of the decimation filters of FM MPX and RDS path and also the stereo decoder.

10.2.2 INPUT SENSITIVITY FOR FM AND RDS

The FM and RDS input sensitivity is designed for tuner front ends which deliver an output voltage of 200 mVrms at a modulation depth of 22.5 kHz of a 1 kHz tone. In this case the I^2C bit pcs_ad_sel must be 'o' and the SEL_FR switch is also low. The MPX part of the FM_MPX signal will be processed via SCAD1, the RDS part is processed via SCAD2..

Another input sensitivity can be obtained by putting the pcs_ad_sel bit high. Biasing of this input must now take place exterenally via high-ohmic resistors connected to the VREFAD pin. In this case the input sensitivity has increased from 200 mVrms to 65 mVrms at modulation depth of 22.5 kHz. Reduction of the input sensitivity can be obtained by an external resistor tap consisting of an in the signal path placed series resistor and a resistor to VREFAD.

10.2.3 THE SIGNAL FLOW OF THE AM, CD ANALOG AND TAPE

The signal AM mono via the AM/AM_R input can be selected by the correct values of the I^2C bits. There is also an option available to connect a left and right signal to the chip. This can be for instance the AM-Right and AM-Left signal. The AM, TAPE and CD inputs are buffered by an opamp to ensure a high ohmic input that makes external signal reduction

possible via an external resistor divider. For correct biasing of the first input buffer it is obligatory to connect the resistor between the tap and the virtual ground of the VREFAD pin (see Fig. 28). The way to make a high common mode input is described in chapter 10.2.5.

10.2.4 ANALOG SOURCE SWITCHING

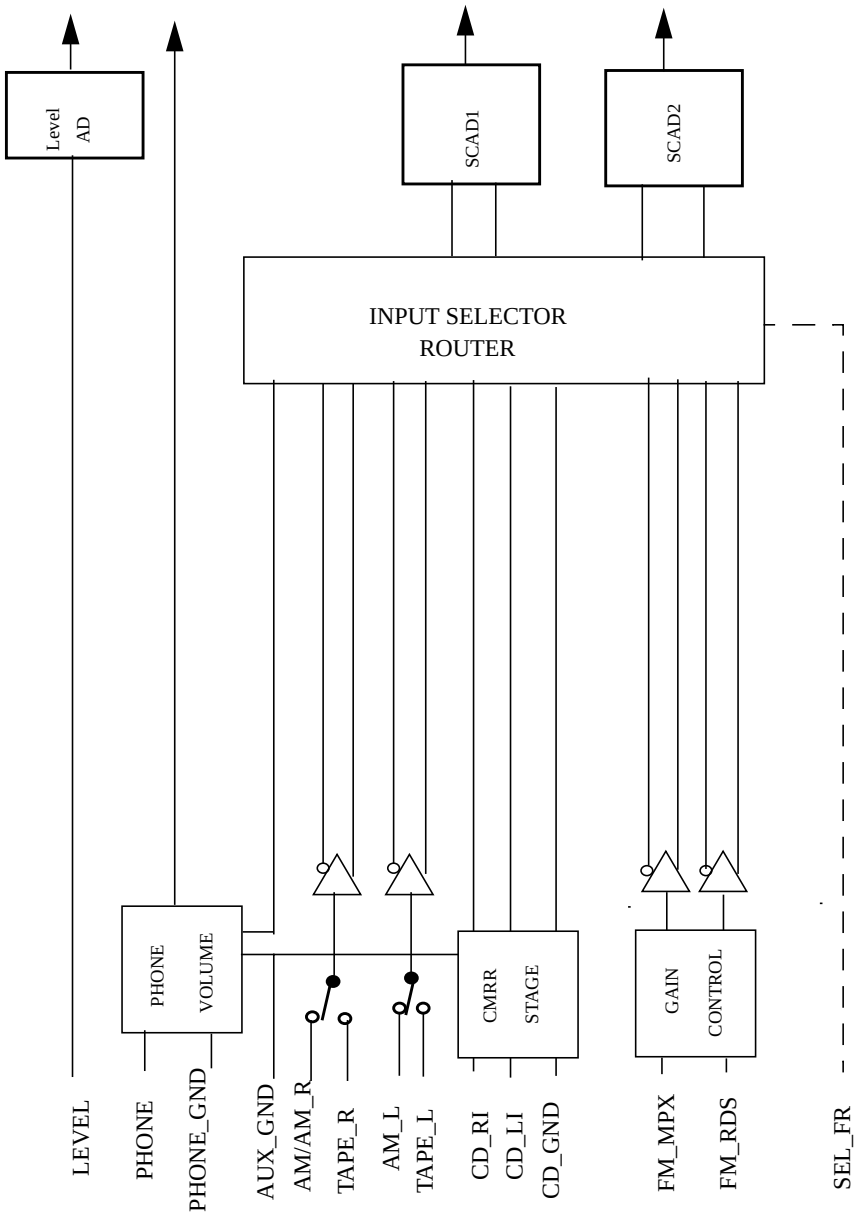


Fig. 4 Analog input switching circuit

10.2.5 THE REALISATION OF COMMON MODE INPUTS

A high Common Mode Rejection Ratio can be created by the use of the either the AUX_GND or the CD_GND pin. One of these pins can be connected via the switches s10 and s11 (see Fig. 5) to the plus input of the second opamp in the signal path of TAPE, CD or AM. The signal of which a high common mode rejection ratio is required has one signal (or two signals) and a common signal as input. The common signal is connected to either the AUX_GND or CD_GND input and for the specific mode selected with the switches 10 and 11. This means that on both signal lines going to the SCAD will contain the common mode signal. The AD's itself will suppress this common mode signal very effectively and this is the way good common mode signal suppression is achieved. The switches needed are drawn in the appropriate position. The inputs CD_LI and CD_RI get in this example a diminished input signal by the external resistor tap of 8k2 and 10k. The 10k resistors provides together with the 1 M resistor from CD_GND to VREFAD also the biasing of the opamps OA1 and OA2. If no external resistor tap is needed still resistors will be needed between the signal inputs and the CD_GND pin. The CD_GND pin is in this configuration connected to the plus input of the opamps OA3 and OA4. Biasing of the opamps OA3 and OA4 is again provided by the 1 M resistor to VREFAD. In this construction the common mode signals on CD_LI / CD_RI and the CD_GND pin will be unchanged in amplitude being present at the AD input and the common mode rejection behaviour of these AD will provide a good common mode rejection ratio. The other common mode input AUX_GND can in the same way be used.

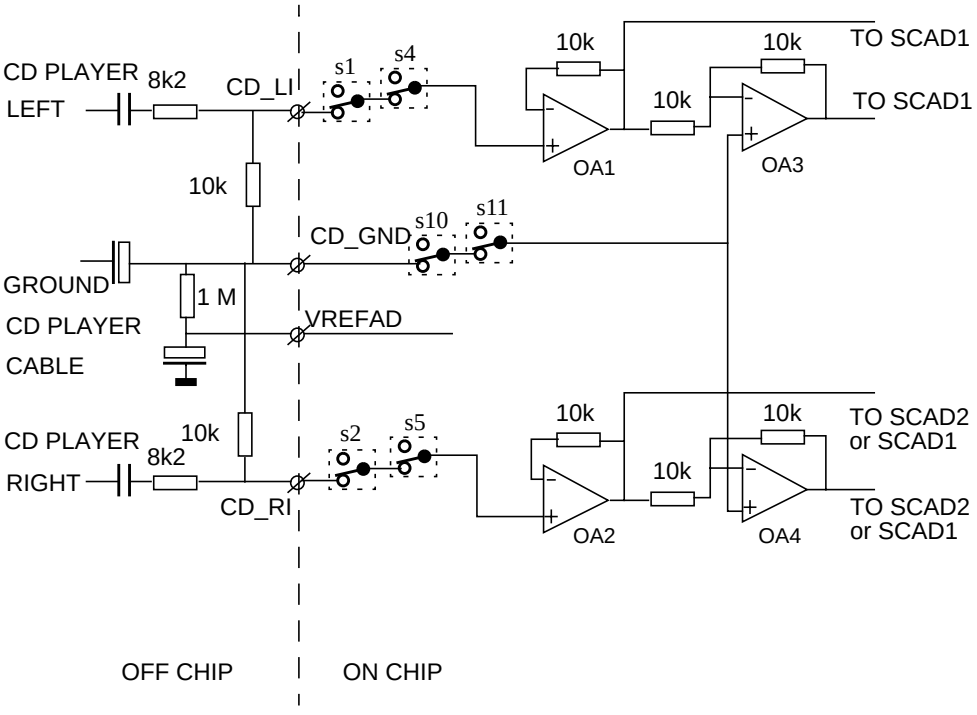


Fig. 5 Example of the use of common mode analog input

10.2.6 PHONE INPUT WITH VOLUME CONTROL

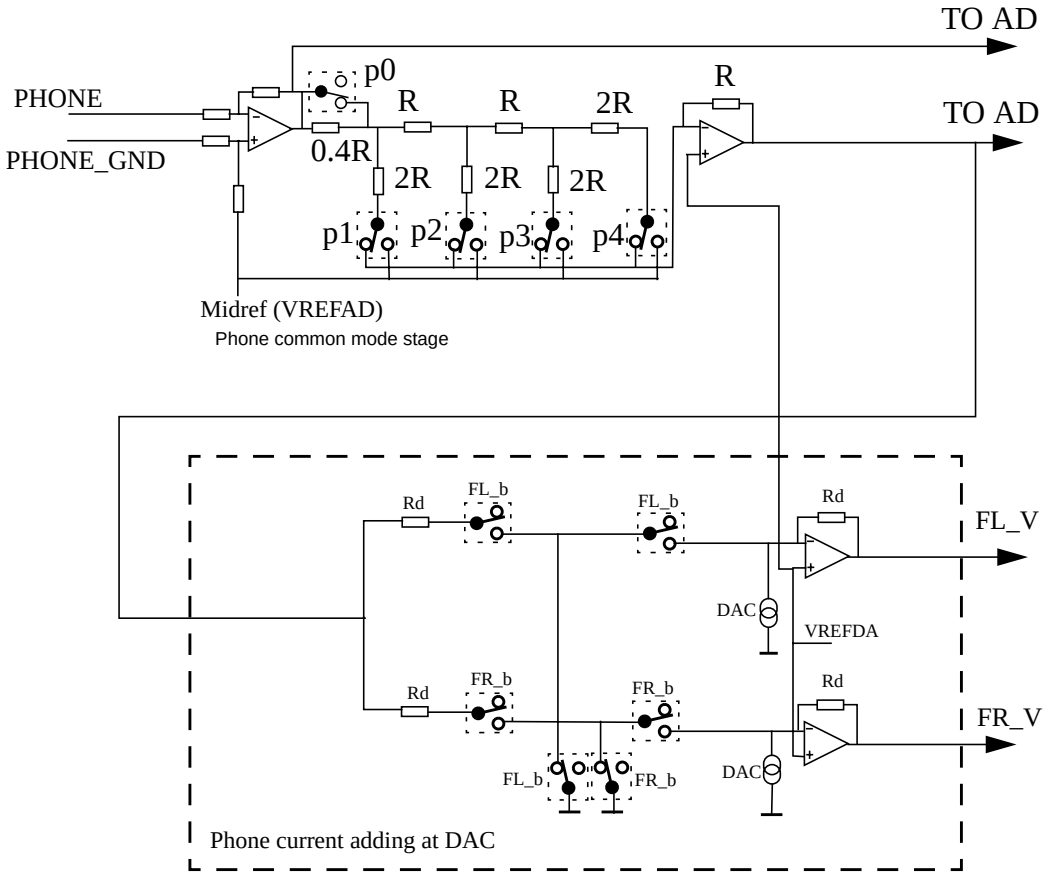


Fig. 6 Volume control setting of PHONE input

A common mode input with volume control for mixing to the Front Left or Front Right or both DAC outputs is provided. The inputs consist of a PHONE input for the signal and a PHONE_GND to be connected to the ground shield of the PHONE cable. By means of two opamps the signal is then converted to a signal with better common mode rejection ratio. Via the switches s6_7 and the multiplex switch in front of the SCAD1 this signal can be processed via the AD signal path. In that case the resistor volume control must be put in an all ‘00000’ position of the I2C bits p4-p0 meaning 0 dB pass through mode (see Fig. 6). Although in this way signal improvement with the DSP can be done, mixing with other analog sources is not possible. Another signal path is the R 2R volume setting block to the DAC current input. The signal from the phone opamp is converted via a R-2R ladder network to a voltage. This voltage can be controlled with the I2C bits p4,p3,p2,p1,p0 according Table 2. This voltage can be connected to two resistors in the DAC block via the I2C controlled switches FL_b and FR_b. The two resistors convert the voltage to a current an this current is added to the already present current of the Front Left DA and/or the Front Right DA. This is the way the phone signal is mixed with the DAC signal in the analog domain.

Table 2 Volume settings of the PHONE input ($0FFE)

VOL_PHONE BITS P4,P3,P2,P1,P0	FL AND FR OUTPUT (DB)
00000	0
00001	-3
00010	-6
00011	-9
00110	-12
01110	-15
01111	-18
01111	-21
1111*	MUTE

10.3 Input selection switches

In Fig. 4 a block diagram of the input is shown. The input selection is controlled by bits in the input selector control register and the input pin SEL_FR. The relation between these bits and the switches is indicated in table 3. This table is not 100% elaborated but gives an idea of the switching possibilities.

Table 3 Analog input selection via I^2Cbits ($0FFD) signal destination

MODE	pcs_ad _sel	en_38 _clk	sw_ ad1	rds_cd _sel	s1_2	s4_5	s6_7	s8_9	wide_ narrow
FM_MPX + RDS mode 200 mV	0	0	0	0	d	d	d	0	0
FM_MPX + RDS mode 65 mV	1	0	0	0	d	d	d	0	0
AM mono + RDS	0 or 1	0	0	0	0	1	d	1	0
AM stereo + RDS	0 or 1	1	d	0	0	1	0	1	0
TAPE STEREO + RDS	0 or 1	1	d	0	1	0	0	1	0
CD-ANALOG + RDS	0 or 1	1	d	0	0	0	0	1	0
CD ANALOG	d	0	1	1	0	0	0	d	1
PHONE via SCAD1 + RDS	0 or 1	0	1	0	d	d	1	d	0

- In all the positions above one supposes that the SEL_FR pin is low.

  The switches s10 and s11 must be switched according the position needed for the correct common mode rejection ratio of the chosen input e.g. s10=0 and s11=1 in case of CD analog input.

10.4 Supply of the analog inputs

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are the VSSA1 for the analog ground and the VDDA1 for the analog power supply.

10.5 The DCS clock block

For the digital stereo decoder a clock signal is needed which is the 512 multiple of the pilot tone frequency of the FM MPX signal. This is done by the DCS clock block, which generates this 512 * 19 kHz = 9.728 MHz clock, the DCS clock, by locking to the pilot frequency. This block is also able to generate other frequencies and controlling is done via a number of I^2C bits of the registers in Table 21 and Table 22. Default I^2C settings of the DCS and the PLL guarantee correct functioning of the DCS block.

10.6 Synchronization with the DSP core

The system can run in case of I^2S input on different audio sample frequencies of Fs=32kHz, 38 kHz, 44.1 kHz or 48 kHz. After each processing period of one input sample with this signal, the Input flag (I-flag) of the status register of the DSP core is set on the falling edge of the I2S WS to I=1 during 4 clock cycles. This flag can be tested with a conditional branch instruction in the DSP. This synchronisation starts really in parallel with the input signal due to the short period that the I flag is set. It is obvious that the higher the Fs the lower the number of cycles available in the DSP program..

10.7 IAC

10.7.1 General description

The Interference Absorption Circuit (IAC) detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. All IAC functions must be switched off if there is no FM MPX signal processing.

The input signal of a first IAC detection circuit is the output signal of ADF1. This interference detector analyses the high frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic like algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The input signal of a second IAC detection circuit is the LEVEL signal (the output of the Level AD). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The characteristics of both IAC detectors can be adapted to the properties of different FM front ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I^2C bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the Dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in case of narrow IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

AM IAC is also implemented. In this case only the AM mono signal is monitored by the on the DSP processor running program. Input from the LEVEL pin is not used.

10.7.2 Parameter setting for the MPX input ignition detector

There are in total 5 different coefficients. The settings of these coefficients are described below. On RESET, the nominal setting for a good performing MPX IAC detector is selected.

10.7.3 AGC SET POINT (1 BIT)

In case the sensitivity and feed forward factor are out of range in a certain application, the set point of the AGC can be shifted. The set point controls the sensitivity of the other IAC control parameters. See bit 11 of $0FFB (Table 25).

10.7.4 THRESHOLD SENSITIVITY OFFSET (3 BITS)

With this parameter the threshold sensitivity of the comparator in the interfering pulse detectors can be set. It also influences the amount of unwanted triggering. Settings are according Table 31.

10.7.5 DEVIATION FEED FORWARD FACTOR (3 BITS)

This parameter determines the reduction of the sensitivity of the detector by the absolute value of the MPX signal. This mechanism prevents the detector from unwanted triggering at noise with modulation peaks. In Table 32 the possible values are given.

10.7.6 SUPPRESION STRETCH TIME (3 BITS)

This parameter sets the duration of the pulse suppression after the detector has stopped sending a trigger pulse. It can be switched off by applying the value 0. The duration can be selected in steps of one period of the 304 kHz (3.3 µs) sample frequency. In Table 33 the possible values are given.

10.7.7 MPX DELAY

With this parameter the delay time between 2 and 5 samples of the 304 kHz sample frequency can be selected. The needed value depends on the used front end of the car radio. Settings are according Table 34.

10.7.8 LEVEL IAC THRESHOLD (4 BITS)

With this parameter the sensitivity of the comparator in the ignition interference pulse detector can be set. It also influences the amount of unwanted triggering. The possible values are given in Table 26. The prefix value ‘0000’ switches the Level IAC function off.

10.7.9 LEVEL IAC FEED FORWARD SETTING (2 BITS)

This parameter allows to adjust for delay differences in the signal paths from the FM antenna to the MPX mute, namely, via the FM level ADC and level IAC detection and via the FM demodulator and MPX conversion and filtering. These differences depend on the front end used in the car radio. With a simultaneous appearance of a peak disturbance at the LEVEL input and the MPX ADC input of the chip, a zero delay setting will make for the level IAC mute pulse to coincide with the passage of the disturbance in the MPX mute circuit. The setting for the Level IAC Feed Forward allows to advance the mute pulse by 1 sample period or to delay it by 1 or 2 sample periods of the 304 kHz clock, with respect to the default. The appropriate I^2C bits for each setting are given in Table 27.

10.7.10 LEVEL IAC SUPPRESSION STRETCH TIME (2 BITS)

This parameter sets the time the mute pulse is stretched when the LEVEL input has stopped exceeding the threshold. The duration can be selected in steps of one period of the 304 kHz (3.3 µs) sample frequency. In Table 28 the possible values are given

10.7.11 DYNAMIC IAC THRESHOLD LEVELS

If enabled by the lev_en_dyn_iac I^2C bit (bit 15, register $0FFC) this block will disable temporarily all IAC action if the MPX mono signal exceeds a threshold deviation (threshold 1) for a given time with a given excess amount (threshold 2). This MPX mono signal is separated from the MPX signal with a low-pass filter with the - 3 dB corner point at 15 kHz. The possible values of the this threshold can be found in Table 29.

10.7.12 IAC TESTING

The internal IAC trigger signal is visible on DSP-OUT2 pin if the IAC_trigger bit of the IAC control register is set. In this mode the effect of the parameter settings on the IAC performance can be verified.

10.8 Analog outputs

10.8.1 D/A CONVERTERS

Each of the two low noise high dynamic range D/A convertors consists of a 15 bit signed magnitude DAC with current output. This DAC current is split in two parts by means of a fader. Each part of the current is fed to an operational amplifier, which converts the current into an output voltage. The fader makes it possible to make 4 outputs with only two DACS.

10.8.2 UPSAMPLE FILTER

To reduce spectral components above the audio band, a fixed 4 times oversampling and interpolating 18 bits digital IIR filter is used. It is realised as a bit serial design and consists of two consecutive filters. The data path in these filters is 22 bits to prevent overflow and to maintain a theoretical SNR above 105 dB.

The word clock for the upsample filter (4*asf) is derived from the audio source timing. If the internal audio source is selected, the sample frequency can be either 44.1 kHz or 38 kHz. In case of external digital sources (CD1, SPDIF), a sample frequency from 32 kHz to 48 kHz is possible.

10.8.3 VOLUME CONTROL

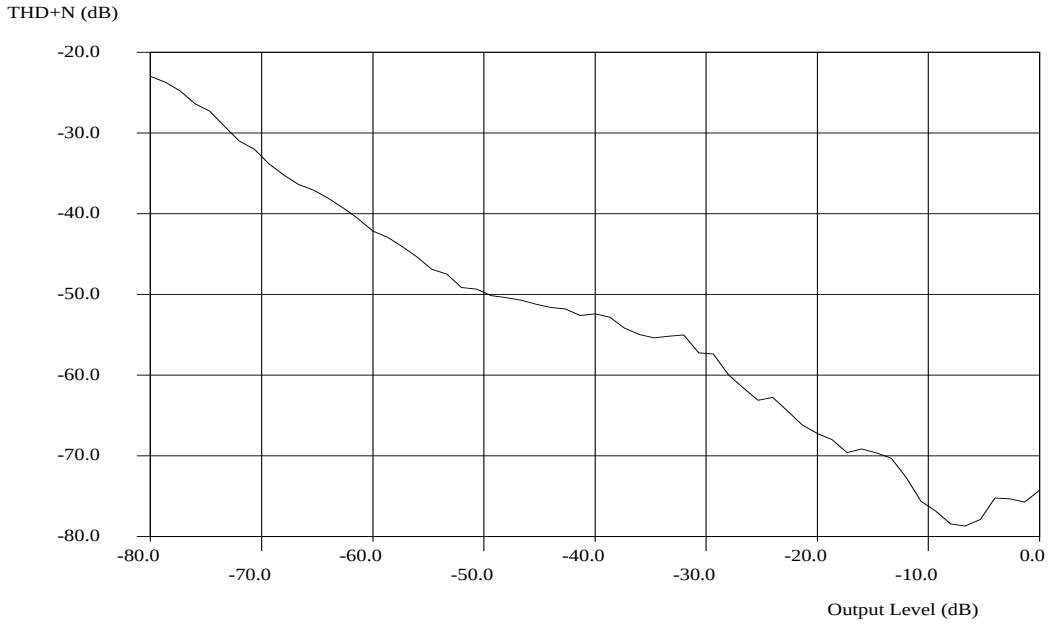


Fig. 7 Typical THD+N curve versus output level

The total volume control has a dynamic range of more than 100 dB. With the signed magnitude noise shaped 15 bit DAC and the internal 18 bits registers of the DSP core a useful digital volume control range of 100 dB is possible by calculating

the corresponding coefficients. The step size is freely programmable and an additional analog volume control is not needed in this design. The SNR of the audio output at full scale is determined by the total 15 bits of the converter. The noise at low outputs is fully determined by the noise performance of the DAC. Since it is a signed magnitude type, the noise at digital silence is also low. As disadvantage the total THD is slightly higher than conventional D/A converters. The typical Signal to Noise and THD versus output level are shown in Fig. 7.

10.8.4 Function of the POM pin

With the POM pin it is possible to switch off the reference current source of the D/A converter. The capacitor on the POM pin determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is 9 times lower than the current loading after the POM pin voltage has past the 1 V level. This results in an almost dB linear behaviour. However the DAC has an a-symmetrical supply and the DC output voltage will be half the supply voltage under functional conditions. During startup the output voltage is not defined as long as the supply voltage is lower than the threshold voltages of the transistors and a small jump in DC is possible at startup. In this DC voltage jump audio components can be present.

10.8.5 The Fader

The fader is a 5 bit I2C (bits 11-15 of $0FFC) controlled volume regulator between the front and the rear outputs. Of the 32 positions of the 5 bit I2C code position 15 is the default position in which front and rear output have the same volume (Fig. 8). Increasing the 5 bits I2C code will keep the front channels at the same volume but will decrease the volume of the rear channels. Decreasing the 5 bits code starting at position 15 will keep the rear channels at the same volume but will decrease the volume of the front channels. Starting at the default position the first 12 steps decrease the volume linearly to -26 dB, step 13 and 14 decrease until -37 dB. The positions 0 and 30 of the fader represent mute for the front- and rear channel respectively. Position 31 is not used.

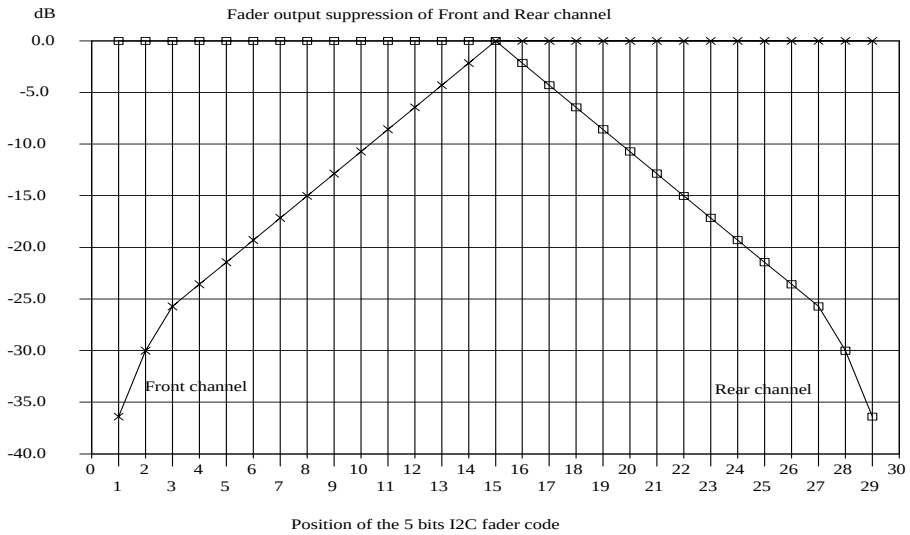


Fig. 8 DAC fader control range

10.8.6 POWER OFF PLOP SUPPRESSION

To reduce the chance of plops in a power amplifier, the supply voltage of the analog part of the D/A converter can be fed from the 5V via a transistor. An capacitor is connected to the 3.3 V to provide still power to the analog part the moment the digital is switching off fast. In this case the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

10.8.7 THE INTERNAL VREFDA PIN

With two internal resistors half the supply voltage VDDA2 is obtained and coupled to an internal buffer. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground.

10.8.8 SUPPLY OF THE ANALOG OUTPUTS

All the analog circuitry of the DACs and the OPAMPS are fed by 2 supply pins, VDDA2 and VSSA2. The VDDA2 must have sufficient decoupling to prevent THD degradation and to ensure a good Power Supply Rejection Ratio. The digital part of the DAC is fully supplied from the chip core supply.

10.9 Clock circuit and oscillator

The chip has an on board crystal clock oscillator. The block schematic of this Pierce oscillator is shown in Fig. 9. The active element needed to compensate for the loss resistance of the crystal is the block Gm. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine-wave with peak to peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine-wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to clock signal.

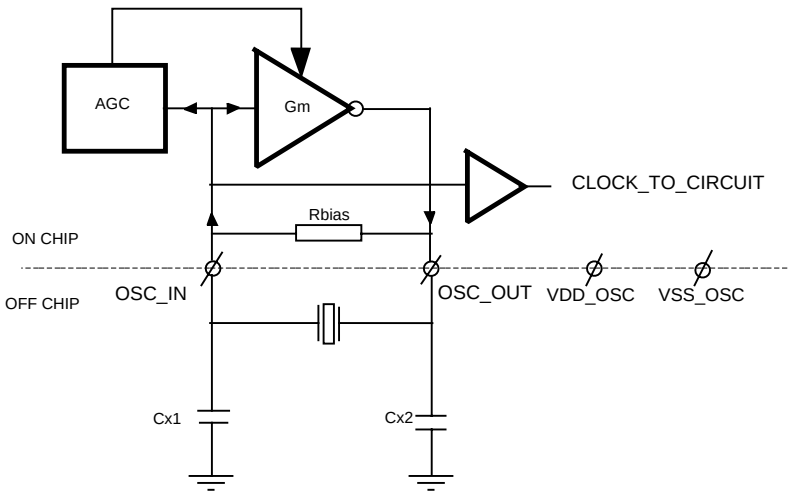


Fig. 9 Block diagram oscillator circuit

10.9.1 SUPPLY OF THE X-TAL OSCILLATOR

The power supply connections of the oscillator are separate from the other supply lines. This to minimize the feedback from the ground bounce of the chip to the oscillator circuit. The VSS_OSC pin is used as ground supply and the VDD_OSC as positive supply.

10.10 The phase lock loop circuit to generate the DSP and other clocks

There are several reasons why two PLL circuits to generate the DSP clock and other clocks are used:

- PLL1 is used to deliver the clock to the DSP core. The deviding factor of this PLL can be changed with I2C bits PLL_DIV(3,2,1,0) but should only be used in the default position to ensure maximum functionality.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 45 MHz, are always third overtone crystals and must also be fabricated on customer demand. This makes these crystals expensive. The PLL2 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256 X 44.1 kHz = 11.2896 MHz crystal is chosen. The clock of this PLL2 is used via a sample rate converter for the AD decimation paths and stereo decoding, the SPDIF logic, the uProcessor interface and the Fader DAC upsample filters.

With the I^2C bit dsp_turbo (bit 11 of $0FFD) the output frequency can be doubled for test purposes by switching this bit to 1, in functional mode only the default ‘0’ position is allowed.

10.11 The DSP core

For this chip a type of DSP core (the actual programmable embedded calculating machine) is used that is adapted to the required calculation power needed and as such is optimized on area. This DSP core is also known under the name EPICS6, of which EPICS is the generic name of this type of DSP and 6 is the version number. This DSP is mainly a calculator designed for real time processing of the digitized (at 38 or 44.1 kHz sample frequency) audio data stream. A DSP is especially suited to calculate the sum of products of the digital datawords representing the audio data.

10.12 DSP core status register and the external control pins

In the DSP core there is a 9 bit long status register. These 9 flags contain information which is used by the conditional branch logic of the DSP core. For direct use with the external world 4 flags are defined, F0, F1, F2 and F3. For external control two input pins, DSP_IN1 and DSP_IN2, have been implemented. These pins control the status of the flags F0 and F1. The two status flags F3 and F4 are controlled by the DSP core and can be read via the output pins DSP_OUT1 and DSP_OUT2. The functions of each pin depends on the DSP program. Another important flag is the I-flag. This flag is an input flag and is set the moment new I^2S data or another type of digital audio data is available to the DSP core.

10.13 I^2C control (SCL and SDA pin)

General description of the I^2C format in a booklet can be obtained at Philips Semiconductors, International Marketing and Sales.

For the external control of the CDSP chip a fast I^2C bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus. There are three different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters. (level, multipath etc.)
- Instructions controlling the DATA I^2S flow, like source selection, IAC control and clock speed

The detailed description of the I^2C bus and the description of the different bits in the memory map is given in paragraph: I^2C Bus control and commands.

10.14 I²S and SPDIF inputs

10.14.1 General description I²S inputs

For communication with external digital sources a I²S digital interface bus can be used. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7708 acts as a slave, so the external source is master and supplies the clock.

The digital audio input is capable of handling multiple input formats. For brevity the serial digital audio in- and outputs are called I²S. However this does not mean that the format is always the Philips I²S standard.

The I²S input is capable of handling Philips I²S, and LSB justified formats of 16, 18 and 20 bits word sizes, fs can vary from 32 kHz until 48 kHz.

See the I²C Memory Map for the bits that must be programmed, for selection of the desired I²S format.

See Fig. 10 for the general waveform formats of the four possible formats.

The number of bitclock (BCK) pulses may vary in the application. When the applied wordlength is smaller than 18 bits (internal resolution), the LSB bits will get internally a zero value.

When the applied wordlength exceeds 18 bits, the LSB's are skipped.

The input circuitry is limited in handling the number of BCK pulses per WS period. The maximum allowed number of bitclocks per WS period is 512.

10.14.2 The timing diagram of the communication is shown in Fig. 11.

The DSP program is synchronised with the external source via the word select signal. On every negative edge of the IIS_WS the I flag of the status register is set.

10.14.3 DIGITAL DATA STREAM FORMATS

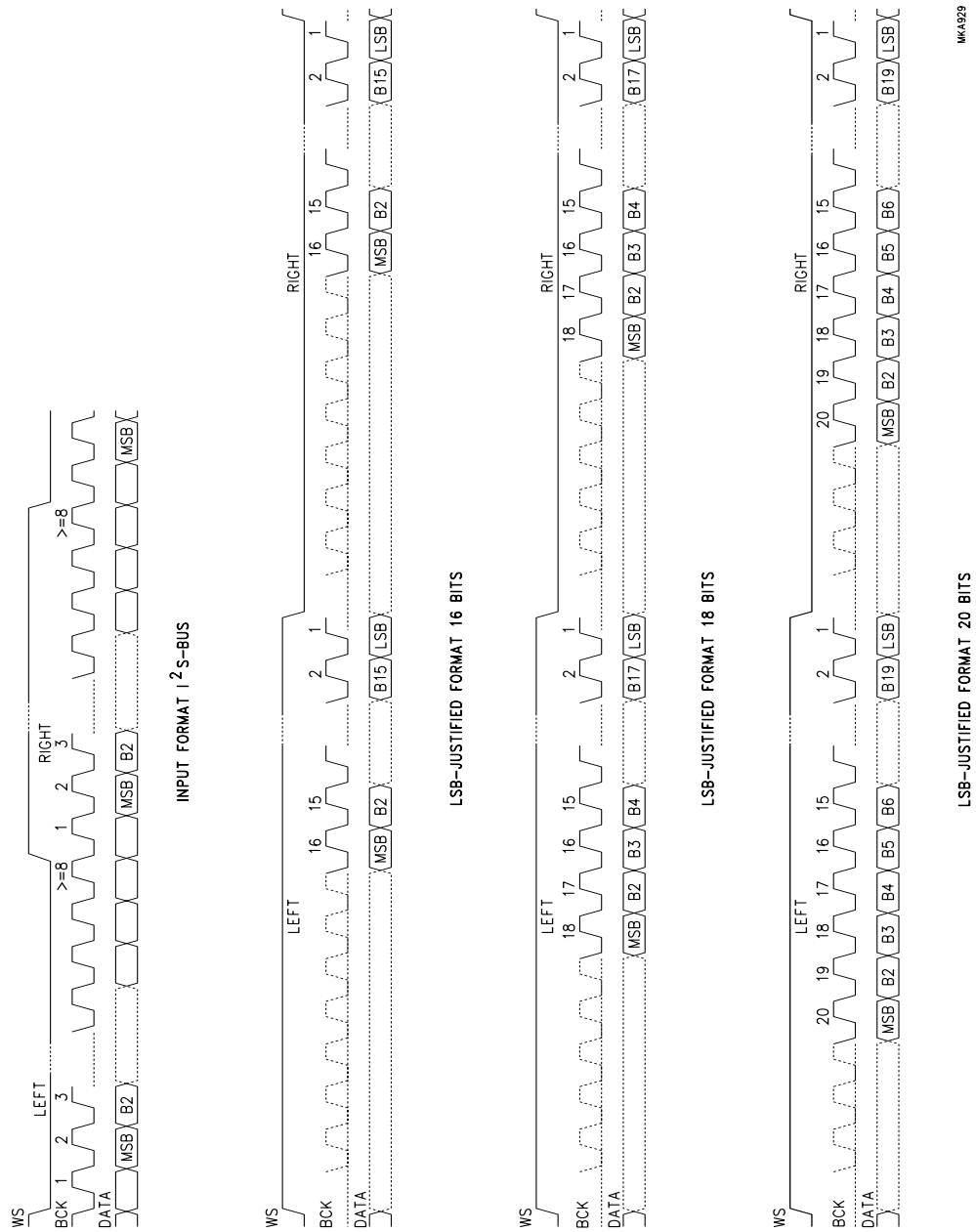


Fig. 10 All serial data in/output formats

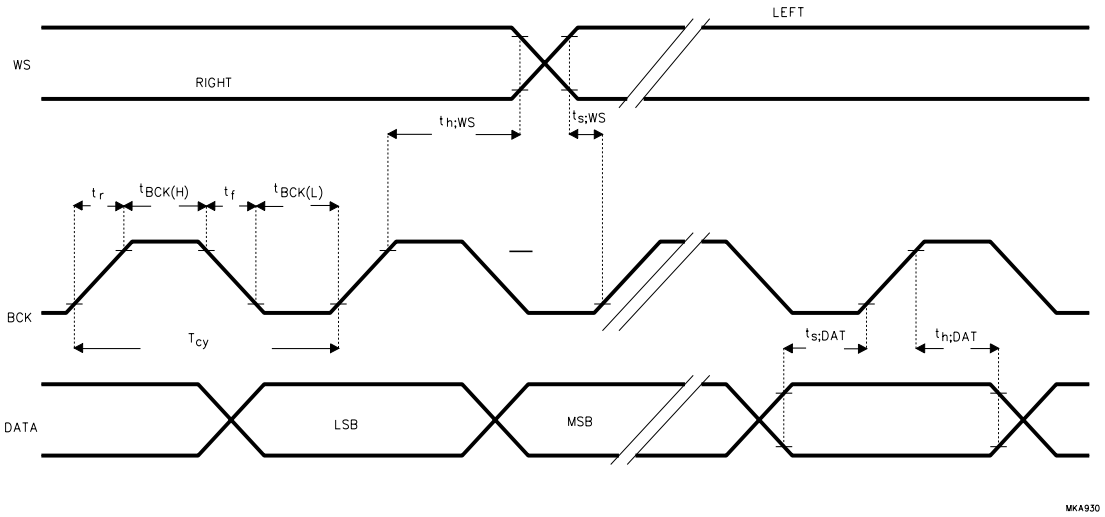


Fig. 11 Input timing digital audio data inputs

Table 4 Timing digital audio inputs/out (see Fig. 11)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NO
t_r	rise time	t_{cy}=50 nS	-	-	0.15*t_{cy}	ns	9.01
t_f	fall time	t_{cy}=50 nS	-	-	0.15*t_{cy}	ns	9.02
t_{cy}	bitclock cycle time		50	-	-	ns	9.03
$t_{BCK(H)}$	bitclock time HIGH	t_{cy}=50 nS	0.35*t_{cy}	-	-	ns	9.04
$t_{BCK(L)}$	bitclock time LOW	t_{cy}=50 nS	0.35*t_{cy}	-	-	ns	9.05
$t_{s;DAT}$	data setup time	t_{cy}=50 nS	0.2*t_{cy}	-	-	ns	9.06
$t_{h;DAT}$	data hold time	t_{cy}=50 nS	0.2*t_{cy}			ns	9.07
$t_{s;WS}$	wordselect setup time	t_{cy}=50 nS	0.2*t_{cy}	-	-	ns	9.1
$t_{h;WS}$	wordselect hold time	t_{cy}=50 nS	0.2*t_{cy}	-	-	ns	9.11

10.14.4 General description SPDIF INPUTS

For communication with external digital sources also a SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analogue PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock. Also a 64*Fs clock is regenerated out of the SPDIF datastream.

From the SPDIF signal a three wire (I2S like) serial bus is made, consisting of a Wordselect, Data and Bitclock line. The FS frequency depends solely on the SPDIF signal input accuracy.

This design does NOT handle the userdata-, channelstatus- and validitybits of the SPDIF stream, but only the audio is given at its outputs. The bits in the audio space are always decoded regardless of any statusbits e.g. 'copy protected', 'professional mode' or 'data mode'.

10.14.4.1 SPDIF format

The SPDIF format used here carries the 2 channel PCM audio over a two wire pair.

The SPDIF format can be partitioned into two main layers, being the abstract model of frames and blocks, and the channel modulation. Currently there are three samples frequencies specified:

Table 5 Sample Frequencies

SAMPLE FREQ [KHZ]	DATA-RATE [MBIT/S]	CHANNEL-RATE [MBIT/S]
44.1	2.8224	5.6448
48.0	3.072	6.144
32.0	2.048	4.096

10.14.4.2 SPDIF channel modulation

The digital signal is coded using “biphase-mark-code” (BMC), which is a kind of phase-modulation. In this scheme, a logic one in the data corresponds to two zero-crossings in the coded signal, and a logic zero to one zero-crossing

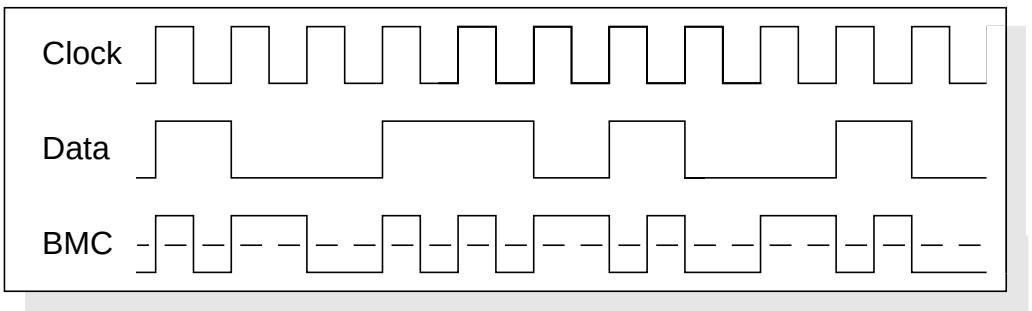


Fig. 12 BiPhase Mark Coding

The SPDIF interface of the SAA7708 is capable of decoding all standardized sampling frequencies with Level3 timing being the whole range of 28 kHz to 54 kHz sampling frequency. However the highest frequency posible is in fact due to the limited cycle budget of the DSP only 44.1 kHz.

10.14.4.3 Timing Characteristicse logic.

The SPDIF specification IEC 958, supports three levels of clock accuracy, being high-accuracy, normal accuracy and variable or pitch shifter clock mode.

- Level 1, high accuracy, tolerance of transmitting sampling frequency shall be within +50x10-6
- Level 2, normal accuracy, all receivers should receive a signal of +1000x10-6 of nominal sampling frequency
- Level 3, variable pitch shifted clock mode, adeviation of 12.5% of the nominal sampling frequency is possible

Rise and fall times are defined as:

Rise time = 100 x R(r) / (T(l)+T(h))%

Fall time = 100 x R(f) / (T(l)+T(h))%

Rise and fall times should be in the range:

0%-20%when the data bit is a “1”

0%-10%when the data bits are two succeeding

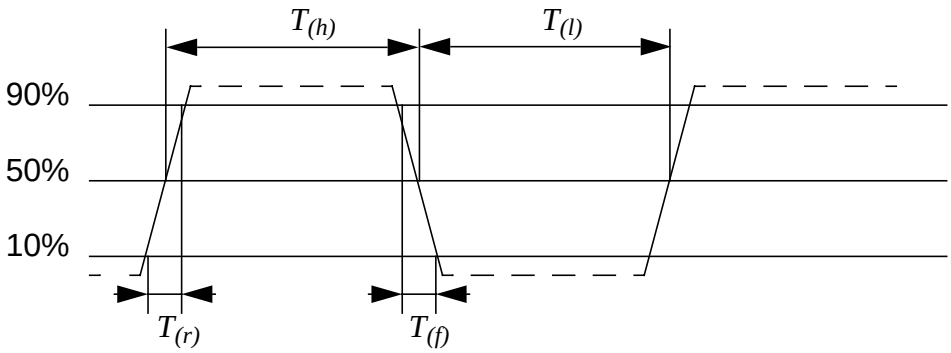


Fig. 13 Rise and fall times

Duty cycle shall be calculated using the equation:

Duty cycle = 100 x T(h) / (T(l)+T(h))%

Duty cycle shall be in the range:

40%-60% when the data bit is a logical “1”

45%-55% when the data bits are two succeeding “0”’s

10.15 RDS decoder (RDS_CLOCK / RDS_DATA pins)

The RDS decoder recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting. The (buffered) data is provided as output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with the EBU specification EN 50067.

The RDS decoder has three different functions:

- Clock and data recovery from the MPX signal
- Buffering of 16 bits if selected
- Interfacing with the micro controller

10.15.1 Clock and data recovery

The RDS-chain has a separate input FM_RDS. This enables RDS updates during tape play.

The RDS chain contains a third order sigma-delta AD convertor, followed by two decimation filters. The first filter passes the multiplex band including the signals around 57 kHz and reduces the sigma- delta noise. The second filter reduces the RDS bandwidth around 57 kHz.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder recovers the clock and data signals. These signals are output on the RDS-Clock and Data pins.

10.15.2 Timing of Clock and Data signals

The timing of the Clock and Data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 µs after the clock transition. The timing of the data change is 100 µs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microprocessor. The RDS timing is shown in Fig. 14.

During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

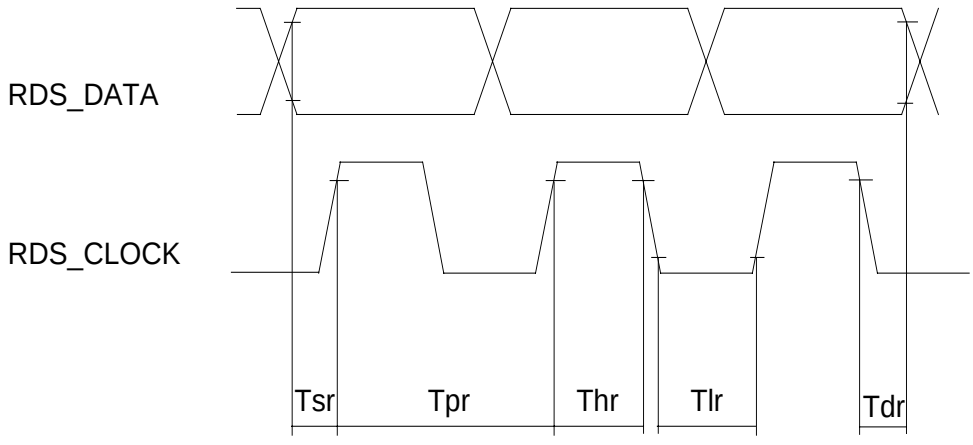


Fig. 14 RDS timing in the direct output mode

10.15.3 Buffering of RDS data

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microprocessor for every 842 uS. In a second mode, the RDS interface has a double 16 bit buffer.

10.15.4 BUFFER INTERFACE

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line in pulled down and the buffer is overwritten. The control microprocessor has to monitor the data line in at most every 13.5 msec. This mode is selected by setting the rds_clkin I^2C bit of the IIC_RDS_ConTrol register ($0FF3) (see Table 29) to “1”. In Fig. 15 the interface signals from the RDS decoder and the microcomputer in buffer mode are shown. When the buffer is filled with 16 bit the data line is pulled down. The data line will remain low until reading of the buffer is started by pulling down the clock line. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set high until the buffer is filled again. The microprocessor stops communication by pulling the line high. The data is written out just after the clock high-low transition. The data is valid when the clock is high.

When a new 16 bit buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.

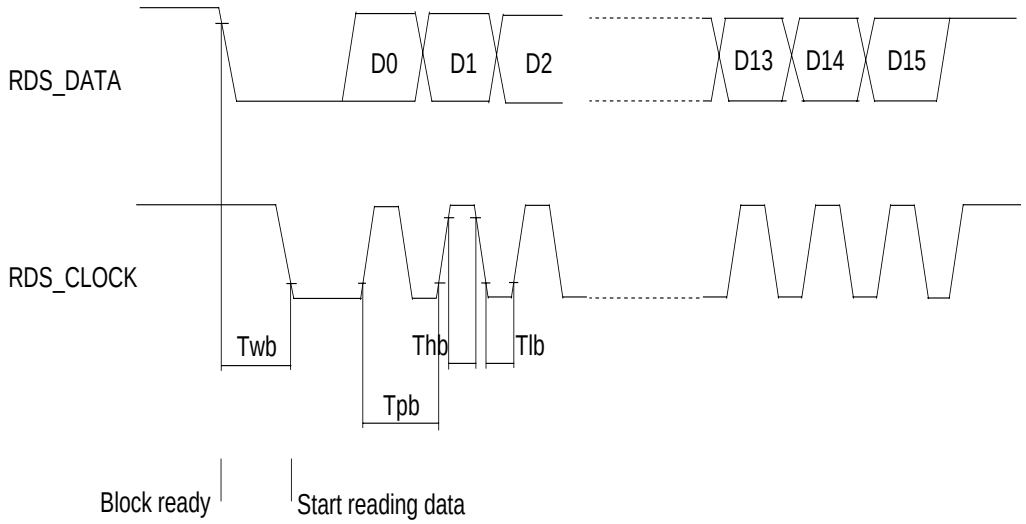


Fig. 15 Interface signals RDS decoder and microcomputer

10.16 DSP Reset

The reset pin is active low and has an internal pull-up resistor. Between this pin and the VDDD ground a capacitor should be connected to allow a proper switch on of the supply voltage. The capacitor value is such that the chip is in reset as long as the power supply is not stabilised. A more or less fixed relationship between the DSP reset (pin) and the POM (pin) time constant is obligatory. The voltage on the POM pin determines the current flowing in the DACs. At 0 V at the POM pin the DAC currents are zero and so also the DACs output voltages. At the VDDA2 voltage the DAC currents are at their nominal (maximal) value. Long before the DAC outputs get to their nominal output voltages, the DSP must be in working mode to reset the output register therefore the DSP time constant must be shorter than the POM time constant. For advised capacitors see the application diagram.

The reset has the following function:

- the bits of the IAC control register are set to their prefix values
- the bits of the IIC_SEL register are set to their prefix values
- the DSP status registers are reset
- the program counter is set to address $0000.

- the two output flags pin 40 and pin 41 are reset to 0

When the level on the reset pin is at logical high, the DSP program starts to run.

10.17 Power supply connection and EMC

The digital part of the chip has in total 7 positive supply line connections and 7 ground connections. To minimise radiation the chip should be put on a double layer pcb with on one side a large ground plane. The ground supply lines should have a short connection to this ground plane. A coil/capacitor network in the positive supply line can be used as high frequency filter.

11 ELECTRICAL CHARACTERISTICS

LIMITING VALUES in accordance with the Absolute Maximum Ratings system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
VDD_3	DC supply voltage		-0.5	5	V
VDD_5	DC supply voltage	Only valid for the voltages in connection with the 5 V I/O's	-0.5	6	V
DELVDD	Voltage difference between two VDDx pins			550	mV
+/-Iik	DC input clamp diode current	Vi<-0.5 V or Vi>VDD+0.5 V	-	10	mA
+/-Iok	DC output clamp diode current output type 4 mA	Vo<-0.5 V or Vo>VDD+0.5 V	-	20	mA
+/-Io	DC output source or sink current output type 4 mA	-0.5 V< Vo <VDD+0.5 V	-	20	mA
+/-Idd +/-Iss	DC VDD or VSS current per supply pin		-	750	mA
Tamb	Ambient operating temperature		-40	85	C
Tstg	Storage temperature range		-65	150	C
ESDV	ESD sensitivity				
	human body model	100 pF,1500 Ω	3000		V
	machine model	100 pF,2.5 µH, 0 Ω	300		V
LTCH	Latch up protection	CIC spec/test method	100		mA
P	Power dissipation per output			100	mW
Ptot	Total power dissipation			1600	mW

12 THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
Rth j-a-pcb	45	K/W

13 DC CHARACTERISTICS

digital I/O at Tamb=-40ºC~+85 ºC,Vd5=4.5~5.5 V, Vd3=3~3.6 V unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
V_{d3}	Operating supply voltage 3.3 Volt analog and digital	All VDD pins of the type VDD3 and VDDCO with respect to Vss all parts	3	3.3	3.6	V	1.01
V_{d5}	Operating supply voltage 5 Volt periphery	All VDD pins of the type VDD5 with respect to Vss all parts	4.5	5	5.5	V	1.02
IP_3	DC supply current of the 3.3 digital core part	high activity of the DSP at 31 MHz DSP frequency	-	57.4	78	mA	1.03
IP_5	DC supply current of the 5V digital periphery part		-	5	7	mA	1.04
IP_A	DC supply current of the analog part	At zero input and output signal	-	17.3	23.6	mA	1.05
Ptot	Total power dissipation	high activity of the DSP at 31 MHz DSP frequency	-	0.273	0.423	W	1.06
VIH	High level input voltage all digital inputs and I/O's	Pin types: IBUFU, BT4CR,BD4CR,B4CR, SCHMITCD,SCHMITC	70	-	-	$\%V_{d5}$	1.07
VIL	Low level input voltage all digital inputs and I/O's	Pin types: IBUFU, BT4CR,BD4CR,B4CR, SCHMITCD,SCHMITC	-	-	30	$\%V_{d5}$	1.08
Vhyst	Schmitt trigger hysteresis	Pin type: SCHMITCD,SCHMITC	1	1.3		V	1.09
VOH	High level output voltage digital outputs	Io=-4 mA, pin types: B4CR, BD4CR,BT4CR	Vd5-0.4	-	-	V	1.10
VOL	Low level output voltage digital outputs	VDD=4.5 V, Io=4 mA, pin types: B4CR, BD4CR,BT4CR	-	-	0.4	V	1.11
VOLI^2C	Low level output voltage digital I^2C data output	Io=8 mA, pin types: BD4SCI4	-	-	0.4	V	1.12
+/-Io	Output leakage current tristate outputs	Vout=0 or VDD voltage Pin types: BD4CR, BD4SCI4,BT4CR	-	-	5	µA	1.13
R_pull up	Internal pull up resistor to VDDD	Pin type: IBUFU	23	50	80	kΩ	1.14
R_pull down	Internal pull down resistor to VSSD	Pin type: SCHMITCD	23	50	80	kΩ	1.15
tri,tfi	Input rise and fall times	V_{d5}=5.5 V	-	6	200	ns	1.16
tro_min	Minimal output rise time	Vd5=5.5 V, Vd3=3.6 V, Tchip= -40 ºC, pintype= BD4CR, BT4CR, B4CR, Cload = 30 pF	7.6	-	18.4	ns	1.17

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
tro_max	Maximal output rise time	Vd5=4.5 V, Vd3=3 V, Tchip= 125 ºC, pintype= BD4CR, BT4CR, B4CR, Cload = 30 pF	13.7	-	33.4	ns	1.19
tfo_min	Minimal output fall time	Vd5=5.5 V, Vd3=3.6 V, Tchip= -40 ºC, pintype= BD4CR, BT4CR, B4CR, Cload = 30 pF	7	-	17	ns	1.21
	Minimal time between 1.5 and 3 V	Vd5=5.5 V, Vd3=3.6 V, Tchip= -40 ºC, pintype= BD4SCI4, Cload = 400 pF, Rpull-up = 550	63	-	-	ns	1.22
		Vd5=5.5 V, Vd3=3.6 V, Tchip= -40 ºC, pintype= BD4SCI4, Cload = 10 pF, Rpull-up = 550	21	-	-	ns	1.225
tfo_max	Maximal output fall time	Vd5=4.5 V, Vd3=3 V, Tchip= 125 ºC, pintype= BD4CR, BT4CR, B4CR,Cload = 30 pF	12.7	-	30.9	ns	1.23
	Maximal time between 1.5 and 3 V	Vd5=4.5 V, Vd3=3 V, Tchip= 125 ºC, pintype= BD4SCI4, Cload = 400 pF, Rpull-up = 550	-	-	197	ns	1.24
		Vd5=4.5 V, Vd3=3 V, Tchip= 125 ºC, pintype= BD4SCI4, Cload = 10 pF, Rpull-up = 550	-	-	184	ns	1.245

14 ANALOG INPUTS

Table 6 DC characteristics

DC characteristics analog inputs at Tamb=25 ºC; VDDA1=3.3 V unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
VDDA1	Supply voltage analog part ADC		3	3.3	3.6	V	2.01
VREFAD	common mode reference voltage SCAD1, 2 and Level AD	w.r.t. VDDA1/VSSA1	47	50	53	%VDDA1	2.02
ZOUT	Output impedance VREFAD		-	600	-	ohm	2.03
VDACP	Positive reference voltage SCAD1, SCAD2 and Level AD		3	3.3	3.6	V	2.04
IVDACP	Positive reference current SCAD1, SCAD2 and Level AD		-	-20	-	µA	2.05
VDACN1 VDACN2	Negative reference voltage SCAD1, SCAD2 and Level AD		-0.3	0	0.3	V	2.06
IVDACN1 IVDACN2	Negative reference current SCAD1 and 2		-	20	-	µA	2.07
AVO_SCAD	Input offset voltage SCAD1 and 2		-	+140	-	mV	2.09

Table 7 AC characteristics

AC characteristics analog level inputs at VDDA1=3.3 V; Tamb=25 ºC

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
ADSNR	Level AD converter SNR RMS (unweighted)	BW=0-29 kHz Max. input	48	54	-	dB	3.01
ADIRES	Input resistance		1.5		2.2	MΩ	3.02
ADICL	Input voltage range level AD for full scale		0		VDDA1	V	3.03
ADOS	DC-offset voltage		-	-	60	mV	3.04
ADDEC	decimation filter attenuation		20			dB/Dec	3.05
ADPCOF	pass band cutoff freq.	at - 3 dB and DCS clock = 9.728 MHz		29		kHz	3.06
ADSF	sample rate after decimation	DCS clock = 9.728 MHz		38		kHz	3.07

Table 8 Analog AC inputs:

Analog AC inputs SCAD1,2, VDDA1=3.3 V; Tamb=25 ºC

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
AILVL	maximum conversion input level at AD input	THD < 1%	0.6	0.66	-	Vrms	3.08
AIIRG	input resistance AM, CD, TAPE		1	-	-	MΩ	3.09
AIIRM	input resistance FM_MPX		31	45	60	kΩ	3.10
AITHDM	THD FM_MPX input	1 kHz 1.1 Vrms, BW= 19 kHz, I²C default setting	-	-70 0.03	-65 0.056	dB %	3.11
AISNRM	SNR FM_MPX input mono	1 kHz, BW=19 kHz, 0 dB ref. = 1.1 Vrms, I²C default setting	80	83	-	dB	3.12
AISNRSS	SNR FM_MPX input stereo	1 kHz, BW=40 kHz, 0 dB ref. = 1.1 Vrms, I²C default setting	74	77	-	dB	3.13
AITHDC	THD CD Inputs not multiplex mode	1 kHz, 0.55 Vrms, BW=20 kHz	-	-80 0.01	-76 0.016	dB %	3.14
AISNRC	SNR CD Inputs not multiplex mode	1 kHz, BW=20 kHz, 0 dB ref.= 0.55 Vrms	81	84	-	dB	3.15
AITHDA	THD AM mono input, not multiplex mode	1 kHz, 0.55 Vrms, BW=5 kHz	- -	-80 0.01	-76 0.016	dB %	3.16
AISNRA	SNR AM mono input, not multiplex mode	1 kHz, BW=5 kHz, 0dB ref. = 0.55 Vrms	83	88	-	dB	3.17
AITHDT	THD Tape input, multiplex mode	1 kHz, BW = 20 kHz, 0.55 Vrms	-	-80 0.01	-76 0.016	dB %	3.18
AISNRT	SNR Tape input, multiplex mode	1 kHz, BW= 20 kHz, 0 dB ref. = 0.55 Vrms	70	77	-	dB	3.19

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
à19	Carrier and harmonic suppression at the output with and without modulation	pilot sig. f=19 kHz	-	81	-	dB	3.21
		no mod	-	98	-	dB	3.22
à38		subcarrier f=38 kHz	-	83	-	dB	3.23
		no mod	-	91	-	dB	3.24
à57	(for 19 kHz, incl. notch (See note 1)	subcarrier f=57 kHz	-	83	-	dB	3.25
		no mod	-	96	-	dB	3.26
à76		subcarrier f=76 kHz	-	84	-	dB	3.27
		no mod	-	94	-	dB	3.28
à2	Intermodulation (see note 2)	fmod=10kHz,f spur=1kHz	77	-	-	dB	3.29
à3		fmod=13kHz,f spur=1kHz	76	-	-	dB	3.30
à57VF	Traffic radio (see note 3)	f=57 kHz	-	110	-	dB	3.31
à67	SCA (note 4)	f=67 kHz	-	110	-	dB	3.32
à114	Adjacent channel interference (note 5)	f=114 kHz	-	110	-	dB	3.33
à190		f=190 kHz	-	110	-	dB	3.34
Vi-pil	pilot threshold voltage (pin 40)	stereo on	-	22.2	-	mVrms	3.35
		stereo off	-	22.1	-	mVrms	3.36
H	hysteresis of Vi-pil		-	0	-	dB	3.37
AIFR	input freq. range MPX	-3 dB, AD via bitstream test output	0	-	55	kHz	3.38
AISEP	FM-stereo channel separation	1 kHz	40	45	-	dB	3.39
		10 kHz	25	30	-	dB	3.40
AIAFR	Audio freq. response FM	at -3 dB via DSP at DAC output	17	-	-	kHz	3.41
AIOGV	overall gain unbalance Left/Right TAPE, CD, AM	Multiplex mode, 1 kHz, SW compensated	-	-	2	dB	3.42
AIOGVNM	overall gain unbalance Left/Right TAPE, CD, AM	Not multiplexed, 1 kHz	-	-	0.5	dB	3.425
AICST	Channel separ. TAPE, CD	1 kHz, SW compensated	40	50	-	dB	3.43
AIFRT	Freq. response TAPE, CD for fs=38 kHz	at -3 dB	18	-	-	kHz	3.46
AICRI	Crosstalk between inputs	1 kHz	65	-	-	dB	3.47
		15 kHz	50	-	-	dB	3.48

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
PSRRAD	Power Supply Ripple Rejection MPX and RDS ADCs (output via I^2S), ADC input shorted	Fripple = 1 kHz Vripple = 100 mVpeak; Cvrefad = 22 μF; Cvdacpm = 10 μF;	35	45	-	dB	3.49
PSRRLD	Power Supply Ripple Rejection Level AD (output via DAC) ADC input shorted	Fripple = 1 kHz Vripple = 100 mVpeak; Cvrefad = 22 μF;	29	39	-	dB	3.50
CMRRCD	Common Mode Rejection Ratio in CD input mode	R CD_GND = 1 MΩ, R CD Player GND cable < 1kΩ Fin= 1 kHz	60	-	-	dB	3.51
PHONE_THD	THD Phone input at max. input voltage	Vin=0.75 Vrms, F=1 kHz	40	-	-	dB	3.52
PHONE_CMRR	Common mode rejection ratio phone input	Vin=0.75 Vrms, F=1 kHz	50	-	-	dB	3.53
PHONE_RIN	Input resistance phone input					kΩ	3.54
PHONE_IPLEV	Maximum input level	F=1 kHz	0.75 Vrms	-	-	V	3.55

Table 9 Analog AC input SCAD2

RDS input

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
ARLVL	maximum conversion input level	THD < 1%	0.6	0.66	-	Vrms	4.01
ARIR	Input resistance FM_RDS		31	-	164	kΩ	4.02
ARTHD	Distortion RDS AD	fc = 57 kHz	-60	-67	-	dB	4.03
ARSNR	Signal to noise ratio RDS AD	BW = 6 kHz, fc = 57 kHz, 0 dB ref. = 1.1 Vrms	54	-	-	dB	4.04
ARPA	Pilot attenuation RDS		50	-	-	dB	4.05
ARNS	Nearby selectivity RDS	neighbour channel at 200 kHz distance	61			dB	4.06
ARNA	RDS AD converter noise attenuation		70			dB	4.07

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
ARPR	Pass band ripple RDS	2.4 kHz BW	-	-	0.5	dB	4.08
ARMA	Multiplex attenuation RDS	mono	70	-	-	dB	4.09
		stereo	40	-	-	dB	4.10
ARAFD	Allowable frequency deviation 57 kHz RDS	Max Crystal deviation of 100 ppm	-	-	6	Hz	4.11

Table 10 Analog SPDIF

SPDIF input 1 and 2

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
SPVL	AC input level		0.2	0.5	3.3	Vpp	11.01
SPIR	Input resistance	@ 1 kHz	-	6	-	kΩ	11.02
SPHYS	Hysteresis of input		-	40	-	mV	11.03

15 ANALOG OUTPUTS

Table 11 DC characteristics analog outputs at Tamb= 25 ºC; VDDA2= 3.3 V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
VREFDA	Voltage on VREFDA pin	w.r.t. VDDA2/VSSA2	47	50	53	%	5.01
IMPP_VREF	Impedance VREFDA to VDDA2 pin		-	40	-	kΩ	5.02
IMPG-VREF	Impedance VREFDA to VSSA2 pin		-	40	-	kΩ	5.03
VOUT_AC	Output voltage AC of Op-Amp outputs at max. I^2S signal	Rload > 5 kΩ AC	0.65	0.75	0.85	Vrms	5.05
VOUT_DC	Average DC output voltage	Rload > 5 kΩ AC	1.5	1.65	1.8	V	5.06
I_POML	Pull-up current to VDDA2 on POM pin	Voltage on POM pin < 0.6 V	3.3	-	5	µA	5.073
I_POMH	Pull-up current to VDDA2 on POM pin	Voltage on POM pin > 0.8 V	50	-	75	µA	5.076
PSRRDA	Power Supply Ripple Rejection DACs (input via I^2S)	Fripple = 1 kHz Vripple = 100 mVpeak Cvref = 22 µF	45	60	-	dB	5.08

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
UNBAL	max. deviation in output level (plus or minus) of the 4 DAC current outputs w.r.t. the average of the 4 outputs	Full scale output. No phone, no fader	-	-	0.38	dB	5.085
XT	Crosstalk between outputs in the audio band Left or right outputs dig. silence, other max. volume		-	-	-69	dB	5.09
ISC	Output short circuit current	Output short circuit to ground	-	-	20	mA	5.10
DAC_Rs	DAC resolution			18		bit	5.11
THD&N/S	Total harmonic distortion +noise vs Output Signal	f = 1 kHz, Vout=0.72 Vrms	-	-75	-65	dBA	5.12
DRAN	Dynamic Range (ref. Vout=0.75 Vrms=0 dB)	f = 1 kHz, -60 dB	92	102	-	dBA	5.13
DSIL	DSIL Digital Silence (ref. Vout=0.75 Vrms=0 dB)	f=20 Hz-17 kHz A-weighted	-	108	102	dBA	5.14
DSNS	Digital Silence Noise level at output	A-weighted	-	3	8	µVrms	5.15
IM	Intermodulation distort./comp	f = 60 Hz and 7 kHz ratio 4: 1	-	-70	-55	dB	5.16
MASF	Maximum sample frequency		48	-	-	kHz	5.17
B	Bandwidth D/A	at - 3 dB		Fs/2			5.18
DAC-Cload	Allowed load capacitance on DAC outputs		-	-	2.5	nF	5.19
DAC-Rload	Allowed load resistor on DAC voltage outputs	Only AC coupled	5	-	-	kΩ	5.20

16 OSCILLATOR

Table 12 Oscillator specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
XTFREQ	X-tal frequency			11.2896		MHz	6.01
	Adjustment tolerance	Tamb = 25 ^{0}C	-30	-	+30	ppm	6.02
	temperature drift		-30	-	+30	ppm	6.03
XSPFRAT	Spurious frequency attenuation		20	-	-	dB	6.04
XVOLT	Voltage across the crystal		-	3	-	V	6.05
XTRCUN	Trans conductance (gm)	At start-up	10.5	19	32	mS	6.06
XTROSC	Transconductance (gm)	In operating range	3.6	-	38	mS	6.07
XLOAD	Load capacitance		-	15	-	pF	6.08
NRCYC	Number of cycles in start up time	Depends on quality of the external crystal	-	1000	-	cycles	6.09
IP_XTAL	Supply current	At start-up	-	7	15	mA	6.10
IP_XTAL	Supply current	At oscillation	-	0.6	2	mA	6.11
XTAL_DL	Drive level	At oscillation	-	0.4	0.5	mW	6.12
XTAL_INP	External clock input	in slave mode	3	3.3	5	V	6.13
RXTAL	Allowed loss resistor of the crystal	Cp = 6pF, Cx1 = 18 pF, Cx2 = 18 pF.	-	20	100	Ω	6.15

17 RDS TIMING

Table 13 Timing of the RDS interface (see Fig. 14and Fig. 15)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
Frdscl	nominal clock frequency RDS clock		-	1187.5	-	Hz	8.01
Tsr	Clock set-up time		100	-	-	µs	8.02
Tpr	Periodic time		-	842	-	µs	8.03
Thr	Clock high time		220	-	640	µs	8.04
Tir	Clock low time		220	-	640	µs	8.05
Tdr	Data hold time		100	-	-	µs	8.06
Twb	Wait time		1	-	-	µs	8.09
Tpb	Periodic time		2	-	-	µs	8.10
Thb	Clock high time		1	-	-	µs	8.11
Tlb	Clock low time		1	-	-	µs	8.12
Fexcl	input frequency Extern RDS-Clock		-	-	22	MHz	8.13

18 SUPPLY CURRENTS

Table 14 Current per supply pin or pin group

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
Vd3	Operating supply voltage 3.3 Volt analog and digital	with respect to Vss all parts	3.0	3.3	3.6	V	7.01
Vd5	Operating supply voltage 5 Volt periphery	with respect to Vss all parts	4.5	5	5.5	V	7.02
IP3	DC supply current of the 3.3 digital core part	high activity of the DSP at 27 MHz DSP frequency	-	57.4	68	mA	7.03
IP5	DC supply current of the 5V digital periphery part	Without external load to ground	-	5	7	mA	7.04
IPAD	Supply current of the AD's	At zero input and output signal	-	11	15	mA	7.05

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NO
IPDAC	Supply current of the DAC's and SPDIF block	At zero input and output signal	-	4.3	5.8	mA	7.06
IP_XTAL	Supply current XTAL oscillator and PLL's	Functional mode	-	2	2.75	mA	7.07
Ptot	Total power dissipation		-	0.273	0.423	W	7.08

19 I²C BUS CONTROL AND COMMANDS

19.1 Characteristics of the I²C Bus

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the VDD via a pull-up resistor when connected to the output stages of a micro controller. For a 400 kHz I²S the recommendation for this type of bus from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 - 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

19.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz. To be able to run on this high frequency all the In-Outputs connected to this bus must be designed for this high speed I²C bus according the Philips specification. See Fig. 16.

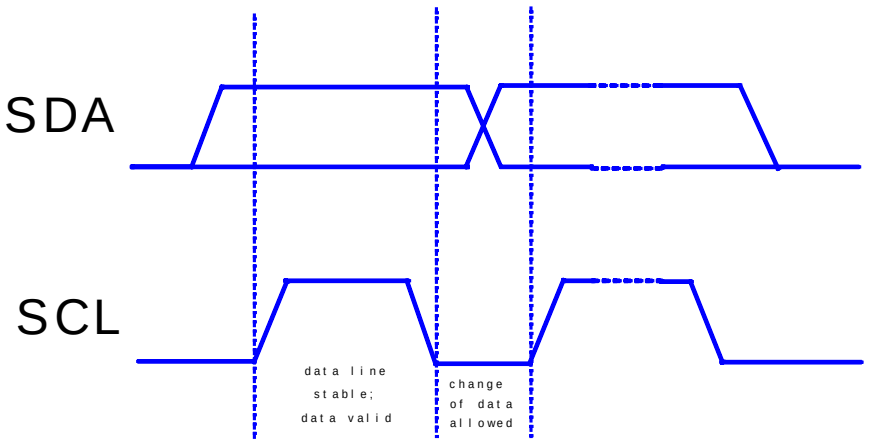


Fig. 16 Bit transfer on the I²C bus

19.3 Start and stop conditions

Both data and clock line will remain HIGH when the bus in not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P). See Fig. 17.

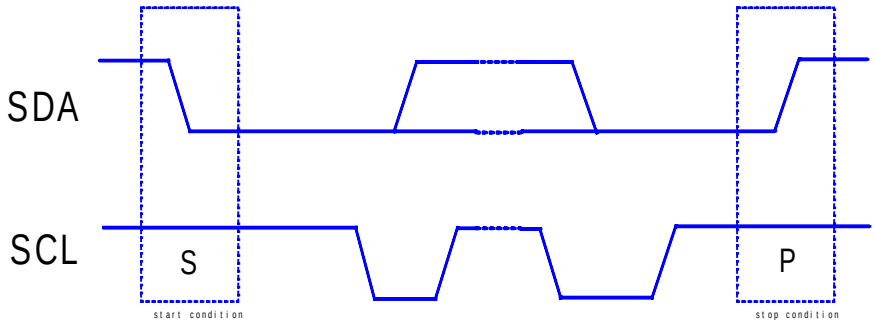


Fig. 17 START and STOP condition

19.4 Data transfer

A device generating a message is a “transmitter”, a device receiving a message is the “receiver”. The device that controls the message is the “master” and the devices which are controlled by the master are the “slaves”. See Fig. 18.

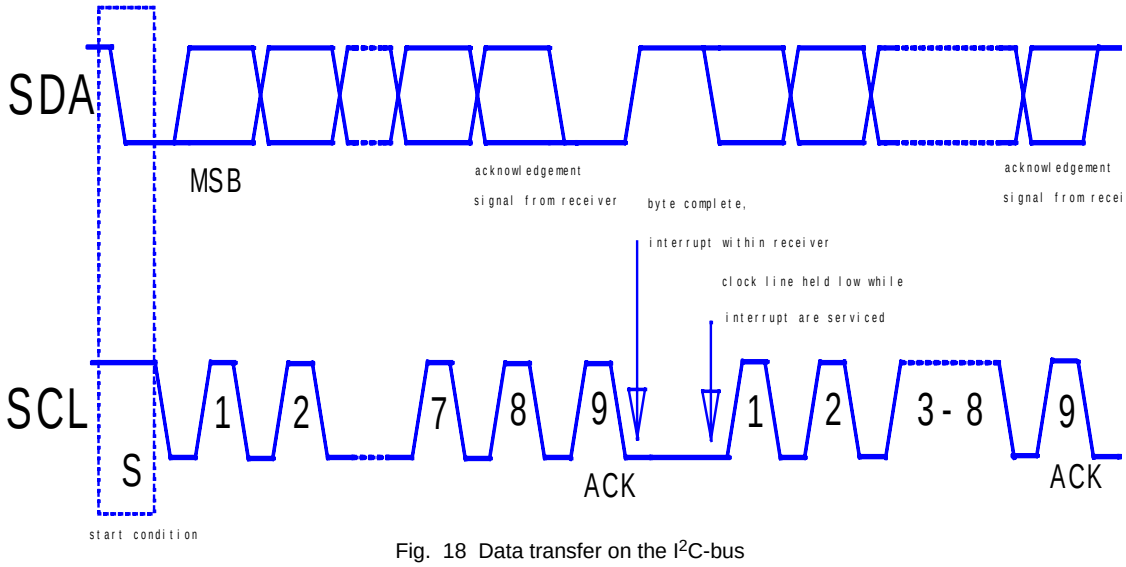


Fig. 18 Data transfer on the I^2C-bus

19.5 Acknowledge

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA

line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. See Fig. 19.

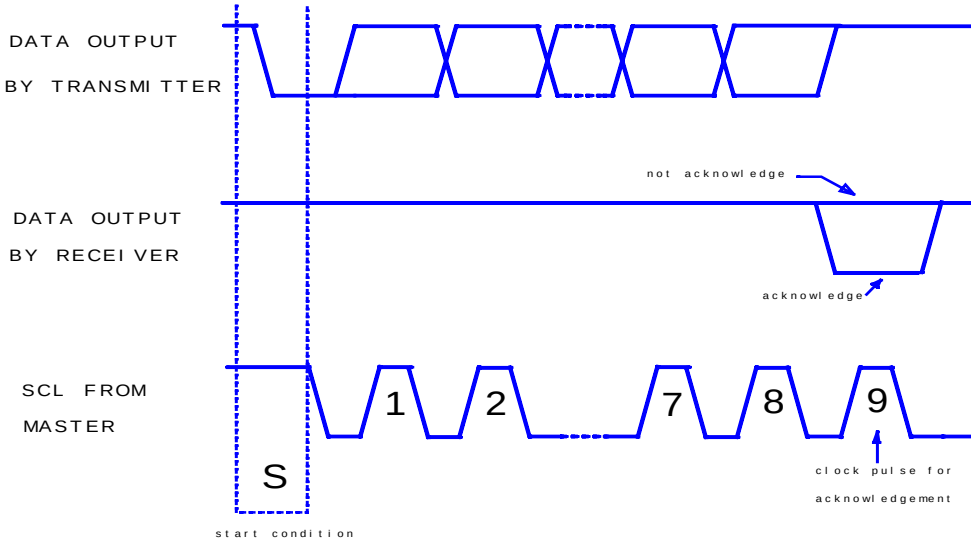


Fig. 19 Acknowledge on the I²C bus.

20 I²C BUS FORMAT

20.1 Addressing

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

20.2 Slave address (A0 pin)

The CDSP acts as slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The CDSP slave address is shown in table Table 15.

Table 15 Slave address

MSB							LSB
0	0	1	1	1	0	A0	R/$\overline{W}$

The sub address bit A0 corresponds to the hardware address pin A0 which allows the device to have 2 different addresses. The A0 input is also used in test mode as serial input of the test control block.

20.3 CDSP write cycles

The I²C bus configuration for a WRITE cycle is shown in table Table 16. The write cycle is used to write the bytes to control the DCS block, the PLL for the DSP clock generation, the IAC settings, the AD volume control settings, the analog input selection, the format of the I²S and some other settings. More detail can be found in the I²C memory map, Table 19.

Table 16 Master transmitter writes to the CDSP registers.

		R/W	**ACKN. CDSP**		**ACKN. CDSP**		**ACKN. CDSP**		**ACKN. CDSP**		**ACKN. CDSP**		**ACKN. CDSP**	
S	0011100	0	A	AddrH	A	AddrL	A	DataH	A	DataM	A	DataL	A	P
								auto increment if repeated n-groups of 3 (2) bytes						

S	= Start condition
P	= Stop condition
A	= Acknowledge from CDSP
AddrH and AddrL	= Address DSP register
DataH, DataM and DataL	= Data of XRAM or registers
DataH and DataM	= Data of YRAM

The datalength is 2 bytes or 3 bytes depending of the accessed memory. If the Y-memory is addressed the data length is 2 bytes, in case of the X-memory the length is 3 bytes. The slave receiver detects the address and adjusts the number of bytes accordingly.

20.4 CDSP READ cycles

The I²C bus configuration for a read cycle is shown in table Table 17. The read cycle is used to read the data values from XRAM or YRAM. The master starts with a start condition S, the CDSP address ‘0011100’ and a ‘0’ (Write) for the read/write bit. This is followed by an acknowledge by the CDSP. Then the Master writes the memory address High and memory addres Low where the reading of the memory content of the CDSP must start. The CDSP acknowledges these addresses both. Then the master generates a repeated Start (Sr) and again the CDSP address ‘0011100’ but this time followed by a ‘1’ (Read) of the read/write bit. From this moment on the CDSP will sent the memory content in groups of 2 (Y-memory) or 3 (X-memory) bytes to the I²C bus each time acknowledged by the Master. The Master stops this cycle by generating a Negative Acknowledge, then the CDSP frees the I²C bus and the Master can generate a Stop condition. The data is transferred from the DSP register to the I²C register at execution of the MPI instruction in the DSP program.

Table 17 Master transmitter reads from the CDSP registers.

		R/W	ACKN. CDSP		ACKN. CDSP		ACKN. CDSP			R/W	ACKN. CDSP		ACKN. MASTER		ACKN. MASTER		ACKN. MASTER		NA. MASTER	
S	0011100	0	A	AddrH	A	AddrL	A	Sr	0011100	1	A	DataH	A	DataM	A	DataL	A		NA	P
												auto increment if repeated n-groups of 3 (2) bytes						R		

S	= Start condition
Sr	= repeated Start condition
P	= Stop condition
A	= Acknowledge from CDSP (SDA low)
R	= Repeat n-times the 2 or 3 byte data group
NA	= Negative Acknowledge Master (SDA high)
AddrH and AddrL	= Address DSP register
DataH, DataM and DataL	= Data of XRAM or registers
DataH and DataM	= Data of YRAM

Table 18 Timing fast I2C-bus(see Fig. 20)

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT	NO
			MIN.	MAX.	MIN.	MAX.		
f_{SCL}	SCL clock frequency		0	100	0	400	kHz	10.01
t_{BUF}	Bus free between a STOP and Start Condition		4.7	-	1.3	–	µS	10.02
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	-	0.6	-	µS	10.03
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µS	10.04
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µS	10.05

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT	NO
			MIN.	MAX.	MIN.	MAX.		
$t_{SU;STA}$	Set-up time for a repeated start condition		4.7	-	0.6	-	µS	10.06
$t_{HD;DAT}$	DATA hold time		0	-	0	0.9	µS	10.07
$t_{SU;DAT}$	DATA set-up time		250	-	100	-	nS	10.08
t_r	Rise time of both SDA and SCL signals	C_b in pF	-	1000	20 + 0.1C_b	300	nS	10.09
t_f	Fall time of both SDA and SCL signals	C_b in pF	-	300	20 + 0.1C_b	300	nS	10.10
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	0.6	-	µS	10.11
C_b	Capacitive load for each bus line		-	400	-	400	pF	10.12
t_{SP}	Pulse width of spikes to be suppressed by input filter		n/a	n/a	0	50	nS	10.13

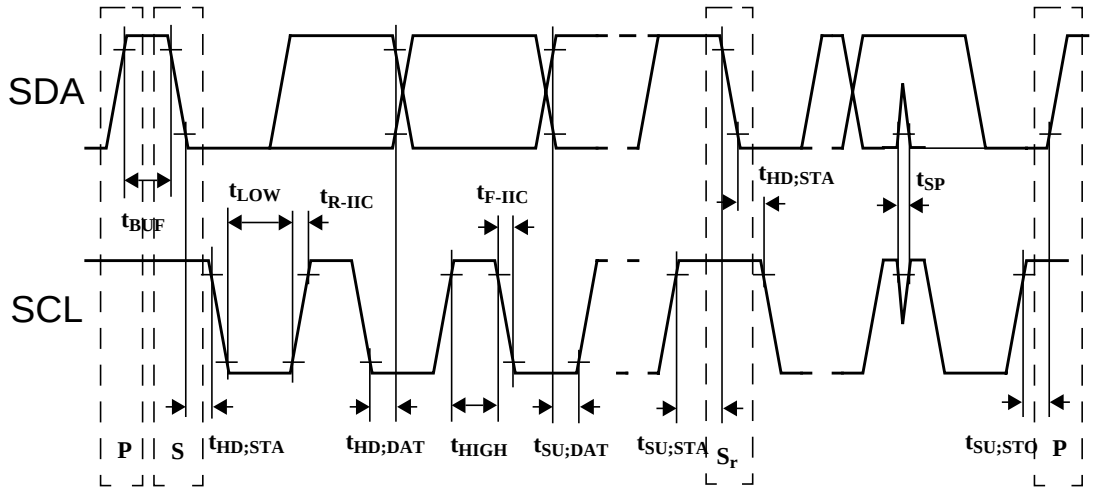


Fig. 20 Definition of timing on the I²C-bus

20.5 I²C memory map specification

The I²C Memory map contains all defined I²C bits. The map is split up in two different sections, hardware memory registers and the RAM definitions. In Table 19 the preliminary memory map is depicted. Table 20 shows the detailed memory map locations.

Table 19 I²C memory map

$8000 - $9FFF	Reserved	
$1000 - $7FFF	Not Used	
$0FFB - $0FFF	EPICS6	5 *16 bits
$0A00 - $0FFA	Reserved	
$0980 - $09FF	Reserved YRAM space	
$0800 - $097F	YRAM	384*12 bits
$0200 - $07FF	Not Used	
$0180 - $01FF	Reserved XRAM space	
$0000 - $017F	XRAM	384*18 bits

Table 20 I²C memory map overview

EPICS6	#REGISTER
IIC_DSP_CNTR	$0FFF
IIC_SELECTION	$0FFE
IIC_ADDA	$0FFD
IIC_LEVEL_IAC	$0FFC
IIC_IAC	$0FFB

20.6 I²C Memory map definition

Table 21 IIC_DSP_CNTR register ($0FFF)

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS.
loopo_on_off	1	Loopo on (1) or off (0)	off	0
bypass_pll	1	Bypasses the PLL with the Oscillator clock signal (1) or PLL active (0)	PLL active	1
PLL_div	4	PLL clock division factor (see Table 30)	176	5-2
dsp_turbo	1	Double PLL output frequency (1)	disable	6
pc_reset	1	Program Counter Reset (1)	no-reset	7
Not Used	8	-	-	15 - 8

Table 22 IIC_SELECTION register ($0FFE)

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS.
phone_vol	5	Phone volume settings according Table 2	1111d (mute)	4 - 0
audio_source	2	Selection AUDIO register according Table 36	ISN	6, 5
audio_format	3	AUDIO register data format according Table 37	ISN	9 - 7
dac_hold	1	Hold sign magnitude data stream (1) going to DAC	no-hold	10
sel_SPDIF	1	Select SPDIF1 (0) or SPDIF2 (1) input	SPDIF1	11
adc_bw_switch	1	Switching SCAD1, SCAD2 and level_AD from 38KHz (0) to 44.1KHz (1) based processing	38KHz	12
locked_preset	1	DCS clock locked (1) or preset (0)	locked	13
gain_h_l	1	Variable loop-gain stereo decoder high (1) or low (0)	high	14
Not Used	1	-	-	15

Table 23 IIC_ADDA register ($0FFD)

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS.
pcs_ad_sel	1	Select two input sensitivities, 200 mVrms (0) or 65 mVrms (1)	200 mVrms	0
en_38_clk	1	Disable 38 kHz Fs clock (0) for pseudo stereo	disable	1
sw_ad1	1	Right (0) vs Left (1) AD channel select according Table 3	Right	2
s1_2	1	CD (0) vs Tape (1) select according Table 3	CD	3
s4_5	1	Tape/CD (0) vs AM (1) select according Table 3	TAPE/CD	4
s6_7	1	AD left channel (0) vs Phone (1) select according Table 3	AD left channel	5
s8_9	1	FM/RDS_MPX (0) vs AD right channel (1) select according Table 3	FM/RDS_MPX	6
rds_cd_sel	1	FM/RDS_MPX (0) vs AD right channel (1) select according Table 3	FM/RDS_MPX	7
rds_clk_in	1	Select RDS output (0) or buffered RDS with RDS clock input (1)	RDS out	8
Not Used	1	-	-	9
s10	1	Selection switch CD_GND (0) or AUX_GND (1) pin	CD_GND	10
s11	1	Selection switch internal Midref-voltage reference (0) or external ground pin (1)	Midref	11
FR_b	1	Enable phone signal (1) to DAC front right output	disable	12
FL_b	1	Enable phone signal (1) to DAC front left output	disable	13
wide_narrow	1	Audio+RDS info (0) or audio data (1)	audio + RDS	14
Not Used	1	-	-	15

Table 24 IIC_LEVEL_IAC register ($0FFC)

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS.
lev_iac_threshold	4	IAC level threshold setting (see Table 26). At '0000' Level IAC is switched off	Level IAC on at 0.063	3 - 0
lev_iac_feedforward	2	IAC level deviaton feed forward factor (see Table 27)	0 periods	5, 4
lev_iac_stretch	2	IAC level stretch time (see Table 28)	13 periods	7, 6
lev_dyn_iac_dev	2	the deviation threshold frequency setting of the dynamic IAC (see Table 29)	74 kHz	9, 8
lev_en_dyn_iac	1	enables FM frequency sweep dependent IAC (1)	1	10
fader_vol	5	Fader volume regulator settings according Fig. 8 in position number 15	01111	15 - 11

Table 25 IIC_IAC register ($0FFB)

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS.
Threshold	3	Threshold sensitivity (see Table 31)	0.031	2 - 0
feed_forward	3	Deviation feed forward factor (see Table 32)	0.01172	5 - 3
Suppression	3	Stretch time suppression (see Table 33)	5 samples	8 - 6
MPX_delay	2	Delay settings MPX (see Table 34)	5 periods	10, 9
AGC	1	AGC set point 1/256 (1) or 1/128 (0)	1/256	11
GDC	3	Group delay compensation (see Table 35)	1200 ns	14 - 12
IAC_trigger	1	IAC output (1) or DSP_OUT2 output selection	DSP	15

20.7 Table definitions

Table 26 Level IAC theshold settings

IIC VALUE				THRESHOLD (DECIMAL VALUE)	THRESHOLD (BINARY VALUE)
Bit3	Bit2	Bit1	Bit0		
0	0	0	0	Level IAC off	Level IAC off
0	0	0	1	0.02	0.0000010
0	0	1	0	0.025	0.0000011
0	0	1	1	0.0316	0.0000100
0	1	0	0	0.04	0.0000101
0	1	0	1	0.05	0.0000110
0	1	1	0	0.063(prefix)	0.0001000 (prefix)
0	1	1	1	0.08	0.0001010
1	0	0	0	0.1	0.0001101
1	0	0	1	0.126	0.0010000
1	0	1	0	0.16	0.0010100
1	0	1	1	0.2	0.0011010
1	1	0	0	0.25	0.0100000

1	1	0	1	0.316	0.0101000
1	1	1	0	0.4	0.0110100
1	1	1	1	0.5	0.1000000

Table 27 IAC level deviaton feed forward factor

IIC VALUE		DELAY (DECIMAL VALUE) IN PERIODS OF 304 KHZ
Bit5	Bit4	
0	0	-2
0	1	-1
1	0	0(prefix value)
1	1	1

Table 28 IAC level stretch time

IIC VALUE		PULSE LENGTH ON SINGLE TRIGGER IN PERIODS OF 304 KHZ
Bit7	Bit6	
0	0	9
0	1	11
1	0	13 (prefix value)
1	1	15

Table 29 Dynamic IAC deviation threshold

CODE		DEVIATION KHZ	VALUE
BIT 9	BIT 8		
0	0	42	0.26
0	1	48	0.30
1	0	57	0.35
1	1	70	0.39(prefix)

Table 30 IIC PLL division settings

VALUE				DIVISION FACTOR N
PLL_DIV(3) BIT 15	PLL_DIV(2) BIT 14	PLL_DIV(1) BIT 13	PLL_DIV(0) BIT 12	
0	0	0	0	93
0	0	0	1	99
0	0	1	0	106
0	0	1	1	113
0	1	0	0	121
0	1	0	1	126
0	1	1	0	132
0	1	1	1	137
1	0	0	0	143

VALUE				DIVISION FACTOR N
PLL_DIV(3) BIT 15	PLL_DIV(2) BIT 14	PLL_DIV(1) BIT 13	PLL_DIV(0) BIT 12	
1	0	0	1	148
1	0	1	0	154
1	0	1	1	159
1	1	0	0	165
1	1	0	1	170
1	1	1	0	176 (prefix)
1	1	1	1	181

Table 31 IIC IAC Threshold settings

VALUE			THRESHOLD (DECIMAL VALUE)	THRESHOLD (BINARY VALUE)
BIT 2	BIT 1	BIT 0		
1	0	0	0.027	0.000001110000
1	0	1	0.031 (prefix)	0.000010000000
1	1	0	0.038	0.000010011100
1	1	1	0.047	0.000011000000
0	0	0	0.055	0.000011100000
0	0	1	0.063	0.000100000000
0	1	0	0.074	0.000100110000
0	1	1	0.085	0.000101100000

Table 32 IIC IAC Feed forward factor settings

VALUE			FACTOR (DECIMAL VALUE)	FACTOR (BINARY VALUE)
BIT 5	BIT 4	BIT 3		
0	1	1	0.00146	0.000000000110
0	1	0	0.00195	0.000000001000
0	0	1	0.00293	0.000000001100
0	0	0	0.00391	0.000000010000
1	1	1	0.00586	0.000000011000
1	1	0	0.00781	0.000000100000
1	0	1	0.01172(prefix)	0.000000110000
1	0	0	0.00000	0.000000000000

Table 33 IIC IAC Suppression stretch time

VALUE			PULSE LENGTH ON SINGLE TRIGGER	STRETCH (# SAMPLES)
BIT 8	BIT 7	BIT 6		
1	0	1	0	N.A.
1	0	0	1	0
1	1	1	2	1
1	1	0	3	2
0	0	1	4	3
0	0	0	5	4
0	1	1	6	5(prefix)
0	1	0	7	6

Table 34 IIC IAC MPX Delay settings

VALUE		DELAY (DECIMAL VALUE) PERIODS OF 304 KHZ
BIT 10	BIT 9	
1	0	2
1	1	3
0	0	4
0	1	5 (prefix)

Table 35 IIC group delay compensation bits

BIT 14	BIT 13	BIT 12	DELAY (TIMES 100 NS)
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11
0	0	0	12 (prefix)
0	0	1	13
0	1	0	14
0	1	1	15

Table 36 IIC audio_source mode bits

AUDIO_SOURCE(1) BIT 6	AUDIO_SOURCE(0) BIT 5	OUTPUT
0	d	**ISN L+R, R-L (prefix)**
1	0	External CD1
1	1	External SPDIF

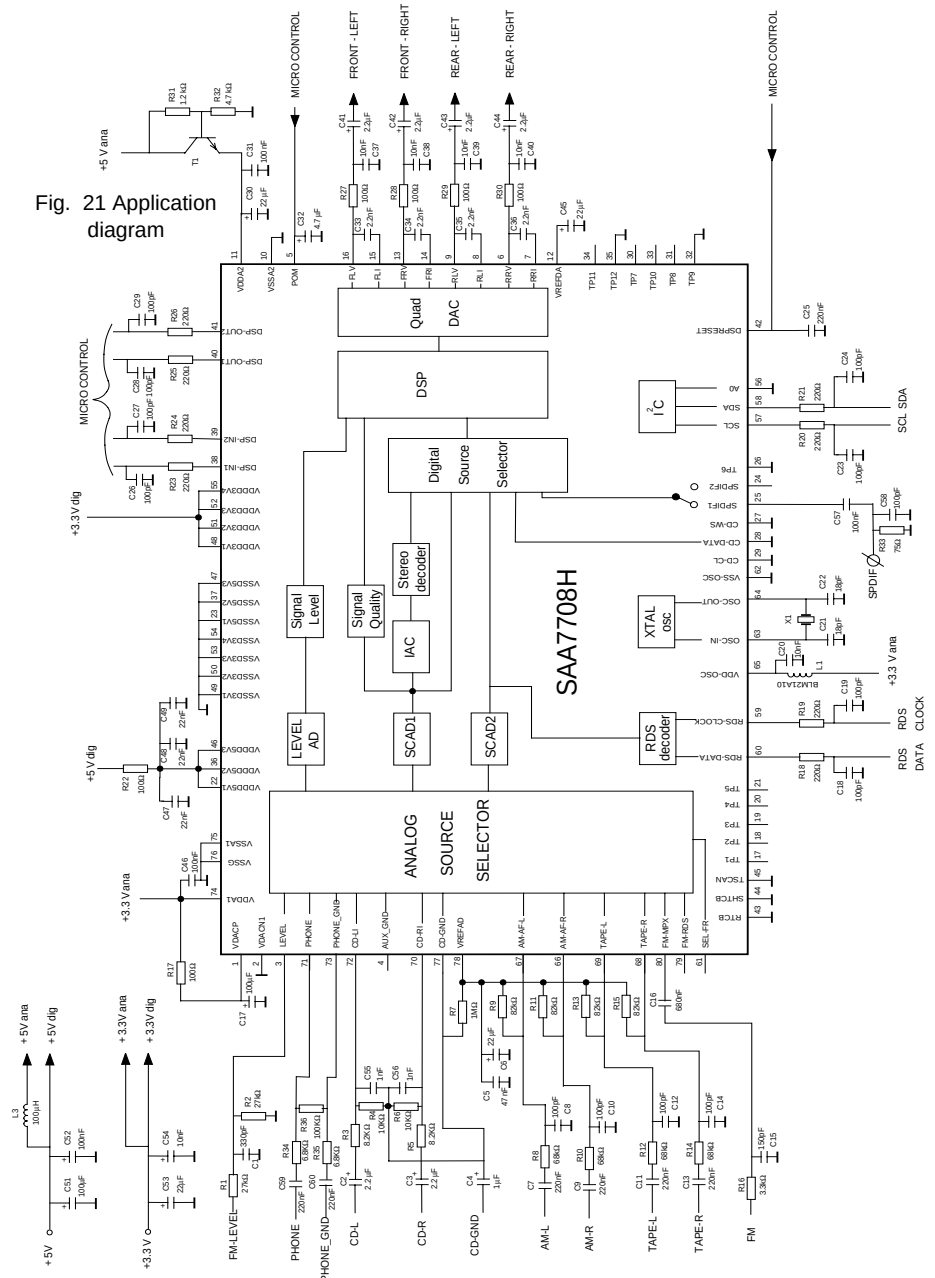
Table 37 IIC audio_format bits

AUDIO_FORMAT(2) BIT 9	AUDIO_FORMAT(0) BIT 8	AUDIO_FORMAT(0) BIT 7	OUTPUT
0	0	0	**ISN, LSB first (prefix)**
0	0	1	LSB justified, 16 bits
-	1	0	LSB justified, 18 bits
-	1	1	LSB justified, 20 bits
1	0	0	Standard I^2S
1	0	1	SPD3 format

21 APPLICATION DIAGRAM

The application diagram shown on the next page must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I^2S inputs of the CD1 and CD2 are not used. For the real application set-up the information of the application report and application support by Philips is necessary on issues like EMC, R_{th} reduction of the package, DSP program etc.

Fig. 21 Application diagram



22 MECHANICAL OUTLINE DRAWING OF PACKAGE

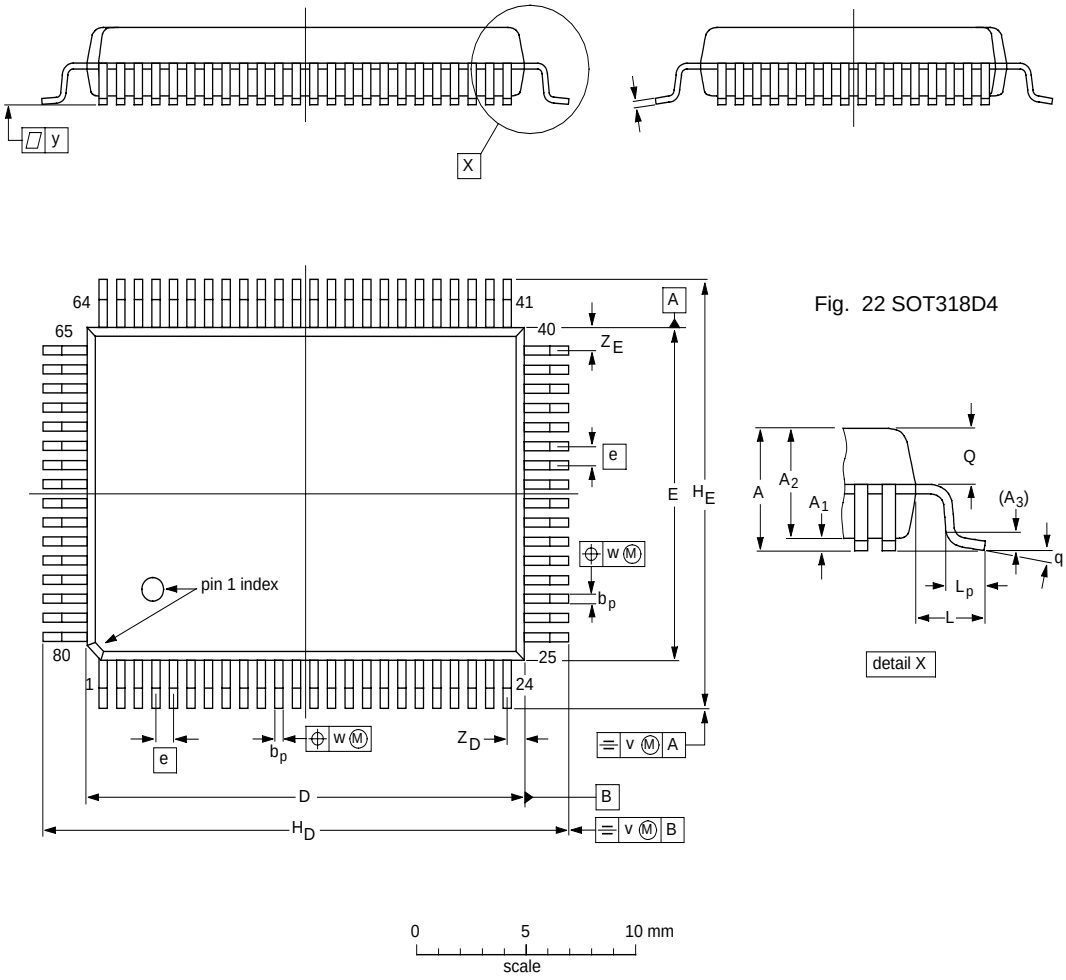


Fig. 22 SOT318D4

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	q
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~92-12-15~~ 95-02-04