

October 1998

## SED1353 GRAPHICS LCD CONTROLLER

### DESCRIPTION

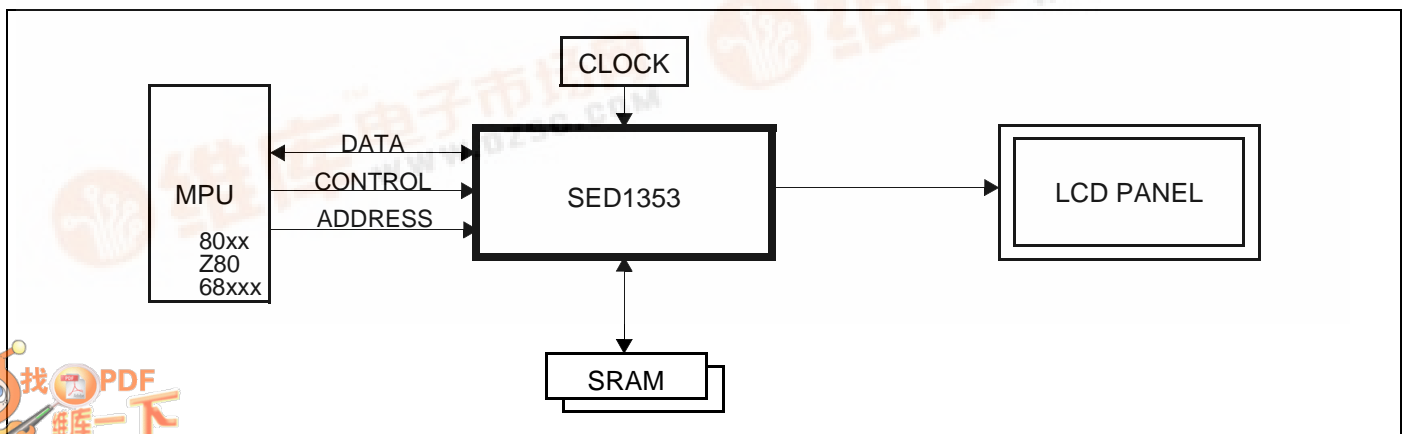
The SED1353 is a dot matrix graphic LCD controller supporting resolutions up to 1024x1024. It is capable of displaying a maximum of 256 simultaneous colors out of a possible 4096 or 16 gray shades. Design flexibility allows the SED1353 to interface to either an MC68000 family microprocessor or an 8/16-bit MPU/bus with minimum external logic. The Static RAM (SRAM) interface used for the display buffer is optimized for speed and performance, supporting up to 128K bytes.

Two power save modes, combined with operating voltages of 2.7 volts through 5.5 volts, allow for a wide range of applications while providing minimum power consumption.

### FEATURES

- pin compatible with the SED1352
- 16-bit 16 MHz MC68xxx MPU interface
- 8/16-bit MPU interface controlled by a READY (or WAIT#) signal
- option to use built-in index register or direct-mapping to access one of sixteen internal registers
- 2-terminal crystal or external oscillator support
- 8/16-bit SRAM interface configurations
- split screen display support allowing two different images to be simultaneously displayed
- virtual display support (displays images larger than the panel size through the use of panning)
- display modes:
  - black-and-white display
  - 2/4 bits per pixel, 4/16-level gray-scale display
  - 2/4/8 bits per pixel, 4/16/256-level color display
- two software power-save modes
- low power consumption
- display memory interface:
  - 128K bytes using one 64Kx16 SRAMs
  - 128K bytes using two 64Kx8 SRAMs
  - 64K bytes using two 32Kx8 SRAMs
  - 40K bytes using one 8Kx8 and one 32Kx8 SRAM
  - 32K bytes using one 32Kx8 SRAM
  - 16K bytes using two 8Kx8 SRAMs
  - 8K bytes using one 8Kx8 SRAM
- LCD panel configurations:
  - single-panel, single-drive passive display
  - dual-panel, dual-drive passive display
- maximum number of vertical lines:
  - 1,024 lines (single-panel, single-drive display)
  - 2,048 lines (dual-panel, dual-drive display)
- QFP5-100-S2 package (F0A)
- QFP15-100-STD package (F1A)

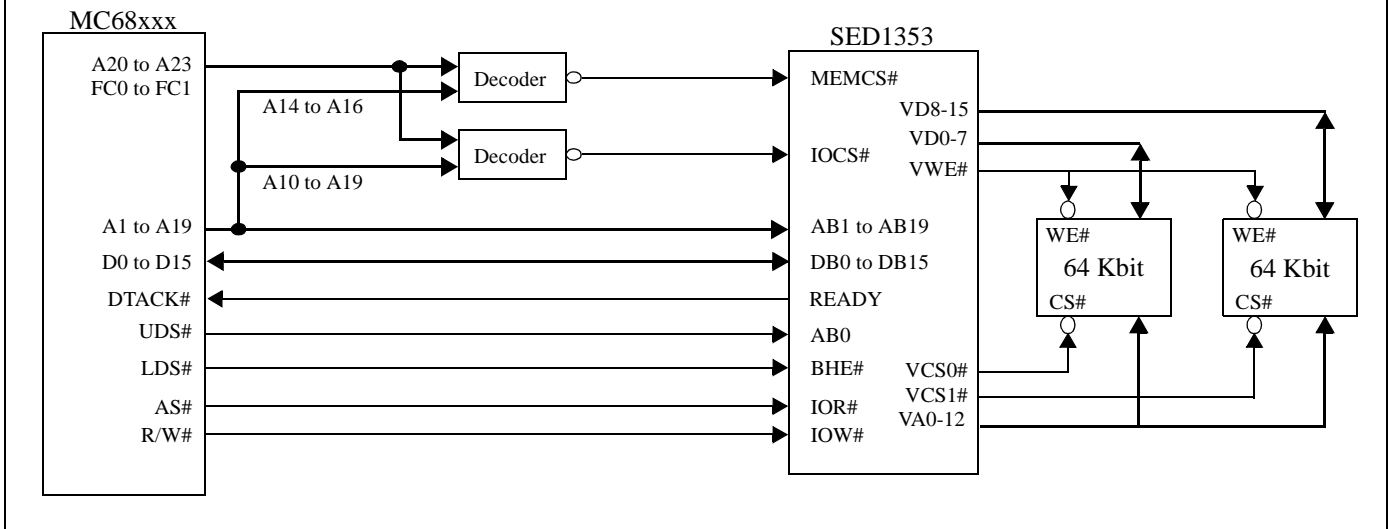
### SYSTEM BLOCK DIAGRAM



## SED1353

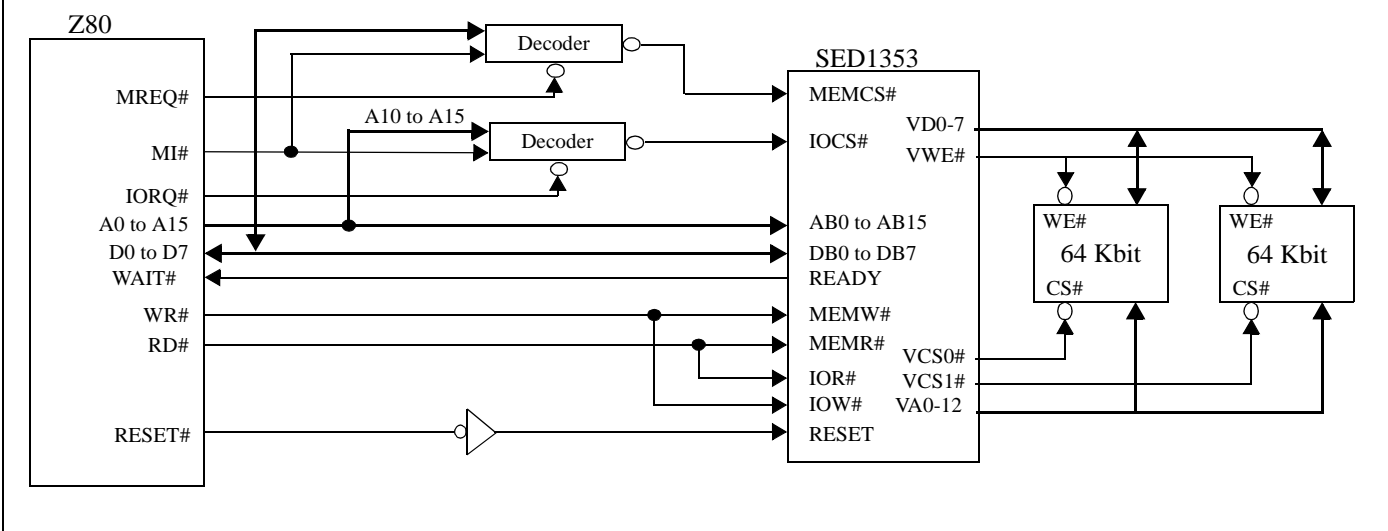
### ■ INTERFACE OPTIONS

#### Interface with 16-Bit MC68xxx MPU and 16K bytes SRAM (2 of 8K x 8)



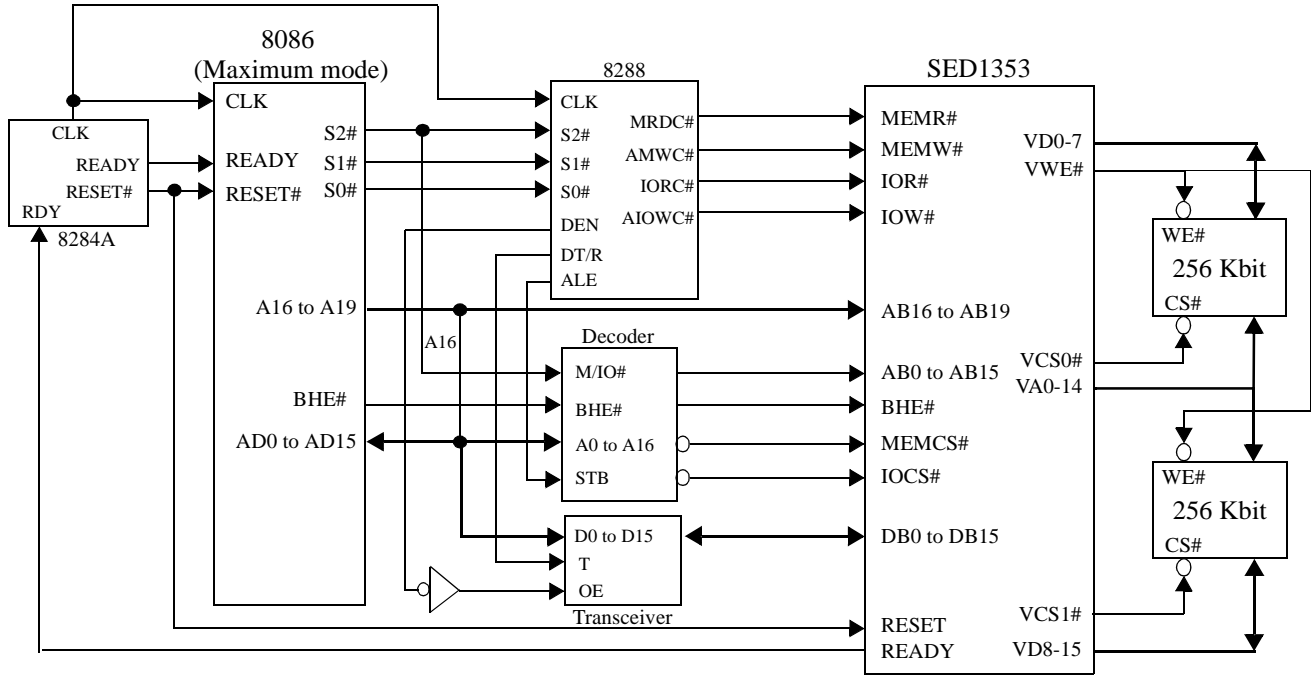
Note: Example implementation, actual may vary.

#### Interface with 8-Bit Z80 MPU and 16K bytes SRAM (2 of 8K x 8)



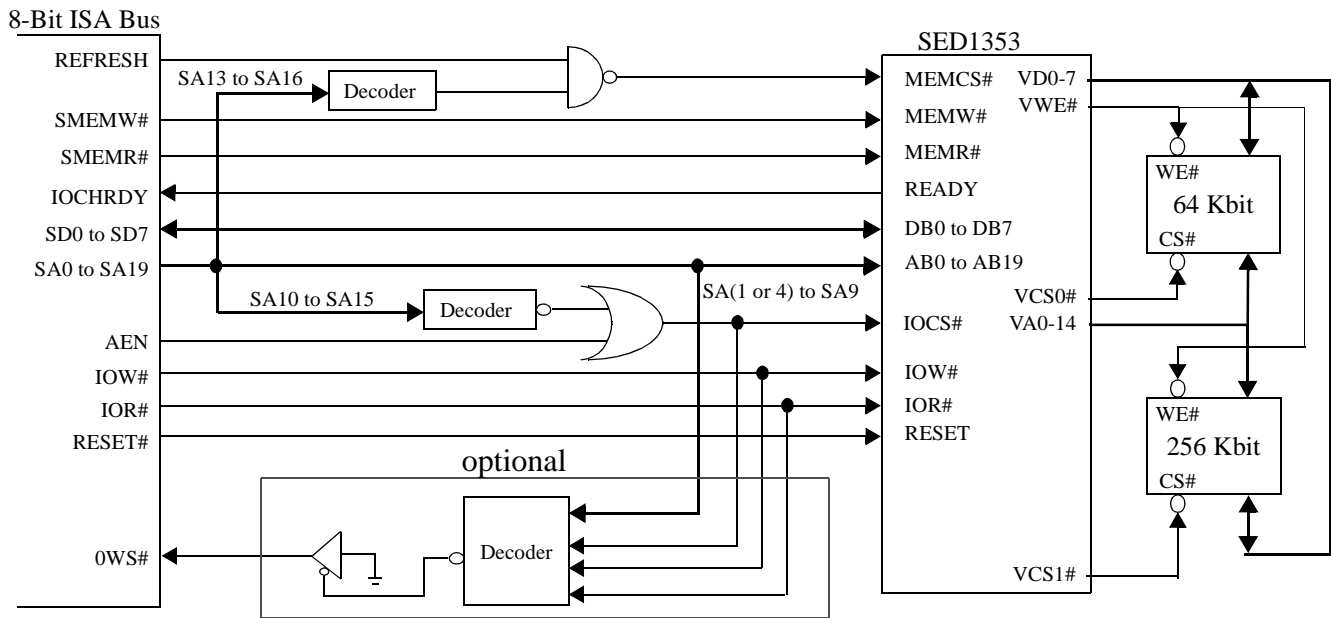
Note: Example implementation, actual may vary.

**Interface with 16-Bit 8086 MPU and 64K bytes SRAM (2 of 32K x 8)**



Note: Example implementation, actual may vary.

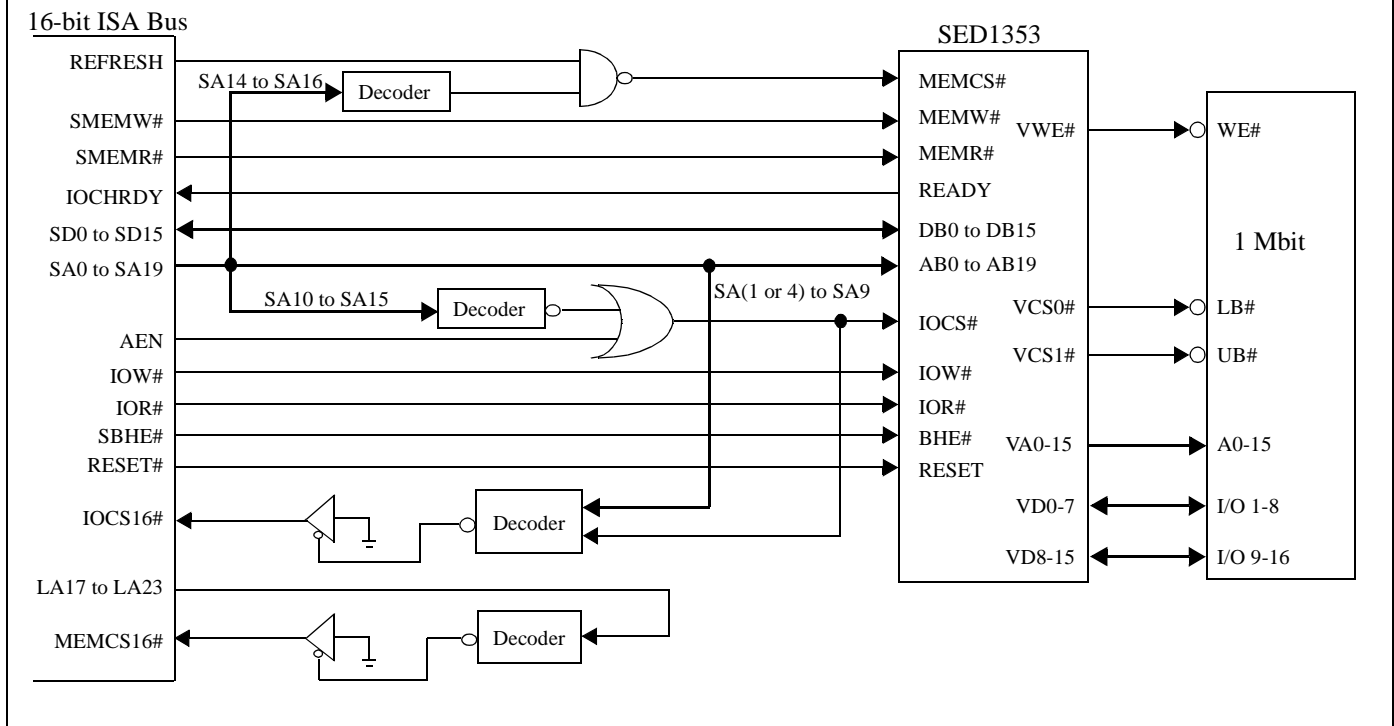
**Interface with 8-Bit ISA Bus and 40K bytes SRAM (1 of 8K x 8 and 1 of 32K x 8)**



Note: Example implementation, actual may vary.

## SED1353

### Interface with 16-Bit ISA Bus and 128K bytes SRAM (1 of 128K x 8)



Note: Example implementation, actual may vary.

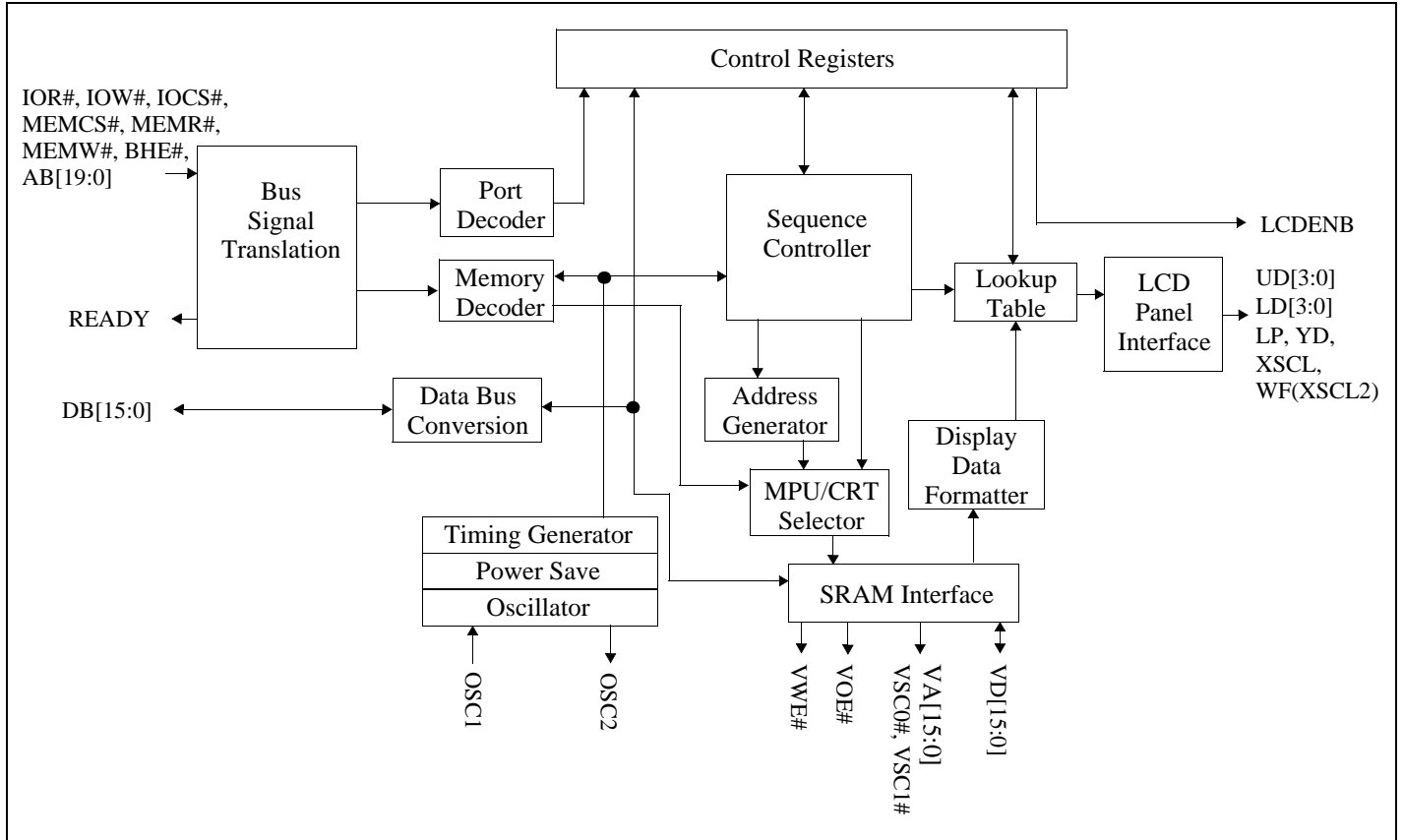
### ■ SUPPORTED RESOLUTIONS

| Display RAM | Example Display Size |   |                 |   | SRAM Type | CPU Interface | SRAM Interface         |                  |                          |                         |              |
|-------------|----------------------|---|-----------------|---|-----------|---------------|------------------------|------------------|--------------------------|-------------------------|--------------|
|             | Monochrome           |   | 4 Grays/ Colors |   |           |               |                        | 16 Grays/ Colors |                          | 256 Colors <sup>a</sup> |              |
|             | X                    | Y | X               | Y |           |               |                        | X                | Y                        | X                       | Y            |
| 8K byte     | 320 x 200            |   | 256 x 128       |   | 128 x 128 |               | —                      |                  | 1 of 8Kx8                | 8-bit                   | 8-bit        |
| 16K byte    | 512 x 256            |   | 320 x 200       |   | 200 x 160 |               | 160 x 100 <sup>a</sup> |                  | 2 of 8Kx8                | 8-bit                   | 8-bit/16-bit |
|             |                      |   |                 |   |           |               |                        |                  |                          | 16-bit                  | 16-bit       |
| 32K byte    | 512 x 512            |   | 512 x 256       |   | 256 x 256 |               | 192 x 100 <sup>a</sup> |                  | 1 of 32Kx8               | 8-bit                   | 8-bit        |
| 40K byte    | 1024 x 320           |   | 512 x 320       |   | 320 x 256 |               | 320 x 128 <sup>a</sup> |                  | 1 of 8Kx8 and 1 of 32Kx8 | 8-bit                   | 8-bit        |
| 64K byte    | 1024 x 512           |   | 512 x 512       |   | 512 x 256 |               | 256 x 256 <sup>a</sup> |                  | 2 of 32Kx8               | 8-bit                   | 8-bit/16-bit |
|             |                      |   |                 |   |           |               |                        |                  |                          | 16-bit                  | 16-bit       |
| 128K byte   | 1024 x 1024          |   | 1024 x 512      |   | 512 x 512 |               | 512 x 256 <sup>a</sup> |                  | 1 of 64Kx16              | 16-bit                  | 16-bit       |
|             |                      |   |                 |   |           |               |                        |                  |                          | 16-bit                  | 16-bit       |

a. 256 colors must use 16-bit SRAM interface

The above listed display sizes are examples based on bits/pixel and available memory.

■ BLOCK DIAGRAM



## SED1353

### ■ FUNCTIONAL BLOCK DESCRIPTION

#### Bus Signal Translation

According to configuration setting VD2, Bus Signal Translation translates either MC68000 type MPU signals or Ready type MPU signals to internal bus interface signals.

#### Control Registers

The Control Register contains 16 internal control and configuration registers. These registers can be accessed by either direct-mapping or using the built-in internal index register.

#### Sequence Controller

The Sequence Controller generates horizontal and vertical display timings according to the configuration registers settings.

#### LCD Panel Interface

The LCD Panel Interface performs frame rate modulation and output data pattern formatting for both passive monochrome and passive color LCD panels.

#### Look-Up Table

The Look-Up Table contains three 16x4-bit wide palettes. In gray shade modes, the "green" palette can be configured for the re-mapping of 16 possible shades of gray. In color modes, all three palettes can be configured for the re-mapping of 4096 possible colors.

#### Port Decoder

According to configuration settings VD1, VD12 - VD4, IOCS# and address lines AB9-1, the Port Decoder validates a given I/O cycle.

#### Memory Decoder

According to configuration settings VD15 - VD13, MEMCS# and address lines AB19-17, the Memory Decoder validates a given memory cycle.

#### Data Bus Conversion

According to configuration setting VD0, Data Bus Conversion maps the external data bus, either 8-bit or 16-bit, into the internal odd and even data bus.

#### Address Generator

The Address Generator generates display refresh addresses to be used to access display memory.

#### MPU / CRT Selector

The MPU / CRT Selector grants access to the display memory from either the MPU or the display refresh circuitry.

#### Display Data Formatter

The Display Data Formatter reads in the display data from the display memory and outputs the correct format for all supported gray shade and color selections.

#### Clock Inputs / Timing

Clock Inputs / Timing generates the internal master clock according to gray-level / color selected and display memory interface. The master clock (MCLK) can be:

- MCLK = input clock
- MCLK = 1/2 input clock
- MCLK = 1/4 input clock.

Pixel clock = input clock =  $f_{osc}$ .

#### SRAM Interface

The SRAM Interface generates the necessary signals to interface to the Display Memory (SRAM).

## ■ DC SPECIFICATIONS

### Absolute Maximum Ratings

| Symbol    | Parameter               | Rating                           | Units |
|-----------|-------------------------|----------------------------------|-------|
| $V_{DD}$  | Supply Voltage          | $V_{SS} - 0.3$ to $+ 6.0$        | V     |
| $V_{IN}$  | Input Voltage           | $V_{SS} - 0.3$ to $V_{DD} + 0.5$ | V     |
| $V_{OUT}$ | Output Voltage          | $V_{SS} - 0.3$ to $V_{DD} + 0.5$ | V     |
| $T_{STG}$ | Storage Temperature     | -65 to 150                       | °C    |
| $T_{SOL}$ | Solder Temperature/Time | 260 for 10 sec. max at lead      | °C    |

### Recommended Operating Conditions

| Symbol    | Parameter                        | Condition                       | Min      | Typ          | Max      | Units |
|-----------|----------------------------------|---------------------------------|----------|--------------|----------|-------|
| $V_{DD}$  | Supply Voltage                   | $V_{SS} = 0$ V                  | 2.7      | 3.0/3.3/5.0  | 5.5      | V     |
| $V_{IN}$  | Input Voltage                    |                                 | $V_{SS}$ | --           | $V_{DD}$ | V     |
| $I_{OPR}$ | Operating Current                | $f_{OSC} = 6$ MHz<br>256 colors |          | 4.5/5.0/11   |          | mA    |
| $T_{OPR}$ | Operating Temperature            |                                 | -40      | 25           | 85       | °C    |
| $P_{TYP}$ | Typical Active Power Consumption | $f_{OSC} = 6$ MHz<br>256 colors |          | 13.5/16.5/55 |          | mW    |

## SED1353

### Input Specifications

| Symbol   | Parameter                | Condition                                             | Min               | Typ | Max               | Units      |
|----------|--------------------------|-------------------------------------------------------|-------------------|-----|-------------------|------------|
| $V_{IL}$ | Low Level Input Voltage  | $V_{DD} = 4.5V$<br>$V_{DD} = 3.0V$<br>$V_{DD} = 2.7V$ |                   |     | 0.8<br>0.4<br>0.3 | V          |
| $V_{IH}$ | High Level Input Voltage | $V_{DD} = 5.5V$<br>$V_{DD} = 3.6V$<br>$V_{DD} = 3.3V$ | 2.0<br>1.3<br>1.2 |     |                   | V          |
| $V_{T+}$ | Positive-going Threshold | $V_{DD} = 5.0$<br>$V_{DD} = 3.3$<br>$V_{DD} = 3.0$    |                   |     | 2.4<br>1.4<br>1.3 | V          |
| $V_{T-}$ | Negative-going Threshold | $V_{DD} = 5.0$<br>$V_{DD} = 3.3$<br>$V_{DD} = 3.0$    | 0.6<br>0.5<br>0.4 |     |                   | V          |
| $V_H$    | Hysteresis Voltage       | $V_{DD} = 5.0$<br>$V_{DD} = 3.3$<br>$V_{DD} = 3.0$    | 0.1<br>0.1<br>0.1 |     |                   | V          |
| $I_{IZ}$ | Input Leakage Current    | --                                                    | -1                |     | 1                 | $\mu A$    |
| $C_{IN}$ | Input Pin Capacitance    | $f = 1 \text{ MHz}$ ,<br>$V_{DD} = 0V$                |                   |     | 12                | pF         |
| $R_{PD}$ | Pull Down Resistance     | $V_{DD} = 5.0V$<br>$V_I = V_{DD}$                     | 50                | 100 | 200               | k $\Omega$ |
| $R_{PD}$ | Pull Down Resistance     | $V_{DD} = 3.3V$<br>$V_I = V_{DD}$                     | 90                | 180 | 360               | k $\Omega$ |
| $R_{PD}$ | Pull Down Resistance     | $V_{DD} = 3.0V$<br>$V_I = V_{DD}$                     | 100               | 200 | 400               | k $\Omega$ |

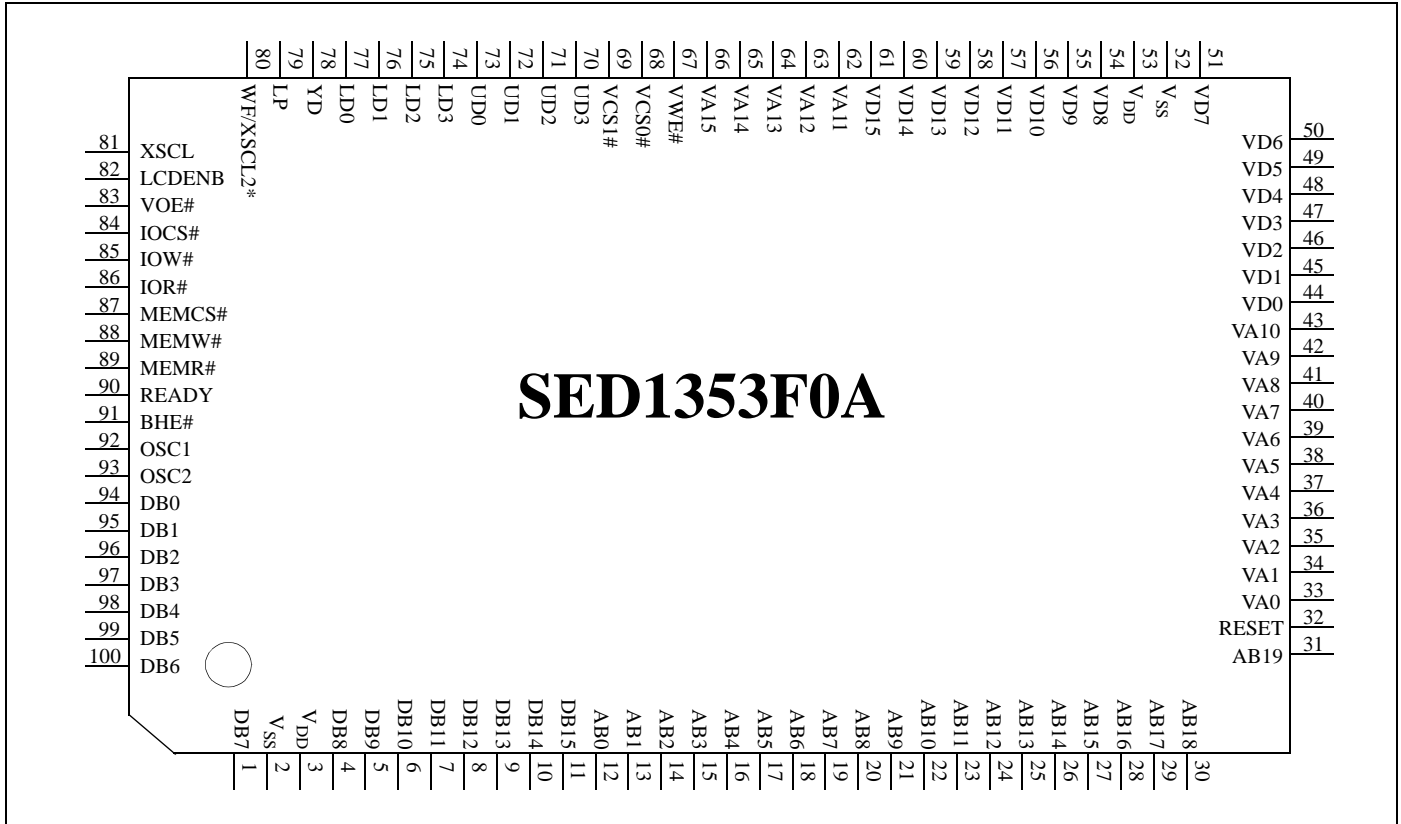


Output Specifications

| Symbol          | Parameter                                                                                        | Condition                                                                                                     | Min          | Typ | Max | Units         |
|-----------------|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------|-----|-----|---------------|
| $V_{OL}$ (5.0V) | Low Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S  | $V_{DD} = \text{Min}$<br>$I_{OL} = 4 \text{ mA}$<br>$I_{OL} = 8 \text{ mA}$<br>$I_{OL} = 12 \text{ mA}$       |              |     | 0.4 | V             |
| $V_{OL}$ (3.3V) | Low Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S  | $V_{DD} = \text{Min}$<br>$I_{OL} = 2 \text{ mA}$<br>$I_{OL} = 4 \text{ mA}$<br>$I_{OL} = 6 \text{ mA}$        |              |     | 0.3 | V             |
| $V_{OL}$ (3.0V) | Low Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S  | $V_{DD} = \text{Min}$<br>$I_{OL} = 1.8 \text{ mA}$<br>$I_{OL} = 3.5 \text{ mA}$<br>$I_{OL} = 5 \text{ mA}$    |              |     | 0.3 | V             |
| $V_{OH}$ (5.0V) | High Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S | $V_{DD} = \text{Min}$<br>$I_{OH} = -4 \text{ mA}$<br>$I_{OH} = -8 \text{ mA}$<br>$I_{OH} = -12 \text{ mA}$    | $V_{DD}-0.4$ |     |     | V             |
| $V_{OH}$ (3.3V) | Low Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S  | $V_{DD} = \text{Min}$<br>$I_{OL} = -2 \text{ mA}$<br>$I_{OL} = -4 \text{ mA}$<br>$I_{OL} = -6 \text{ mA}$     | $V_{DD}-0.3$ |     |     | V             |
| $V_{OH}$ (3.0V) | High Level Output Voltage<br>Type 1 - TS1D2, CO1<br>Type 2 - TS2, CO2<br>Type 3 - TS3, CO3, CO3S | $V_{DD} = \text{Min}$<br>$I_{OH} = -1.8 \text{ mA}$<br>$I_{OH} = -3.5 \text{ mA}$<br>$I_{OH} = -5 \text{ mA}$ | $V_{DD}-0.3$ |     |     | V             |
| $I_{OZ}$        | Output Leakage Current                                                                           | --                                                                                                            | -1           |     | 1   | $\mu\text{A}$ |
| $C_{OUT}$       | Output Pin Capacitance                                                                           | $f = 1 \text{ MHz}$ ,<br>$V_{DD} = 0 \text{ V}$                                                               |              |     | 12  | pF            |
| $C_{BID}$       | Bidirectional Pin Capacitance                                                                    | $f = 1 \text{ MHz}$ ,<br>$V_{DD} = 0 \text{ V}$                                                               |              |     | 12  | pF            |

## SED1353

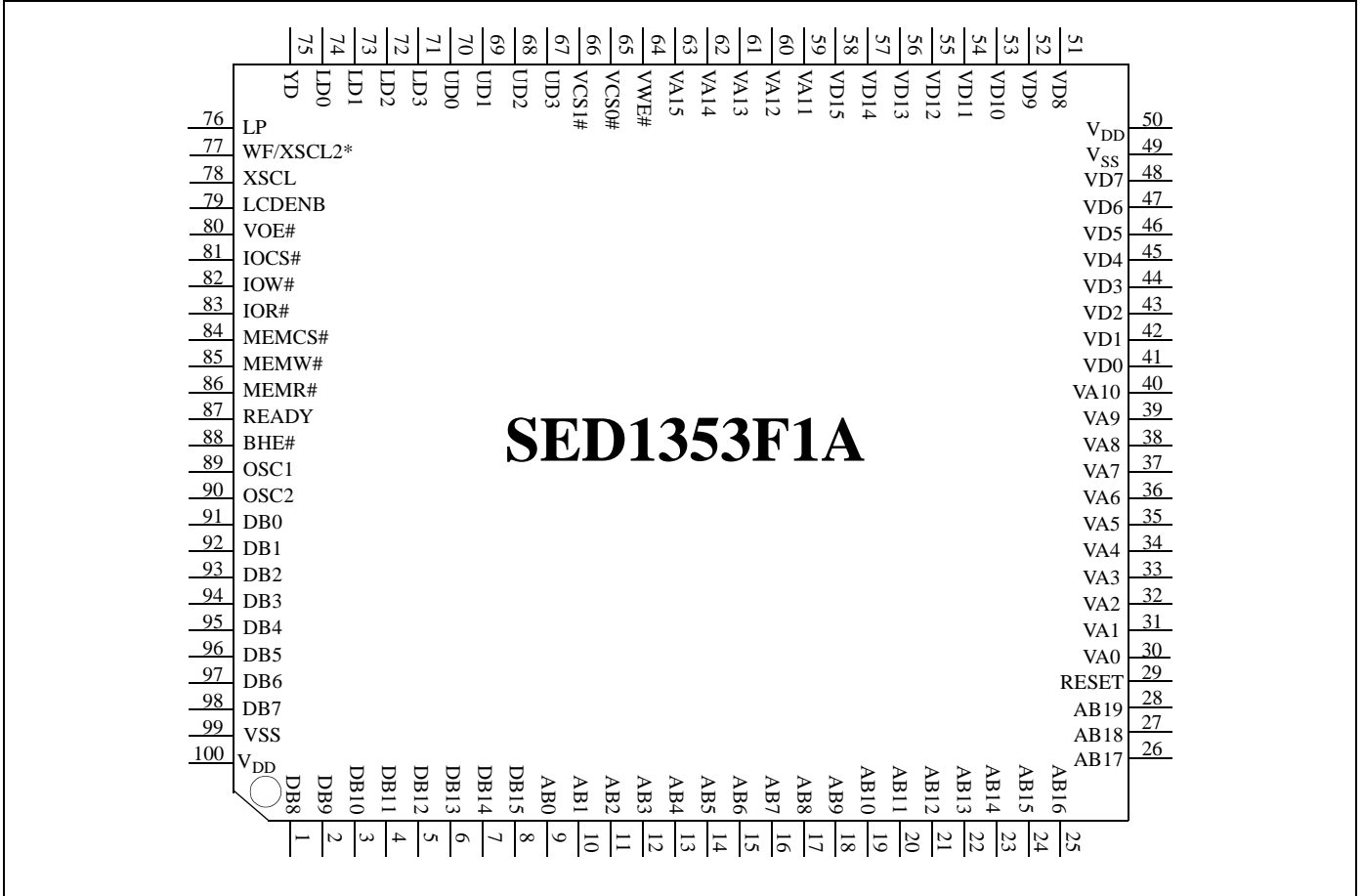
### ■ SED1353F0A PIN OUT



\* Pin 80 = WF in all display modes except format 1 for 8-bit single color panel.

\* Pin 80 = XSCL2 in format 1 for 8-bit single color panel.

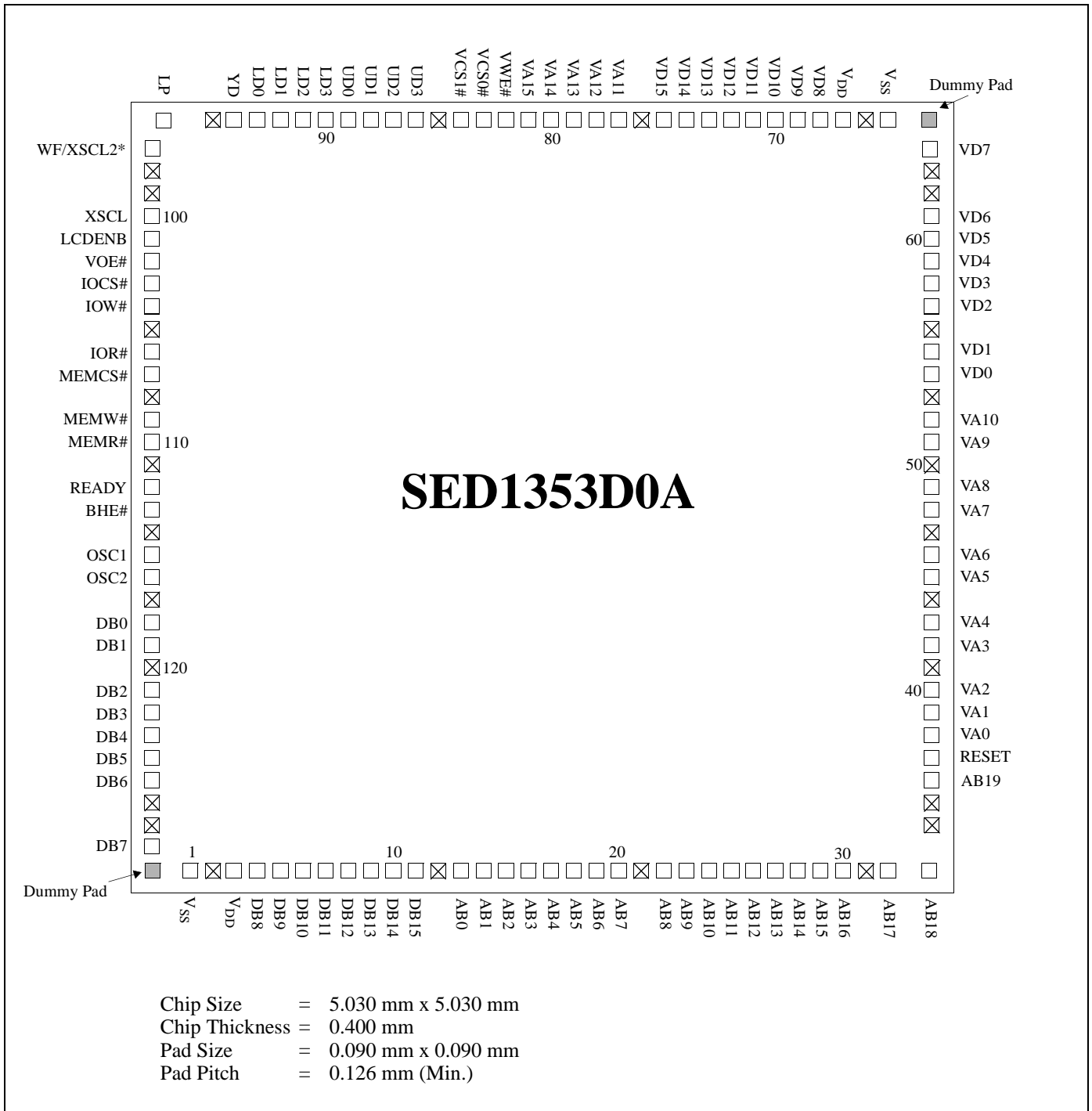
■ SED1353F1A PIN OUT



\* Pin 77 = WF in all display modes except format 1 for 8-bit single color panel.  
 \* Pin 77 = XSCL2 in format 1 for 8-bit single color panel.

## SED1353

### ■ SED1353D0A PIN OUT



\* Pad 97 = WF in all display modes except format 1 for 8-bit single color panel.

\* Pad 97 = XSCL2 in format 1 for 8-bit single color panel.

**PAD Coordinates**

| Pad No. | Pin Name | Pad Center Coordinate |        |
|---------|----------|-----------------------|--------|
|         |          | X                     | Y      |
| 1       | VSS      | -2.165                | -2.390 |
| 2       | ---      | -2.000                | -2.390 |
| 3       | VDD      | -1.840                | -2.390 |
| 4       | DB8      | -1.685                | -2.390 |
| 5       | DB9      | -1.535                | -2.390 |
| 6       | DB10     | -1.388                | -2.390 |
| 7       | DB11     | -1.246                | -2.390 |
| 8       | DB12     | -1.106                | -2.390 |
| 9       | DB13     | -0.969                | -2.390 |
| 10      | DB14     | -0.835                | -2.390 |
| 11      | DB15     | -0.703                | -2.390 |
| 12      | ---      | -0.573                | -2.390 |
| 13      | AB0      | -0.444                | -2.390 |
| 14      | AB1      | -0.317                | -2.390 |
| 15      | AB2      | -0.190                | -2.390 |
| 16      | AB3      | -0.063                | -2.390 |
| 17      | AB4      | 0.063                 | -2.390 |
| 18      | AB5      | 0.190                 | -2.390 |
| 19      | AB6      | 0.317                 | -2.390 |
| 20      | AB7      | 0.444                 | -2.390 |
| 21      | ---      | 0.573                 | -2.390 |
| 22      | AB8      | 0.703                 | -2.390 |
| 23      | AB9      | 0.835                 | -2.390 |
| 24      | AB10     | 0.969                 | -2.390 |
| 25      | AB11     | 1.106                 | -2.390 |
| 26      | AB12     | 1.246                 | -2.390 |
| 27      | AB13     | 1.388                 | -2.390 |
| 28      | AB14     | 1.535                 | -2.390 |
| 29      | AB15     | 1.685                 | -2.390 |
| 30      | AB16     | 1.840                 | -2.390 |
| 31      | ---      | 2.000                 | -2.390 |
| 32      | AB17     | 2.165                 | -2.390 |
| 33      | AB18     | 2.390                 | -2.340 |
| 34      | ---      | 2.390                 | -2.000 |
| 35      | ---      | 2.390                 | -1.840 |
| 36      | AB19     | 2.390                 | -1.685 |

| Pad No. | Pin Name | Pad Center Coordinate |        |
|---------|----------|-----------------------|--------|
|         |          | X                     | Y      |
| 37      | RESET    | 2.390                 | -1.535 |
| 38      | VA0      | 2.390                 | -1.388 |
| 39      | VA1      | 2.390                 | -1.246 |
| 40      | VA2      | 2.390                 | -1.106 |
| 41      | ---      | 2.390                 | -0.969 |
| 42      | VA3      | 2.390                 | -0.835 |
| 43      | VA4      | 2.390                 | -0.703 |
| 44      | ---      | 2.390                 | -0.573 |
| 45      | VA5      | 2.390                 | -0.444 |
| 46      | VA6      | 2.390                 | -0.317 |
| 47      | ---      | 2.390                 | -0.190 |
| 48      | VA7      | 2.390                 | -0.063 |
| 49      | VA8      | 2.390                 | 0.063  |
| 50      | ---      | 2.390                 | 0.190  |
| 51      | VA9      | 2.390                 | 0.317  |
| 52      | VA10     | 2.390                 | 0.444  |
| 53      | ---      | 2.390                 | 0.573  |
| 54      | VD0      | 2.390                 | 0.703  |
| 55      | VD1      | 2.390                 | 0.835  |
| 56      | ---      | 2.390                 | 0.969  |
| 57      | VD2      | 2.390                 | 1.106  |
| 58      | VD3      | 2.390                 | 1.246  |
| 59      | VD4      | 2.390                 | 1.388  |
| 60      | VD5      | 2.390                 | 1.535  |
| 61      | VD6      | 2.390                 | 1.685  |
| 62      | ---      | 2.390                 | 1.840  |
| 63      | ---      | 2.390                 | 2.000  |
| 64      | VD7      | 2.390                 | 2.165  |
| 65      | VSS      | 2.165                 | 2.390  |
| 66      | ---      | 2.000                 | 2.390  |
| 67      | VDD      | 1.840                 | 2.390  |
| 68      | VD8      | 1.685                 | 2.390  |
| 69      | VD9      | 1.535                 | 2.390  |
| 70      | VD10     | 1.388                 | 2.390  |
| 71      | VD11     | 1.246                 | 2.390  |
| 72      | VD12     | 1.106                 | 2.390  |

## SED1353

| Pad No. | Pin Name | Pad Center Coordinate |       |
|---------|----------|-----------------------|-------|
|         |          | X                     | Y     |
| 73      | VD13     | 0.969                 | 2.390 |
| 74      | VD14     | 0.835                 | 2.390 |
| 75      | VD15     | 0.703                 | 2.390 |
| 76      | ---      | 0.573                 | 2.390 |
| 77      | VA11     | 0.444                 | 2.390 |
| 78      | VA12     | 0.317                 | 2.390 |
| 79      | VA13     | 0.190                 | 2.390 |
| 80      | VA14     | 0.063                 | 2.390 |
| 81      | VA15     | -0.063                | 2.390 |
| 82      | VWE#     | -0.190                | 2.390 |
| 83      | VCS0#    | -0.317                | 2.390 |
| 84      | VCS1#    | -0.444                | 2.390 |
| 85      | ---      | -0.573                | 2.390 |
| 86      | UD3      | -0.703                | 2.390 |
| 87      | UD2      | -0.835                | 2.390 |
| 88      | UD1      | -0.969                | 2.390 |
| 89      | UD0      | -1.106                | 2.390 |
| 90      | LD3      | -1.246                | 2.390 |
| 91      | LD2      | -1.388                | 2.390 |
| 92      | LD1      | -1.535                | 2.390 |
| 93      | LD0      | -1.685                | 2.390 |
| 94      | YD       | -1.840                | 2.390 |
| 95      | ---      | -2.000                | 2.390 |
| 96      | LP       | -2.340                | 2.390 |
| 97      | WF/XSCL2 | -2.390                | 2.165 |
| 98      | ---      | -2.390                | 2.000 |
| 99      | ---      | -2.390                | 1.840 |
| 100     | XSCL     | -2.390                | 1.685 |
| 101     | LCDENB   | -2.390                | 1.535 |

| Pad No. | Pin Name  | Pad Center Coordinate |        |
|---------|-----------|-----------------------|--------|
|         |           | X                     | Y      |
| 102     | VOE#      | -2.390                | 1.388  |
| 103     | IOCS#     | -2.390                | 1.246  |
| 104     | IOW#      | -2.390                | 1.106  |
| 105     | ---       | -2.390                | 0.969  |
| 106     | IOR#      | -2.390                | 0.835  |
| 107     | MEMCS#    | -2.390                | 0.703  |
| 108     | ---       | -2.390                | 0.573  |
| 109     | MEMW#     | -2.390                | 0.444  |
| 110     | MEMR#     | -2.390                | 0.317  |
| 111     | ---       | -2.390                | 0.190  |
| 112     | READY     | -2.390                | 0.063  |
| 113     | BHE#      | -2.390                | -0.063 |
| 114     | ---       | -2.390                | -0.190 |
| 115     | OSC1      | -2.390                | -0.317 |
| 116     | OSC2      | -2.390                | -0.444 |
| 117     | ---       | -2.390                | -0.573 |
| 118     | DB0       | -2.390                | -0.703 |
| 119     | DB1       | -2.390                | -0.835 |
| 120     | ---       | -2.390                | -0.969 |
| 121     | DB2       | -2.390                | -1.106 |
| 122     | DB3       | -2.390                | -1.246 |
| 123     | DB4       | -2.390                | -1.388 |
| 124     | DB5       | -2.390                | -1.535 |
| 125     | DB6       | -2.390                | -1.685 |
| 126     | ---       | -2.390                | -1.840 |
| 127     | ---       | -2.390                | -2.000 |
| 128     | DB7       | -2.390                | -2.165 |
| 129     | Dummy Pad | 2.390                 | 2.390  |
| 130     | Dummy Pad | -2.390                | -2.390 |

■ PIN DESCRIPTION

Key

- I = Input
- O = Output
- I/O = Bidirectional
- P = Power

Bus Interface

| Pin Name | Type | F0A Pin #              | F1A Pin #         | D0A Pad #                            | Description                                                                                                                                                                                                                                                                                                                                    |
|----------|------|------------------------|-------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DB0-DB15 | I/O  | 94 - 100,<br>1, 4 - 11 | 91 - 98,<br>1 - 8 | 118-119,<br>121-125,<br>128,<br>4-11 | These pins are connected to the system data bus. In 8-bit bus mode, DB8-DB15 must be tied to V <sub>DD</sub> .                                                                                                                                                                                                                                 |
| AB0      | I    | 12                     | 9                 | 13                                   | In MC68000 MPU interface, this pin is connected to the Upper Data Strobe (UDS#) pin of MC68000. In other bus interfaces, this pin is connected to the system address bus.                                                                                                                                                                      |
| AB1-AB19 | I    | 13 - 31                | 10 - 28           | 14-20,<br>22-30,<br>32-33,<br>36     | These pins are connected to the system address bus.                                                                                                                                                                                                                                                                                            |
| BHE#     | I    | 91                     | 88                | 113                                  | In MC68000 MPU interface, this pin is connected to the Lower Data Strobe (LDS#) pin of MC68000. In other bus interfaces, this pin is the Byte High Enable input for use with 16-bit system. In 8-bit bus mode, tie BHE# input to V <sub>DD</sub> .                                                                                             |
| IOCS#    | I    | 84                     | 81                | 103                                  | Active low input to select one of fifteen internal registers.                                                                                                                                                                                                                                                                                  |
| IOW#     | I    | 85                     | 82                | 104                                  | In MC68000 MPU interface, this pin is connected to the R/W# pin of MC68000. This input pin will define whether the data transfer is a read (active high) or write (active low) cycle. In other bus interfaces, this is the active low input to write data into an internal register.                                                           |
| IOR#     | I    | 86                     | 83                | 106                                  | In MC68000 MPU interface, this pin is connected to the AS# pin of MC68000. This input pin will indicate a valid address is available on the address bus. In other bus interfaces, this is the active low input to read data from an internal register.                                                                                         |
| MEMCS#   | I    | 87                     | 84                | 107                                  | Active low input to indicate the attempt to access the display memory.                                                                                                                                                                                                                                                                         |
| MEMW#    | I    | 88                     | 85                | 109                                  | Active low input to write data to the display memory. This pin should be tied to V <sub>DD</sub> in an MC68000 MPU interface.                                                                                                                                                                                                                  |
| MEMR#    | I    | 89                     | 86                | 110                                  | Active low input to read data from the display memory. This pin should be tied to V <sub>DD</sub> in an MC68000 MPU interface.                                                                                                                                                                                                                 |
| READY    | O    | 90                     | 87                | 112                                  | For MC68000 MPU interface, this pin is connected to the DTACK# pin of MC68000 and will be driven low when ever a data transfer is complete. In other bus interfaces, this output is driven low to force the system to insert wait states when needed.<br><br>READY is placed in a high-impedance (Hi-Z) state after the transfer is completed. |
| RESET    | I    | 32                     | 29                | 37                                   | Active high input to force all signals to their inactive states.                                                                                                                                                                                                                                                                               |

## SED1353

### Display Memory Interface

| Pin Name | Type | F0A<br>Pin #        | F1A<br>Pin #        | D0A<br>Pad #                                            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|------|---------------------|---------------------|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VD0-VD15 | I/O  | 44 - 51,<br>54 - 61 | 41 - 48,<br>51 - 58 | 54-55,<br>57-61,<br>64,<br>68-75                        | These pins are connected to the display memory data bus. For 16-bit interface, VD0-VD7 are connected to the display memory data bus of even byte addresses and VD8-VD15 are connected to the display memory data bus of odd byte addresses. The output drivers of these pins are tri-stated when RESET is high.<br><br>On the falling edge of RESET the values of VD0-VD15 are latched into the chip to configure various hardware options. |
| VA0-VA15 | O    | 33 - 43,<br>62 - 66 | 30 - 40<br>59 - 63  | 38-40,<br>42-43,<br>45-46,<br>48-49,<br>51-52,<br>77-81 | These pins are connected to the display memory address bus.                                                                                                                                                                                                                                                                                                                                                                                 |
| VCS1#    | O    | 69                  | 66                  | 84                                                      | Active low chip-select output to the second or odd byte address SRAM.                                                                                                                                                                                                                                                                                                                                                                       |
| VCS0#    | O    | 68                  | 65                  | 83                                                      | Active low chip-select output to the first or even byte address SRAM.                                                                                                                                                                                                                                                                                                                                                                       |
| VWE#     | O    | 67                  | 64                  | 82                                                      | Active low output used for writing data to the display memory. This pin is connected to the WE# input of the SRAMs.                                                                                                                                                                                                                                                                                                                         |
| VOE#     | O    | 83                  | 80                  | 102                                                     | Active low output to enable reading of data from the display memory. This pin is connected to the OE# input of the SRAMs.                                                                                                                                                                                                                                                                                                                   |

### LCD Interface

| Pin Name           | FPDI-1™<br>Pin Name <sup>a</sup> | Type | F0A<br>Pin #       | F1A<br>Pin #       | D0A<br>Pad #       | Description                                                                                                                                                                                                 |
|--------------------|----------------------------------|------|--------------------|--------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UD3-UD0<br>LD3-LD0 | UD3-UD0<br>LD3-LD0               | O    | 70 - 73<br>74 - 77 | 67 - 70<br>71 - 74 | 86 - 89<br>90 - 93 | Panel display data bus. The data format depends on the specific panel connected. For 4-bit single panels, these bits are driven 0 (low state).                                                              |
| XSCL               | FPSHIFT                          | O    | 81                 | 78                 | 100                | Display data shift clock. Data is shifted into the LCD X-drivers on the falling edge of this signal.                                                                                                        |
| LP                 | FPLINE                           | O    | 79                 | 76                 | 96                 | Display data latch clock. The falling edge of this signal is used to latch a row of display data in the LCD X-drivers and to turn on the row driver (Y driver).                                             |
| WF/XSCL2           | MOD<br>FPSHIFT2                  | O    | 80                 | 77                 | 97                 | For format 1 of 8-bit single color panels this is the second shift clock. For all other modes, this is the LCD backplane BIAS signal. This output toggles once every n LP periods, as programmed in AUX[05] |
| YD                 | FPFRAME                          | O    | 78                 | 75                 | 94                 | Vertical scanning start pulse. A logic '1' on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row driver (Y driver) to indicate the start of the vertical frame.     |
| LCDENB             | ---                              | O    | 82                 | 79                 | 101                | LCD enable signal output. It can be used externally to turn off the panel supply voltage and backlight.                                                                                                     |

a. VESA Flat Panel Display Interface Standard (FPDI-1™)



**Clock Inputs**

| Pin Name | Type | F0A Pin # | F1A Pin # | D0A Pad # | Description                                                                                                                                                                                                      |
|----------|------|-----------|-----------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| OSC1     | I    | 92        | 89        | 115       | This pin, along with OSC2 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.         |
| OSC2     | O    | 93        | 90        | 116       | This pin, along with OSC1 is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected. |

**Power Supply**

| Pin Name        | Type | F0A Pin # | F1A Pin # | D0A Pad # | Description     |
|-----------------|------|-----------|-----------|-----------|-----------------|
| V <sub>DD</sub> | P    | 3, 53     | 50, 100   | 3, 67     | Voltage supply. |
| V <sub>SS</sub> | P    | 2, 52     | 49, 99    | 1, 65     | Voltage Ground. |

■ **SUMMARY OF CONFIGURATION OPTIONS**

| Pin Name  | value on this pin at falling edge of RESET is used to configure: (1/0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                               |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|           | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 0                                                                             |
| VD0       | 16-bit host bus interface                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 8-bit host bus interface                                                      |
| VD1       | Use direct-mapping for I/O accesses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Use indexed mapping for I/O accesses                                          |
| VD2       | MC68000 MPU interface                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MPU / Bus interface with memory accesses controlled by a READY (WAIT#) signal |
| VD3       | Swap of high and low data bytes in 16-bit bus interface                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | No byte swap of high and low data bytes in 16-bit bus interface               |
| VD12-VD4  | Select I/O mapping address bits [9:1].<br>These nine bits are latched on power-up and are compared to the MPU address bits [9-1]. A valid I/O cycle combined with a valid address will enable the internal I/O decoder. Therefore, both types of I/O mapping are limited to even address boundaries to determine either the absolute or indexed I/O address of the first register. Note that a “valid I/O cycle” includes IOCS# being toggled low.                                                                                                                                                                                 |                                                                               |
| VD15-VD13 | Select memory mapping address bits [3:1]<br>These three bits are latched on power-up and are compared to the MPU address bits [19-17]. A valid memory cycle combined with a valid address will enable the internal memory decoder. As only the three most significant bits of the address are compared, the maximum amount of memory supported is 128K bytes. Note that a “valid memory cycle” includes MEMCS# being toggled low.<br>When using 128K byte memory it must be mapped at an even address such that all 128K bytes is available without a change in state on A17, as this would invalidate the internal compare logic. |                                                                               |

## SED1353

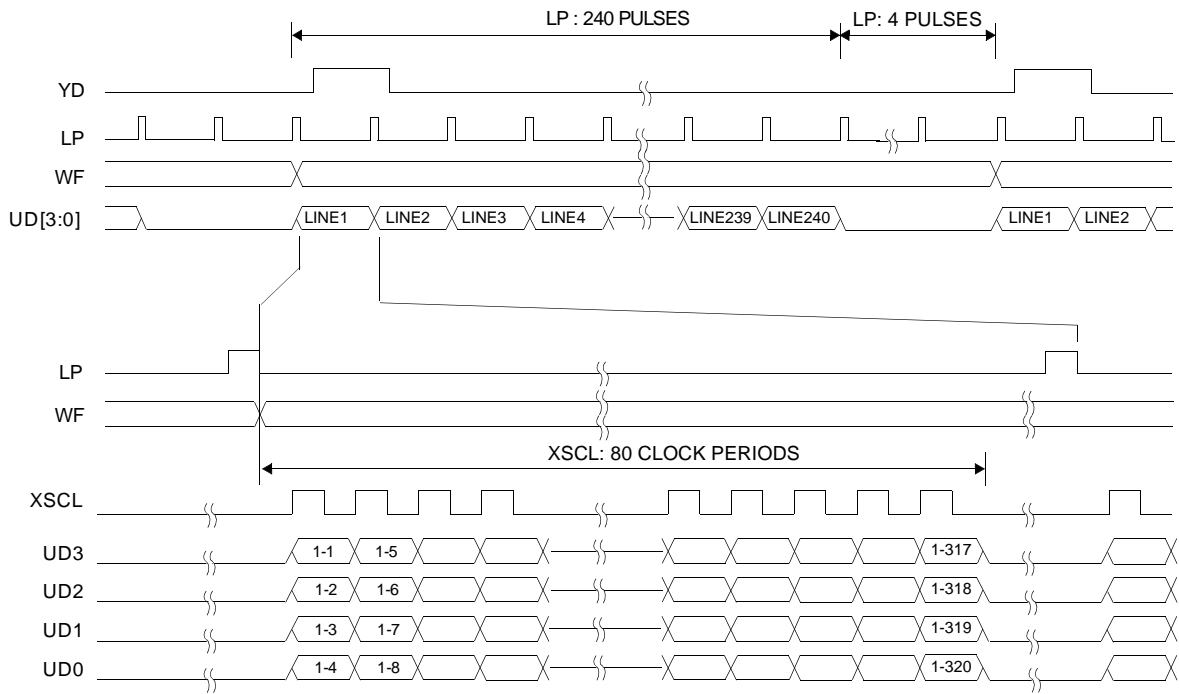
Example: If an ISA bus (no byte swap) with memory segment “A” and I/O location 300h are used, the corresponding settings of VD15-VD0 would be:

| Pin Name  | 8-Bit ISA Bus  |                | 16-Bit ISA Bus |                |
|-----------|----------------|----------------|----------------|----------------|
|           | Index Register | Direct Mapping | Index Register | Direct Mapping |
| VD0       | 0              | 0              | 1              | 1              |
| VD1       | 0              | 1              | 0              | 1              |
| VD2       | 0              | 0              | 0              | 0              |
| VD3       | 0              | 0              | 0              | 0              |
| VD12-VD4  | 11 0000 000    | 11 0000 xxx    | 11 0000 000    | 11 0000 xxx    |
| VD15-VD13 | 101            | 101            | 101            | 101            |

Where x = don't care; 1 = connected to pull-up resistor; 0 = not connected to pull-up resistor

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

4-Bit Single Panel

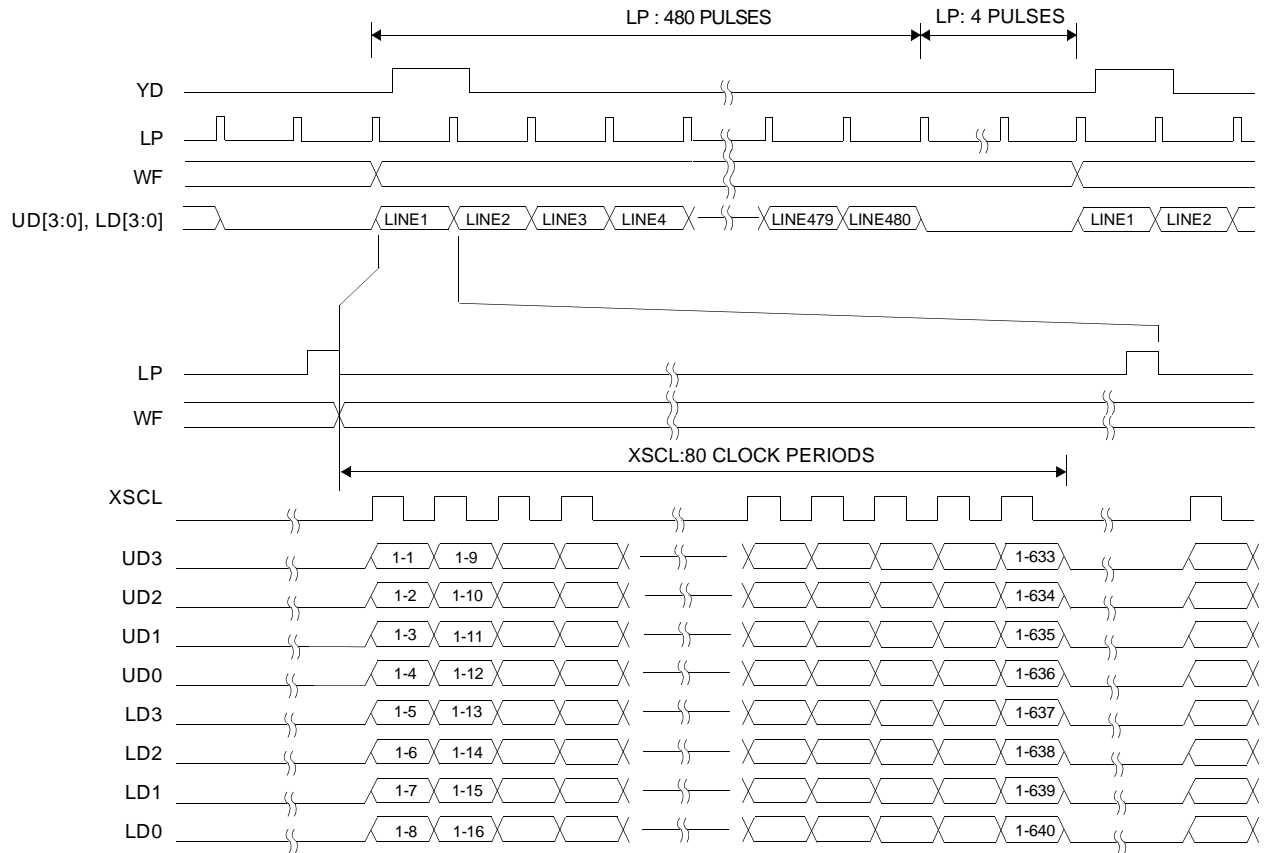


Example Timing for a 320x240 single panel

## SED1353

### MONOCHROME PASSIVE STN LCD PANEL INTERFACE

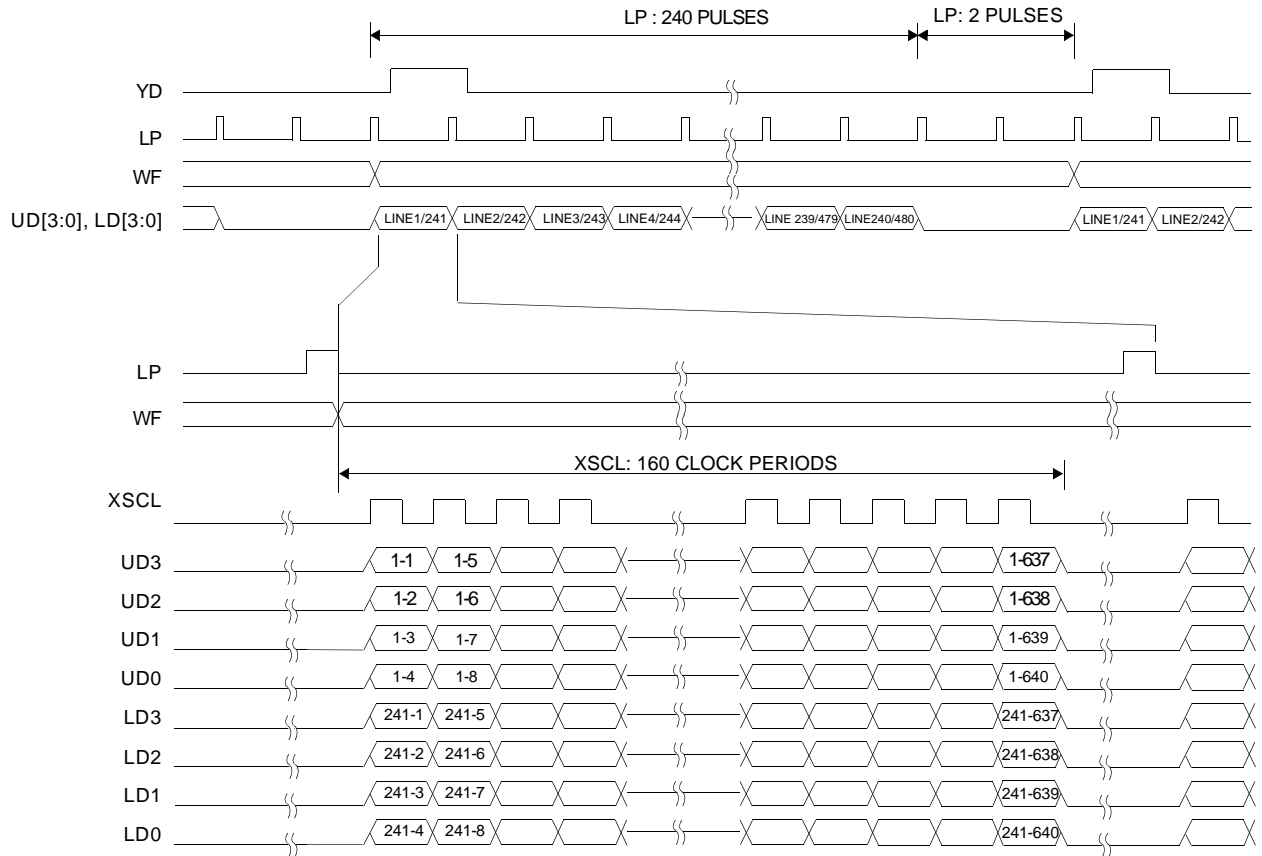
#### 8-Bit Single Panel



Example timing for a 640x480 panel

■ MONOCHROME PASSIVE STN LCD PANEL INTERFACE

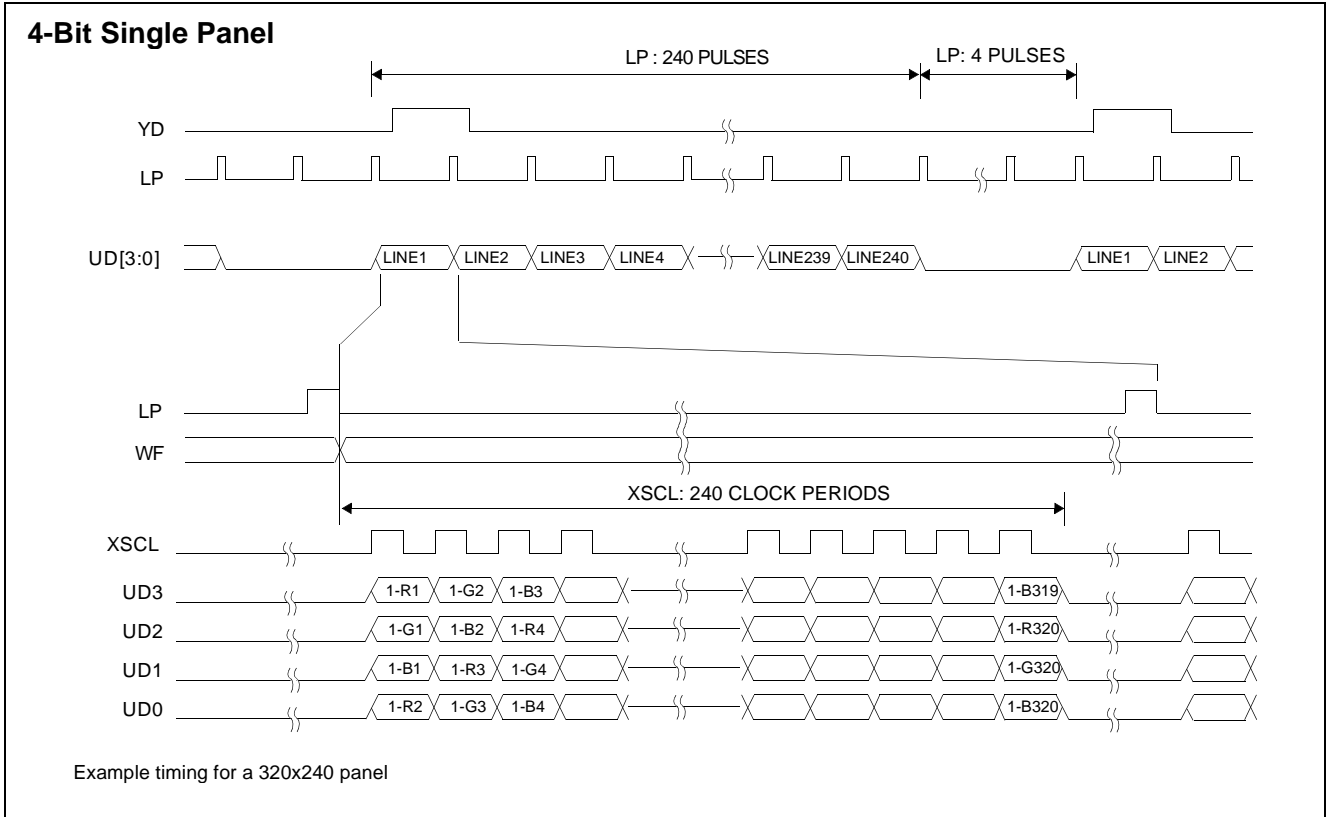
8-Bit Dual Panel



Example timing for a 640x480 panel

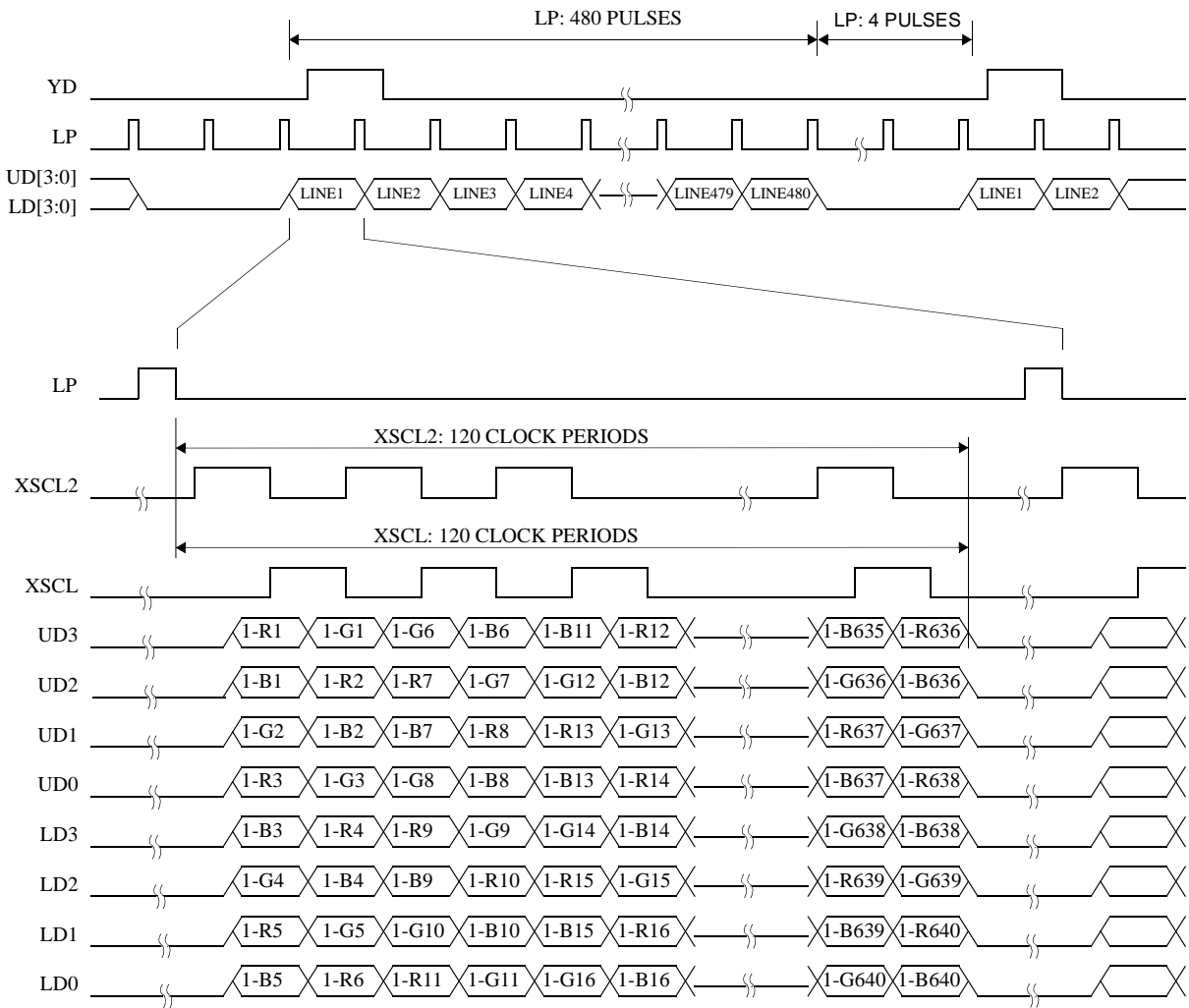
## SED1353

### ■ COLOR PASSIVE STN LCD PANEL INTERFACE



■ COLOR PASSIVE STN LCD PANEL INTERFACE

8-Bit Single Panel - Format 1

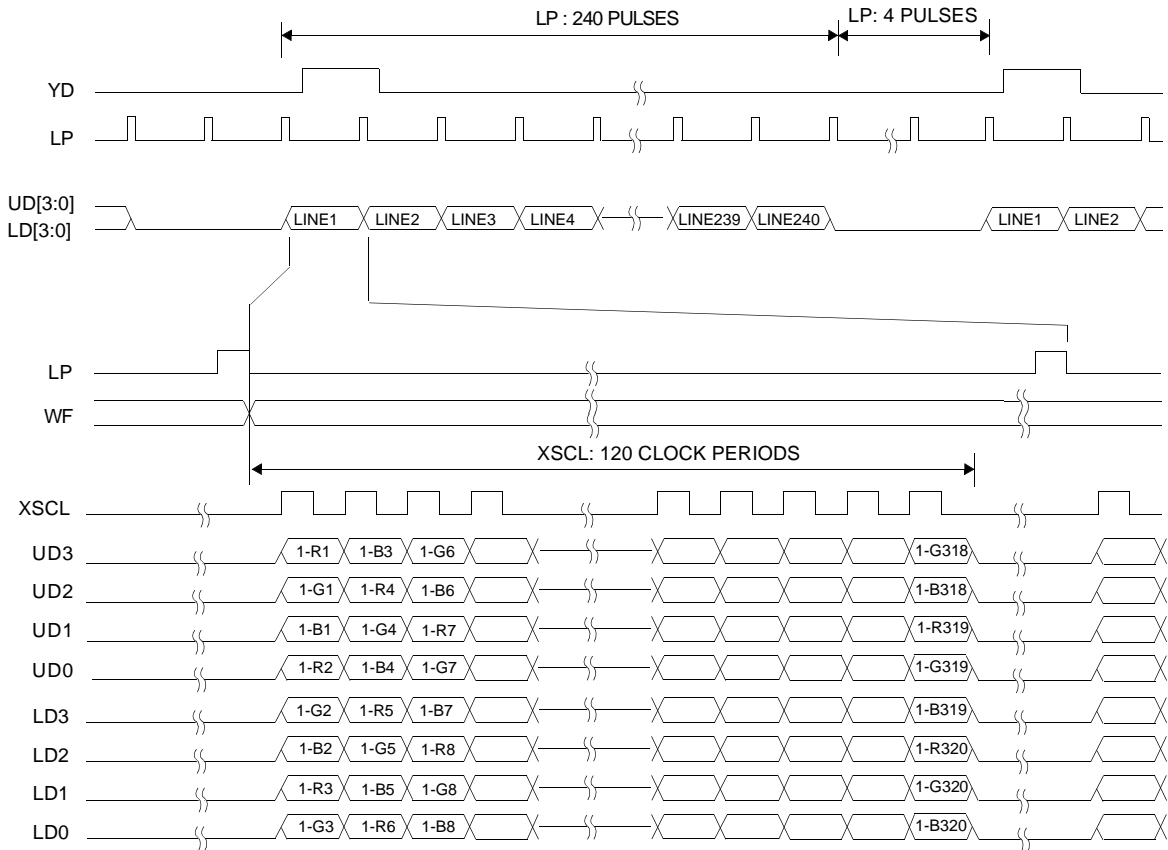


Example timing for a 640x480 panel

## SED1353

### ■ COLOR PASSIVE STN LCD PANEL INTERFACE

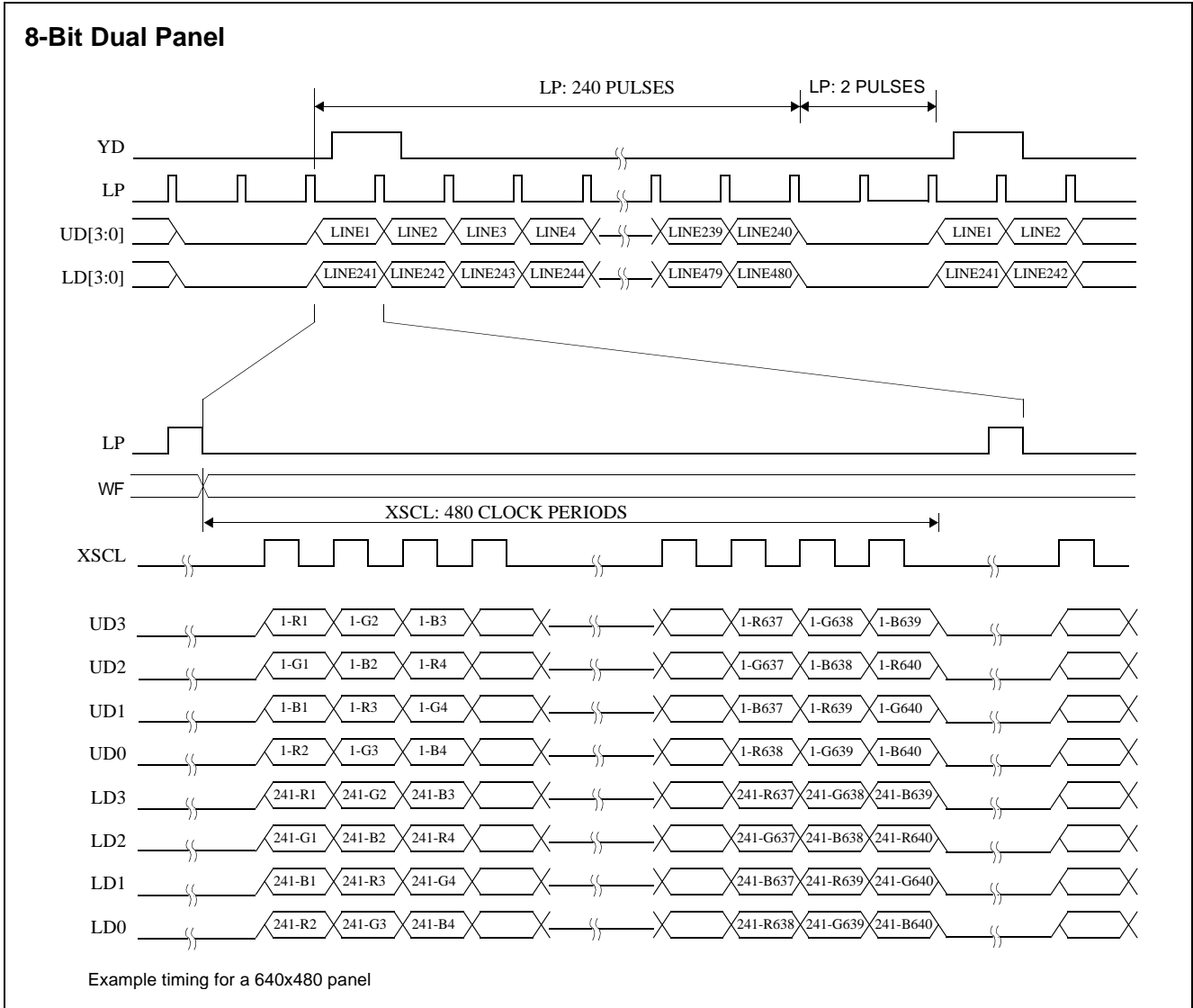
#### 8-Bit Single Panel - Format 2



Example timing for a 320x240 panel



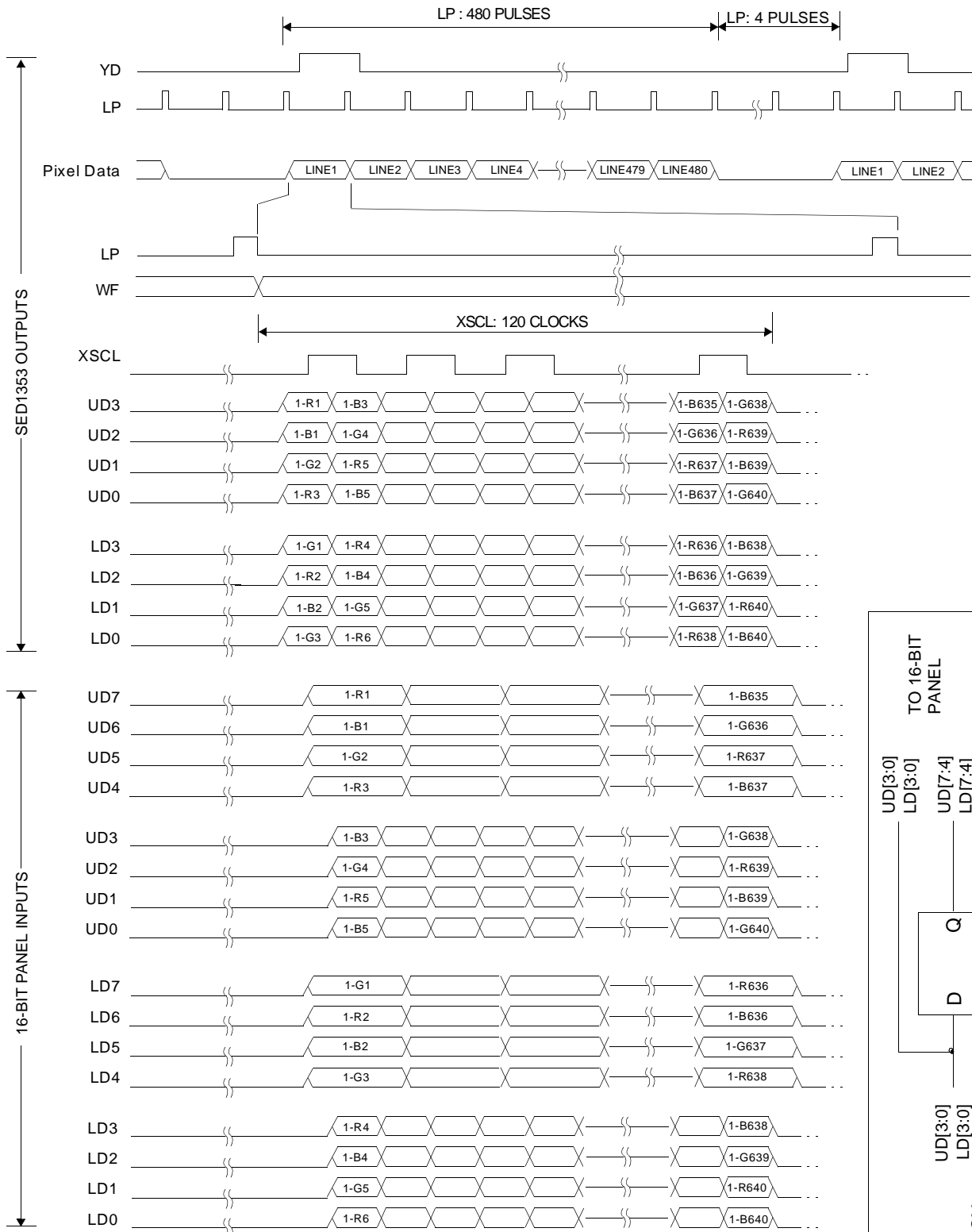
■ COLOR PASSIVE STN LCD PANEL INTERFACE



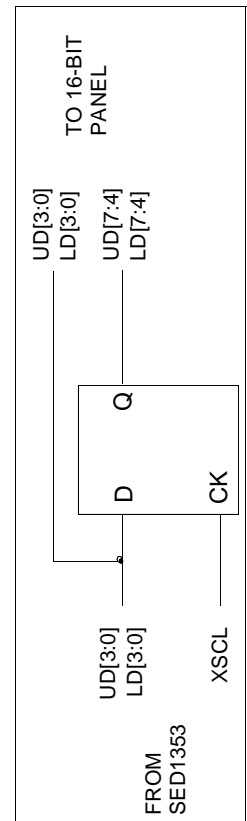
## SED1353

### ■ COLOR PASSIVE STN LCD PANEL INTERFACE

#### 16-Bit Single Panel With External Circuit

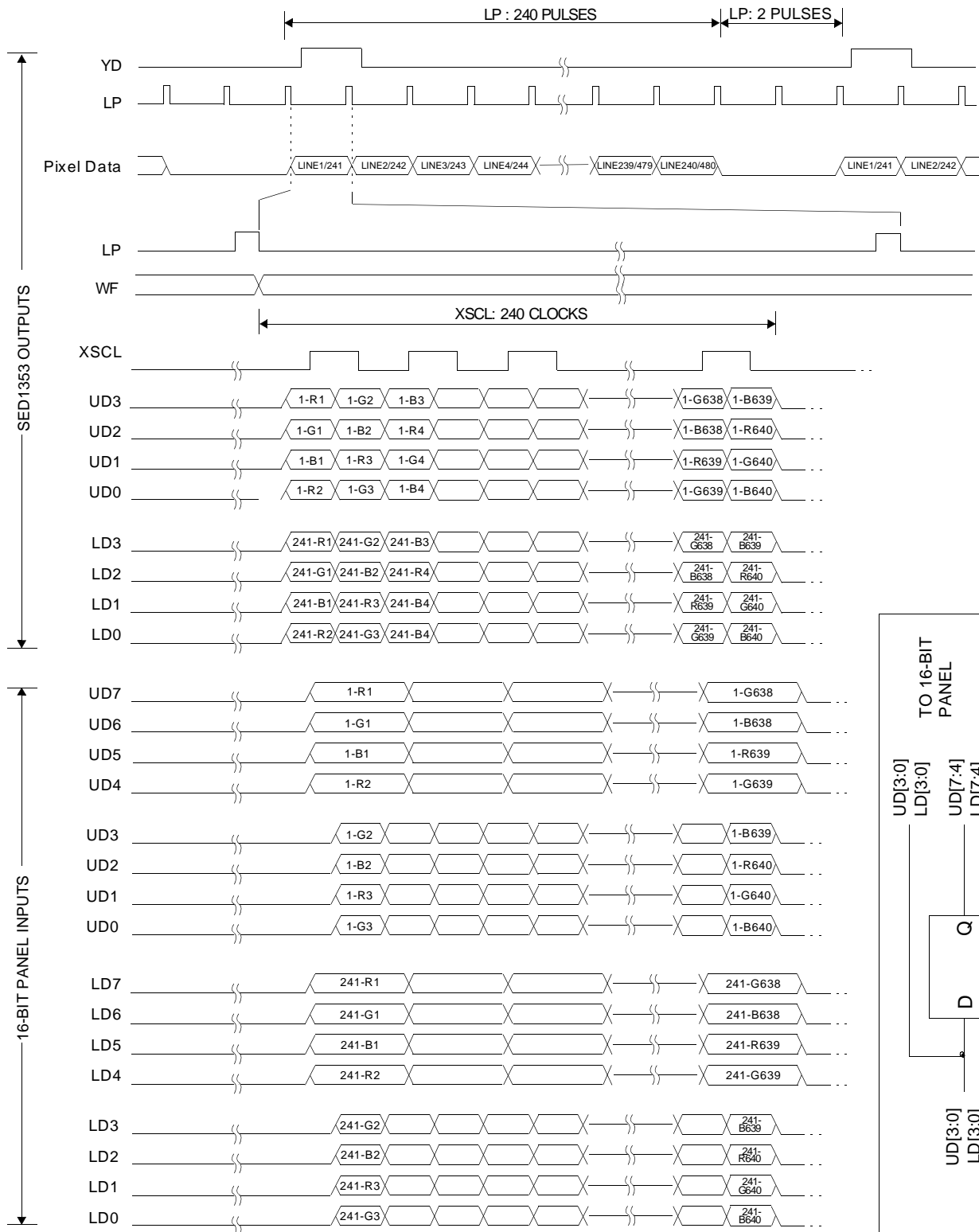


Example timing for a 640x480 panel



■ COLOR PASSIVE STN LCD PANEL INTERFACE

16-Bit Dual Panel With External Circuit

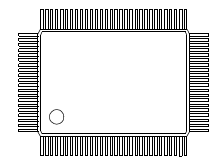
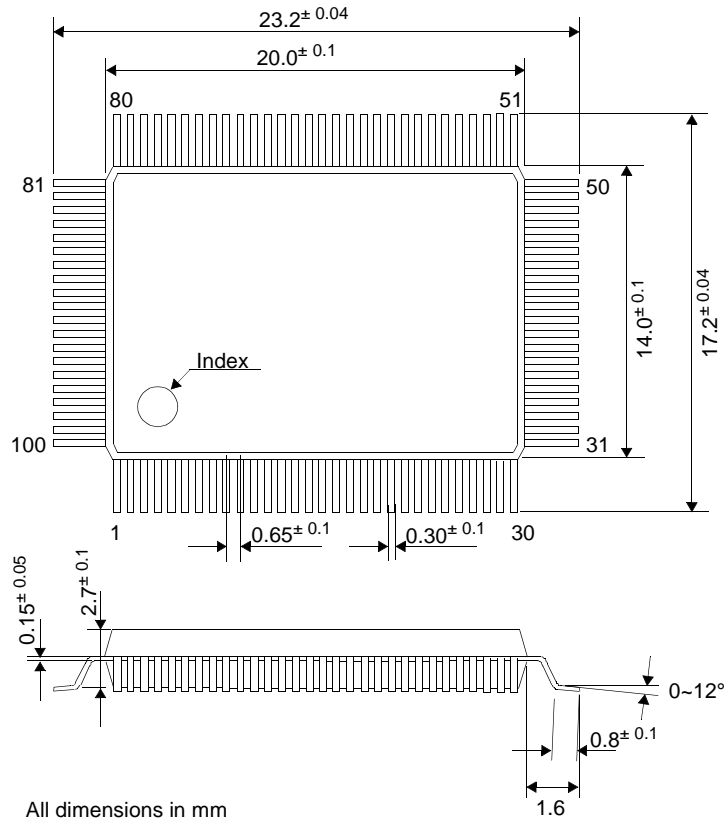


Example timing for a 640x480 panel

SED1353

■ PACKAGE DIMENSIONS: SED1353F0A

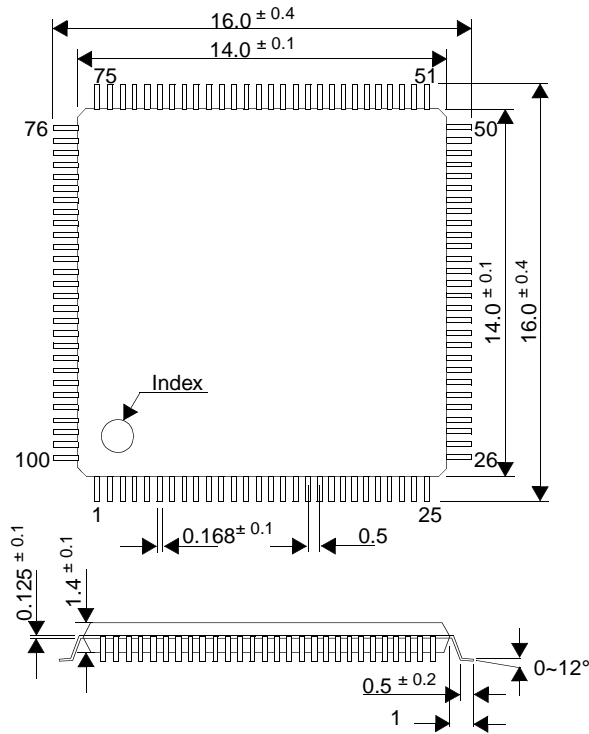
QFP5-100PIN-S2  
(SED1353F0A)



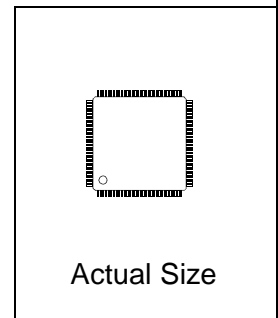
Actual Size

■ PACKAGE DIMENSIONS: SED1353F1A

QFP15-100PIN-STD  
(SED1353F1A)



All dimensions in mm



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