



SMP75-8

TRISIL™

FEATURES

- Bidirectional surge arrester.
- Very low stand-off voltage : $V_{RM} = 8\text{ V}$.
- High repetitive surge capability :
 $I_{PP} = 75\text{ A}$ (10/1000 μs).
- Very low capacitance : $C < 75\text{ pF}$
- Low leakage current : $< 2\text{ }\mu\text{A}$

DESCRIPTION

The SMP75-8 is a very low voltage transient surge arrester especially designed to protect sensitive telecommunication equipment against lightning strikes and other transients.

MAIN APPLICATION

XDSL TRANSMISSION EQUIPMENT

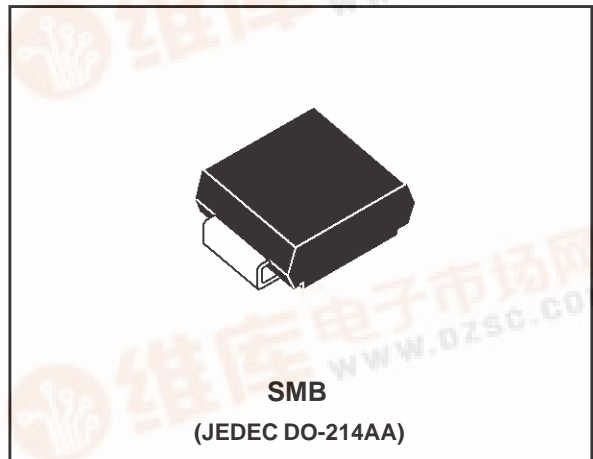
BENEFITS

- Protection against high energy surges.
- Very low breakover voltage : $V_{BO} < 15\text{ V}$, thus avoiding saturation of transformer.
- No signal distortion thanks to very low capacitance.

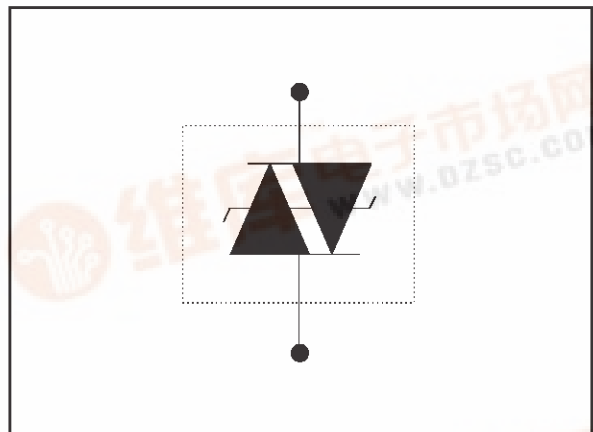
COMPLIES WITH THE FOLLOWING STANDARDS :

- BELLCORE TR-NWT		
-000974:	10/1000 μs	1 kV
	10/1000 μs	75A *
- CCITT K20:	10/700 μs	4 kV
	5/310 μs	100A
- VDE 0433:	10/700 μs	4 kV
	5/310 μs	100A
- VDE 0878:	1.2/50 μs	4 kV
	1/20 μs	100A

* with series resistor or PTC.



SCHEMATIC DIAGRAM



SMP75-8

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^{\circ}\text{C}$)

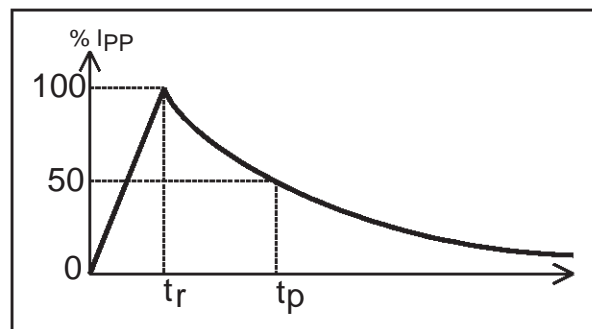
Symbol	Parameter	Value	Unit
I_{pp}	Peak pulse current	10/1000 μs	75
		8/20 μs	250
I_{TSM}	Non repetitive surge peak on-state current One cycle	50Hz	35
		60Hz	37
	Non repetitive surge peak on-state current F = 50Hz	0.2s	14
		2s	6
T_l	Maximum lead temperature for soldering during 10s	260	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 55 to + 150	$^{\circ}\text{C}$
T_j	Maximum junction temperature	150	$^{\circ}\text{C}$

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to leads	20	$^{\circ}\text{C}/\text{W}$
$R_{th(j-a)}$	Junction to ambient on printed circuit (with standard footprint dimensions)	100	$^{\circ}\text{C}/\text{W}$

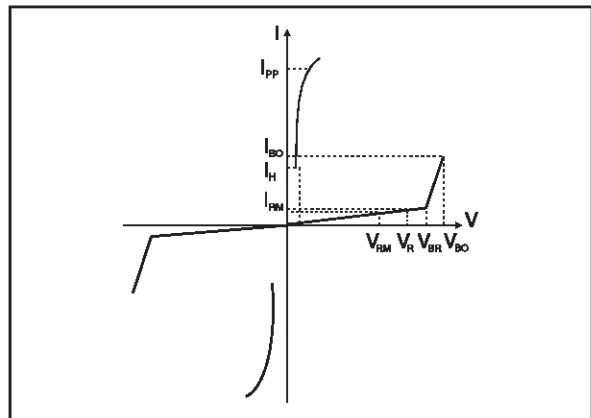
Note 1: Pulse waveform

10 / 1000 μs	$t_r = 10 \mu\text{s}$	$t_p = 1000 \mu\text{s}$
8 / 20 μs	$t_r = 8 \mu\text{s}$	$t_p = 20 \mu\text{s}$
5 / 310 μs	$t_r = 5 \mu\text{s}$	$t_p = 310 \mu\text{s}$
1 / 20 μs	$t_r = 1 \mu\text{s}$	$t_p = 20 \mu\text{s}$
2 / 10 μs	$t_r = 2 \mu\text{s}$	$t_p = 10 \mu\text{s}$



ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{RM}	Stand-off voltage
I_{RM}	Leakage current at stand-off voltage
V_R	Continuous Reverse voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
I_{BO}	Breakover current
I_{PP}	Peak pulse current
C	Capacitance



STATIC PARAMETERS

Type	$I_{RM} @ V_{RM}$ max.		$I_R @ V_R$ max. note 1		$V_{BO} @ I_{BO}$ max. note 2		I_H typ. note 3	C max. note 4
	μA	V	μA	V	V	mA	mA	pF
SMP75-8	2	6	50	8	15	800	50	75

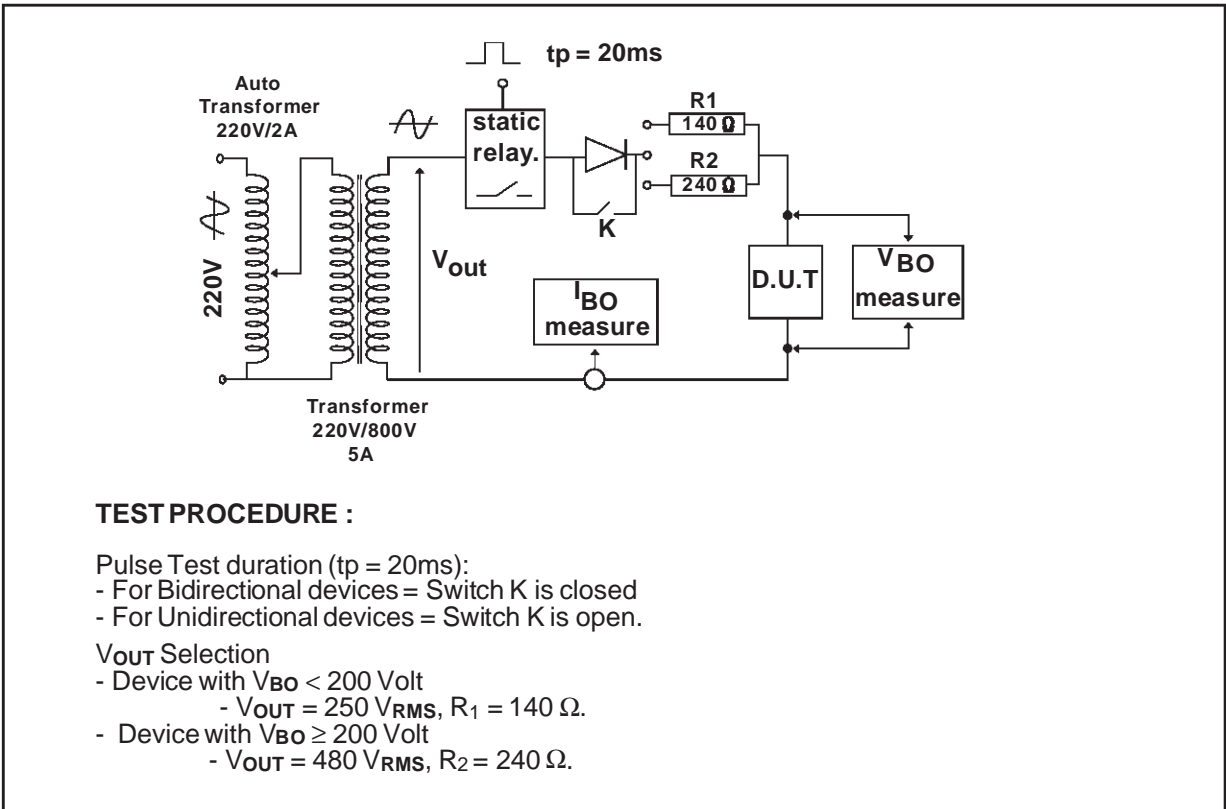
Note 1 : I_R measured at V_R guarantees $V_{BR} > V_R$
Note 2 : Measured at 50Hz, see test circuit 1. In any case $V_{BOmin} \geq V_{BR}$
Note 3 : See functional holding current test circuit 2.
Note 4 : $V_R=1V$ bias, $V_{RMS}=1V$, $F=1MHz$.

DYNAMIC PARAMETERS

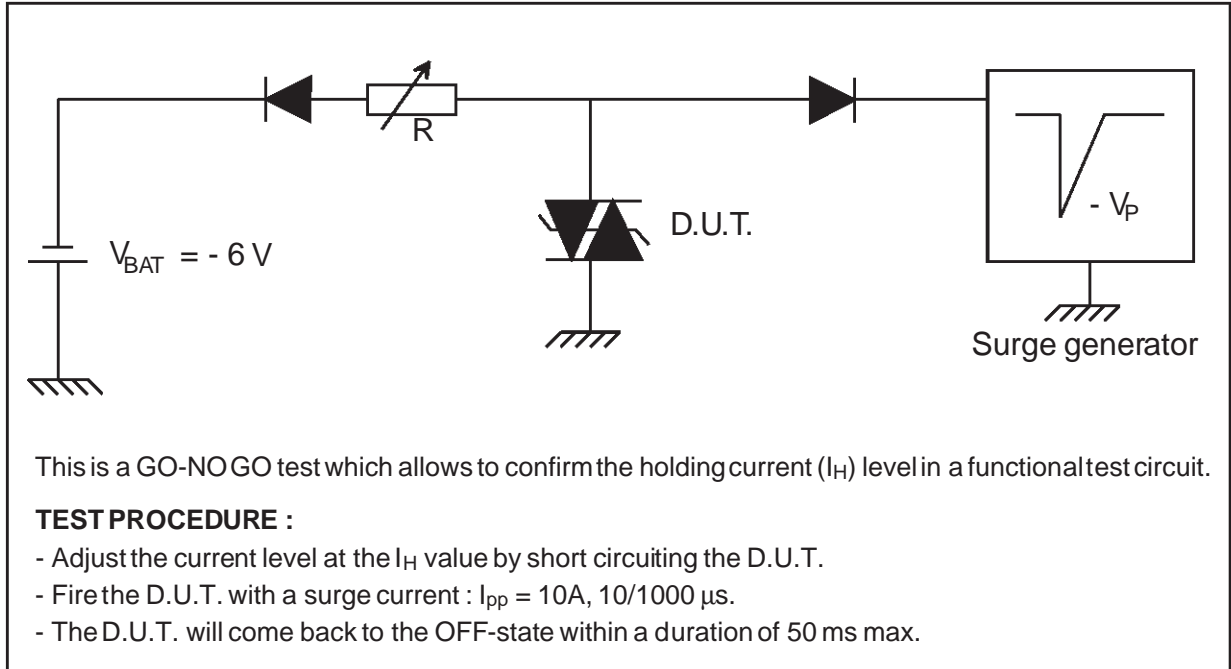
Symbol	Test conditions (see note 5)	Type	Max.	Unit
V_{BO}	<p>Test conditions 1 $V_{RISE} = 100 V/\mu s, di/dt < 10 A/\mu s, I_{PP} = 75 A$</p> <p>Test conditions 2 $V_{RISE} = 1 kV/\mu s, di/dt < 10 A/\mu s, I_{PP} = 10 A$</p>	SMP75-8	20	V

Note 5 : V_{BO} parameters are given by a KeyTek 'System 2' generator with PN246I module.
 See test circuits (3) for V_{BO} dynamic parameters.

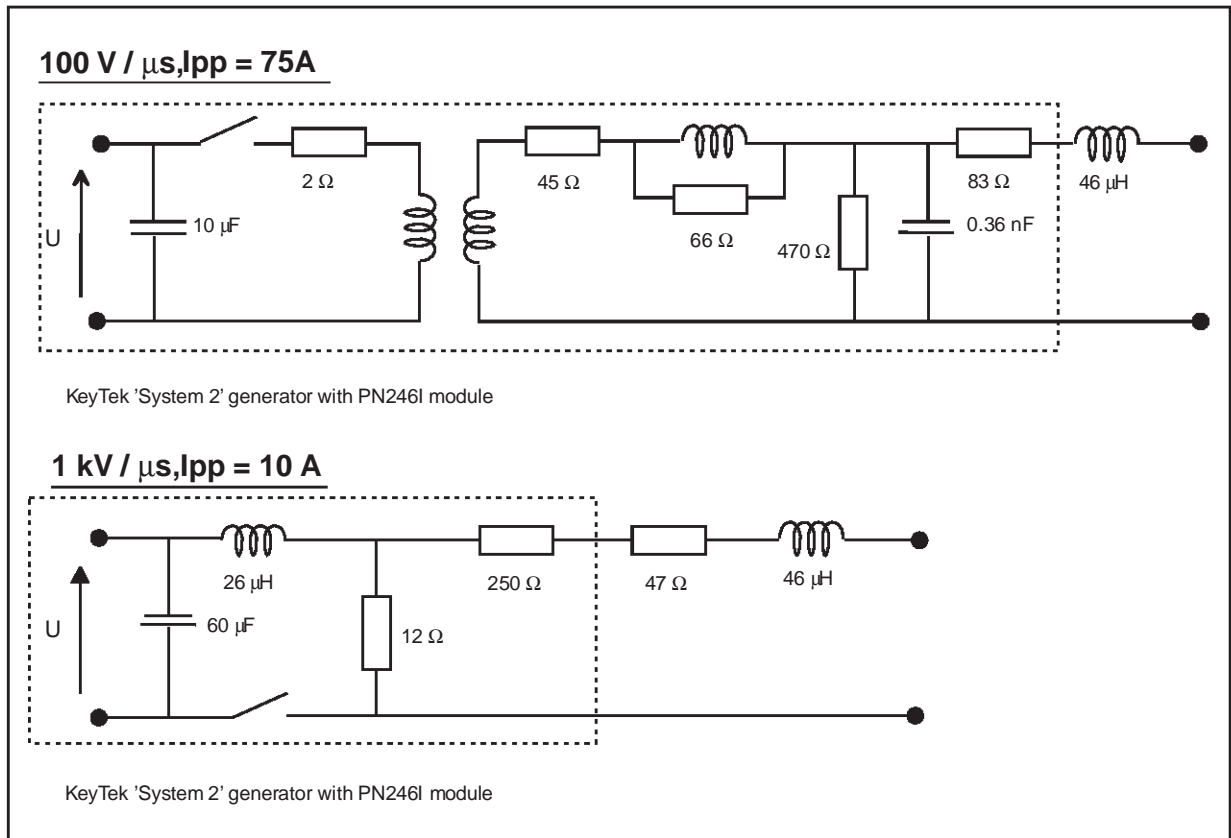
TEST CIRCUIT 1 FOR I_{BO} and V_{BO} parameters :



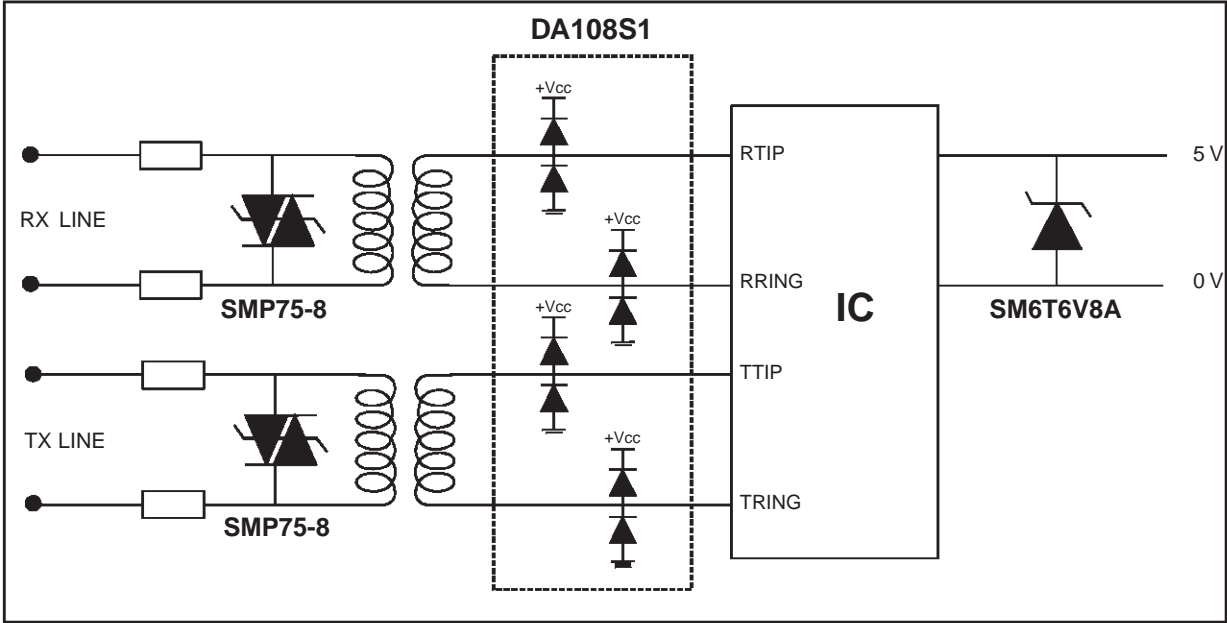
FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT 2: GO-NO GO TEST



TEST CIRCUITS 3 FOR V_{BO} DYNAMIC PARAMETERS



TYPICAL APPLICATION : T1 / E1 protection



The above schematic shows a T1 / E1 application circuit. This type of line protection may be used in premises equipment or telephone company equipment on ports directly connected to metallic plant lines.

During the lightning surge, the low voltage Trisil **SMP75-8** provides an efficient crowbar protection on the primary side of the transformer.

The SMP75-8 has a maximum peak pulse current of 75A (10/1000µs pulse) and a maximum breakover voltage of 15V. This low voltage prevents the transformer to be saturated when a surge occurs on the line. Additionally, the low capacitance (65pF) is required to avoid significant signal degradation in the case of high speed digital pulses.

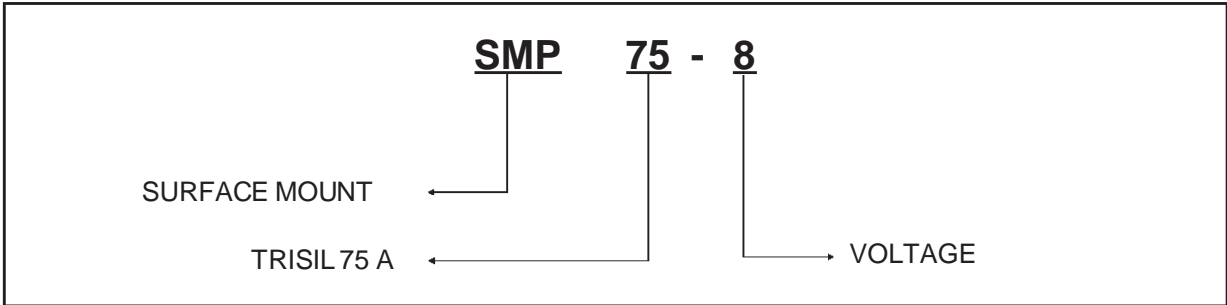
To protect the IC line interface from the remaining energy which is coupled through the transformer,

additional voltage protection is recommended on the line input / output pins of the IC. The diode array DA108S1 connected between +Vcc and GND is then used to limit the remaining overvoltage within a safe level.

The DA108S1 is especially dedicated to this application because. Its fast response time and low forward voltage drop enable it to clamp any surge before the IC line interface internal protection fails. Additionally, the low capacitance (30pF) is required to prevent signal degradation of the high speed data.

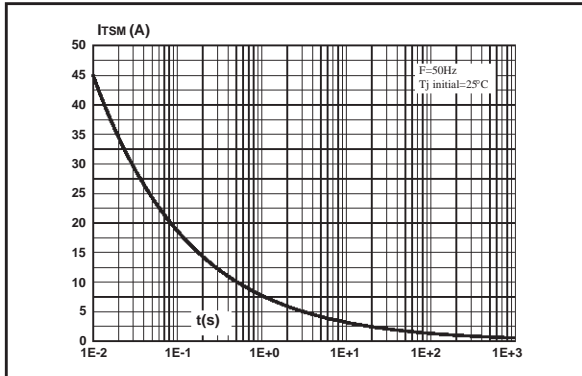
The DA108S1 is a fully integrated (1 chip) device and results from the ST ASD™ (Application Specific Discretes) technology. ASDs™ combine the functions of several components into a single monolithic device that is tailored to meet the exact requirement of a specific application, allowing higher density and improved reliability.

ORDER CODE



SMP75-8

Non repetitive surge peak current versus overload duration.

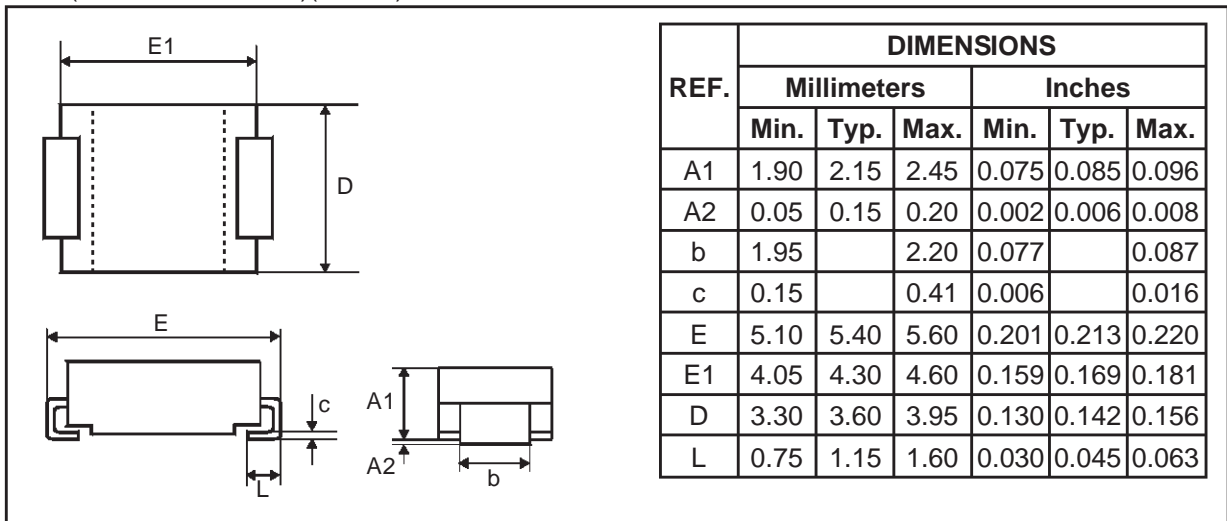


MARKING

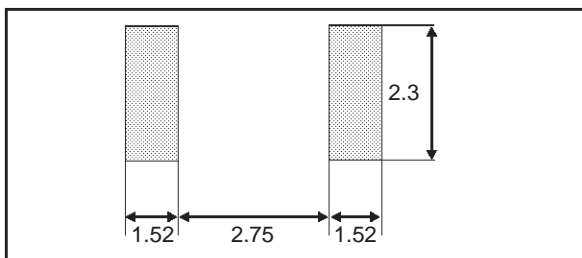
Package	Type	Marking
SMB	SMP75-8	L08

PACKAGE MECHANICAL DATA

SMB (JEDEC DO-214AA)(Plastic)



FOOT PRINT (in millimeters)



Packaging : tape and reel

Weight : 0.12g

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