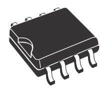
STSR3

SYNCHRONOUS RECTIFIERS SMART DRIVER FOR FLYBACK

- SUPPLY VOLTAGE RANGE: 4V TO 5.5V
- TYPICAL PEAK OUTPUT CURRENT: (SOURCE 2A, SINK 3.5A)
- OPERATING FREQUENCY: 30 TO 750 KHz
- SMART TURN-OFF ANTICIPATION TIMING
- AUTOMATIC TURN OFF FOR DUTY CYCLE LESS THAN 14%
- POSSIBILITY TO OPERATE IN DISCONTINUOUS MODE



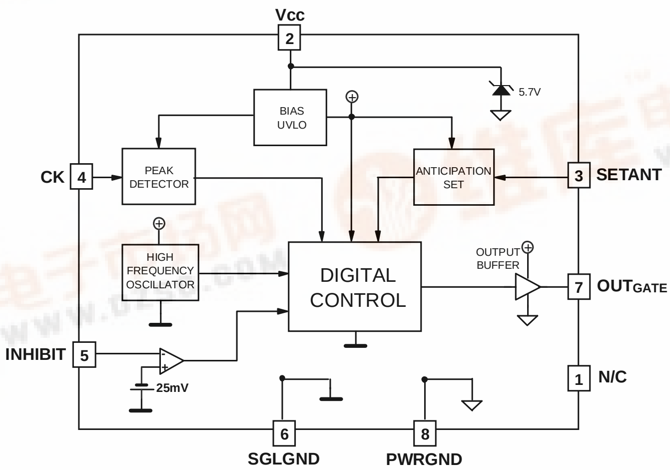
SO-8

DESCRIPTION

STSR3 Smart Driver IC provides a high current outputs to properly drive secondary Power Mosfets used as Synchronous Rectifier in low output voltage, high efficiency Flyback Converters. From a synchronizing clock input, withdrawn on the secondary side of the isolation transformer, the IC generates a driving signal with set dead times with respect to the primary side PWM signal.

The IC operation prevents secondary side shoot-through conditions at turn-on of the primary switch providing anticipation in turn-off the output. This smart function is implemented by a fast cycle-after-cycle logic control mechanism, based on a high frequency oscillator synchronized by the clock signal. This anticipation is externally set through external component. A special Inhibit function allows to shut-off the drive output. This feature makes discontinuous conduction mode possible and avoids reverse conduction of the synchronous rectifier.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Input Voltage		-0.3 to 6	V
$V_{OUTGATE}$	Max Gate Drive Output Voltage		-0.3 to V_{CC}	V
$V_{INHIBIT}$	Max INHIBIT Voltage (*)		-0.6 to V_{CC}	V
V_{CK}	Clock Input Voltage Range (*)		-0.3 to V_{CC}	V
P_{TOT}	Continuous Power Dissipation at T_A=105°C without heatsink		270	mW
ESD	Human Body Model	Pins 1,2, 4, 5, 6, 7, 8	±1	KV
		Pin 3	±0.9	KV
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_{op}	Operating Junction Temperature Range		-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) A higher positive voltage level can be applied to the pin with a resistor which limits the current flowing into the pin to 10mA maximum

THERMAL DATA

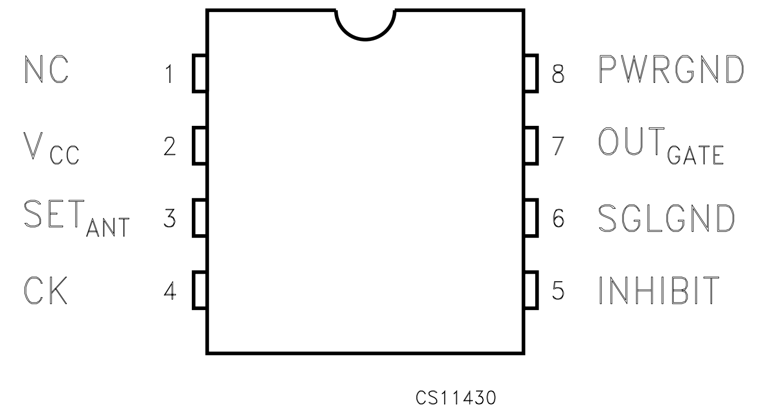
Symbol	Parameter	SO-8	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-case	40	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (*)	160	°C/W

(*) This value is referred to one layer pcb board with minimum copper connections for the leads. a minimum value of 120 °C/W can be obtained improving thermal conductivity of the board

ORDERING CODES

TYPE	SO-8	SO-8 (T&R)
STSR3	STSR3CD	STSR3CD-TR

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

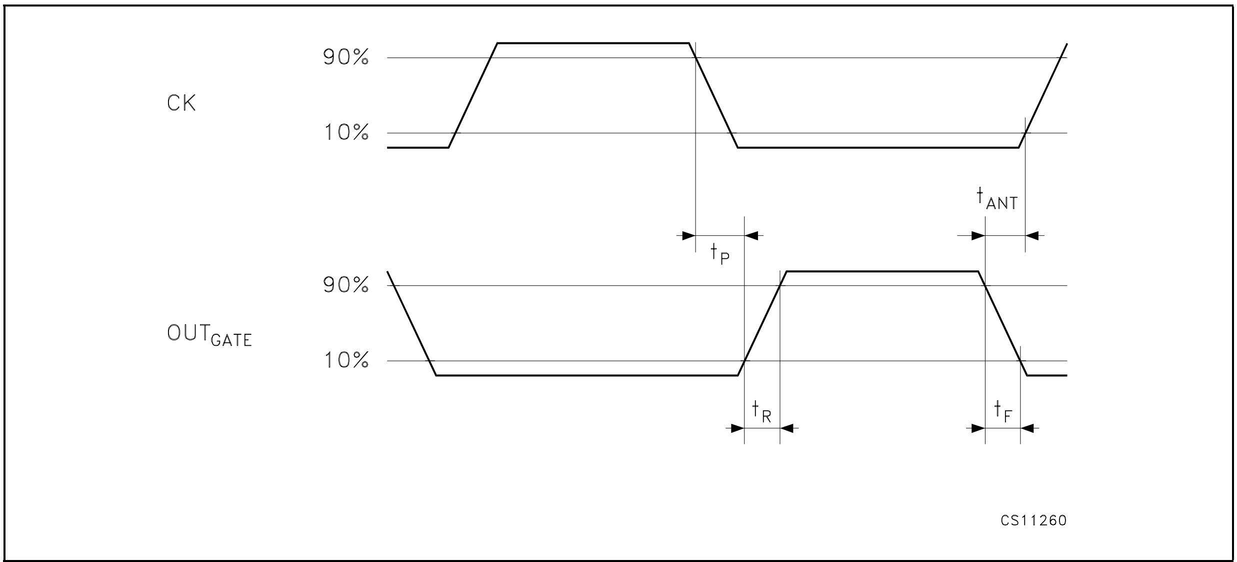
Pin N°	Symbol	Name and Function
1	NC	No internally connected
2	V_{CC}	The supply voltage range from 4.0V to 5.5V allows applications with logic gate threshold mosfets. UVLO feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
3	SET_{ANT}	The voltage on this pin sets the anticipation (t_{ANT}) in turning off the OUT_{GATE} It is possible to choose among three different anticipation times by discrete partitioning of the supply voltage.
4	CK	This input provides synchronization for IC's operations, being the transitions between the two output conditions based on a positive threshold, equal for the two slopes. A smart internal control logic mechanism using a 15MHz internal oscillator generates proper anticipation timing at the turn-off of each output. This feature allows safe turn-off of Synchronous Rectifier avoiding any eventual shoot-through situation on secondary side at both transitions. Smart clock revelation mechanism makes these operations independent by false triggering pulses generated in light load conditions. Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
5	INHIBIT	This input enables OUT_{GATE} to work when its voltage is lower than the negative threshold voltage ($V_{INHIBIT}<V_H$). If $V_{INHIBIT}>V_H$ the OUT_{GATE} will be high for a minimum conduction time ($t_{ON(GATE)}$). In typical flyback converter application, it is possible to turn off the synchronous MOSFET when the current through it tends to reverse, allowing discontinuous conduction mode and providing protection to the converter from eventual sinking current from the load.Absolute maximum voltage rating of the pin can be exceeded limiting the current flowing into the pin to 10mA max.
6	SGLGND	Reference for all the control logic signals. This pin is completely separated from the PWRGND to prevent eventual disturbances to affect the control logic.
7	OUT_{GATE}	Gate Drive signal for synchronous MOSFET. Anticipation [t_{ANT}] in turning off OUT_{GATE} is provided during the transition in which the clock input goes to high level.
8	PWRGND	Reference for power signals, this pin carries the full peak currents for the two outputs.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, CK= 250kHz, duty-cycle=50%, $V_{INHIBIT}$ =-200mV, T_J =-40 to 125°C, unless otherwise specified.)

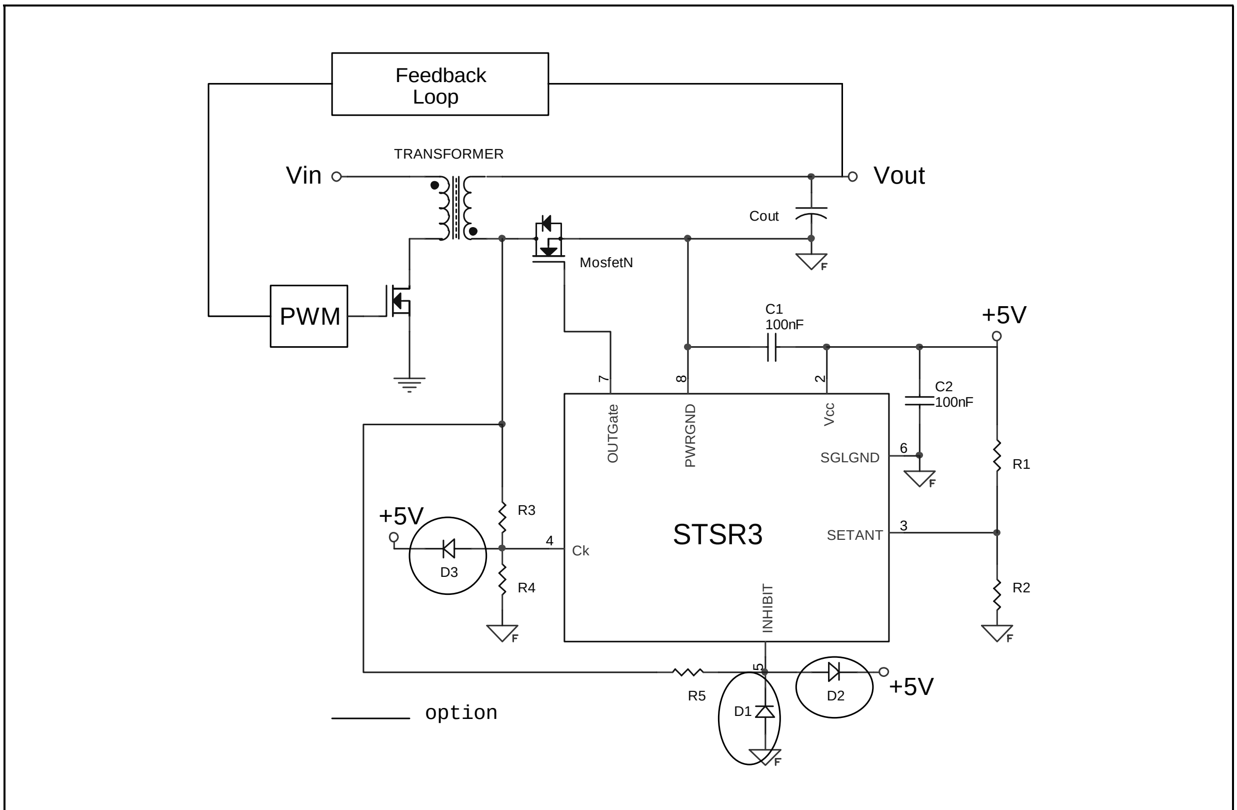
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT AND UNDER VOLTAGE LOCK OUT						
V_{CCON}	Start Threshold			3.8	4	V
V_{CCOFF}	Turn OFF Threshold After Start		3.5	3.6		V
V_Z	Zener Voltage	CK=0V I_Z = 2mA	5.5	5.8	6	V
I_{CC}	Unloaded Supply Current	OUT_{GATE}= no load		15	20	mA
		CK=0V OUT_{GATE}= no load		3	5	
GATE DRIVER OUTPUTS						
V_{OL}	Output Low Voltage	$I_{OUTGATE}$=-200mA		0.10	0.16	V
V_{OH}	Output High Voltage	$I_{OUTGATE}$=200mA	4.70	4.85		V
I_{OUT}	Output Source Peak Current			2		A
	Output Sink Peak Current			3.5		
R_{OUT}	Output Series Source Resistance	$I_{OUTGATE}$=-200mA		0.75	1.5	Ω
	Output Series Sink Resistance	$I_{OUTGATE}$=200mA		0.5	0.8	
t_R	OUT_{GATE} Rise Time	C_{LOAD}=5nF (Note 1)		40		ns
t_F	OUT_{GATE} Fall Time	C_{LOAD}=5nF (Note 1)		30		ns
t_P	Clock Propagation Delay to Turn ON of OUT_{GATE}	No Load		50		ns
TURN-OFF ANTICIPATION TIME						
t_{ANT}	OUT_{GATE} Turn-off Anticipation Time	V_{ANT} = 0 to 1/3V_{CC}; no load		75		ns
		V_{ANT} = 1/3V_{CC} to 2/3V_{CC}; no load		150		
		V_{ANT} = 2/3V_{CC} to V_{CC}; no load		225		
I_{SETANT}	Leakage Current (Note 2)		-0.1		0.1	µA
INHIBIT OUT_{GATE} ENABLE						
V_H	Threshold Voltage	T_J = 25°C	-30	-25		mV
I_H	Leakage Current (Note 2)	$V_{INHIBIT}$ = 200mV		-400		nA
		$V_{INHIBIT}$ = -200mV			1	µA
$t_{ON(GATE)}$	Minimum OUT_{GATE} On time	$V_{INHIBIT}$ = +200mV		250		ns
SYNCHRONIZATION INPUT						
V_{CK}	Reference Voltage	T_J = 25°C		2.6	2.8	V
D_{OFF}	Duty Cycle Shut Down	T_J = 25°C	13	14		%
	Duty Cycle Turn ON after Shut Down	T_J = 25°C		18	20	

Note1: t_R is measured between 10% and 90% of the final voltage; t_F is measured between 90% and 10% on the initial voltage
Note2: Parameter guaranteed by design

TIMING DIAGRAM



APPLICATION INFORMATION: STSR3 IN FLYBACK CONVERTER SECONDARY SIDE



NOTES
1) Ceramic Capacitors C1 and C2 must be placed very close to the IC;
2) R1 and R2 set the anticipation time by partitioning the V_{CC} voltage;
3) R3 and R4 is a resistor divider meant to provide the correct CK voltage range;
4) R5 limits the current flowing through diode D2 when Freewheeling drain voltage is high;
5) D1 could be necessary to protect INHIBIT pin from negative voltages.
6) D2 could be necessary to protect INHIBIT pin from voltages higher than V_{CC}
7) D3 could be necessary to protect CK pin from voltages higher than V_{CC}.
8) SGLGND layout trace must not include OUT_{GATE} current paths.
9) A capacitor in parallel with R4 could be necessary to eliminate turn off voltage spike.

EXAMPLE OF COMPONENTS SELECTION FOR A FLYBACK CONVERTER

Flyback Specification:

V_{IN}=36-72V

V_{OUT}=3.3V

n=Np/Ns=4.5

R_3 and R_4 are calculated assuring a minimum voltage of 2.8V at Ck pin. At 36V input, the voltage on the secondary winding is 36/4.5=8V. Choosing R_3=1.5KΩ, R_4 results to be:

$$R_4 \geq \frac{V_{CK} \times R_3}{V_{IN} - I_{CK(2.8)} \times R_3 - V_{CK}} = 1k\Omega \times \frac{2.8V \times 1.5k\Omega}{8V - 220\mu A \times 1.5k\Omega - 2.8V} = 862\Omega$$

R_4=1kΩ is chosen. At 72V input the current at Ck pin is calculated as:

$$I_{CK} = \frac{V_{IN(max)} - V_{CC} - 0.3}{R_3} = \frac{16 - 5 - 0.3}{1.5k\Omega} = 7.13mA$$

This value is below the maximum allowable current flowing into the Ck pin (10mA). If the 10mA value is exceeded an external diode connected to V_{CC} must be added (D3).

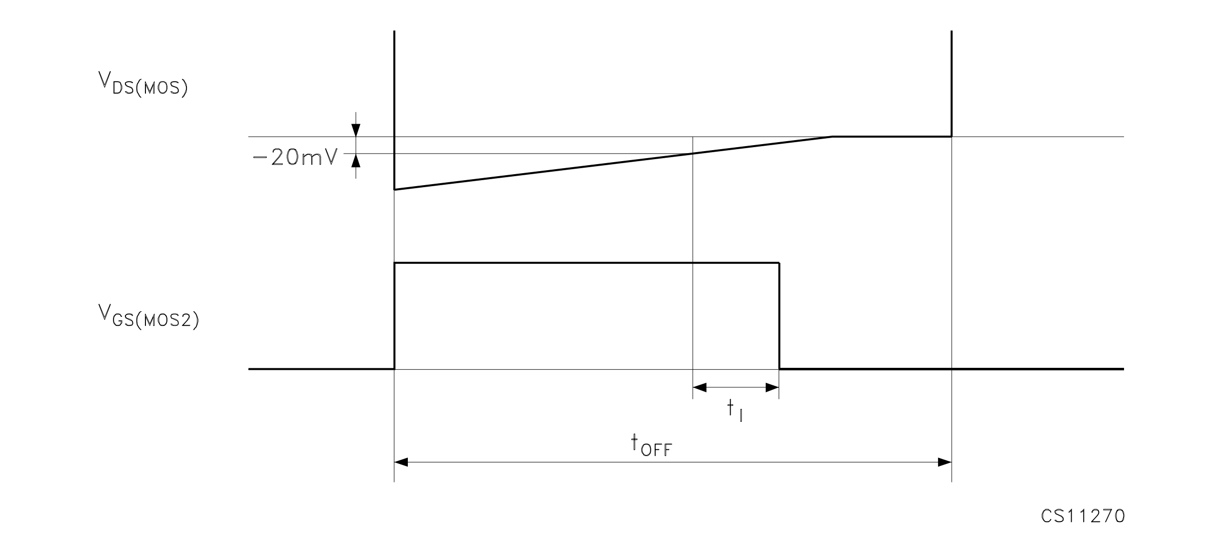
R_1 and R_2 values set the anticipation time for OUT_{GATE}. For $R_1=\infty$ and R_2=0, t_{ANT}=75ns; for $R_1=R_2$=10kΩ, t_{ANT}=150ns; for R_1=0 and $R_2=\infty$, t_{ANT}=225ns.

The RC group composed by R_5 and the parasitic capacitance of Inhibit pin (typically 5pF) delays the signal on Inhibit comparator. This delay must be lower than 200ns. This condition imposes a maximum value for R_5 of about 20kΩ.

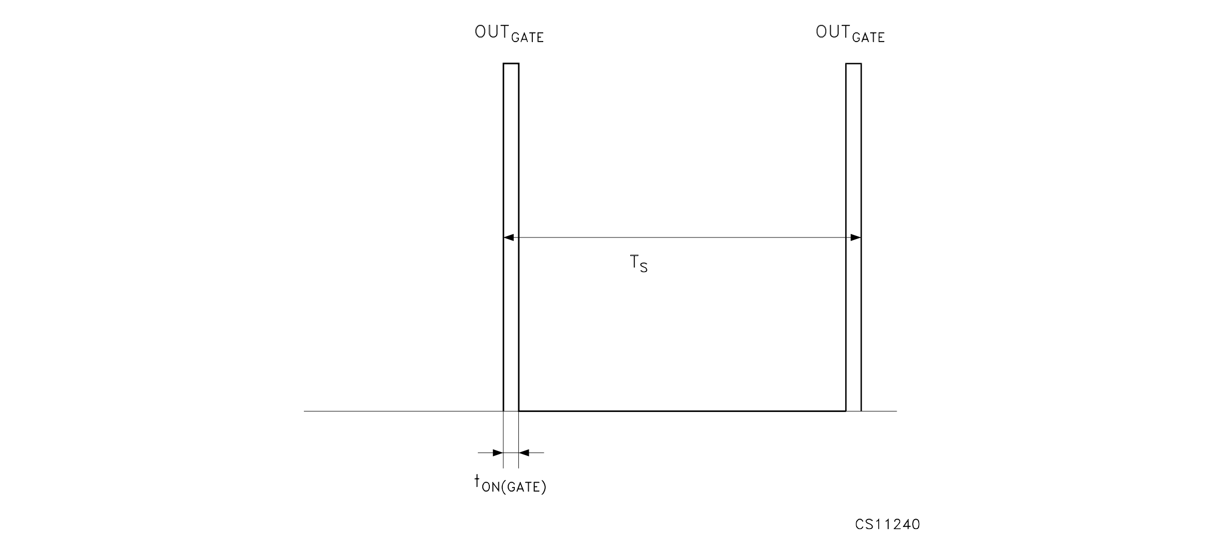
In general a suggested value for R_5 is 10kΩ. At 72V input, the secondary voltage is 16V, so the maximum current flowing into Inhibit pin is 16V/10kΩ=1.6mA which is below the maximum allowable current for the pin (10mA). If the 10mA value is exceeded an external diode (D2) connected to V_{CC} must be added.

The maximum negative voltage of –0.6V must be guaranteed for the Inhibit pin. If this negative voltage is exceeded the current must be limited to 50mA. If necessary, a diode (D1) connected to SGLGND can be added to satisfy this specification.

INHIBIT OPERATION OF OUT_{GATE} IN DISCONTINUOUS CONDUCTION MODE



INHIBIT OPERATION OF OUT_{GATE}



TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C

Figure 1 : Zener Characteristics

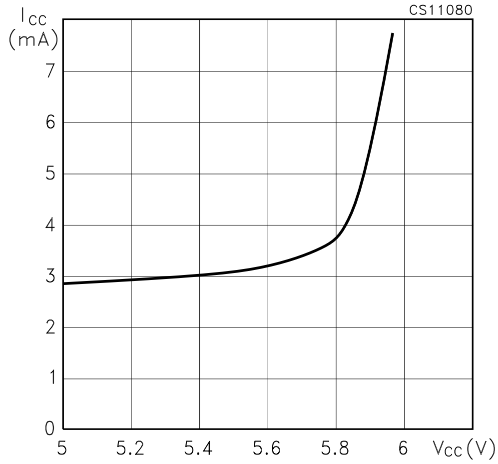


Figure 4 : Sink-Source ON Resistance vs Temperature

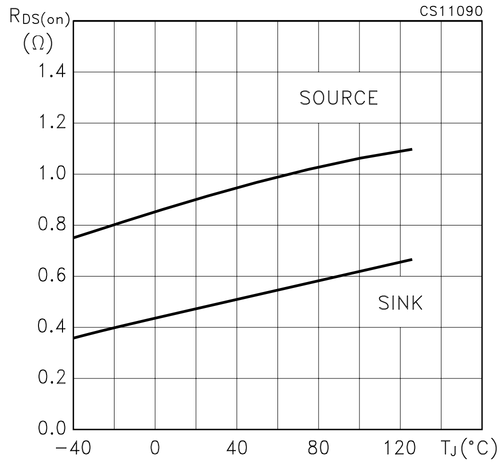


Figure 2 : Rise and Fall Time vs Load Capacitor

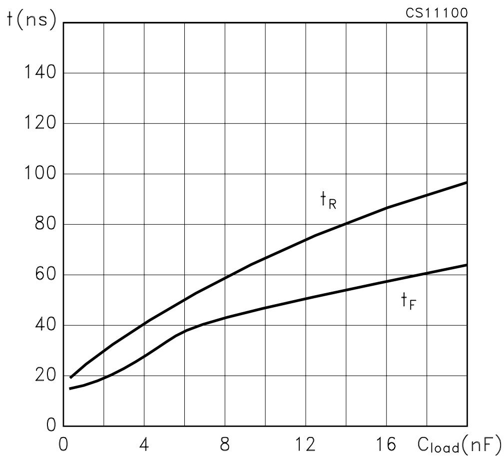


Figure 5 : Clock Threshold Voltage vs Temperature

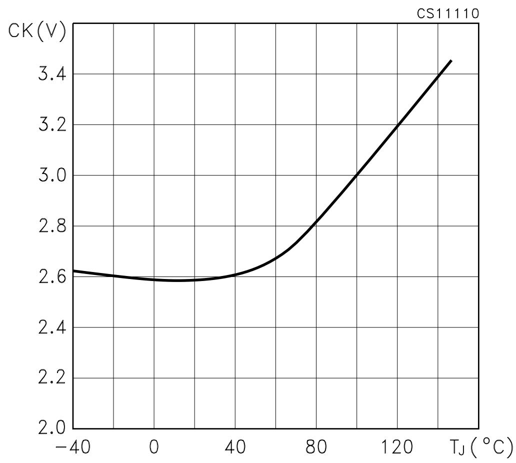


Figure 3 : OUT_{GATE} vs Characteristics

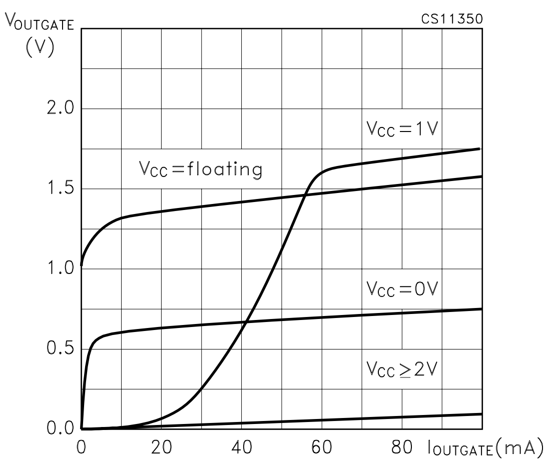


Figure 6 : INHIBIT Threshold Voltage vs Temperature

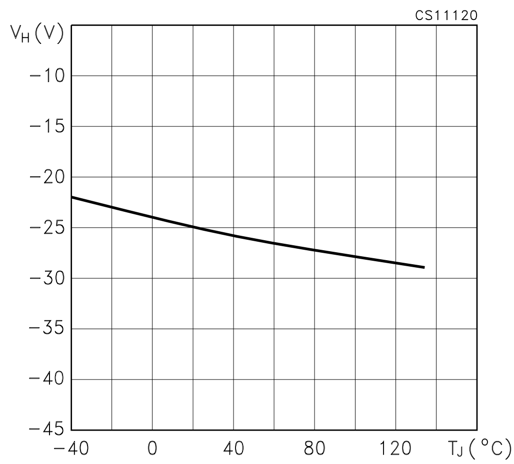


Figure 7 : Supply Current vs Load Capacitor

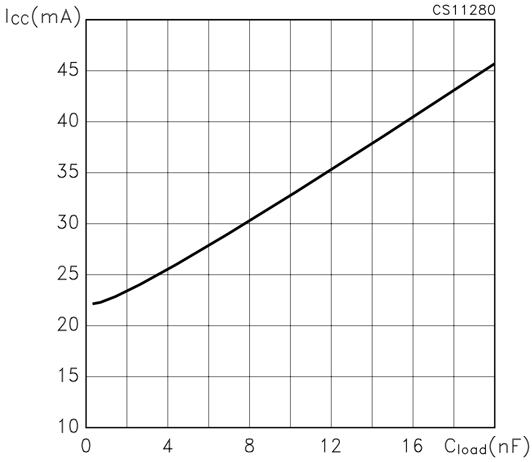


Figure 8 : Supply Current vs Clock Frequency

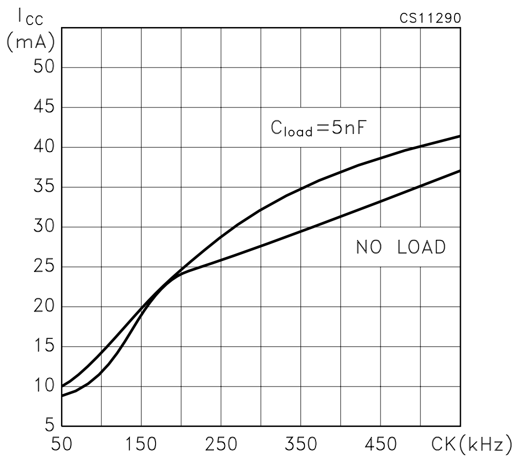


Figure 9 : GATE ON Time vs Temperature

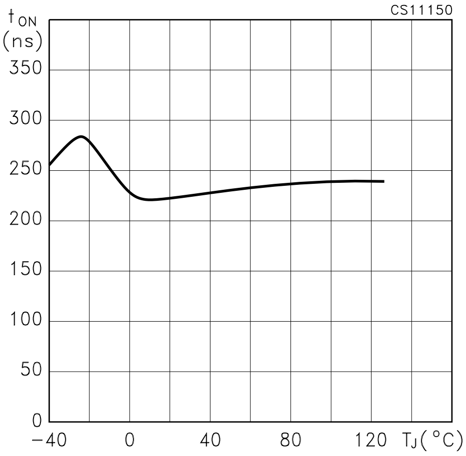


Figure 10 : Duty Cycle Shut Down vs Temperature

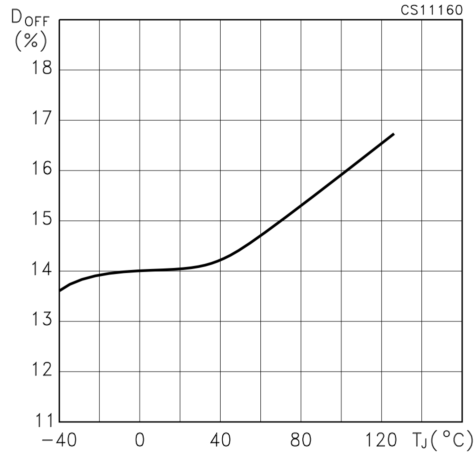


Figure 11 : Duty Cycle Turn ON After Shut Down vs Temperature

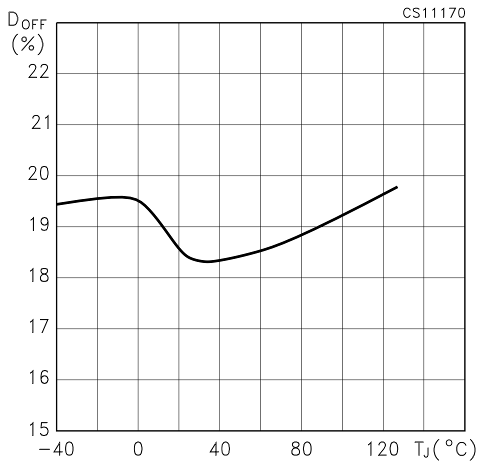
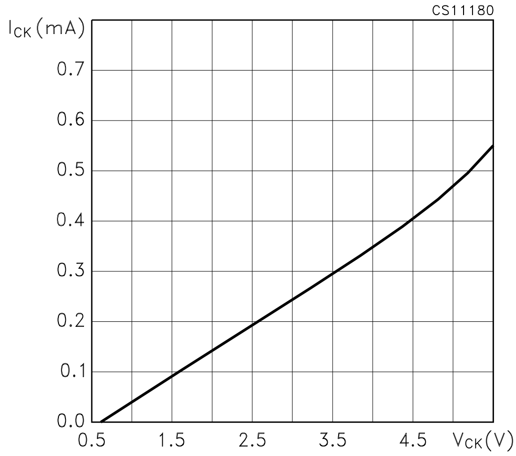
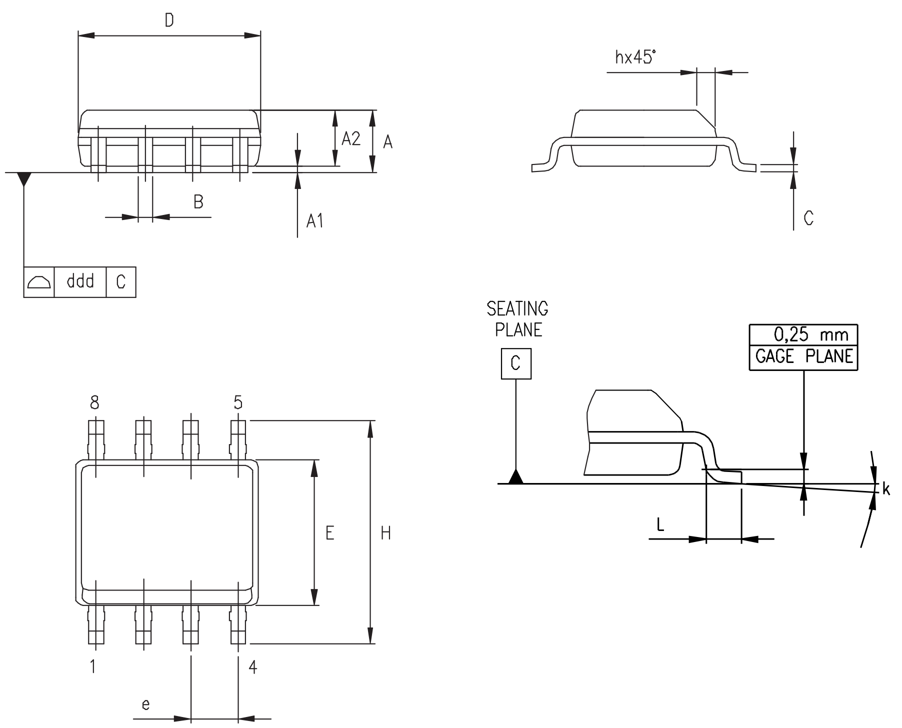


Figure 12 : Clock Leakage Current vs Clock Voltage



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



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Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319