PurePath Digital™ AUDIO SIX-CHANNEL PWM PROCESSOR

FEATURES

- Audio Input/Output
  - Automatic Master Clock Rate and Data Sample Rate Detection
  - Four Serial Audio Inputs (Eight Channels)
  - Support for 32, 44.1, 48, 88.2, 96, 176.4, and 192-kHz Sampling Rates
  - Data Formats: 16-, 20-, or 24-Bit Input Data Left, Right, and I^2S,
  - 64 or 48 × Fs Bit Clock Rate
  - 128, 192, 256, 384, and 512 × Fs Master Clock Rates (Up to a Maximum of 50 MHz)
  - Six PWM Audio Output Channels
  - Any Output Channel Can be Mapped to Any Output Pin
  - Support Single-Ended and Bridge Tied Load
  - I^2S Serial Audio Output
- Audio Processing
  - Volume Control Range +48 dB to – 100 dB
  - Master Volume Control +24 dB to –100 dB in 0.5 dB Increments
  - Eight Individual Channel Volume Controls With +24 dB to –100 dB Attenuation in 0.5 dB Increments
  - Serial Output Can be Produced by Down-Mix of 5.1 Channel Input or 4^{th} Serial Input
  - 5.1 Channel Down Mix to 2.1 or 3.1 PWM Output Speaker System
  - Integrated Bass Management
  - Two Programmable Biquads in Subwoofer Channel
  - Full Six Channel Input and Output Mapping
  - Selectable DC Blocking Filters
- PWM Processing
  - 8x Over Sampling With 4^{th} Order Noise Shaping at 44.1–48 kHz, 4x Over Sampling at 88.2, 96 kHz, 2x Over Sampling at 176.4, 192 kHz, and 12x Over Sampling at 32 kHz
  - ≥105-dB Dynamic Range (TAS5086+TAS5186)
  - THD < 0.06% (TAS5086 Only)
  - 20 – 20 kHz Flat Noise Floor for 44.1, 48, 88.2, 96, 176.4 and 192 kHz Data Rates
  - Digital De-emphasis for 32 kHz, 44.1 kHz and 48 kHz Data Rates
  - Intelligent AM Interference Avoidance System Provides Clear AM Reception
  - Adjustable Modulation Limit From 93.8% to 99.2%
- General Features
  - Automated Operation With Easy to Use Control Interface
  - I^2C Serial Control Slave Interface
  - Control Interface Operational Without MCLK
  - Single 3.3-V Power Supply
  - 38-Pin TSSOP Package

DESCRIPTION

The TAS5086 is a six channel digital pulse width modulator (PWM) that provides both advanced performance and a high level of system integration. TAS5086 is designed to interface seamlessly with most audio digital signal processors and MPEG decoders accepting a wide range of input data and clock formats.

The TAS5086 drives six channels of speakers in either single-ended or bridge tied load configurations that accept a 1N+1 interface format. TAS5086 also supports 2N+1 power stages with the use of some external logic (e.g. TAS5112). Stereo line out in I^2S format is available with either a pass-through signal (SDIN4) or an internal down mix.

TAS5086 uses AD modulation operating at a 384-kHz switching rate for 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz data. The 8 x over sampling combined with the 4th order noise shaper provides a broad flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

TAS5086 is clock slave only device. TAS5086 receives MCLK, SCLK and LRCLK from other system components. TAS5086 accepts master clock rates of 128, 192, 256, 384, and 512 Fs. TAS5086 accepts a 64 Fs master clock for 176.4-kHz and 192-kHz data.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The TAS5086 accepts a 64-Fs bit clock for all data rates. The TAS5086 can also accept a 48 Fs SCLK rate for MCLK ratios of 192 Fs and 384 Fs.

The TAS5086 is composed of five functional blocks.

1. Power Supply
2. Clock, PLL, and Serial Data Interface
3. Serial Control Interface
4. Device Control
5. PWM Section

Figure 1 shows the functional structure of the TAS5086.

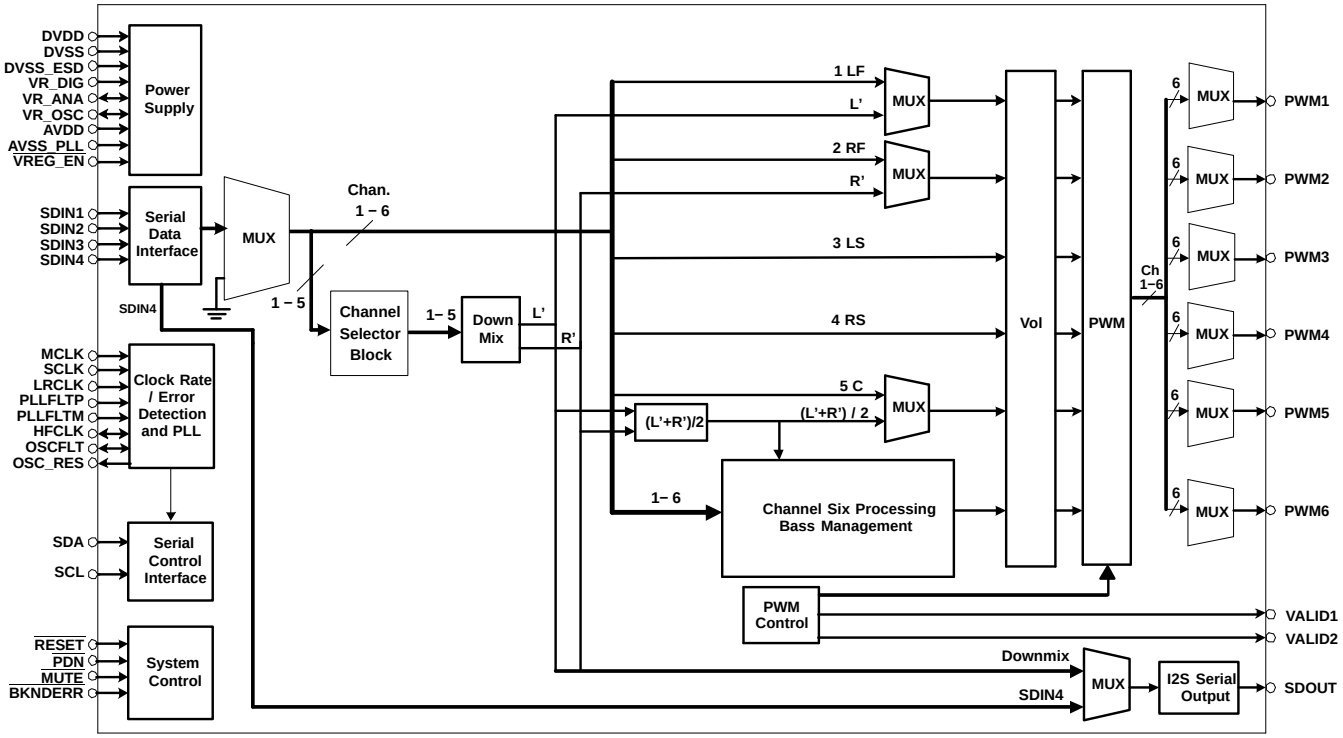


Figure 1. TAS5086 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage	DVDD and DVD_ESD	–0.3 V to 3.6 V
	AVDD	–0.3 V to 3.6 V
Input voltage	3.3-V digital input	–0.5 V to DVDD + 0.5 V
	5 V tolerant(2) digital input	–0.5 V to to 6 V
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V		±20 mA
Operating free-air temperature		0°C to 70°C
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under “absolute ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operation conditions” are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDA, and SCL.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBT	817.16 W	10.214 mW/C	357.5 mW	204.29 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Digital supply voltage	DVDD	3	3.3	3.6	V
	Analog supply voltage	AVDD	3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3-V TTL, 5-V tolerant	2			V
V_{IL}	Low-level input voltage	3.3-V TTL, 5-V tolerant			0.8	V
T_A	Operating ambient air temperature range		0	25	70	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

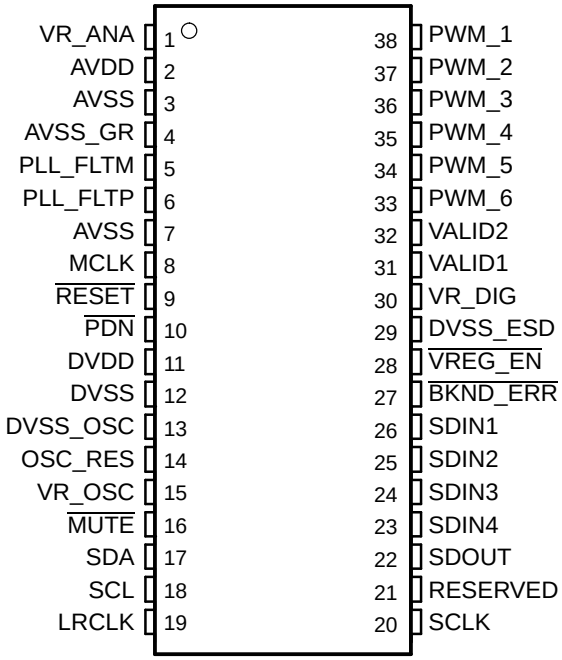
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V(1) tolerant	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	3.3-V TTL and 5 V(1) tolerant	I_{OL} = 4 mA			0.5	V
I_{OZ}	High-impedance output current	3.3-V TTL				±20	µA
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±1	µA
		5 V tolerant	V_I = 0 V, DVDD = 3 V			±1	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±1	µA
		5 V tolerant	V_I = 5.5 V, DVDD = 3 V			±20	
I_{DD}	Input supply current	Digital supply voltage, DVDD	Fs = 48 kHz		140		mA
			Fs = 96 kHz		150		
			Fs = 192 kHz		155		
			Power down		8		
		Analog supply voltage, AVDD	Normal		20		mA
			Power down		2		

(1) 5-V tolerant outputs are SCL and SDA

PHYSICAL CHARACTERISTICS

DBT PACKAGE

(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O(1)	5 V TOLERANT	TERMINATION(2)	DESCRIPTION
NO.	NAME				
1	VR_ANA	P			Voltage reference for analog supply 1.8 V. A pin-out of the internally regulated 1.8-V power. A 0.1-µF low ESR capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
2	AVDD	P			3.3-V analog power supply
3	AVSS	P			Analog supply ground
4	AVSS_GR	P			Connection to guard ring
5	PLL_FLTM	AO			PLL negative input
6	PLL_FLTP	AI			PLL positive input
7	AVSS	P			Analog supply ground
8	MCLK	DI	5V	Pulldown	MCLK is a 3.3-V clock master clock input. The input frequency of this clock can range from 4 MHz to 50 MHz.
9	$\overline{\text{RESET}}$	DI	5V	Pullup	A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5086 to its default conditions, sets the VALID2 output low, and places the PWM in the hard mute (M) state. Master Volume is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4-5 ms. device initialization and set the volume at mute.

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

(2) All pullups are 20-µA *weak* pull-ups and all pulldowns are 20-µA *weak* pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups => logic 1 input; pulldowns => logic 0 input). Devices that drive inputs with pullups must be able to sink 20 µA, while maintaining a logic '0' drive level. Devices that drive inputs with pulldowns must be able to source 20 µA, while maintaining a logic 1 drive level.

PHYSICAL CHARACTERISTICS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O(1)	5 V TOLERANT	TERMINATION(2)	DESCRIPTION
NO.	NAME				
10	$\overline{\text{PDN}}$	DI	5V	Pullup	Power down, active low. PDN powers down all logic and stops all clocks and performs a soft stop whenever a logic low is applied. The internal parameters are preserved through a power down cycle, as long as a RESET is not active. The duration for system recovery from power down is 100 ms. When released the PDN powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration.
11	DVDD	P			3.3-V digital power supply
12	DVSS	P			Digital ground
13	DVSS_OSC	P			Digital ground for oscillator
14	OSC_RES 1	AO			Oscillator trim resistor
15	VR_OSC	P			Voltage reference for analog supply 1.8 V. A pin-out of the internally regulated 1.8-V power. A 0.1-µF low ESR(3) capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
16	/MUTE	DI	5V	Pullup	Performs a soft mute of outputs, active low (muted signal = a logic low, normal operation = a logic high) The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
17	SDA	DIO	5V		I^2C serial control data interface input/output
18	SCL	DI	5V		I^2C serial control clock iInput output
19	LRCLK	DI	5V	Pulldown	Input serial audio data left/right clock (sampling rate clock)
20	SCLK	DIO	5V	Pulldown	Serial audio data clock (shift clock) SCLKIN is the serial audio port (SAP) input data bit clock that is supplied to the serial bit clock to other I2S bus.
21	RESERVED				RESERVED
22	SDOUT	DI			Serial audio data 1 output is the only serial data output port. SDOUT supports I2S format only. SDOUT pin is used as input pin for selecting OSC bypass mode.
23	SDIN4	DI		Pulldown	Serial audio data 4 input is one of the serial data input ports. SDIN4 supports four discrete (stereo) data formats
24	SDIN3	DI		Pulldown	Serial audio data 3 input is one of the serial data input ports. SDIN3 supports four discrete (stereo) data formats.
25	SDIN2	DI		Pulldown	Serial audio data 2 input is one of the serial data input ports. SDIN2 supports four discrete (stereo) data formats.
26	SDIN1	DI		Pulldown	Serial audio data 1 input is one of the serial data input ports. SDIN1 supports four discrete (stereo) data formats.
27	$\overline{\text{BKND\_ERR}}$	DI		Pullup	Active low. A backend error sequence is generated by applying logic LOW to this terminal. The $\overline{\text{BKND\_ERR}}$ results in all system parameters unaffected while VALID2 goes low.
28	$\overline{\text{VREG\_EN}}$	P			Voltage regulator enable. When enabled – low this input causes the power supply regulators to be enabled.
29	DVSS_ESD	P			ESD pin for digital supply
30	VR_DIG	P			Voltage reference for digital PWM core supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by digital PWM core logic. A 0.1-µF low ESR(4) capacitor should be connected between this terminal and DVSS_PWM. This terminal must not be used to power external devices
31	VALID2	DIO			Output indicating validity of PWM outputs - active high.
32	VALID1	DO			Soft start valid - Output indicating validity of soft start PWM output - active high.

(3) If desired, low ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provide an extended high frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.

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PHYSICAL CHARACTERISTICS (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O[1]	5 V TOLERANT	TERMINATION[2]	DESCRIPTION
NO.	NAME				
33	PWM_ 6	DO			PWM 6 Output
34	PWM_ 5	DO			PWM 5 Output
35	PWM_ 4	DO			PWM 4 Output
36	PWM_ 3	DO			PWM 3 Output
37	PWM_ 2	DO			PWM 2 Output
38	PWM_ 1	DO			PWM 1 Output

DETAILED DESCRIPTION

POWER SUPPLY

The TAS5086 power supply section contains regulators that provide analog and digital regulated power for various sections of the TAS5086. The analog supply supports the analog PLL while digital supplies support the digital PLL, the digital audio processor, the pulse width modulator, and the output control (reclocker). The power supply section is enabled via /VREG_EN.

CLOCK, ERROR RATE DETECTION, AND PLL

This module provides the timing and serial data interface for the TAS5086.

The TAS5086 is a clock slave only device. It accepts MCLK, SCLK, and LRCLK.

The TAS5086 supports 64 Fs MCLK for the 176.4-kHz and 192-kHz data rates.

The TAS5086 accepts a 64 Fs SCLK rate for all MCLK ratios and a 48 Fs SCLK rate for MCLK ratios of 192 Fs and 384 Fs.

TAS5086 checks to verify that the SCLK is a specific value of 64 Fs or 48 Fs.

The TAS5086 supports a 1 × Fs LRCLK

The timing relationship of these clocks to SDIN1-4 and SDOUT are shown in subsequent sections.

The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to derive all internal to produce a 196-MHz PLL output.

The TAS5086 can auto-detect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz and 192 kHz). The automatic sample rate detection can be disabled and the values set via I^2C.

The TAS5086 also supports a AM interference avoidance mode during which the clock rate is adjusted, in concert with the PWM sample rate converter to produce an PWM output at 7×Fs, 8×Fs, or 9×Fs.

The sample rate must be set manually set during AM interference avoidance and when de-emphasis is enabled.

The TAS5086 uses an internal oscillator time base to provide reference timing information for the following:

MCLK, SCLK and LRCLK error detection

Permit I^2C communication when power is first applied to the device

Automatic data rate detection and setting (32 kHz, normal, double, and quad speed)

Automatic MCLK rate detection and setting (64, 128, 192, 256, 384, and 512 Fs)

SERIAL DATA INTERFACE

Serial data is input on SDIN1, SDIN2, SDIN3, and SDIN4. The PWM outputs and down mix are derived from SDIN1, SDIN2, and SDIN3. SDIN4 is a selectable pass-through signal that is available at SDOUT as an I^2S output. The TAS5086 accepts 32, 44.1, 48, 88.2, 96, 176.4, and 192-kHz serial data in 16-, 20-, or 24-bit data in left, right, and I^2S serial data formats.

Serial Data is output on SDOUT. The SDOUT data format is I^2S 24 bit at the same data rate as the input. The SDOUT output is synchronized to use the SCLK and LRCLK signals. There is a 1 to 2.5 LRCLK frame delay from the input data to the output data depending upon the input serial data format. The SDOUT output has no I^2C controllable functions. It is always operational.

The parameters of this clock and serial data interface input format are I^2C configurable.

I^2C SERIAL CONTROL INTERFACE

The TAS5086 has an I^2C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal speed (100 kHz) and high speed (400 kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

The serial control interface supports both single byte and multi-byte read and write operations for status registers and the general control registers associated with the PWM.

DETAILED DESCRIPTION (continued)

The I^2C interface supports a special mode which permits I^2C write operations to be broken up into multiple data write operations that are multiples of 4 data bytes These are 6, 10, 14, 18 ... etc., byte write operations that are composed of a device address, read/write bit, and subaddress and any multiple of 4 bytes of data. This permits the system to incrementally the write large register values without blocking other I^2C transactions.

Figure 2 shows the data flow and control through the TAS5086. The major I^2C registers are shown above each applicable block (e.g., 0×04 is the Serial Data Format Control register).

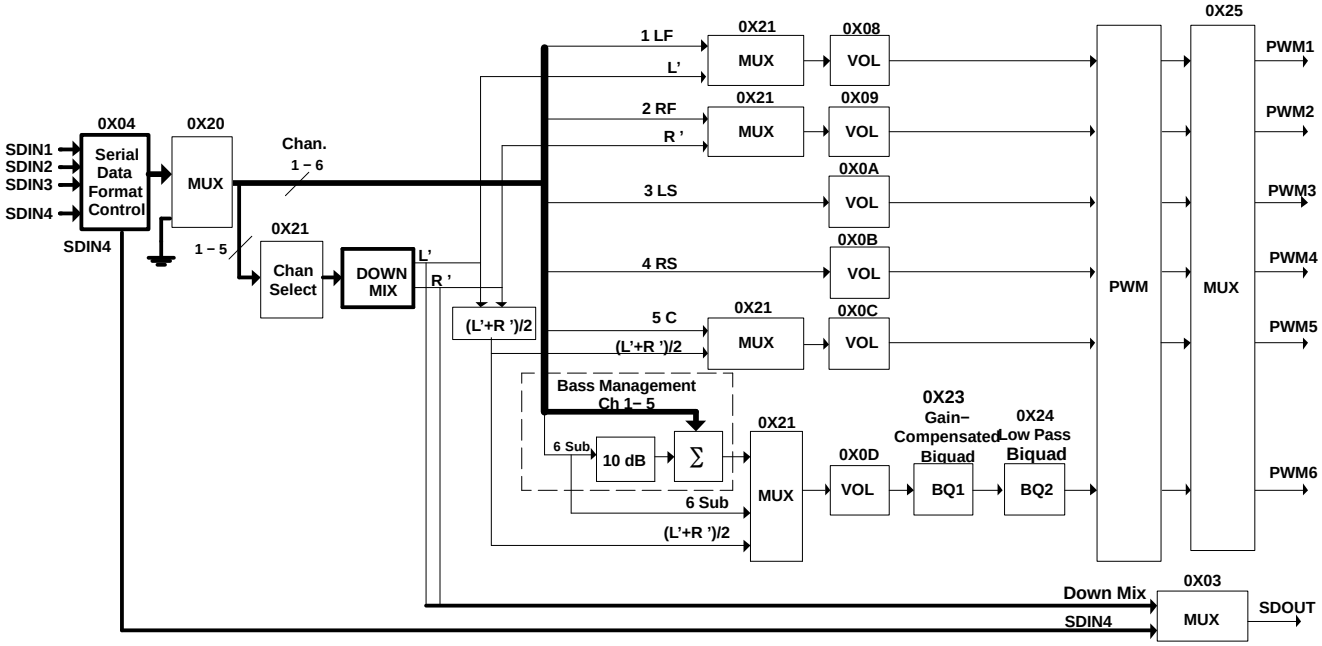


Figure 2. TAS5086 Data Flow Diagram With I^2C Registers

Channel 6 Processing Section

Channel 6 has processing features that are directly applicable to the subwoofer channel.

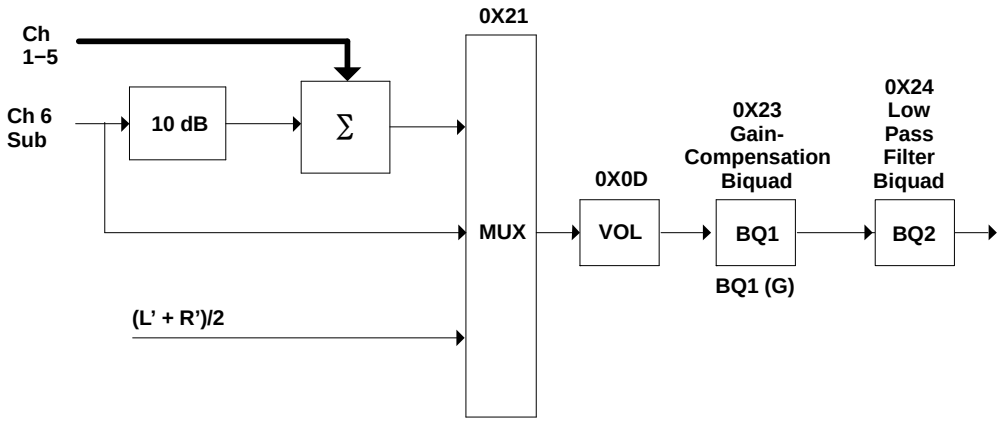


Figure 3. Channel 6 Processing Block Diagram

DETAILED DESCRIPTION (continued)

PWM Section

The TAS5086 has six channels of high performance digital PWM Modulators that are designed to drive switching output stages (back-ends) in both single-ended (SE) and H-bridge (bridge tied load) configuration. The TAS5086 device uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The TAS5086 uses a 4^{th} order noise shaper to provide >105-dB SNR performance from 20 Hz to 20 kHz.

The TAS5086 PWM interface is described by using the following notation:

PN + V

Where,

P = number of PWM signals per channel

N = number of channels

V = total number of valid signals used to reset the power stage

For example, the TAS5086 initial interface format means that there is 1 PWM signal per channel (N = 6) and 1 valid signal is used to reset the power stages.

The PWM section accepts 24-bit PCM data from the serial data interface and outputs six PWM audio output channels to drive power 1N+1 compatible single-ended and BTL power stages.

The PWM interface supports:

- TAS5186 in BTL or SE mode without any external glue logic, uses 1N+1 signaling.
- TAS5142 in BTL or SE mode without any external glue logic, uses 1N+1 signaling.
- TAS5111 SE without any external glue logic with a pulldown on the output, uses 1N+1 signaling.
- TAS5111 BTL or TAS5112 BTL with one inverter per BTL channel of glue logic and a pulldown on the output, uses 1N+1 signaling from TAS5086, 2N+1 input to TAS5111/12.
- TAS5112 SE (with external glue logic)

See the application schematics for an example of the TAS5086 with the TAS5186 and the TAS5086 with TAS5112 SE and TAS5111 SE.

The TAS5086 has input multiplexers that allow any of the input channels to be routed to any PWM channel and output multiplexers to enable any PWM output to be routed to any PWM output pin.

It also has individual channel dc-blocking filters that are enabled by default.

Individual channel de-emphasis filters for 32, 44.1, and 48 kHz are included and can be enabled and disabled.

There is also a two channel down mix result that can be output on SDOUT (I2S format). This result can also be sent to the left and right front channels (channels 1 and 2) and/or to the center and subwoofer (channels 5 and 6) as well.

A mixer on the subwoofer channel supports bass management configuration 1.

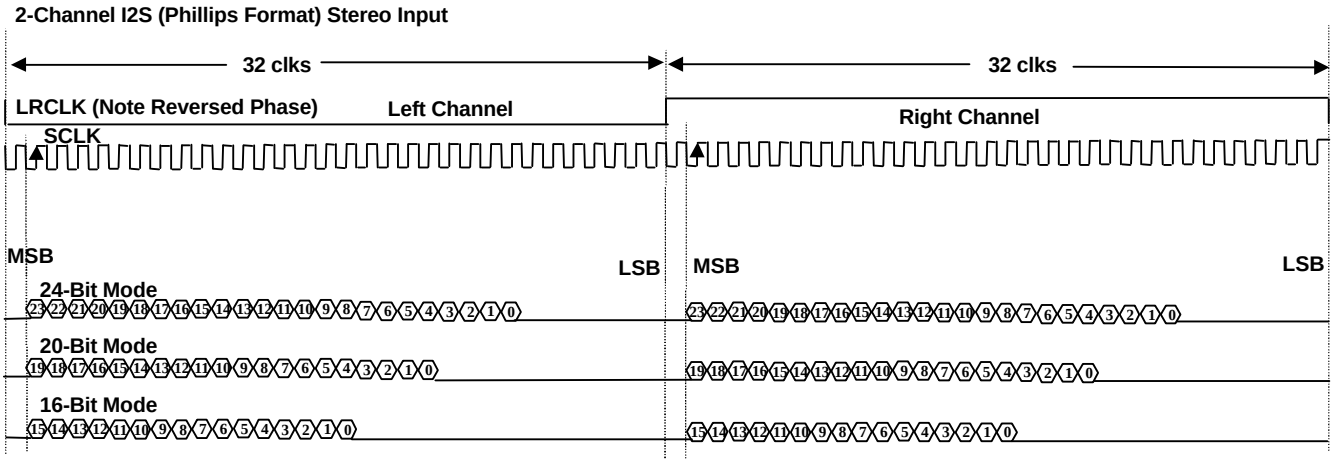
PWM output characteristics

1. Up to 8x over sampling
2. 12x at Fs = 32 kHz, 8x at Fs = 48 kHz, 4x at Fs = 96 kHz, 2x at Fs = 192 kHz
3. 4th order noise shaping
4. ≥105-dB dynamic range 0–20 kHz (TAS5086 + TAS5186 system measured at speaker terminals)
5. THD < 0.06% (measured at TAS5086 outputs)
6. Adjustable maximum modulation limit of 93.8% to 99.2%

SERIAL INTERFACE CONTROL AND TIMING

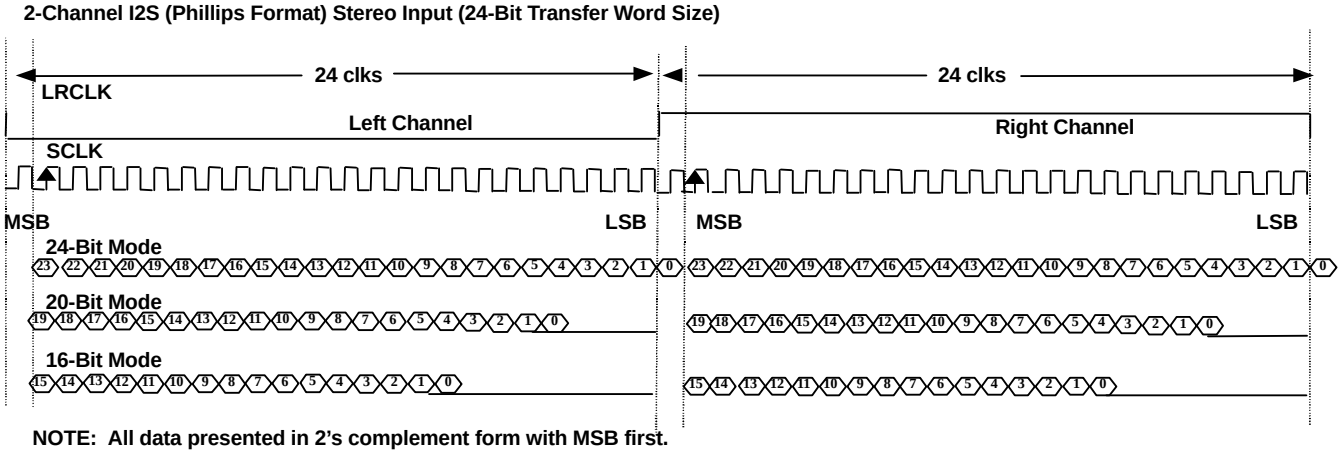
I²S TIMING

I²S timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is low for the left channel and high for the right channel. A bit clock running at 64 × Fs is used to clock in the data. There is a delay of one bit clock from the time the L/RCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5086 masks unused trailing data bit positions.



NOTE: All data presented in 2's complement form with MSB first.

Figure 4. I²S Format 64 Fs Format



NOTE: All data presented in 2's complement form with MSB first.

Figure 5. I²S 48 Fs Format

LEFT JUSTIFIED

Left justified (LJ) timing uses an L*R*CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L*R*CLK is high for the left channel and low for the right channel. A bit clock running at 64 × Fs is used to clock in the data. The first bit of data appears on the data lines at the same time the L/*R*CLK toggles. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5086 masks unused trailing data bit positions.

SERIAL INTERFACE CONTROL AND TIMING (continued)

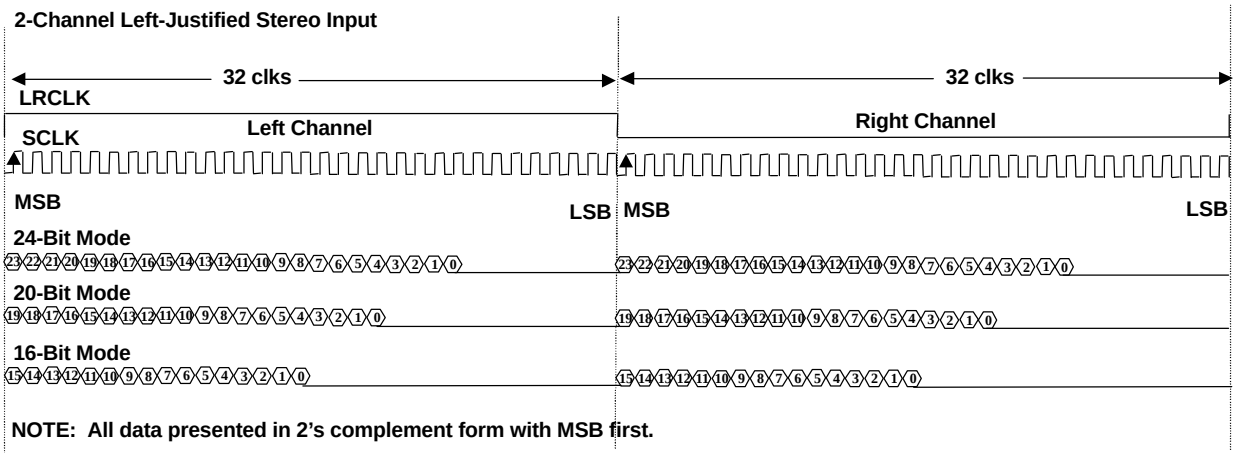


Figure 6. Left Justified 64 Fs Format

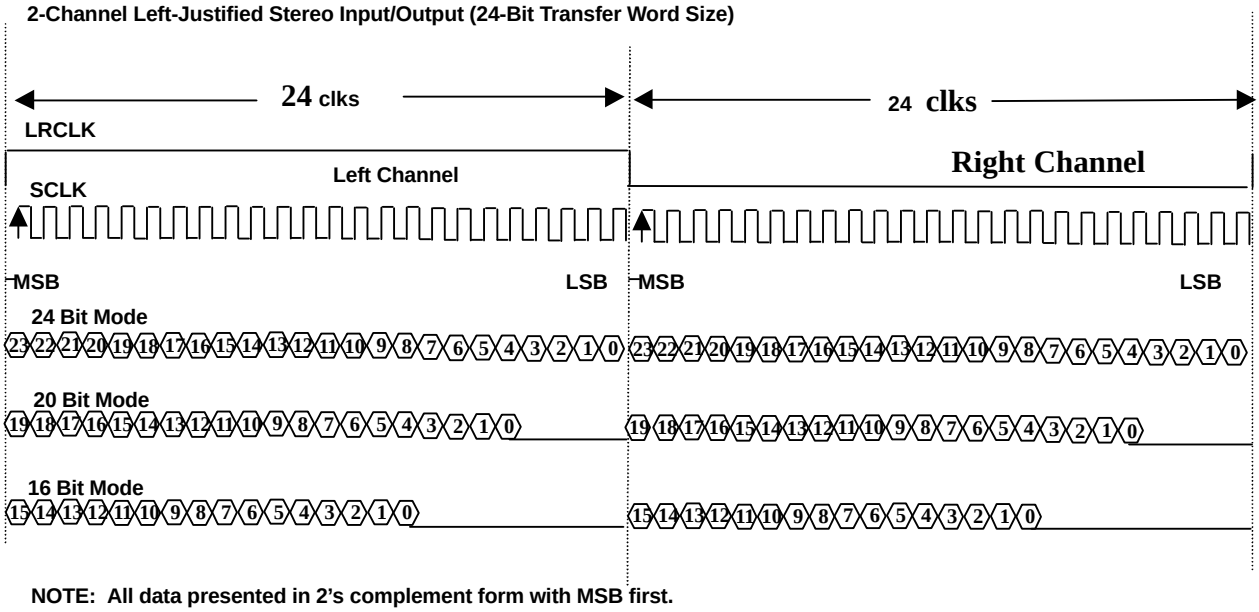


Figure 7. Left Justified 48 Fs Format

Right Justified

Right justified (RJ) timing uses an L*R*CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L*R*CLK is high for the left channel and low for the right channel. A bit clock running at 64 × Fs is used to clock in the data. The first bit of data appears on the data 8-bit clock periods (for 24-bit data) after L/*R*CLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before L/*R*CLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5086 masks unused leading data bit positions.

SERIAL INTERFACE CONTROL AND TIMING (continued)

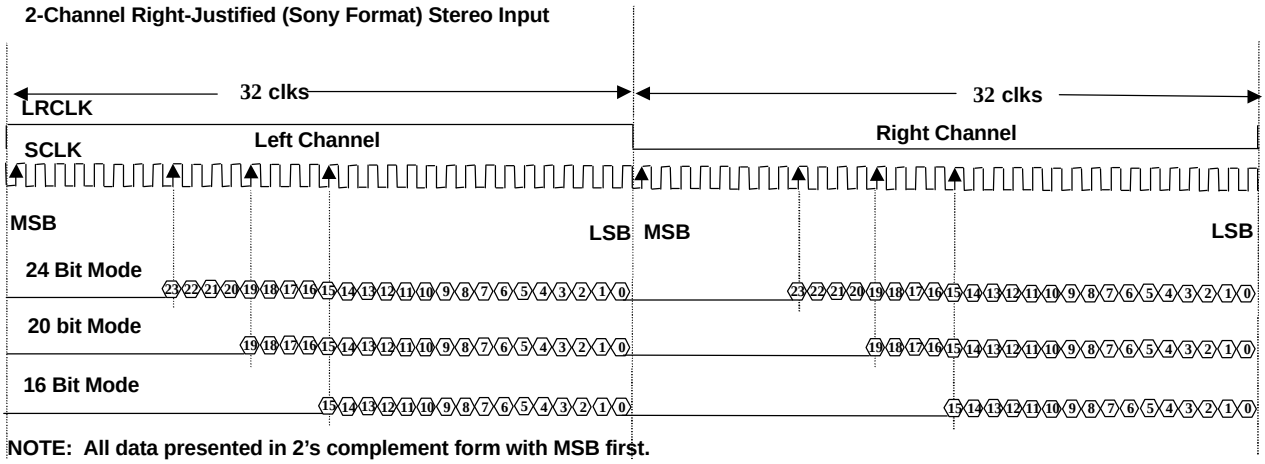


Figure 8. Right Justified 64 Fs Format

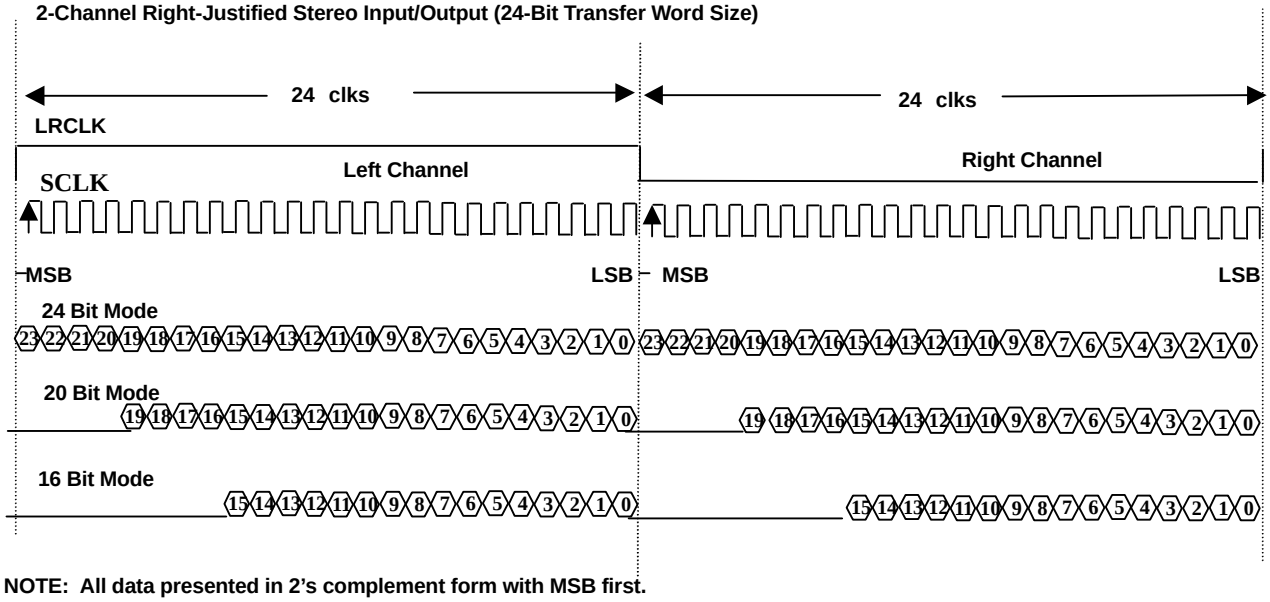


Figure 9. Right Justified 48 Fs Bit Format

I²C SERIAL CONTROL INTERFACE

The TAS5086 has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports both 100 KBPS and 400 KBPS data transfer rates for single and multiple byte write and read operations. The control interface is used to program the registers of the device and to read device status.

The TAS5086 supports wait state insertions by other I²C devices on the bus. However, the TAS5086 perform all I²C operations without I²C wait cycles.

The TAS5086 supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum).

I²C SERIAL CONTROL INTERFACE (continued)

GENERAL I²C OPERATION

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data be transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 10. The master generate the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TAS5086 holds SDA low during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus.

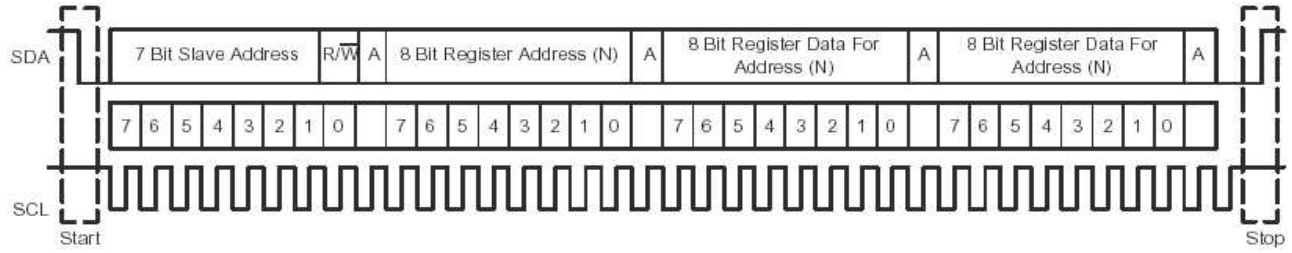


Figure 10. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 10.

The 7-bit address for the TAS5086 is 0011011.

SINGLE AND MULTIPLE BYTE TRANSFERS

The serial control interface supports both single byte and multi-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface supports only multiple byte (4 byte) read/write operations.

During multiple byte read operations, the TAS5086 responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple byte write operations, the TAS5086 compares the number of bytes transmitted to the number of bytes that are required for each specific sub address. If a write command is received for a biquad subaddress, the TAS5086 expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the TAS5086 expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5086 also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the fifteen subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5086. For I²C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

I²C SERIAL CONTROL INTERFACE (continued)

SINGLE BYTE WRITE

As shown is Figure 11, a single byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to a 0. After receiving the correct I²C device address and the read/write bit, the TAS5086 device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5086 internal memory address being accessed. After receiving the address byte, the TAS5086 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5086 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single byte data write transfer.

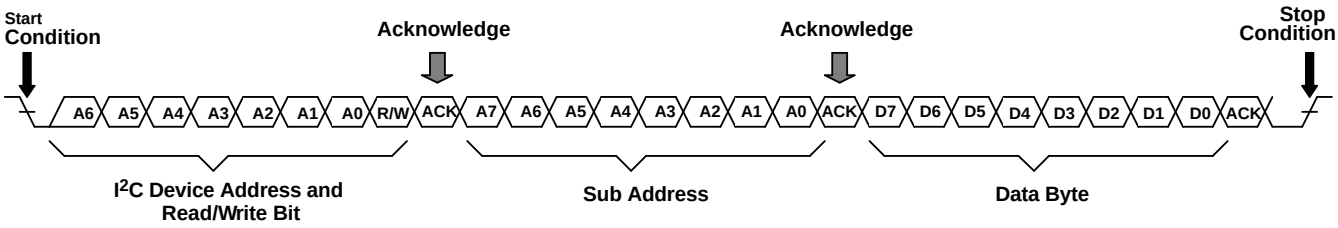


Figure 11. Single Byte Write Transfer

MULTIPLE BYTE WRITE AND INCREMENTAL MULTIPLE BYTE WRITE

A multiple byte data write transfer is identical to a single byte data write transfer except that multiple data bytes are transmitted by the master device to TAS5086 as shown in Figure 12. After receiving each data byte, the TAS5086 responds with an acknowledge bit.

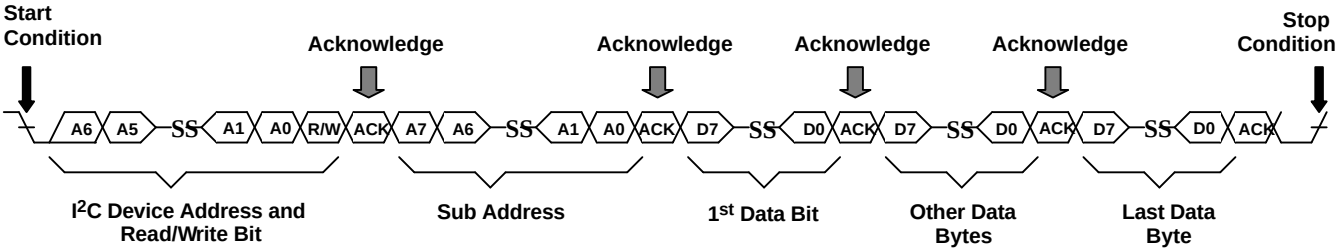


Figure 12. Multiple Byte Write Transfer

The I²C supports a special mode which permits I²C write operations to be broken up into multiple data write operations that are multiples of 4 data bytes These are 6, 10, 12, 16 ... etc., byte write operations that are composed of a device address, read/write bit, and subaddress and any multiple of 4 bytes of data. This permits the system to incrementally the write large register values without blocking other I²C transactions.

This feature is enabled by the a*ppend* subaddress (0xFE) in the TAS5086. The append address, 0×FE, enables the TAS5086 to append an integer number of 4, 8, 12, 16… byte blocks of data to a register that was opened by a previous I²C register write operation but has not received it's complete number of data bytes.

When the correct number of bytes has been received, the TAS5086 starts processing the data.

The procedure to perform a multi-byte write operation is as follows.

1. Start a normal I²C write operation by sending the device address, write bit, and register subaddress and an integer number of four byte data blocks. At the end of that sequence send a stop condition.

   At this point the register has been opened and accepts the remaining data is sent by writing one or more write operation of an integer number of 4 byte blocks of data to the append subaddress (0×FE).

I²C SERIAL CONTROL INTERFACE (continued)

2. At a later time one or more append data transfers are performed to incrementally transfer the remaining number of bytes in sequential order to complete the register write operation. Each of these append operations is composed of the device address, write bit, append subaddress (0×FE), an integer number of four bytes of data followed by a stop condition.
3. The operation is terminated due to an error condition and the data is flushed - IF
   – If a new subaddress is written to the TAS5086 before the correct number of bytes has been written.
   – If a noninteger number of 4 bytes are written at the beginning or during any of the append operations.
   – If a read bit is sent.

SINGLE BYTE READ

As shown in Figure 13, a single byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is set to a 0. After receiving the TAS5086 address and the read/write bit, the TAS5086 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5086 address and the read/write bit again. This time the read/write bit is set to a 1 indicating a read transfer. After receiving the TAS5086 and the read/write bit the TAS5086 again responds with an acknowledge bit. Next, the TAS5086 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single byte data read transfer.

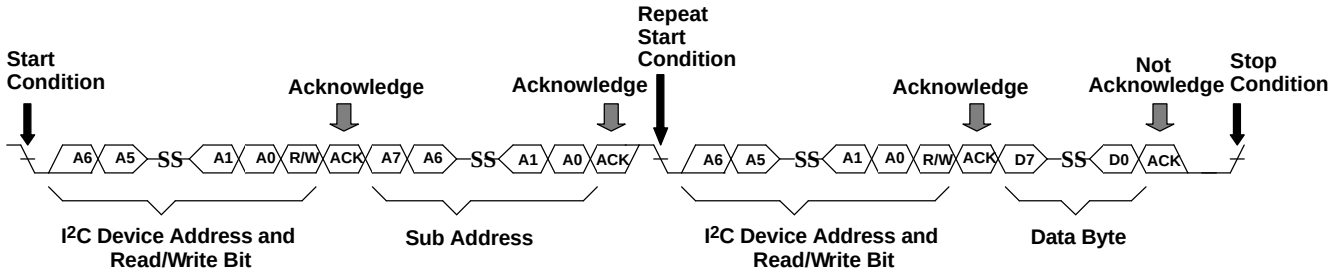


Figure 13. Single Byte Read Transfer

MULTIPLE BYTE READ

A multiple byte data read transfer is identical to a single byte data read transfer except that multiple data bytes are transmitted by the TAS5086 to the master device as shown in Figure 14. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

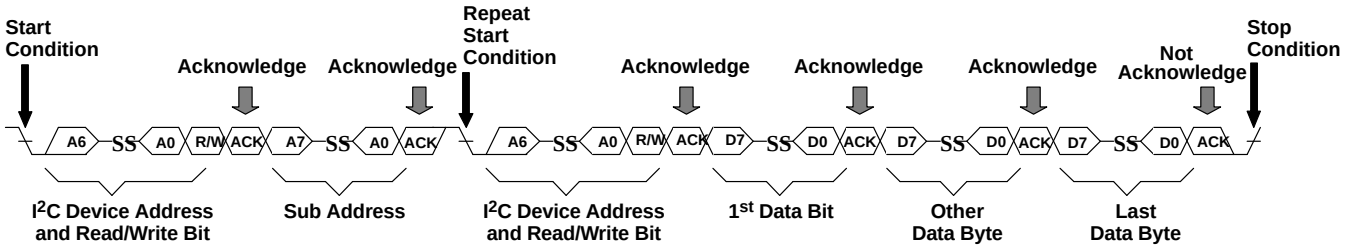


Figure 14. Multiple Byte Read Transfe

COMMAND CHARACTERISTICS

I²C SERIAL CONTROL INTERFACE (continued)

The TAS5086 has two groups of I²C commands. One set is designed to be commands that are designed specifically to be operated while audio is streaming that has built in mechanisms to prevent noise, clicks, and pops. The other set does not have this built in protection.

Commands that are designed to be adjusted while audio is streaming

- Master Volume
- Master Mute
- Individual Channel Volume
- Individual Channel Mute

Command that the system executes without additional processing to prevent noise, clicks, or pops (in a number of cases this does not produce an audible click and pop)

- Serial Data Interface Format
- De-emphasis
- Sample Rate Conversion
- Input Multiplexer
- Output Multiplexer
- Biquads
- Down Mix
- Channel Delay
- Enable/Disable Automatic MCLK and Data Rate Frequency Detection
- Manual or Automatic MCLK and Data Rate Setting
- Enable/Disable DC Blocking
- Hard/Soft Unmute from Clock Error

SERIAL CONTROL INTERFACE REGISTER SUMMARY

SUB-ADDRESS (0xSS)	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
			A u indicates unused bits	
0x00	Clock Control Register	1	Description shown in subsequent section	6C
0x01	Device ID Register	1	Description shown in subsequent section	03
0x02	Error Status Register	1	Description shown in subsequent section	00
0x03	System Control Register 1	1	Description shown in subsequent section	A0
0x04	Serial Data Interface Register	1	Description shown in subsequent section	05
0x05	System Control Register 2	1	Description shown in subsequent section	60
0x06	Softmute Register	1	Description shown in subsequent section	00
0x07	Master Volume	1	Description shown in subsequent section	FF (Mute)
0x08	Channel 1 Vol	1	Description shown in subsequent section	30 (0 dB)
0x09	Channel 2 Vol	1	Description shown in subsequent section	30 (0 dB)
0x0A	Channel 3 Vol	1	Description shown in subsequent section	30 (0 dB)
0x0B	Channel 4 Vol	1	Description shown in subsequent section	30 (0 dB)
0x0C	Channel 5 Vol	1	Description shown in subsequent section	30 (0 dB)
0x0D	Channel 6 Vol	1	Description shown in subsequent section	30 (0 dB)
0x0E	Volume Control Register	1	Description shown in subsequent section	B1
0x0F			RESERVED(1)	
0x10	Modulation Limit Register	1	Description shown in subsequent section	02
0x11–0x17			RESERVED(1)	
0x18	PWM Start Register	1	Description shown in subsequent section	3F

(1) Reserved registers should not be accessed.

SERIAL CONTROL INTERFACE REGISTER SUMMARY (continued)

SUB-ADDRESS (0xSS)	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x19	Surround Register	1	Description shown in subsequent section	00
0x1A	Split Cap Charge Period Register	1	Description shown in subsequent section	18
0x1B	OSC_TRIM	1	Oscillator Trim Register	82
0X1C	BKNDERR Register	1	BKNDErr Register	05
0x1D–0x1F			RESERVED(1)	
0x20	Input MUX Register	4	Description shown in subsequent section	0x00 0x01 0x23 0x45
0x21	Downmix Input MUX Register	4	Description shown in subsequent section	0x00 0x00 0x00 0x3F
0x22	Am Tuned Frequency	4	Description shown in subsequent section	0x00 0x00 0x00 0x00
0X23	ch6_bq[1]	20	b0 (25:24) b0(23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00,0x00
			b1 (25:24) b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00,0x00
			b2 (25:24) b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00,0x00
			a1 (25:24) a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00,0x00
			A2 (25:24) a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00,0x00
0X24	ch6_bq[2]	20	b0 (25:24) b0(23:16), b0(15:8), b0(7:0)	0x00, 0x80, 0x00,0x00
			b1 (25:24) b1(23:16), b1(15:8), b1(7:0)	0x00, 0x00, 0x00,0x00
			b2 (25:24) b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00,0x00
			a1 (25:24) a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00,0x00
			A2 (25:24) a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00,0x00
0x25	PWM Mux Register		Shown in Subsection section	0x00, 0x32, 0x45, 0x10,
0x26	1/G Register	4	x (25:24) x(23:16), x(15:8), x(7:0)	0x00, 0x80, 0x00,0x00
0x27			RESERVED(2)	
0x28	Scale Register	4	x (25:24) x(23:16), x(15:8), x(7:0)	0x00, 0x80, 0x00,0x00
0x29–0xFD			RESERVED(2)	
0XFE	Repeat Subaddress	4+4N		0x00,0x00,0x00,0x00
0xFF			RESERVED(2)	

(2) Reserved registers should not be accessed.

CLOCK CONTROL REGISTER (0x00)

In the manual mode, the clock control register provides a way for the system micro to update the data and clock rates based on the sample rate and associated clock frequencies. In the auto detect mode, the clocks are automatically determined by the TAS5086. In this case, the clock control register contains the auto-detected clock status as automatically detected. Bits D7–D5 selects the sample rate. Bits D4–D2 selects the MCLK frequency. Bit D1 selects the bit clock (SCLK) frequency. Bit D0 is used in manual mode only. In this mode, when the clocks are updated a 1 must be written to D1 to inform the TAS5086 that the written clocks are valid.

Table 1. Clock Control Register(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	Fs = 32-kHz sample rate
0	0	1	–	–	–	–	–	Fs = 38-kHz sample rate
0	1	0	–	–	–	–	–	Fs = 44.1-kHz sample rate
0	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**Fs = 48-kHz sample rate**
1	0	0	–	–	–	–	–	Fs = 88.2- kHz sample rate
1	0	1	–	–	–	–	–	Fs = 96-kHz sample rate
1	1	0	–	–	–	–	–	Fs = 176.4-kHz sample rate
1	1	1	–	–	–	–	–	Fs = 192-kHz sample rate

(1) Default values are in **bold**

Table 1. Clock Control Register (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	0	0	0	–	–	MCLK frequency = 64 x Fs(2)
–	–	–	0	0	1	–	–	MCLK frequency = 128 x Fs
–	–	–	0	1	0	–	–	MCLK frequency = 192 x Fs
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 x Fs**
–	–	–	1	0	0	–	–	MCLK frequency = 384 x Fs
–	–	–	1	0	1	–	–	MCLK frequency = 512 x Fs
–	–	–	1	1	0	–	–	Reserved
–	–	–	1	1	1	–	–	Reserved
–	–	–	–	–	–	1	–	Bit clock (SCLK) frequency = 48 x Fs
–	**–**	**–**	**–**	**–**	**–**	**0**	**–**	**Bit clock (SCLK) frequency = 64 x Fs**
–	**–**	**–**	**–**	**–**	**–**	**–**	**0**	**Clock not valid (in manual mode only)**
–	–	–	–	–	–	–	1	Clock valid iIn manual mode only)

(2) Rate not available for 32-, 44.1-, 48-, 88.2-, and 96-kHz data rates

DEVICE ID REGISTER (0X01)

The device ID register contains the ID code for the TAS5086.

Table 2. General Status Register (x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								Default
–	**0**	**0**	**0**	**0**	**0**	**1**	**1**	Identification code for the TAS5086

ERROR STATUS REGISTER (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if there are any persistent errors.

Table 3. ErrorStatus Register (x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	1	–	–	–	–	–	–	PLL auto lock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
–	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors**

SYSTEM CONTROL REGISTER 1 (0X03)

System Control Register 1 has several functions:

Bit D7: If 0 the dc-blocking filter for each channel is disabled

If 1 the dc-blocking filter (-3 dB cutoff < 1 Hz) for each channel is enabled (default)

Bit D6: Not used

Bit D5: If 0 use soft unmute on recovery from clock error. This is a slow recovery.

If 1 use hard unmute on recovery from clock error (default). This is a fast recovery.

Bit D4: If 0 the down mix is output on SDOUT as I2S signal (default)

If 1 SDIN4 is output on SDOUT as I2S signal

Bit D3: If 0 Clock Auto Detect is enabled (default)

If 1 Clock Auto Detect is disabled

Bit D2: If 0 Soft Start is enabled (default)

If 1 Soft start is disabled

Bit D1-D2: Select de-emphasis

Table 4. System Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM High Pass (DC Blocking) Disabled
1	**–**	**–**	**–**	**–**	**–**	**–**	**–**	**PWM High Pass (DC Blocking) Enabled**
–	–	0	–	–	–	–	–	Soft Unmute on Recovery from Clock Error
–	**–**	**1**	**–**	**–**	**–**	**–**	**–**	**Hard Unmute on Recovery from Clock Error**
–	**–**	**–**	**0**	**–**	**–**	**–**	**–**	**Output Down mix on SDOUT**
–	–	–	1	–	–	–	–	Output SDIN4 mix on SDOUT
–	**–**	**–**	**–**	**0**	**–**	**–**	**–**	**Enable Clock Auto Detect**
–	–	–	–	1	–	–	–	Disable Clock Autodetect
–	**–**	**–**	**–**	**–**	**0**	**–**	**–**	**Enable Soft Start**
–	–	–	–	–	1	–	–	Disable Soft Start
–	**–**	**–**	**–**	**–**	**–**	**0**	**0**	**NO De-emphasis**
–	–	–	–	–	–	0	1	De-emphasis for Fs = 32 kHz
–	–	–	–	–	–	1	0	De-emphasis for Fs = 44.1
–	–	–	–	–	–	1	1	kHz De-Emphasis for Fs = 48 kHz

SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 5, the TAS5086 supports nine serial data modes. The default is 24-bit, I2S mode.

Table 5. Serial Data Interface Control Register Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTHS	D7–D4	D3	D2	D1	D0
Right justified	16	0000	0	0	0	0
Right justified	20	0000	0	0	0	1
Right justified	24	0000	0	0	1	0
I2S	16	0000	0	0	1	1
I2S	20	0000	0	1	0	0
I2S	**24**	0000	**0**	**1**	**0**	**1**
Left justified	16	0000	0	1	1	0
Left justified	20	0000	0	1	1	1
Left justified	24	0000	1	0	0	0
Illegal		0000	1	0	0	1
Illegal		0000	1	0	1	0
Illegal		0000	1	0	1	1
Illegal		0000	1	1	0	0
Illegal		0000	1	1	0	1
Illegal		0000	1	1	1	0
Illegal		0000	1	1	1	1
Default values are in **bold**						

SYSTEM CONTROL REGISTER 2 (0x05)

Bit D6 is a **control** bit and bit D5 is a **configuration** bit.

When bit D6 is set low, the system starts playing, otherwise the outputs are shut down.

Bit D5 defines the configuration of the system, i.e. it determines what configuration the system will be running in when bit D6 is set low. When this bit is asserted the system is configured to surround meaning all channels are switching. Otherwise only a subset of the PWM's will be running corresponding to a 2.0 or 2.1 configuration as determined surround register (0x19).

Bit D5 should only be changed when bit D6 is set, meaning the it is only possible to switch configuration from surround to 2.1/2.0 by shutting down the system and then restarting it again in the new configuration.

Table 6. System Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	1	X	–	–	–	–	–	All Channels are shut down (hard mute)
–	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**All Channels are shut down (hard mute) VALID1 = 0 and VALID2 = 0**
–	0	1	–	–	–	–	–	When D6 is deasserted all channels are started. VALID1 = 1 and VALID2 = 1
–	0	0	–	–	–	–	–	When D6 is deasserted all channels not belonging to Shut Down Group 1 are started VALID1 = 0 and VALID2 = 1

SOFT MUTE REGISTER (0x06)

Table 7. Soft Mute Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	1	Soft Mute Channel 1
–	–	–	–	–	–	1	–	Soft Mute Channel 2
–	–	–	–	–	1	–	–	Soft Mute Channel 3
–	–	–	–	1	–	–	–	Soft Mute Channel 4
–	–	–	1	–	–	–	–	Soft Mute Channel 5
–	–	1	–	–	–	–	–	Soft Mute Channel 6
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Unmute All Channels**

VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D)

Master Volume – 0x07 (default is mute)
Channel 1 Volume – 0x08 (default is 0dB)
Channel 2 Volume – 0x09 (default is 0dB)
Channel 3 Volume – 0x0A (default is 0dB)
Channel 4 Volume – 0x0B (default is 0dB)
Channel 5 Volume – 0x0C (default is 0dB)
Channel 6 Volume – 0x0D (default is 0dB)

Table 8. Volume Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	+24 dB
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0 dB (Default for Individual Channel Volume)**
1	1	1	1	1	1	1	0	–103 dB
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**MUTE (Default for Master Volume)**

VOLUME CONTROL REGISTER (0x0E)

Bit D7: Reserved = 1

Bit D6: If 0 then Biquad 1 (BQ1) Volume Compensation part only is disabled (default)

If 1 then BQ1 Volume Compensation is enabled

Bit D5: If 0 Disable 38-kHz detection (38 kHz should be set manually by micro)

If 1 Enable 38-kHz detection

Bit D4: Reserved = 1

Bit D3: Not Used

Bit D2–D0: Volume slew rate

Table 9. Volume Control Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	Reserved (Must be 1)
–	**0**	**–**	**–**	**–**	**–**	**–**	**–**	**Disable Biquad Volume Compensation**
–	1	–	–	–	–	–	–	Enable Biquad Volume Compensation
–	–	1	–	–	–	–	–	Reserved = 1
–	**–**	**–**	**1**	**–**	**–**	**–**	**–**	**Reserved (Must be 1)**

MODULATION LIMIT REGISTER (0x10)

Set modulation limit. See the appropriate power stage data sheet for recommended modulation limits.

Table 10. Modulation Limit Unit

D7	D6	D5	D4	D3	D2	D1	D0	LIMIT [DCLKs]	MIN WIDTH [DCLKs]	MODULATION LIMIT
–	–	–	–	–	0	0	0	1	2	99.2%
–	–	–	–	–	0	0	1	2	4	98.4%
–	**–**	**–**	**–**	**–**	**0**	**1**	**0**	**3**	**6**	**97.7%**
–	–	–	–	–	0	1	1	4	8	96.9%
–	–	–	–	–	1	0	0	5	10	96.1%
–	–	–	–	–	1	0	1	6	12	95.3%
–	–	–	–	–	1	1	0	7	14	94.5%
–	–	–	–	–	1	1	1	8	16	93.8%

PWM START REGISTER (0X18)

Bit D7 and D6 should always be set to 0.

Bits D5-D0: Define which PWM's will be used for charging the split caps and which PWM's should stay low to for the output stages to be held in hi-Z under split capacitor charging.

For most systems this register is always 0X3F. The setting depends on how the back-end is connected.

Table 11. PWM Start Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	**–**	**–**	**–**	**–**	**–**	**Reserved = 0**
–	**0**	**–**	**–**	**–**	**–**	**–**	**–**	**Reserved = 0**
–	**–**	**1**	**–**	**–**	**–**	**–**	**–**	**Start channel 6 under part 1 of the start**
–	–	0	–	–	–	–	–	Start channel 6 under part 2 of the start

Table 11. PWM Start Register (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	**1**	–	–	–	–	**Start channel 5 under part 1 of the start**
–	–	–	0	–	–	–	–	Start channel 5 under part 2 of the start
–	–	–	–	**1**	–	–	–	**Start channel 4 under part 1 of the start**
–	–	–	–	0	–	–	–	Start channel 4 under part 2 of the start
–	–	–	–	–	**1**	–	–	**Start channel 3 under part 1 of the start**
–	–	–	–	–	0	–	–	Start channel 3 under part 2 of the start
–	–	–	–	–	–	**1**	–	**Start channel 2 under part 1 of the start**
–	–	–	–	–	–	0	–	Start channel 2 under part 2 of the start
–	–	–	–	–	–	–	**1**	**Start channel 1 under part 1 of the start**
–	–	–	–	–	–	–	0	Start channel 1 under part 2 of the start

SURROUND REGISTER (0x19)

Defines which channels should be running in the 2.0/2.1 mode.

The channels having their surround register set belongs to shut down group 1 are associated with Valid 1. Valid 1 is the signal we bring low to disable channels when the system is operating in for example stereo mode or 2.1 mode.

Example: If,

PWM_1 connects to Front Left
PWM_2 connects to Front Right
PWM_3 connects to Surround Left
PWM_4 connects to Surround Right
PWM_5 connects to Center
PWM_6 connects to Sub

And you have a 2.1 mode, then VALID1 connects to reset of Surround Left, Surround Right, and Center. VALID2 connects to reset of Front Left, Front Right, and Sub.

That means that Surround Register (0x19) is loaded with 0b00011100 = 0x1C.

Important Note: You must always change channel modes with all channels shutdown (Reg. 0x05 = 60).

Table 12. Surround Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	1	–	–	–	–	–	PWM_6 belongs to shut down group 1 (VALID1)
–	–	**0**	–	–	–	–	–	PWM_6 **belongs to shut down group 2 (VALID2)**
–	–	–	1	–	–	–	–	PWM_5 belongs to shut down group 1 (VALID1)
–	–	–	**0**	–	–	–	–	PWM_5 **belongs to shut down group 2 (VALID2)**
–	–	–	–	1	–	–	–	PWM_4 belongs to shut down group 1 (VALID1)
–	–	–	–	**0**	–	–	–	PWM_4 **belongs to shut down group 2 (VALID2)**
–	–	–	–	–	1	–	–	PWM_3 belongs to shut down group 1 (VALID1)
–	–	–	–	–	**0**	–	–	PWM_3 **belongs to shut down group 2 (VALID2)**
–	–	–	–	–	–	1	–	PWM_2 belongs to shut down group 1 (VALID1)
–	–	–	–	–	–	**0**	–	PWM_2 **belongs to shut down group 2 (VALID2)**
–	–	–	–	–	–	–	1	PWM_1 belongs to shut down group 1 (VALID1)
–	–	–	–	–	–	–	**0**	PWM_1 **belongs to shut down group 2 (VALID2)**

SPLIT CAPACITOR CHARGE PERIOD REGISTER (0x1A)

This register should contain the code that closely matches the external single-ended split capacitor charge period. The TAS5086 waits for this period of time before starting the PWM signals. This helps reduce pops and clicks. This is only used with the split-cap configuration.

Table 13. Split Capacitor Charge Period Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	0	0	–	–	–	No split capacitor charge period
–	–	–	0	1	0	0	0	13-ms split capacitor charge period
–	–	–	0	1	0	0	1	16.9-ms split capacitor charge period
–	–	–	0	1	0	1	0	23.4-ms split capacitor charge period
–	–	–	0	1	0	1	1	31.2-ms split capacitor charge period
–	–	–	0	1	1	0	0	41.6-ms split capacitor charge period
–	–	–	0	1	1	0	1	54.6-ms split capacitor charge period
–	–	–	0	1	1	1	0	72.8-ms split capacitor charge period
–	–	–	0	1	1	1	1	96.2-ms split capacitor charge period
–	–	–	1	0	0	0	0	130-ms split capacitor charge period
–	–	–	1	0	0	0	1	156-ms split capacitor charge period
–	–	–	1	0	0	1	0	234-ms split capacitor charge period
–	–	–	1	0	0	1	1	312-ms split capacitor charge period
–	–	–	1	0	1	0	0	416-ms split capacitor charge period
–	–	–	1	0	1	0	1	546-ms split capacitor charge period
–	–	–	1	0	1	1	0	728-ms split capacitor charge period
–	–	–	1	0	1	1	1	962-ms split capacitor charge period
–	**–**	**–**	**1**	**1**	**0**	**0**	**0**	**1300-ms split capacitor charge period**
–	–	–	1	1	0	0	1	1690-ms split capacitor charge period
–	–	–	1	1	0	1	0	2340-ms split capacitor charge period
–	–	–	1	1	0	1	1	3120-ms split capacitor charge period
–	–	–	1	1	1	0	0	4160-ms split capacitor charge period
–	–	–	1	1	1	0	1	5460-ms split capacitor charge period
–	–	–	1	1	1	1	0	7280-ms split capacitor charge period
–	–	–	1	1	1	1	1	9620-ms split capacitor charge period

OSCILLATOR TRIM REGISTER (0x1B)

The TAS5086 PWM processor contains an internal oscillator for PLL reference. This reduces system cost since an external reference is not required. Currently, we recommend a trim resistor value of 18.2 kΩ (1%). This should be connected between TAS5086 pin 14 (OSC_RES) and pin 12 (DVSS).

There are two procedures available for trimming the internal oscillator. The Field Trim procedure #1 (recommended) requires that the LRCLK frequency be pre-determined whereas the Field Trim procedure #2 does not require that the LRCLK frequency is known.

Note that only one trim procedure should be used. It should always be run following RESET of the TAS5086.

Oscillator Field Trim Procedure #1 (Recommended if LRCLK Frequency is Known):

1. Reset the TAS5086 (power-up or toggle reset pin).
2. Provide a known LRCLK (e.g. 48 kHz)
3. Write LRCLK frequency to register 0x00 (e.g. for 48 kHz write 0x6D to register 0x00)
4. Write data 0x03 to register 0x1B

Oscillator Field Trim Procedure #2 (LRCLK Frequency is Not Known):

1. Reset the TAS5086 (power-up or toggle reset pin).

2. Write data 0x6D to register 0x00
3. Write data 0x01 to register 0x1B
4. Read and save data from register 0x27 = 0x$H_7H_6H_5H_4H_3H_2H_1H_0$

   Where,

   $H_7H_6H_5H_4$ = Factory Trim Value

   H_3H_2 H_1H_0 = Location to Write Factory Trim
5. Continually read register 0x27 until H_3H_2 and H_1H_0 are non-zero
6. Write data 0xA5 A5 A5 A5 to register 0xF8
7. Write data 0x00 06 00 EF to register 0xC9
8. Write data 0x00 00 00 00

   0x00 00 00 H5H4 to register 0xCA
9. Write data 0x00 06 00 F1 to register 0xC9
10. Write data 0x00 00 00 00

    0x00 00 00 H7H6 to register 0xCA

Table 14. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	0	–	–	–	–	–	–	Oscillator Trim Not Done (Read Only)
–	1	–	–	–	–	–	–	Oscillator Trim Done
–	–	0	0	0	0	–	–	Reserved
–	–	–	–	–	–	0	–	Select Factory Trim
–	–	–	–	–	–	1	–	Select Field Trim
–	–	–	–	–	–	–	1	Trim Oscillator Command

BKNDERR REGISTER (0x1C)

When a back-end error signal is received, all the output stages are reset by setting all PWM, Valid1, and Valid2 signals low. Hereafter, the modulator waits for approximately the time indicated in the table before it starts.

Table 15. BKNDERR Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	0	0	0	0	Set back end reset period < 1.3 ms
–	–	–	–	0	0	0	1	Set back end reset period 1.3 ms
–	–	–	–	0	0	1	0	Set back end reset period 2.6 ms
–	–	–	–	0	0	1	1	Set back end reset period 3.9 ms
–	–	–	–	0	1	0	0	Set back end reset period 5.2 ms
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**Set back end reset period 6.5 ms**
–	–	–	–	0	1	1	0	Set back end reset period 7.8 ms
–	–	–	–	0	1	1	1	Set back end reset period 9.1 ms
–	–	–	–	1	0	0	0	Set back end reset period 10.4 ms
–	–	–	–	1	0	0	1	Set back end reset period 11.7 ms
–	–	–	–	1	0	1	0	Set back end reset period 13 ms
–	–	–	–	1	0	1	1	Set back end reset period 13 ms
–	–	–	–	1	1	X	X	Set back end reset period 13 ms

INPUT MULTIPLEXER REGISTER (0x20)

The hex value for each nibble is the channel number. For each Input Mux any input from SDIN1, SDIN2, and SDIN3 can be mapped to any internal TAS5086 channel.

Default is 0X00012345.

Table 16. Input Mixer Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved = 0x00**

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	**0**	**0**	**0**	**–**	**–**	**–**	**–**	**SDIN1-L to Channel 1**
0	0	0	1	–	–	–	–	SDIN1-R to Channel 1
0	0	1	0	–	–	–	–	SDIN2-L to Channel 1
0	0	1	1	**–**	**–**	**–**	**–**	SDIN2-R to Channel 1
0	1	0	0	–	–	–	–	SDIN3-L to Channel 1
0	1	0	1	–	–	–	–	SDIN3-R to Channel 1
–	–	–	–	0	0	0	0	SDIN1-L to Channel 2
–	–	–	–	**0**	**0**	**0**	**1**	**SDIN1-R to Channel 2**
–	**–**	**–**	**–**	0	0	1	0	SDIN2-L to Channel 2
–	–	–	–	0	0	1	1	SDIN2-R to Channel 2
–	–	–	–	0	1	0	0	SDIN3-L to Channel 2
–	–	–	–	0	1	0	1	SDIN3-R to Channel 2

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	–	–	–	–	SDIN1-L to Channel 3
0	0	0	1	–	–	–	–	SDIN1-R to Channel 3
0	**0**	**1**	**0**	–	–	–	–	**SDIN2-L to Channel 3**
0	0	1	1	–	–	–	–	SDIN2-R to Channel 3
0	1	0	0	**–**	**–**	**–**	**–**	SDIN3-L to Channel 3
0	1	0	1	–	–	–	–	SDIN3-R to Channel 3
–	–	–	–	0	0	0	0	SDIN1-L to Channel 4
–	–	–	–	0	0	0	1	SDIN1-R to Channel 4
–	–	–	–	0	0	1	0	SDIN2-L to Channel 4
–	–	–	–	**0**	**0**	**1**	**1**	**SDIN2-R to Channel 4**
–	–	–	–	0	1	0	0	SDIN3-L to Channel 4
–	**–**	**–**	**–**	0	1	0	1	SDIN3-R to Channel 4

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	–	–	–		SDIN1-L to Channel 5
0	0	0	1	**–**	**–**	**–**	**–**	SDIN1-R to Channel 5
0	0	1	0	–	–		–	SDIN2-L to Channel 5
0	0	1	1	–	–		–	SDIN2-R to Channel 5
0	**1**	**0**	**0**	–		–	–	**SDIN3-L to Channel 5**
0	1	0	1	–	–	–	–	SDIN3-R to Channel 5
–	**–**	**–**	**–**	0	0	0	0	SDIN1-L to Channel 6
–	–	–	–	0	0	0	1	SDIN1-R to Channel 6
–	–	–	–	0	0	1	0	SDIN2-L to Channel 6
–	–	–	–	0	0	1	1	SDIN2-R to Channel 6
–	–	–	–	0	1	0	0	SDIN3-L to Channel 6
–	–	–	–	**0**	**1**	**0**	**1**	**SDIN3-R to Channel 6**

DOWNMIX INPUT MULTIPLEXER REGISTER (0x21)

Bits D31-D16: Unused

Bits D15-D13: For this description, see Figure 2

Bit D12: If 1, selects downmix data L' to TAS5086 internal channel 1

If 0, selects channel 1 data (from Input Mux 1) to the TAS5086 internal channel 1

Bit D11: If 1, selects downmix data R' to the TAS5086 internal channel 2

If 0, selects channel 2 data (from Input Mux 2) to the TAS5086 internal channel 2

Bit D10: If 1, selects downmix data (L'+R')/2 to the TAS5086 internal channel 5

If 0, selects channel 5 data (from Input Mux 5) to the TAS5086 internal channel 5

Bits D9-D8: Selects either channel 6 data (from Input Mux 6) or channel 6 data that has been processed through Bass Management block or downmix data (L'+R')/2 to the TAS5086 internal channel 6

Bits D7-D5: Unused.

Bit D4: If 1, enable data from Input Mux 5 to Downmix Block

If 0, disable data from Input Mux 5 to Downmix Block

Bit D3: If 1, enable data from Input Mux 4 to Downmix Block

If 0, disable data from Input Mux 4 to Downmix Block

Bit D2: If 1, enable data from Input Mux 3 to Downmix Block

If 0, disable data from Input Mux 3 to Downmix Block

Bit D1: If 1, enable data from Input Mux 2 to Downmix Block

If 0, disable data from Input Mux 2 to Downmix Block

Bit D0: If 1, enable data from Input Mux 1 to Downmix Block

If 0, disable data from Input Mux 1 to Downmix Block

Table 17. Downmix Input Mixer Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
–	–	–	–	–	–	–	–	Unused

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
–	–	–	–	–	–	–	–	Unused

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	1	0	–	–	–	–	–	RESERVED
–	–	–	1	–	–	–	–	Enable Downmix Data L' to Channel 1
–	**–**	**–**	**0**	**–**	**–**	**–**	**–**	**Enable Channel 1 Data to Channel 1**
–	–	–	–	1	–	–	–	Enable Downmix Data R' to Channel 2
–	**–**	**–**	**–**	**0**	**–**	**–**	**–**	**Enable Channel 2 Data to Channel 2**
–	–	–	–	–	1	–	–	Enable Downmix Data (L'+R')/2 to Channel 5
–	**–**	**–**	**–**	**–**	**0**	**–**	**–**	**Enable Channel 5 Data to Channel 5**
–	**–**	**–**	**–**	**–**	**–**	**0**	**0**	**Enable Channel 6 Data to Channel 6**
–	–	–	–	–	–	0	1	Bass Management on Channel 6
–	–	–	–	–	–	1	0	Enable Downmix Data (L'+R')/2 to Channel 6
–	–	–	–	–	–	1	1	Enable Downmix Data (L'+R')/2 to Channel 6

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	1	Enable Data from Input Mux 1 to Downmix Block
–	–	–	–	–	–	–	0	Disable Data from Input Mux 1 to Downmix Block
–	–	–	–	–	–	1	–	Enable Data from Input Mux 2 to Downmix Block
–	–	–	–	–	–	0	–	Disable Data from Input Mux 2 to Downmix Block
–	–	–	–	–	1	–	–	Enable Data from Input Mux 3 to Downmix Block
–	–	–	–	–	0	–	–	Disable Data from Input Mux 3 to Downmix Block
–	–	–	–	1	–	–	–	Enable Data from Input Mux 4 to Downmix Block
–	–	–	–	0	–	–	–	Disable Data from Input Mux 4 to Downmix Block
–	–	–	1	–	–	–	–	Enable Data from Input Mux 5 to Downmix Block
–	–	–	0	–	–	–	–	Disable Data from Input Mux 5 to Downmix Block

AM Mode REGISTER (0x22)

See the AM Interference application note (SLEA040).

Table 18. AM Mode Register

D20	D19	D18	D17	D16	FUNCTION
0	**–**	**–**	**–**	**–**	**AM Mode Disabled**
1	–	–	–	–	AM Mode Enabled
–	**0**	**0**	**–**	**–**	**Select Sequence 1**
–	0	1	–	–	Select Sequence 2
–	1	0	–	–	Select Sequence 3
–	**–**	**–**	**0**	**–**	**IF Frequency 455**
–	–	–	1	–	IF Frequency 262.5
–	**–**	**–**	**–**	**0**	**Use BCD Tuned Frequency**
–	–	–	–	1	Use Binary Tuned Frequency

Table 19. AM Tuned Frequency Register in BCD Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	X	–	–	–	–	BCD Frequency (1000s kHz)
–	–	–	–	–	–	–	–	
–	–	–	–	X	X	X	X	BCD Frequency (100s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default Value**

Table 20. AM Tuned Frequency Register in BCD Mode

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
X	X	X	X	–	–	–	–	BCD Frequency (10s kHz)
–	–	–	–	–	–	–	–	
–	–	–	–	X	X	X	X	BCD Frequency (1s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default Value**

OR

Table 21. AM Tuned Frequency Register in Binary Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	X	X	X	BCD Frequency
–	–	–	–	–	–	–	–	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default Value**

Table 22. AM Tuned Frequency Register in Binary Mode

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
X	X	X	X	X	X	X	X	BCD Frequency
–	–	–	–	–	–	–	–	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default Value**

PWM OUTPUT MUX REGISTER 0x25

This TAS5086 output mux selects which internal PWM channel is output to which pin. Any channel can be output to any pin. The default values are used in systems with the TAS5186.

Bits D31-D25: Reserved = 0x00

Bits D23-D20: Selects which PWM channel is output to PWM_1 (pin 38)

Bits D19-D16: Selects which PWM channel is output to PWM_2 (pin 37)

Bits D15-D12: Selects which PWM channel is output to PWM_3 (pin 36)

Bits D11-D08: Selects which PWM channel is output to PWM_4 (pin 35)

Bits D07-D04: Selects which PWM channel is output to PWM_5 (pin 34)

Bits D03-D00: Selects which PWM channel is output to PWM_6 (pin 33)

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 6 = 0x05.

Table 23. PWM Mux Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved = 0x00**

Table 24. PWM Mux Register

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	0	0	0	–	–	–	–	Multiplex channel 1 to PWM_1 (pin 38)
0	0	0	1	–	–	–	–	Multiplex channel 2 to PWM_1 (pin 38)
0	0	1	0	–	–	–	–	Multiplex channel 3 to PWM_1 (pin 38)
0	**0**	**1**	**1**	**–**	**–**	**–**	**–**	**Multiplex channel 4 to PWM_1 (pin 38)**
0	1	0	0	–	–	–	–	Multiplex channel 5 to PWM_1 (pin 38)
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_1 (pin 38)
–	–	–	–	0	0	0	0	Multiplex channel 1 to PWM_2 (pin 37)
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_2 (pin 37)
–	**–**	**–**	**–**	**0**	**0**	**1**	**0**	**Multiplex channel 3 to PWM_2 (pin 37)**
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_2 (pin 37)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_2 (pin 37)
–	–	–	–	0	1	0	1	Multiplex channel 6 to PWM_2 (pin 37)

Table 25. PWM Mux Register

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	–	–	–	–	Multiplex channel 1 to PWM_3 (pin 36)
0	0	0	1	–	–	–	–	Multiplex channel 2 to PWM_3 (pin 36)
0	0	1	0	–	–	–	–	Multiplex channel 3 to PWM_3 (pin 36)
0	0	1	1	–	–	–	–	Multiplex channel 4 to PWM_3 (pin 36)
0	**1**	**0**	**0**	**–**	**–**	**–**	**–**	**Multiplex channel 5 to PWM_3 (pin 36)**
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_3 (pin 36)
–	–	–	–	0	0	0	0	Multiplex channel 1 to PWM_4 (pin 35)
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_4 (pin 35)
–	–	–	–	0	0	1	0	Multiplex channel 3 to PWM_4 (pin 35)
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_4 (pin 35)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_4 (pin 35)
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**Multiplex channel 6 to PWM_4 (pin 35)**

Table 26. PWM Mux Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	–	–	–		Multiplex channel 1 to PWM_5 (pin 34)
0	**0**	**0**	**1**	**–**	**–**	**–**	**–**	**Multiplex channel 2 to PWM_5 (pin 34)**
0	0	1	0	–	–		–	Multiplex channel 3 to PWM_5 (pin 34)
0	0	1	1	–	–		–	Multiplex channel 4 to PWM_5 (pin 34)
0	1	0	0	–		–	–	Multiplex channel 5 to PWM_5 (pin 34)
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_5 (pin 34)
–	**–**	**–**	**–**	**0**	**0**	**0**	**0**	**Multiplex channel 1 to PWM_6 (pin 33)**
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_6 (pin 33)
–	–	–	–	0	0	1	0	Multiplex channel 3 to PWM_6 (pin 33)
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_6 (pin 33)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_6 (pin 33)
–	–	–	–	0	1	0	1	Multiplex channel 6 to PWM_6 (pin 33)

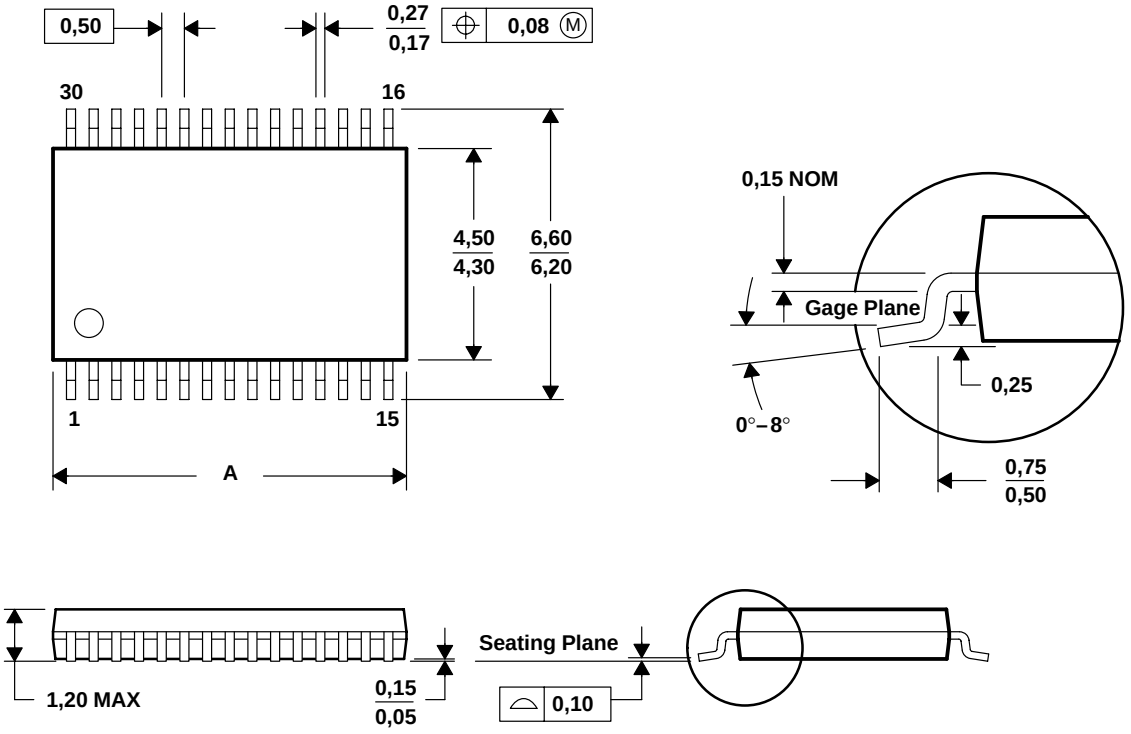
APPENDIX A. TAS5086 APPLICATIONS

See the attached TAS5086 application schematics.

MPDS019D – FEBRUARY 1996 – REVISED FEBRUARY 2002

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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