

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4024BP, TC4024BF, TC4024BFN

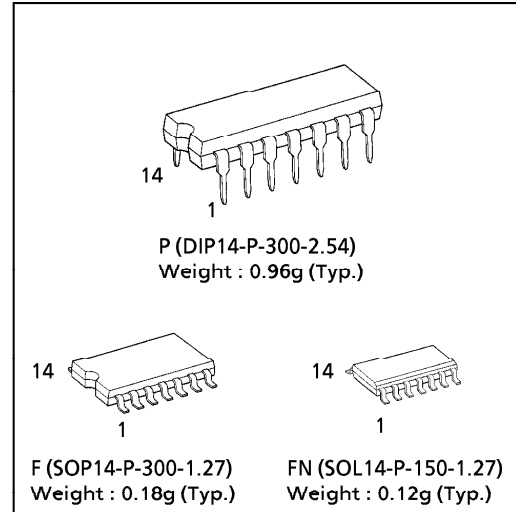
TC4024B 7 STAGE RIPPLE-CARRY BINARY COUNTER / DIVIDERS

TC4024B is 7 stage ripple carry type binary counter having asynchronous clear function.
 The counter advances its counting state by falling edge of **CLOCK** input.
 When **RESET** input is placed at "H", all the internal flip-flop are reset making all the outputs Q1 through Q7 to be "L" regardless of **CLOCK** input.
 This is suitable for frequency divider circuits and control circuits.

(Note) The JEDEC SOP (FN) is not available in Japan.

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	-40~85	°C
Storage Temperature Range	T_{stg}	-65~150	°C

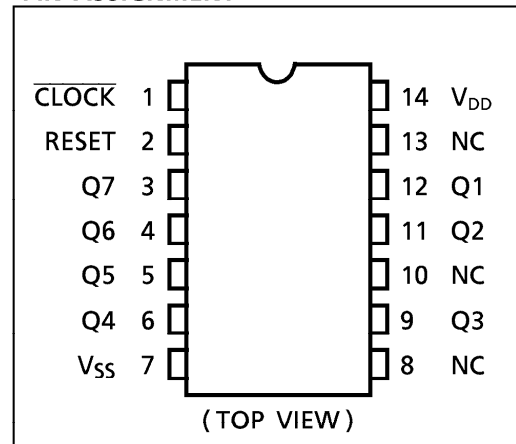


TRUTH TABLE

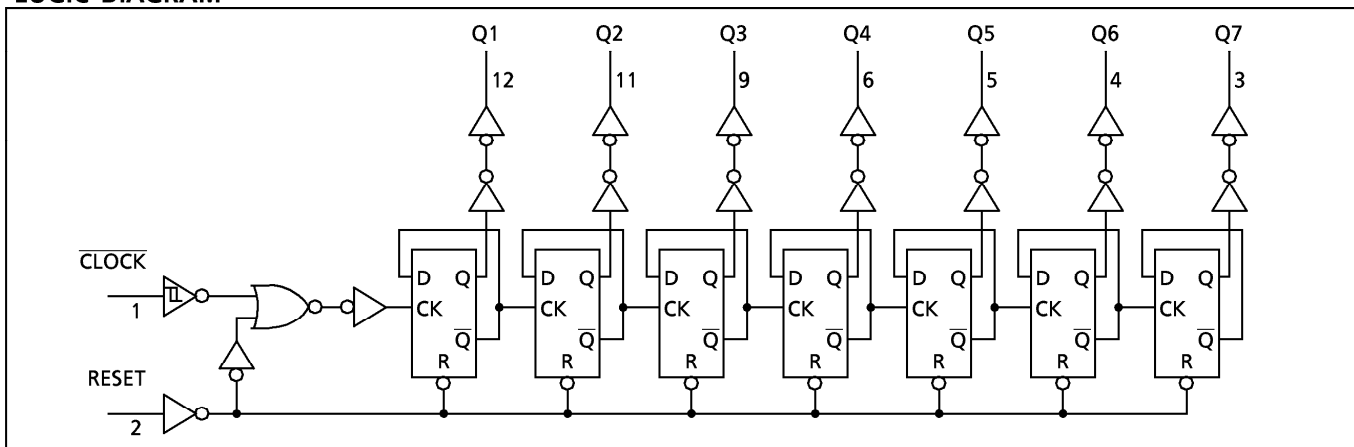
$\overline{\text{CLOCK}} \Delta$	RESET	OUTPUT STAGE
*	H	All Outputs = "L"
\uparrow	L	No Change
\downarrow	L	Advance to Next State

Δ : Level Change, * : Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}$	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output High Current	I_{OH}	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
			5	-2.50	—	-2.10	-4.0	—	-1.70	—		
			10	-1.50	—	-1.30	-2.2	—	-1.10	—		
			15	-4.00	—	-3.40	-9.0	—	-2.80	—		
Output Low Current	I_{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	0.61	—	0.51	1.2	—	0.42	—	mA	
			10	1.50	—	1.30	3.2	—	1.10	—		
			15	4.00	—	3.40	12.0	—	2.80	—		
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	3.5	—	3.5	2.75	—	3.5	—	V	
			10	7.0	—	7.0	5.50	—	7.0	—		
			15	11.0	—	11.0	8.25	—	11.0	—		
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}^*$	5	—	5	—	0.005	5	—	150	μA	
			10	—	10	—	0.010	10	—	300		
			15	—	15	—	0.015	20	—	600		

* All valid input combinations.

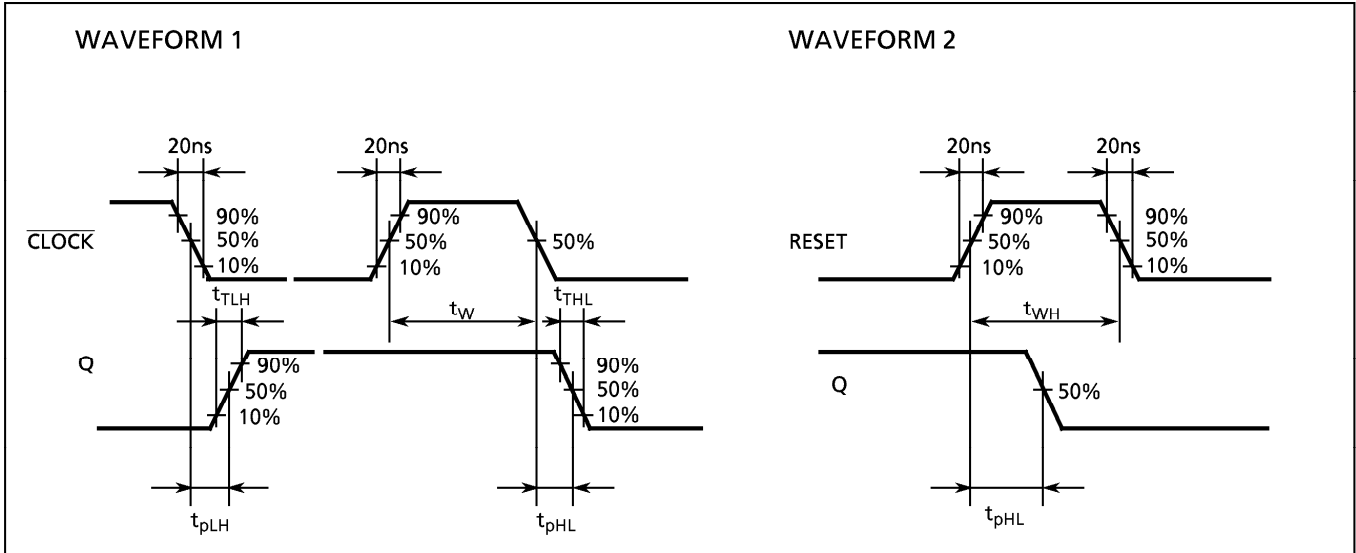
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DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

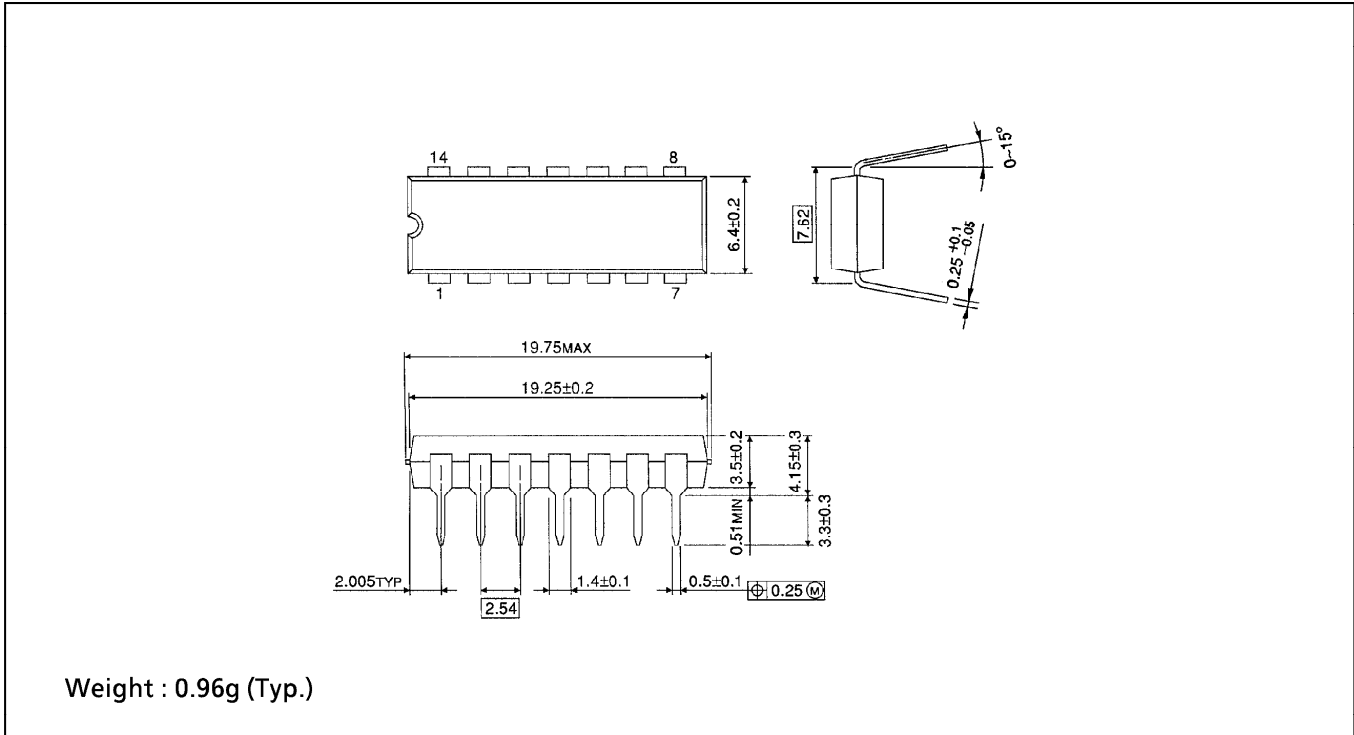
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time (High to Low)	t _{THL}		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time ($\overline{\text{CLOCK}}$ - Q1)	t _{pLH}		5	—	140	360	
			10	—	70	160	
			15	—	50	130	
Propagation Delay Time ($\overline{\text{CLOCK}}$ - Q1)	t _{pHL}		5	—	140	360	
			10	—	70	160	
			15	—	50	130	
Propagation Delay Time ($\overline{\text{CLOCK}}$ - Q7)	t _{pLH}		5	—	400	1200	
			10	—	160	520	
			15	—	115	430	
Propagation Delay Time ($\overline{\text{CLOCK}}$ - Q7)	t _{pHL}		5	—	400	1200	
			10	—	160	520	
			15	—	115	430	
Propagation Delay Time (RESET - Q)	t _{pHL}		5	—	140	280	
			10	—	70	120	
			15	—	50	100	
Max. Clock Frequency	f _{CL}		5	3.5	14	—	MHz
			10	8.0	30	—	
			15	12.0	40	—	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t _{rCL} t _{fCL}		5	No Limit			μs
			10				
			15				
Max. Clock Pulse Width	t _w		5	—	40	140	ns
			10	—	20	60	
			15	—	15	40	
Max. Pulse Width (RESET)	t _{WH}		5	—	40	200	
			10	—	20	80	
			15	—	15	60	
Minimum Removal Time	t _{rem}		5	—	0	350	
			10	—	0	150	
			15	—	0	100	
Input Capacitance	C _{IN}			—	5	7.5	

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



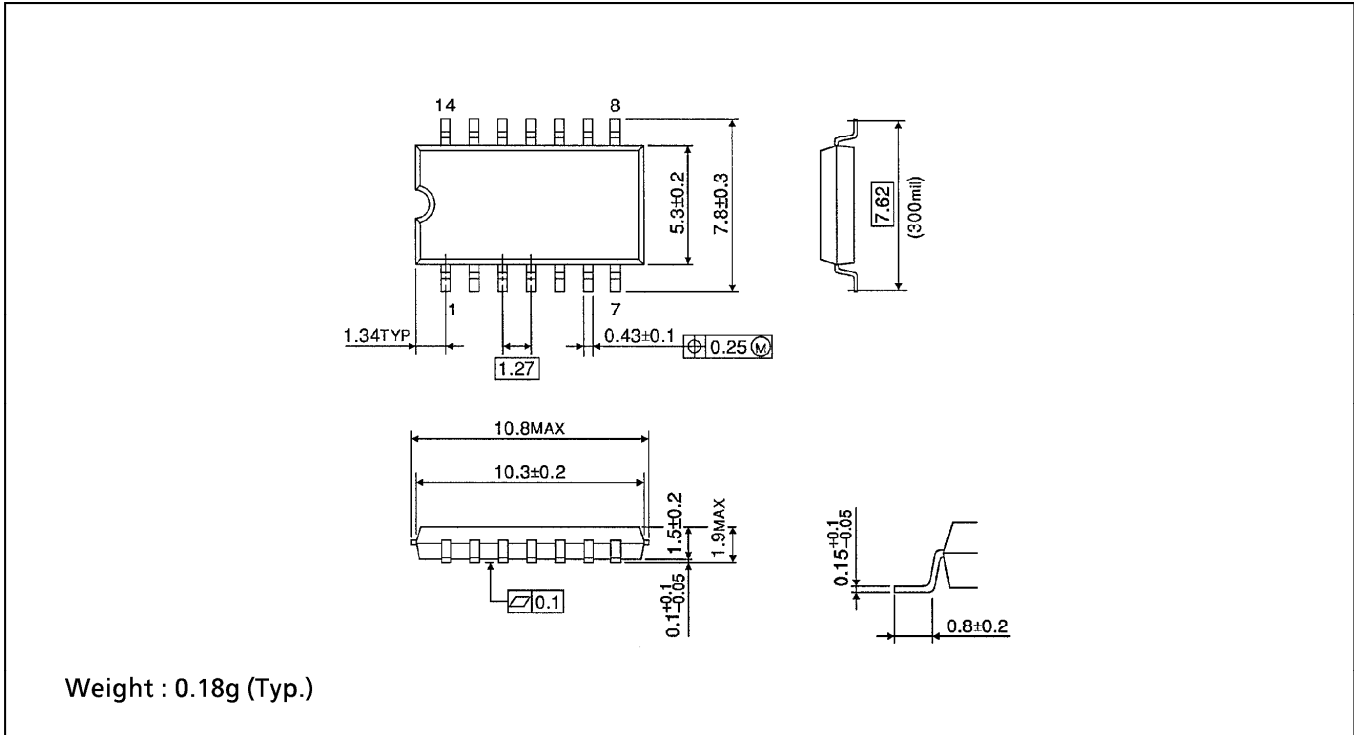
DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

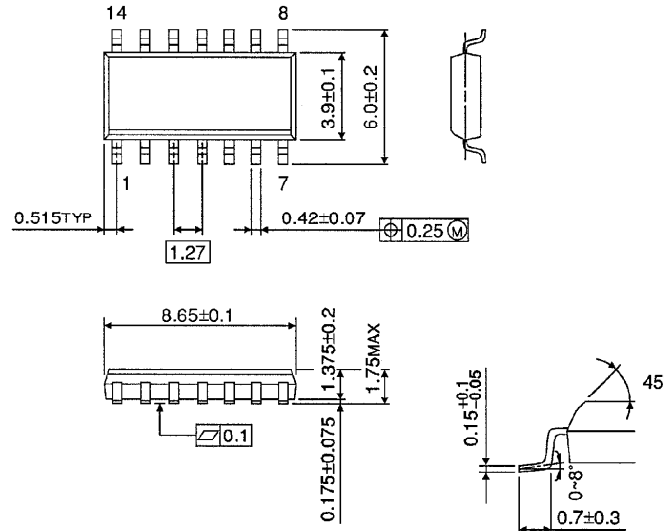
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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