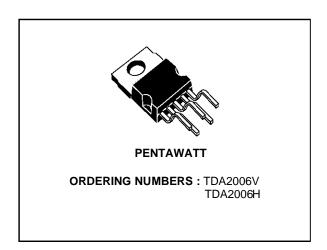




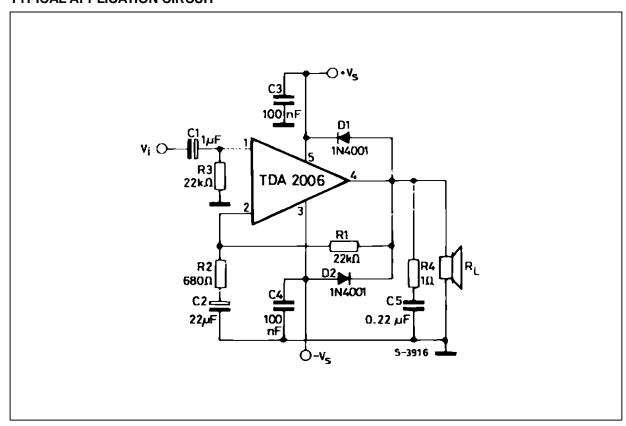
12W AUDIO AMPLIFIER

DESCRIPTION

The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At $\pm 12\text{V}$, d = 10 % typically it provides 12W output power on a 4Ω load and 8W on a 8Ω . The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.

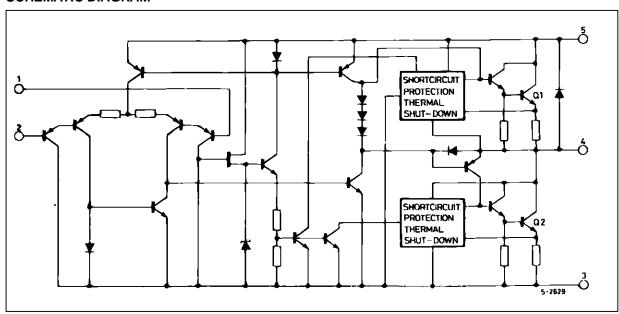


TYPICAL APPLICATION CIRCUIT



May 1995 1/12

SCHEMATIC DIAGRAM



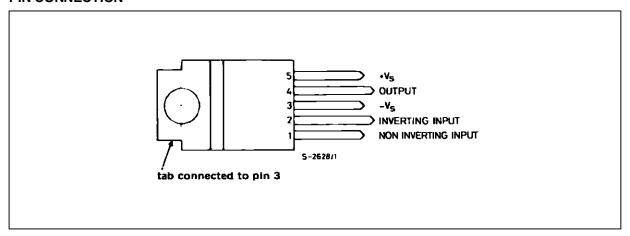
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	± 15	V
Vi	Input Voltage	Vs	
Vi	Differential Input Voltage	± 12	V
Io	Output Peak Current (internaly limited)	3	Α
Ptot	Power Dissipation at T _{case} = 90 °C	20	W
T_{stg}, T_{j}	Storage and Junction Temperature	- 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
R _{th (j-c)}	Thermal Resistance Junction-case Ma	ax	3	°C/W

PIN CONNECTION



ELECTRICAL CHARACTERISTICS

(refer to the test circuit; $V_S = \pm 12V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Supply Voltage		± 6		± 15	V
Id	Quiescent Drain Current	V _s = ± 15V		40	80	mA
I _b	Input Bias Current	$V_s = \pm 15V$		0.2	3	μΑ
Vos	Input Offset Voltage	V _s = ± 15V		± 8		mV
Ios	Input Offset Current	V _s = ± 15V		± 80		nA
Vos	Output Offset Voltage	V _s = ± 15V		± 10	± 100	mV
Po	Output Power	$d=10\%, f=1kHz$ $R_L=4\Omega$ $R_L=8\Omega$	6	12 8		W
d	Distortion	$\begin{aligned} P_o &= 0.1 \text{ to } 8W, R_L = 4\Omega, f = 1 \text{kHz} \\ P_o &= 0.1 \text{ to } 4W, R_L = 8\Omega, f = 1 \text{kHz} \end{aligned}$		0.2 0.1		% %
Vi	Input Sensitivity	$\begin{aligned} P_o &= 10W, R_L = 4\Omega, f = 1 \text{kHz} \\ P_o &= 6W, R_L = 8\Omega, f = 1 \text{kHz} \end{aligned}$		200 220		mV mV
В	Frequency Response (- 3dB)	$P_0 = 8W, R_L = 4\Omega$	2	20Hz to	100kHz	Z
Ri	Input Resistance (pin 1)	f = 1kHz	0.5	5		МΩ
G√	Voltage Gain (open loop)	f = 1kHz		75		dB
Gv	Voltage Gain (closed loop)	f = 1kHz	29.5	30	30.5	dB
e _N	Input Noise Voltage	B (– 3dB) = 22Hz to 22kHz, $R_L = 4\Omega$		3	10	μV
i _N	Input Noise Current	B (– 3dB) = 22Hz to 22kHz, $R_L = 4\Omega$		80	200	рА
SVR	Supply Voltage Rejection	$R_L = 4\Omega$, $R_g = 22k\Omega$, $f_{ripple} = 100Hz$ (*)	40	50		dB
ld	Drain Current	$P_o = 12W, R_L = 4\Omega$ $P_o = 8W, R_L = 8\Omega$		850 500		mA mA
Tj	Thermal Shutdown Junction Temperature				145	°C

^(*) Referring to Figure 15, single supply.

Figure 1: Output Power versus Supply Voltage

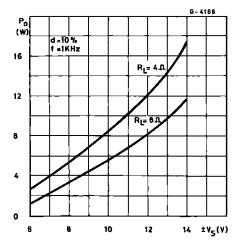


Figure 3: Distortion versus Frequency

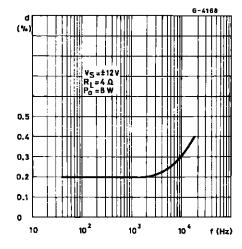


Figure 5: Sensitivity versus Output Power

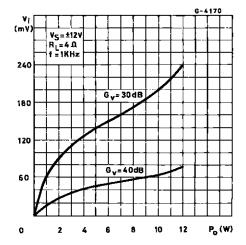


Figure 2: Distortion versus Output Power

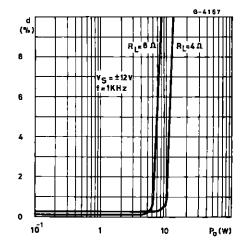


Figure 4: Distortion versus Frequency

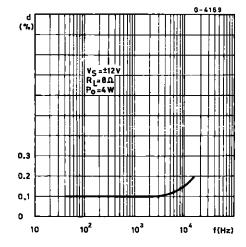


Figure 6: Sensitivity versus Output Power

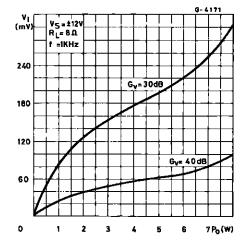


Figure 7: Frequency Response with different values of the rolloff Capacitor C8 (see Figure 13)

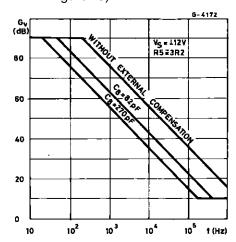


Figure 9: Quiescent Current versus Supply Voltage

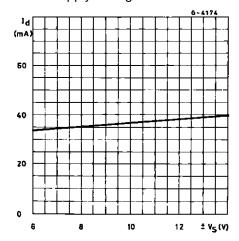


Figure 11: Power Dissipation and Efficiency versus Output Power

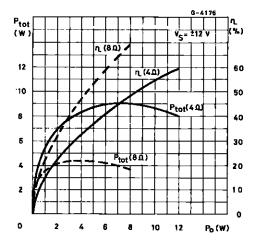


Figure 8: Value of C8 versus Voltage Gain for different Bandwidths (see Figure 13)

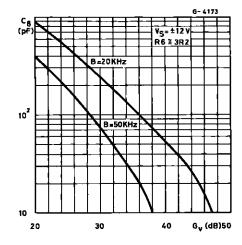


Figure 10 : Supply Voltage Rejection versus Voltage Gain

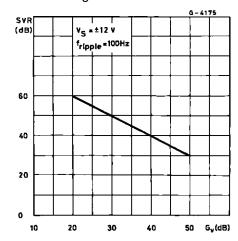


Figure 12: Maximum Power Dissipation versus Supply Voltage (sine wave operation)

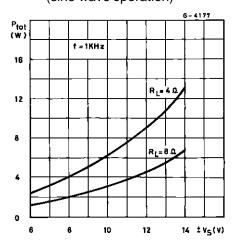


Figure 13: Application Circuit with Spilt Power Supply

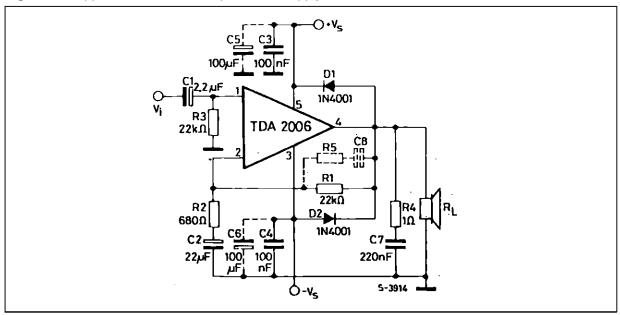


Figure 14: P.C. Board and Components Layout of the Circuit of Figure 13 (1:1 scale)

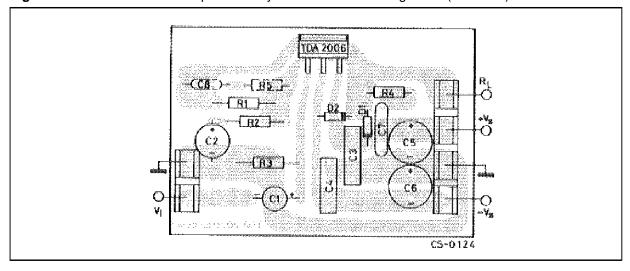


Figure 15: Application Circuit with Single Power Supply

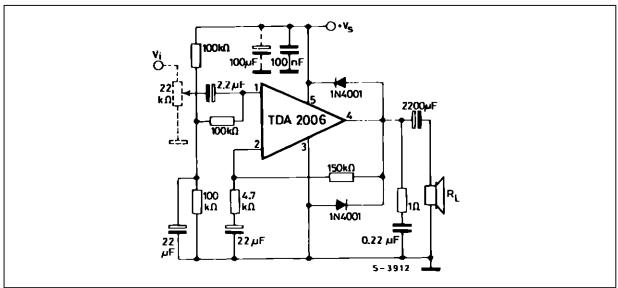
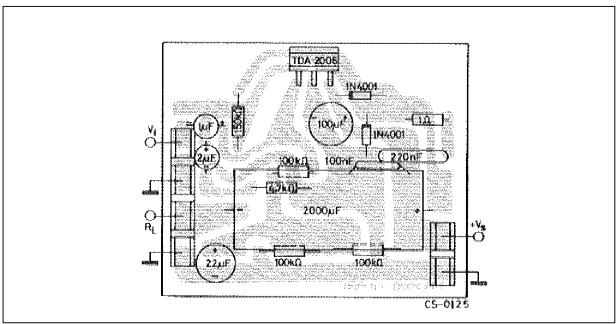


Figure 16: P.C. Board and Components Layout of the Circuit of Figure 15 (1:1 scale)



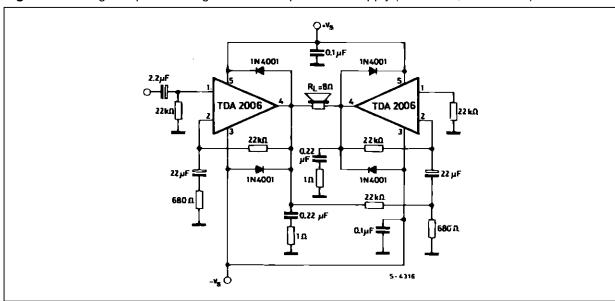


Figure 17: Bridge Amplifier Configuration with Split Power Supply (Po = 24W, $V_S = \pm 12V$)

PRACTICAL CONSIDERATIONS

Printed Circuit Board

The layout shown in Figure 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly Suggestion

No electrical isolation is needed between the pack-

age and the heat-sink with single supply voltage configuration.

Application Suggestion

The recommended values of the components are the ones shown on application circuits of Figure 13. Different values can be used. The table 1 can help the designers.

Table 1

Component	Recommanded Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value		
R ₁	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)		
R ₂	680 Ω	Closed Loop Gain Setting	Decrease of Gain (*)	Increase of Gain		
R ₃	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance		
R ₄	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads			
R ₅	3 R ₂	Upper Frequency Cut-off	Poor High Frequencies Attenuation	Danger of Oscillation		
C ₁	2.2 μF	Input DC Decoupling		Increase of Low Frequencies Cut-off		
C ₂	22 μF	Inverting Input DC Decoupling		Increase of Low Frequencies Cut-off		
C ₃ C ₄	0.1 μF	Supply Voltage by Pass		Danger of Oscillation		
C ₅ C ₆	100 μF	Supply Voltage by Pass		Danger of Oscillation		
C ₇	0.22 μF	Frequency Stability		Danger of Oscillation		
C ₈	1 2πBR ₁	Upper Frequency Cut-off	Lower Bandwidth	Larger Bandwidth		
D ₁ D ₂	1N4001	To Protect the Device Against Output Voltage Spikes.				

^(*) Closed loop gain must be higher than 24dB.



SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Figure 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Figure 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT DOWN

The presence of a thermal limiting circuit offers the following advantages:

- 1) an overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_i cannot be higher than 150°C.
- 2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 $^{\circ}$ C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); Figure 22 shows the dissipable power as a function of ambient temperature for different thermal resistances.

Figure 18: Maximum Output Current versus Voltage V_{CE (sat)} accross each Output Transistor

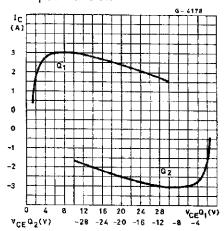


Figure 19: Safe Operating Area and Collector Characteristics of the Protected Power Transistor

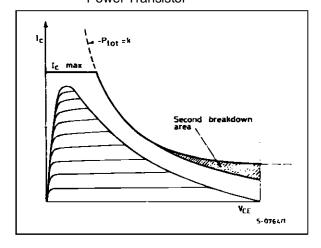


Figure 20 : Output Power and Drain Current versus Case Temlperature ($R_L = 4\Omega$)

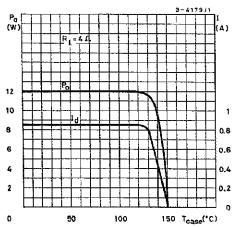


Figure 21 : Output Power and Drain Current versus Case Temlperature ($R_L = 8\Omega$)

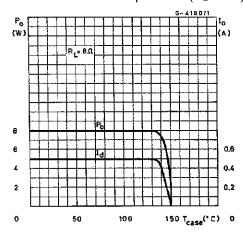
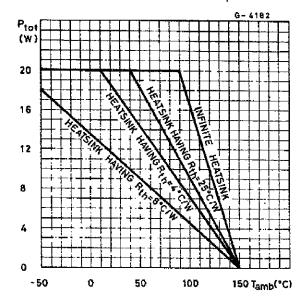


Figure 22: Maximum Allowable Power Dissipation versus Ambient Temperature

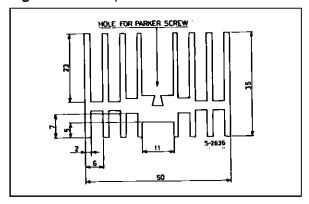


DIMENSION SUGGESTION

The following table shows the length of the heatsink in Figure 23 for several values of P_{tot} and R_{th} .

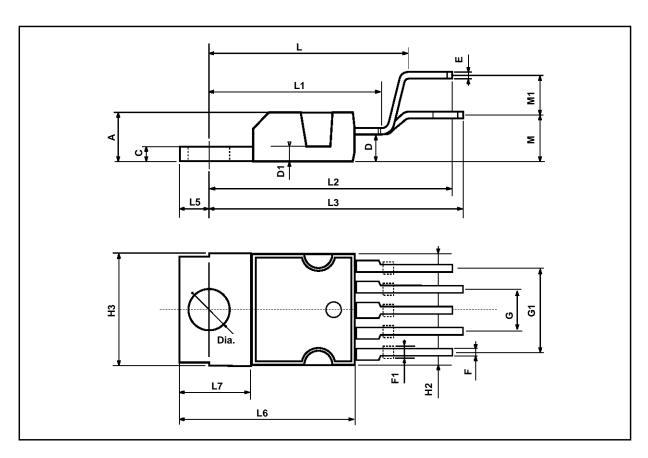
P _{tot} (W)	12	8	6
Lenght of Heatsink (mm)	60	40	30
R _{th} of Heatsink (°C/W)	4.2	6.2	8.3

Figure 23 : Example of Heatsink



PENTAWATT PACKAGE MECHANICAL DATA

DIM.		mm			inch		
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			4.8			0.189	
С			1.37			0.054	
D	2.4		2.8	0.094		0.110	
D1	1.2		1.35	0.047		0.053	
E	0.35		0.55	0.014		0.022	
F	0.8		1.05	0.031		0.041	
F1	1		1.4	0.039		0.055	
G		3.4		0.126	0.134	0.142	
G1		6.8		0.260	0.268	0.276	
H2			10.4			0.409	
H3	10.05		10.4	0.396		0.409	
L		17.85			0.703		
L1		15.75			0.620		
L2		21.4			0.843		
L3		22.5			0.886		
L5	2.6		3	0.102		0.118	
L6	15.1		15.8	0.594		0.622	
L7	6		6.6	0.236		0.260	
М		4.5			0.177		
M1		4			0.157		
Dia	3.65		3.85	0.144		0.152	



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