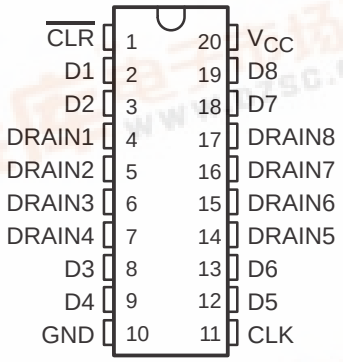
TPIC6B273
POWER LOGIC OCTAL D-TYPE LATCH

SLIS031 – APRIL 1994 – REVISED JULY 1995

- Low $r_{DS(on)}$ . . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Low Power Consumption

DW OR N PACKAGE
(TOP VIEW)



description

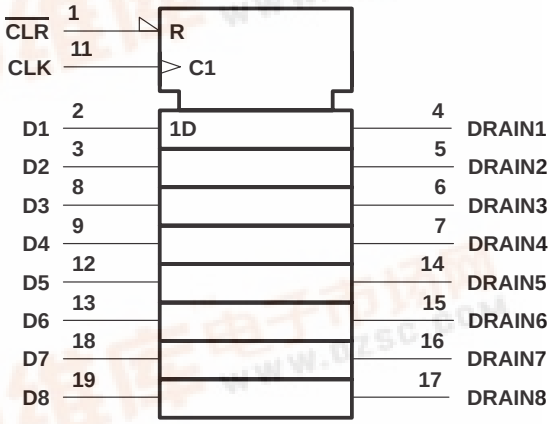
The TPIC6B273 is a monolithic, high-voltage, medium-current, power logic octal D-type latch with DMOS-transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

The TPIC6B273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS-transistor output.

When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all eight DMOS-transistor outputs off. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

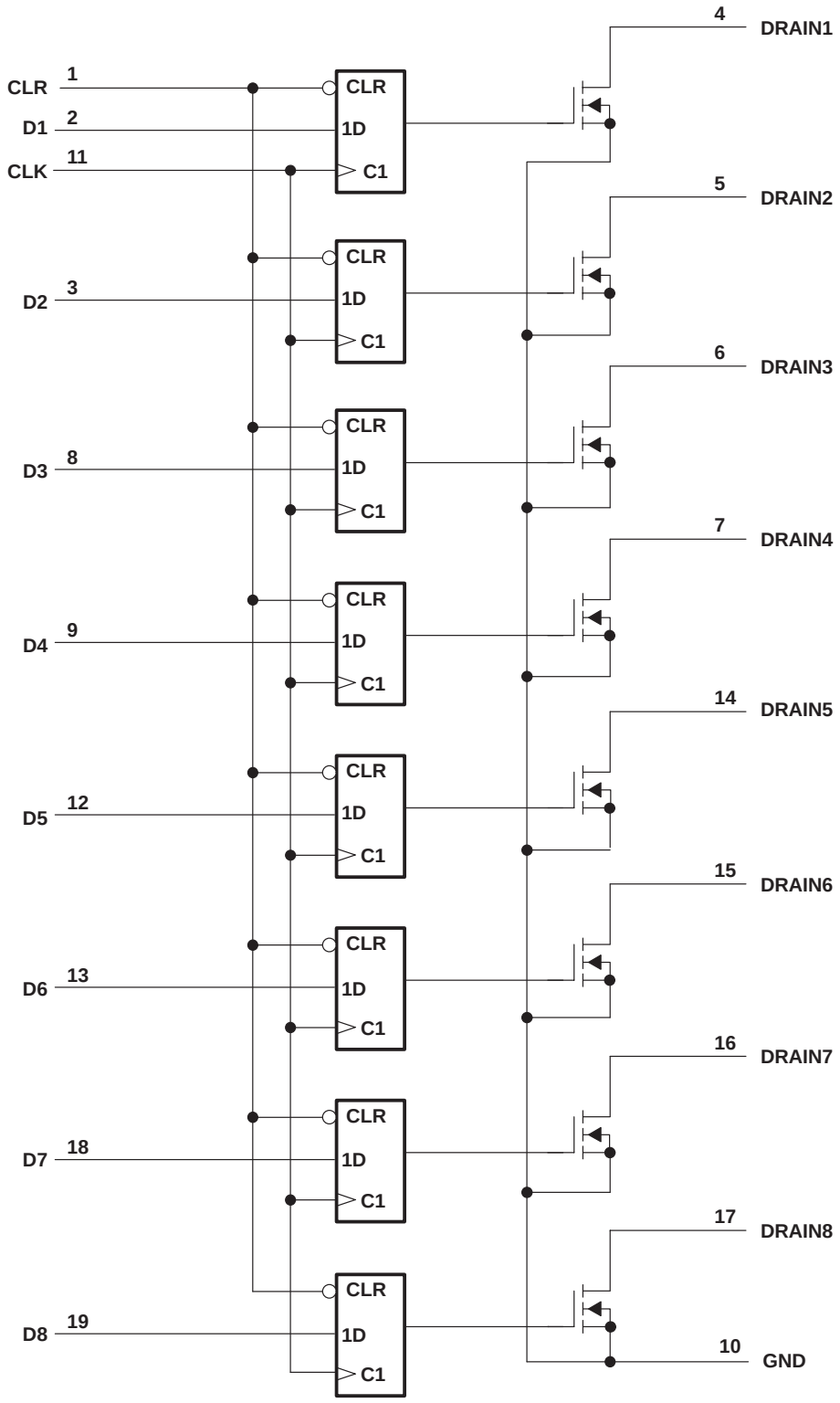
FUNCTION TABLE
(each channel)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

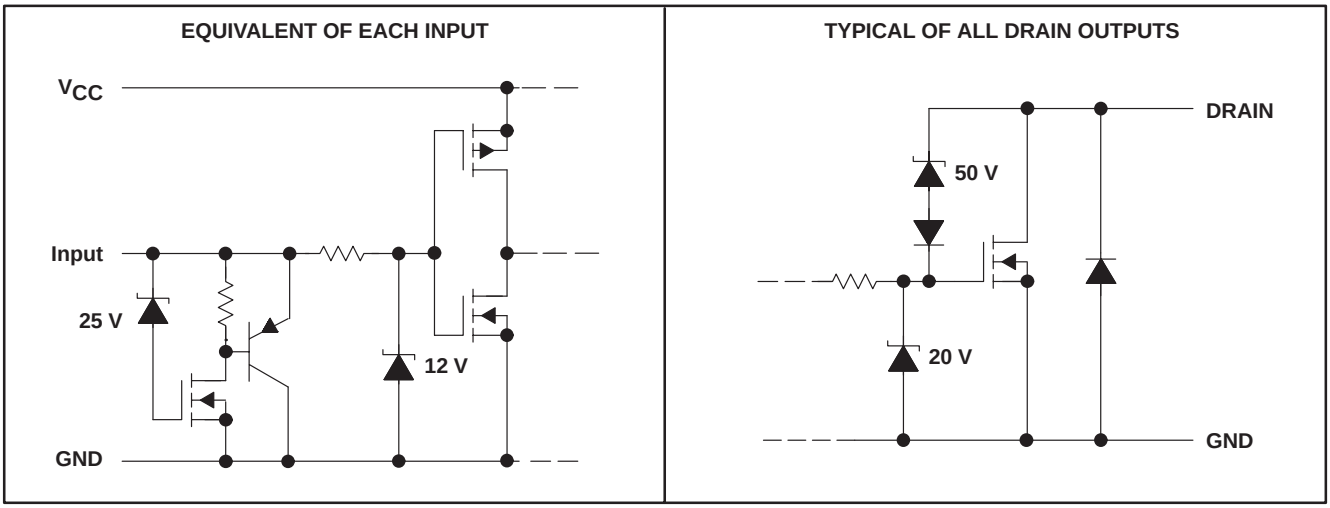
H = high level, L = low level, X = irrelevant

The TPIC6B273 is characterized for operation over the operating case temperature range of –40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	–0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, I_D, T_C = 25°C	150 mA
Peak drain current single output, I_{DM}, T_C = 25°C (see Note 3)	500 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 200 mH, I_{AS} = 0.5 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	–500	500	mA
Setup time, D high before CLK↑, t_{su} (see Figure 2)	20		ns
Hold time, D high after CLK↑, t_h (see Figure 2)	20		ns
Pulse duration, t_w (see Figure 2)	40		ns
Operating case temperature, T_C	–40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA				0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				–1	µA
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off			20	100	µA
			All outputs on			150	300	
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, See Notes 5, 6, and 7	T_C = 85°C,			90		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	V_{CC} = 5.5 V			0.1	5	µA
		V_{DS} = 40 V,	V_{CC} = 5.5 V,	T_C = 125°C		0.15	8	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 100 mA,	V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 6 and 7		4.2	5.7	Ω
		I_D = 100 mA, T_C = 125°C	V_{CC} = 4.5 V,			6.8	9.5	
		I_D = 350 mA,	V_{CC} = 4.5 V			5.5	8	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, See Figures 1, 2, and 8	I_D = 100 mA,		150		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK				90		ns
t_r	Rise time, drain output				200		ns
t_f	Fall time, drain output				200		ns
t_a	Reverse-recovery-current rise time	I_F = 100 mA, See Notes 5 and 6 and Figure 3	di/dt = 20 A/µs,		100		ns
t_{rr}	Reverse-recovery time				300		

NOTES: 3. Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		90	°C/W
		N package			95	

PARAMETER MEASUREMENT INFORMATION

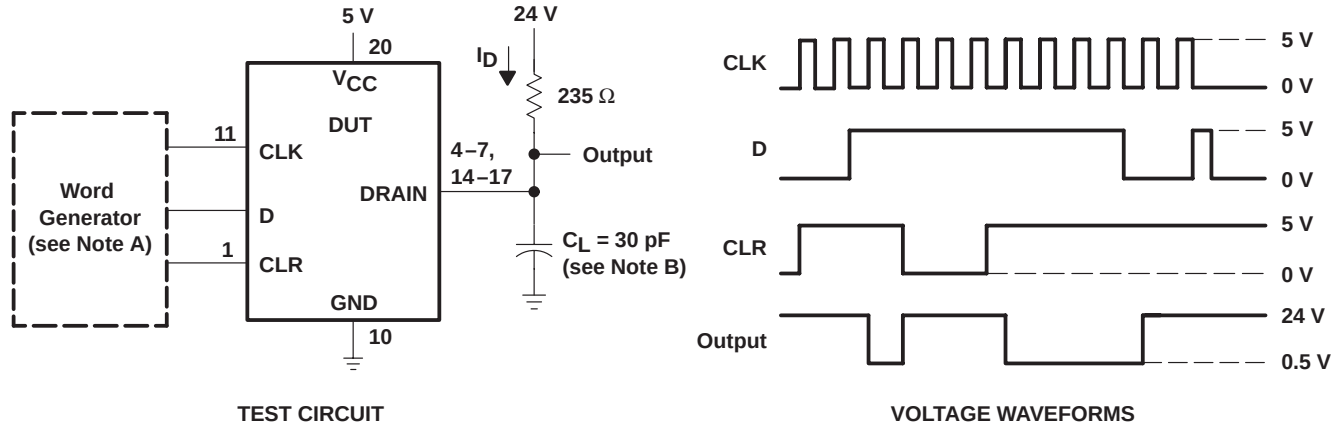


Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

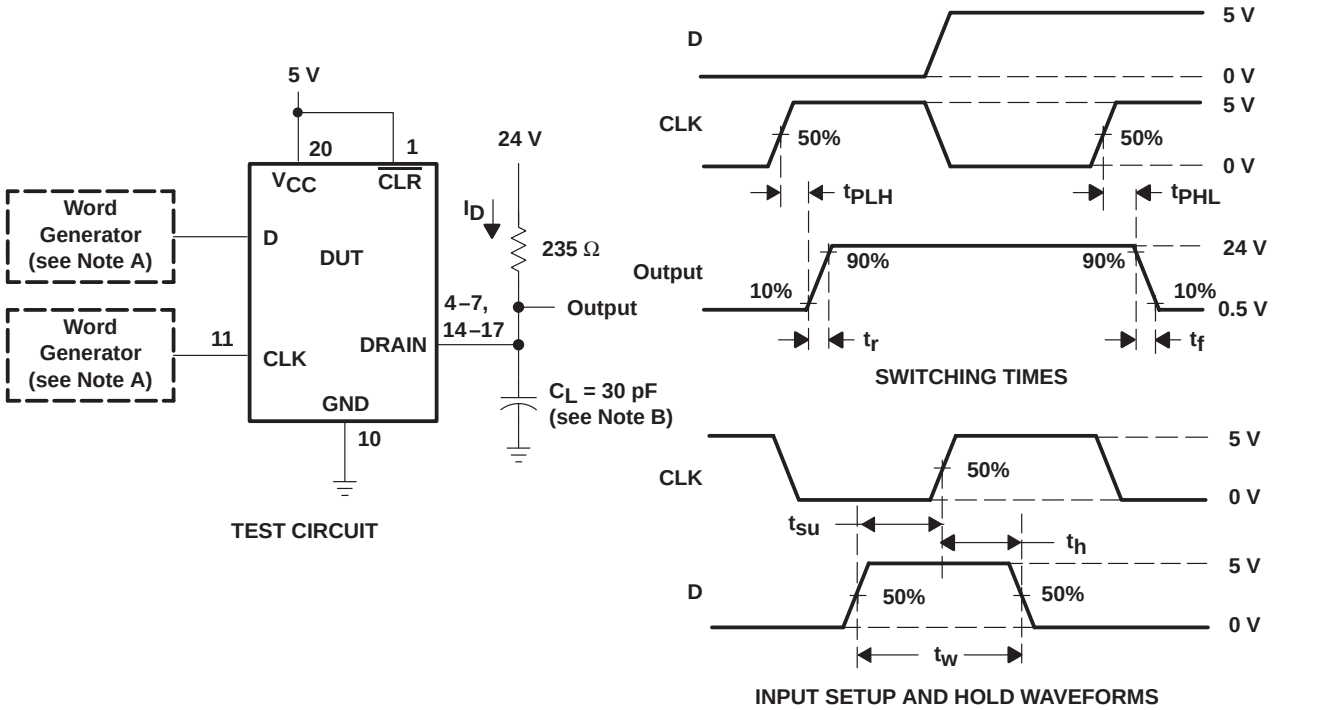
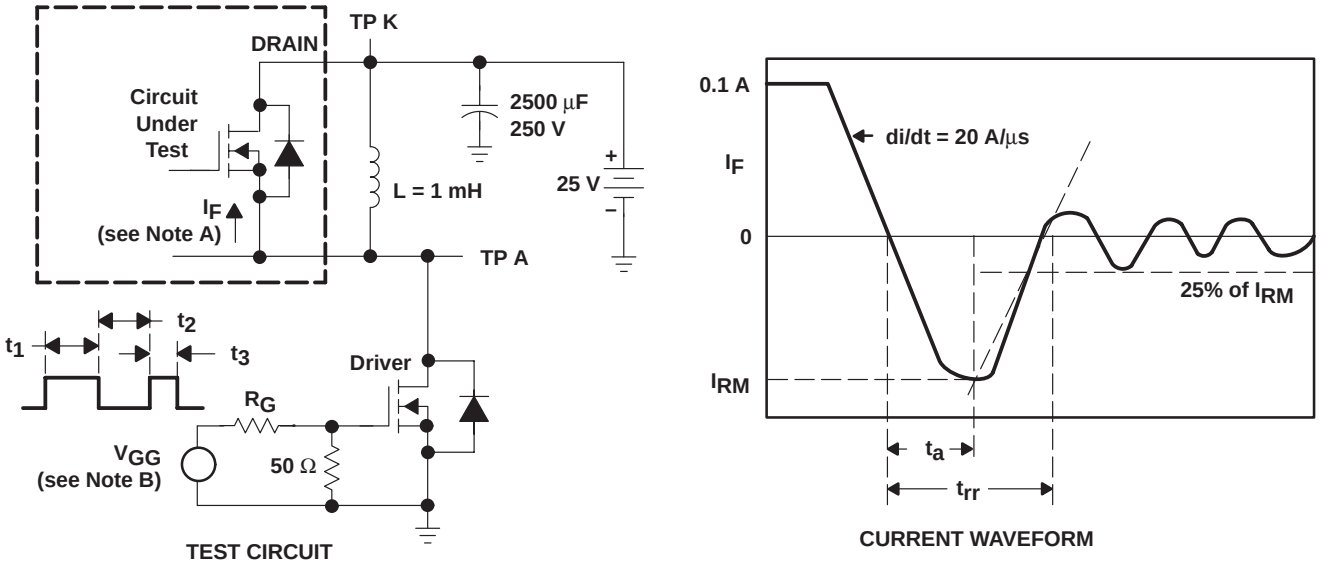


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

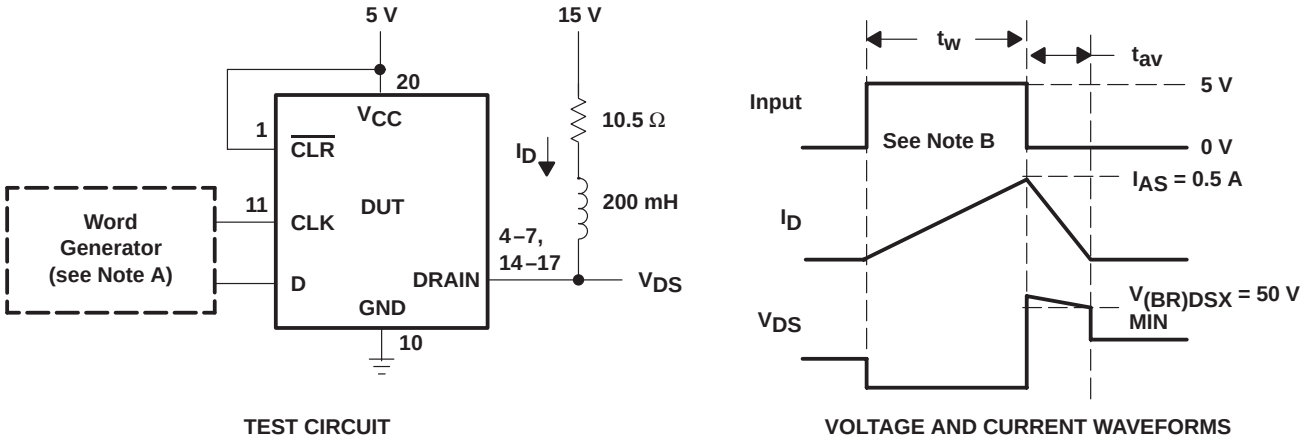
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

B. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.1 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 0.5 A.
Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 30 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

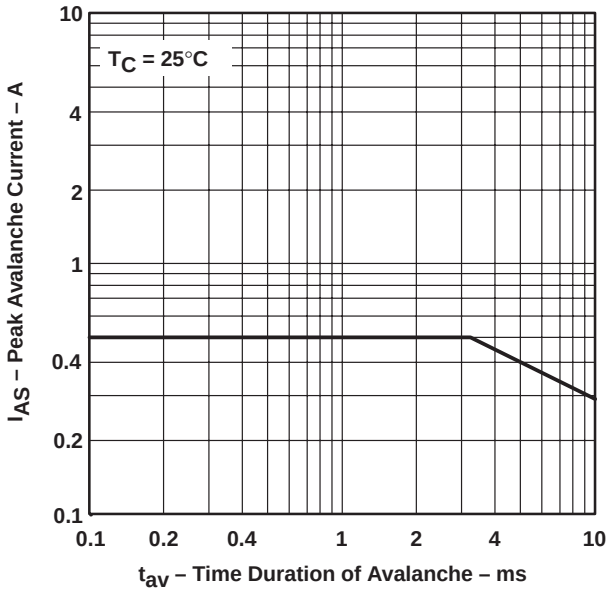


Figure 5

DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

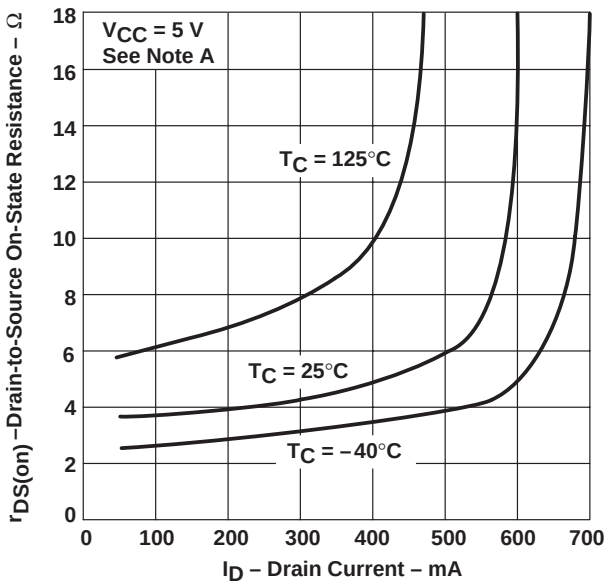


Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

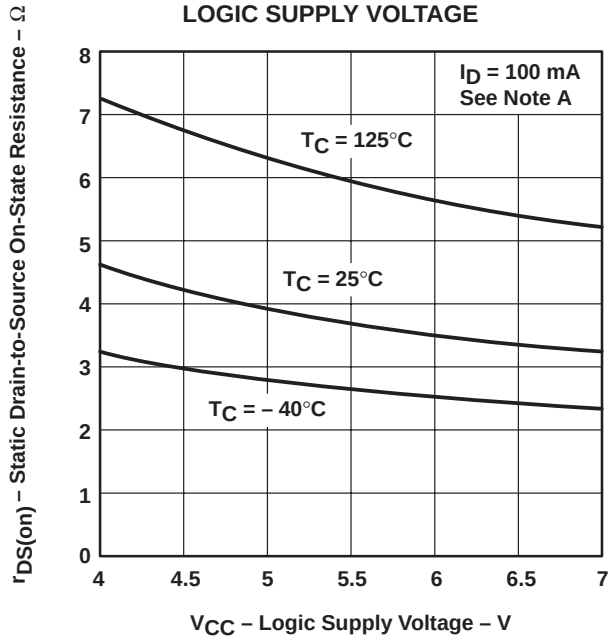


Figure 7

SWITCHING TIME vs CASE TEMPERATURE

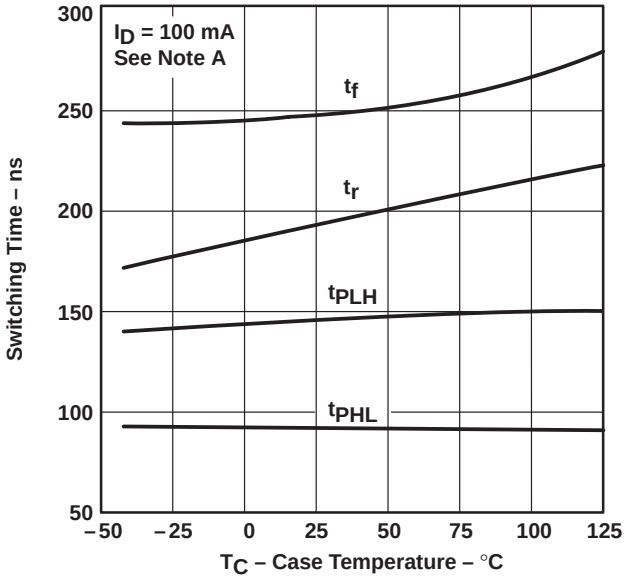


Figure 8

NOTE C: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

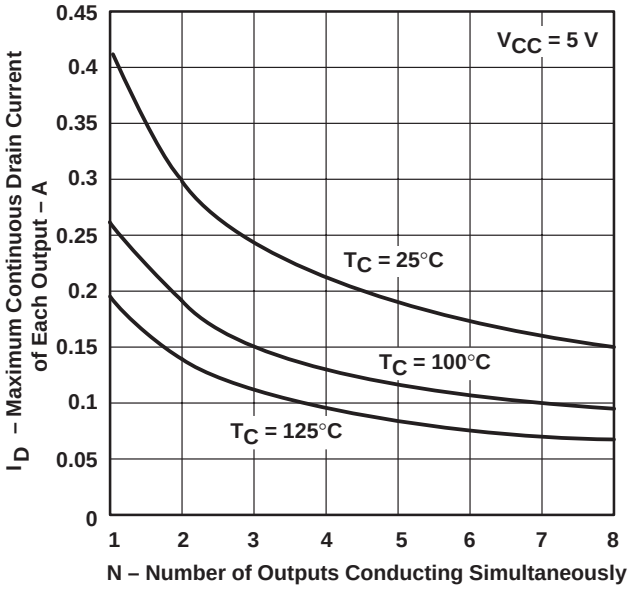


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

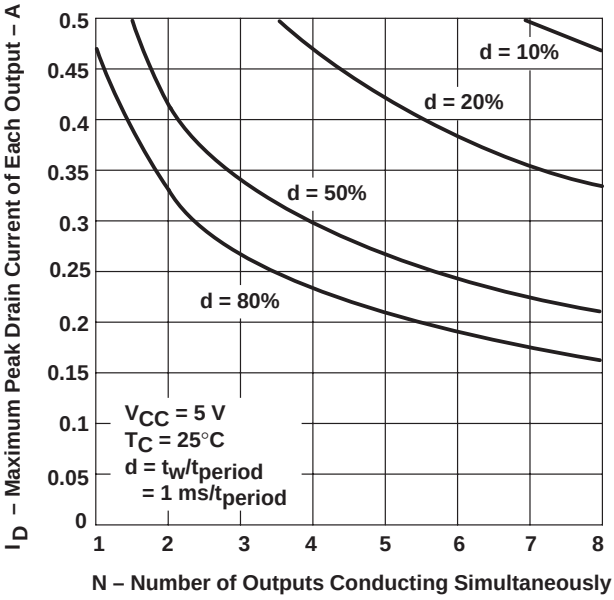


Figure 10

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