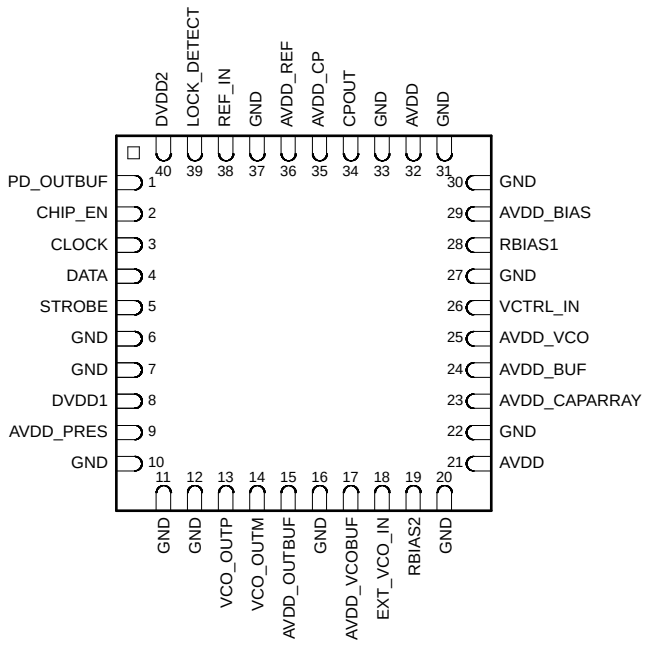
INTEGER-N PLL WITH INTEGRATED VCO

FEATURES

- Fully Integrated VCO
- Low Phase Noise: -138 dBc/Hz (at 600 kHz, f_{VCO} of 1.9 GHz)
- Low Noise Floor: -160dBc/Hz at 10 MHz Offset
- Integer-N PLL
- Input Reference Frequency range: 10 104 MHz
- VCO Frequency Divided by 2-4 Output
- Output Buffer Enable Pin
- Programmable Charge Pump Current
- Hardware and Software Power Down
- 3-Wire Serial Interface
- Single Supply: 4.5 V 5.25 V Operation
- Silicon Germanium Technology

RHA PACKAGE
(TOP VIEW)



APPLICATIONS

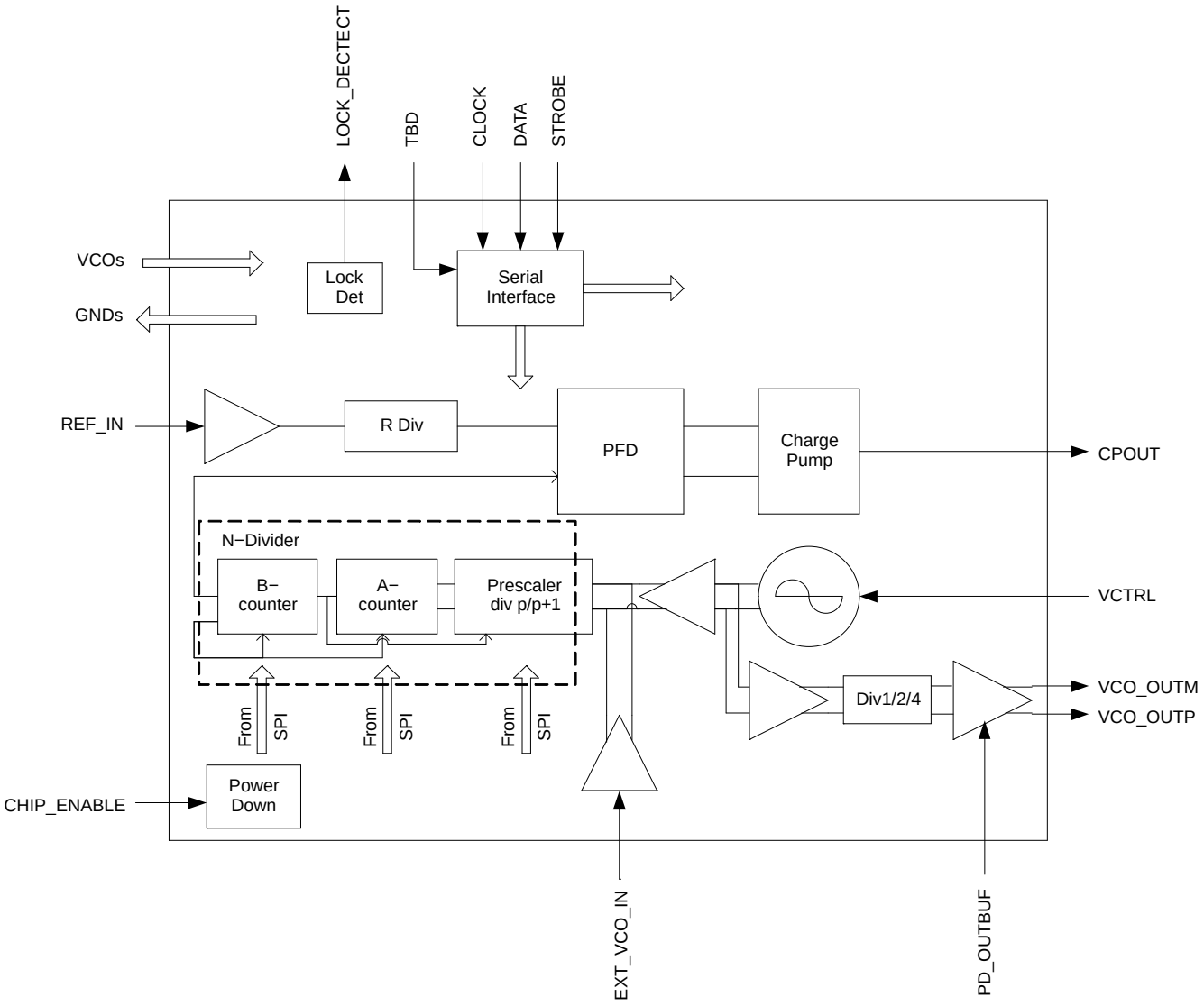
- Wireless Infrastructure
  - WCDMA
  - CDMA
  - GSM

DESCRIPTION

TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for wireless infrastructure applications. TRF3761 includes a low noise voltage controlled oscillator (VCO) and an integer-N PLL.

TRF3761 integrates a divide-by-2 or 4 options for a more flexible output frequency range. It is controlled through a 3-wire serial interface programming (SPI) interface. It can be powered down when it is not used by the SPI or external pin.

PRODUCT PREVIEW



DEVICE INFORMATION

Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PD_OUTBUF	1	I	Output Buffer Power Down
CHIP_EN	2	I	Chip Enable
CLOCK	3	I	Serial Interface Clock
DATA	4	I/O	Serial Interface Data
STROBE	5	I	Serial Interface Strobe
GND	6		Digital Ground
GND	7		Digital Ground
DVDD1	8		Power Supply for DIG regulator
AVDD_PRES	9		Power Supply for Prescaler
GND	10		Analog Ground
GND	11		Analog Ground
GND	12		Analog Ground
VCO_OUTP	13	O	VCO Output
VCO_OUTM	14	O	VCO Output
AVDD_OUTBUF	15		Power Supply for Output Buffers
GND	16		Analog Ground
AVDD_VCOBUF	17		Power Supply for VCO buffers
EXT_VCO_IN	18	I	External VCO input to prescaler
RBIAS2	19	I/O	External Bias Resistor
GND	20		Analog Ground
AVDD	21		Analog Power Supply
GND	22		Analog Ground
AVDD_CAPARRAY	23		Power Supply for VCO Core and Buffer
AVDD_BUF	24		Power Supply for VCO Core and Buffer
AVDD_VCO	25		Power Supply for VCO Core and Buffer
VCTRL_IN	26	I	VCO Control Voltage
GND	27		Analog Ground
RBIAS1	28	I/O	External Bias Resistor
AVDD_BIAS	29		Power Supply for BG Current Bias
GND	30		Analog Ground
GND	31		Analog Ground
AVDD	32		Power Supply for FUSE Cell
GND	33		Analog Ground
CPOUT	34	O	Charge Pump Output
AVDD_CP	35		Analog Power Supply for Charge Pump
AVDD_REF	36		Power Supply for REF FREQ Block
GND	37		Analog Ground
REF_IN	38	I	Reference Signal Input
LOCK_DETECT	39	O	Lock Detect Output
DVDD2	40		Power Supply for DIG Regulator

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
Supply voltage range(2)	-0.3 to 5.5	V
Digital I/O voltage range	-0.3 to V_I +0.3	V
ESD rating, human-body model (HBM)(3)	TBD	
ESD rating, charged-device model (CDM)(3)	TBD	
Operating virtual junction temperature range, T_J	-40 to 150	°C
Operating free-air temperature range, T_A	-40 to 85	°C
Storage temperature range, T_{stg}	-65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolutemaximumrated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD rating not valid for RF sensitive pins.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	4.5	5	5.25	V

ELECTRICAL CHARACTERISTICS

supply voltage = 4.5 V to 5.25 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC Parameters							
I_{CC}	Total supply current	T_A = 25°C	Divide by 1 output		130		mA
			Divide by 2 output		140		mA
			Divide by 4 output		150		mA
	Power-down current				TBD		A
RF Output Parameters							
f	Frequency range				TBD		
P_O	RF output power(1)	Output Buffer On	Divide by 1 output		1		dBm
		Output buffer on	Divide by 2 and 4		3		
	Output Buffer On/Off isolation	Output buffer on//off power ratio			60		dBc
	Output Buffer turn on time	Amplitude (10% to 90% final level)			2		µs
	2nd Harmonic Suppression	Divide by 1 output (1)(2)			-26		dBc
		Divide by 2 and 4 output (1)(2)			-35		
	3rd Harmonic Suppression	Divide by 1 output (1)(2)			-26		dBc
		Divide by 2 output (1)(2)			-20		
		Divide by 4 output (1)(2)			-15		
	Lock time	Within 500 Hz final frequency			300		µs
Reference Oscillator Parameters							
f_{ref}	Reference frequency			10		104	MHz
	Reference input sensitivity			0.2		2.5	Vpp
	Reference input impedance	Parallel capacitance			5	TBD	pF
		Parallel resistance		TBD			Ω

(1) See Application Circuit Figure TBD
(2) Expected performance with external resistive load on output buffer. By using an external tuned load it is possible to further improve harmonics suppression.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

supply voltage = 4.5 V to 5.25 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PFD Charge Pump							
	PFD frequency					30	MHz
	Charge pump current	SPI programmable			5.6		mA
RF Input Parameters							
f_I	RF input frequency			400		2500	MHz
	RF input sensitivity			-5		5	dBm
Noise Characteristics							
	VCO phase noise, Free running VCO direct output	f_{VCO} = 1800 MHz, f_O = 1800 MHz	100 kHz offset		-120		dBc/Hz
			600 kHz offset		-138.5		
			1 MHz offset		-143.5		
			6 MHz offset		-157		
			10 MHz offset		-159		
	VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1800 MHz, f_O = 900 MHz	100 kHz offset		-126.5		dBc/Hz
			600 kHz offset		-145		
			1 MHz offset		-150		
			6 MHz offset		-156.5		
			10 MHz offset		-159		
	VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1800 MHz, f_O = 450 MHz	100 kHz offset		-131		dBc/Hz
			600 kHz offset		-149.5		
			1 MHz offset		-154		
			6 MHz offset		-159		
			10 MHz offset		-159		
	VCO phase noise, Closed loop phase noise direct output(3)(4)	f_{VCO} = 1800 MHz, f_O = 1800 MHz	1 kHz offset		-84		dBc/Hz
			600 kHz offset		-138.5		
			1 MHz offset		-143.5		
			10 MHz offset		-159		
	RMS phase error Closed loop phase noise direct output	100 Hz to 10 MHz			1°		
	VCO phase noise, Closed loop phase noise divide-by-2 output(3)(5)	f_{VCO} = 1800 MHz, f_O = 900 MHz	1 kHz offset		-94		dBc/Hz
			600 kHz offset		-145		
			1 MHz offset		-150		
			10 MHz offset		-159		
	RMS phase error Closed loop phase noise divide-by-2	100 Hz to 10 MHz			0.35°		
	VCO phase noise, Closed loop phase noise divide-by-4 output(3)(6)	f_{VCO} = 1800 MHz, f_O = 1800 MHz	1 kHz offset		-100		dBc/Hz
			600 kHz offset		-149.5		
			1 MHz offset		-154		
			10 MHz offset		-159		
	RMS phase error Closed loop phase noise divide-by-4 output	100 Hz to 10 MHz			0.19°		
	VCO gain	VCO free running			30		MHz/V
	Reference spur				-80		dBc

(3) See Application Circuit Figure TBD
(4) PFD = 200 kHz, Loop Filter BW = 15 kHz, Output frequency step = 200 kHz.
(5) PFD = 400 kHz, Loop Filter BW = 15 kHz, Output frequency step = 200 kHz.
(6) PFD = 400 kHz, Loop Filter BW = 15 kHz, Output frequency step = 100 kHz.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

supply voltage = 4.5 V to 5.25 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Interface						
V_{IH}	High-level input voltage		2.5		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage		$0.8V_{CC}$			V
V_{OL}	Low-level output voltage				$0.2V_{CC}$	V

TIMING REQUIREMENTS

supply voltage = 4.5 V to 5.25 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{su1}	Setup time, data		10			ns
t_h	Hold time, data		10			ns
t_w	Pulse width, STROBE		20			ns
t_{su2}	Setup time, STROBE		10			ns

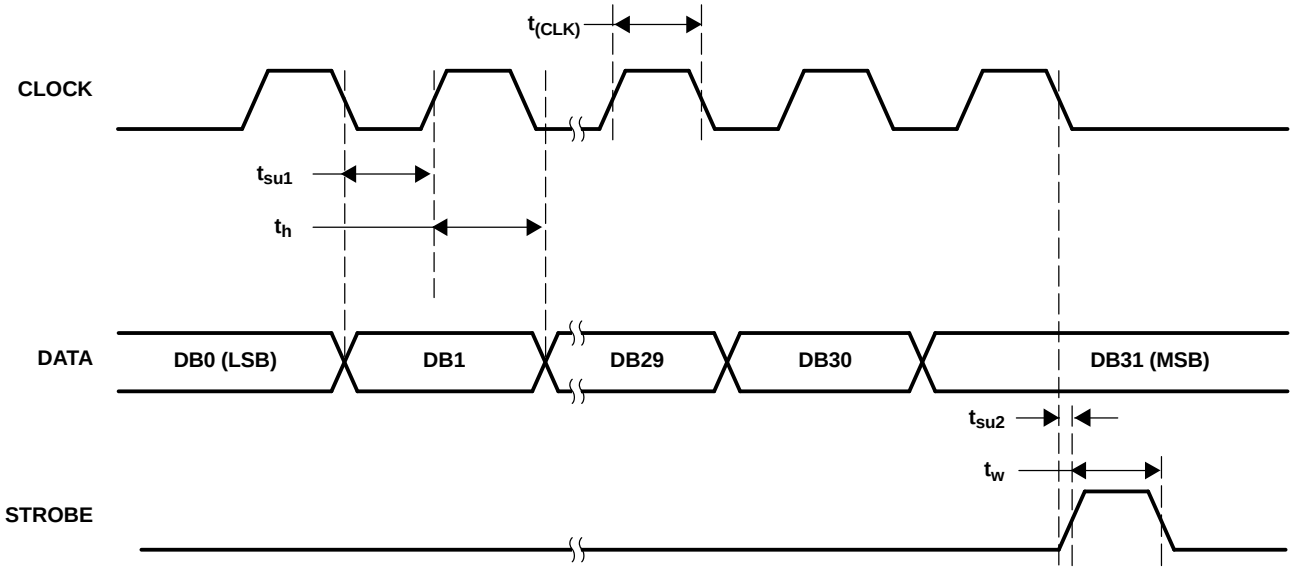


Figure 1. Serial Programming Timing Diagram

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF3761 features a 3-wire serial programming interface that controls an internal 32-bit shift register. There are a total of 3 signals that need to be applied: the CLOCK (pin 3), the serial DATA (pin 4) and the STROBE (pin 5). The DATA (DB0-DB31) is loaded LSB first and is read on the rising edge of the CLOCK. The STROBE is asynchronous to the CLOCK and at its rising edge the data in the shift register gets loaded onto the selected internal register. The first four bits (DB0-DB3) are the address to select the available internal registers.

PRODUCT PREVIEW

Table 2. Register 1: Device Setup

Register 1 Mapping				
Data Field	**DB31**	FULL_CAL_REQ	This is a read only bit, that indicates if a power-up cal is required	0 power-up cal is not needed 1 power-up cal is needed
	DB30	CP_TEST	Up and down pulse charge pump test	1 Test enabled
	DB29	TRIS_CP	High-impedance state charge pump output	1 CP high-impedance state
	DB28	PFD_POL	Select Polarity of PFD	0 negative 1 positive
	DB27	ABPW1	ABPW<1,0>: antibacklash pulse width	00 1.5ns delay 01 0.9ns delay 10 3.8ns delay 11 2.7ns delay
	DB26	ABPW0		
	DB25	RDIV_13	14-bit reference clock divider	RDIV<13,0>:00...01: div by 1 RDIV<13,0>:00...10: div by 2 RDIV<13,0>:00...11: div by 3
	DB24	RDIV_12		
	DB23	RDIV_11		
	DB22	RDIV_10		
	DB21	RDIV_9		
	DB20	RDIV_8		
	DB19	RDIV_7		
	DB18	RDIV_6		
	DB17	RDIV_5		
	DB16	RDIV_4		
	DB15	RDIV_3		
	DB14	RDIV_2		
	DB13	RDIV_1		
	DB12	RDIV_0		
	DB11	PD_BUFOUT	If Bit10 = 0 then it controls power down of output buffer	<DB10:11>: 00 default; output buffer on 01 output buffer off 1x output buffer on/off controlled by OUTBUF_EN pin
	DB10	OUTBUF_EN_SEL	Select Output Buffer enable control: 0 internal 1 through OUTBUF_EN pin	
	DB9	OUT_MODE_1	OUTBUFMODE<1,0>: Selection of RF output buffer division ratio	00 Divide by 1 01 Divide by 2 10 Divide by4
	DB8	OUT_MODE_0		
	DB7	ICP2	ICP<2,0>: select Charge Pump current (1 mA step)	
	DB6	ICP1		
	DB5	ICP0		
	DB4	RESET	Registers reset	
Address Bits	**DB3**	0		
	DB2	0		
	DB1	0		
	DB0	0		

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OUT_MODE<1,0>: TRF3761 has an optional divider by 2 or 4 output, that is selectable by programming bits <OUT_MODE_1, OUT_MODE_0> of register 1 (see Table 2).

Up and Down Pulse Test: by setting bit DB30 to 1 it is possible to test the PFD up or down pulses.

Charge Pump Tristate: if bit DB29 is set to 1, the Charge Pump output goes in tristate. For normal operation DB29 has to be set to 0.

Anti-Backlash Pulse: bits <DB27, DB26> can be used to program the width of the anti-backlash pulses of the PFD. The user can select one of the following values: 0.9 ns, 1.5 ns, 2.7 ns and 3.8 ns.

PFD Polarity: bit DB28 of register 0 sets the polarity of the PFD: a 0 select a negative polarity whereas a 1 gives a positive one. By choosing the correct polarity, TRF3761 can work with external VCO having both positive and negative Kv.

Reference Divider: a 14-bit word is used to program the R divider for the reference signal, DB25 is the MSB while DB12 is the LSB.

Charge Pump Current: bits <DB7, DB5> are used to set the charge pump current.

OUTBUF_EN_SEL: output buffer on/off state can be controlled trough serial interface or external pin. If bit DB10 is 0 (default state) then output buffers state is elected through bit DB11. If DB10 is 1, then the buffers on/off are directly controlled by the OUTBU_EN pin.

Reset: setting bit DB4 to 1, all registers are reset to default values.

Table 3. Register 2: VCO Calibration

Register 2 Mapping				
Data Field	**DB31**	START_CAL	Start Calibration	1 Start Cal
	DB30	FOUT12	VCO frequency in MHz	
	DB29	FOUT11		
	DB28	FOUT10		
	DB27	FOUT9		
	DB26	FOUT8		
	DB25	FOUT7		
	DB24	FOUT6		
	DB23	FOUT5		
	DB22	FOUT4		
	DB21	FOUT3		
	DB20	FOUT2		
	DB19	FOUT1		
	DB18	FOUT0		
	DB17	REF_FRAC6	Reference Frequency in MHz (Fraction part)	0000000 = X.00 MHz 0000001 = X.01 MHz 0000010 = X.02 MHz . . . . . 1100011 = X.99 MHz
	DB16	REF_FRAC5		
	DB15	REF_FRAC4		
	DB14	REF_FRAC3		
	DB13	REF_FRAC2		
	DB12	REF_FRAC1		
	DB11	REF_FRAC0		
	DB10	REF6	Reference Frequency in MHz (Integer part)	0001010 =10 MHz 0001011 =11 MHz . . . . . 1101000 = 104 MHz
	DB9	REF5		
	DB8	REF4		
	DB7	REF3		
	DB6	REF2		
	DB5	REF1		
	DB4	REF0		
Address Bits	**DB3**	0		
	DB2	0		
	DB1	0		
	DB0	1		

Reference Frequency: the 14-bit <DB17, DB4> are used to specify the input reference frequency as multiple of 10 KHz. Bits <DB17,DB11> specify the integer part of the Reference frequency expressed in MHz. Bits <DB10,DB4> are used to set the fraction part. Those values are then used during the calibration of the internal VCO.

Start Calibration: a 1 in DB31 starts the internal VCO calibration. When the calibration is done, this bit is internally reset to 0.

FOUT<12,0>: This 13 bit words <DB30,DB18> specifies the VCO output frequency in MHz. If output frequency is not a integer multiple of MHz, this value has to be approximated to the closest integer MHz.

Table 4. Register 3: A and B Counters

Register 3 Mapping				
Data Field	**DB31**	Rsrv	Reserved	
	DB30	Rsrv	Reserved	
	DB29	START_LK	Lock PLL to frequency	1 active
	DB28	TEST_MUX_3		0110 = LOCK_DETECT enabled
	DB27	TEST_MUX_2		
	DB26	TEST_MUX_1		
	DB25	TEST_MUX_0		
	DB24	B_12	13-Bit B counter	
	DB23	B_11		
	DB22	B_10		
	DB21	B_9		
	DB20	B_8		
	DB19	B_7		
	DB18	B_6		
	DB17	B_5		
	DB16	B_4		
	DB15	B_3		
	DB14	B_2		
	DB13	B_1		
	DB12	B_0		
	DB11	A_5	6-bit A counter	
	DB10	A_4		
	DB9	A_3		
	DB8	A_2		
	DB7	A_1		
	DB6	A_0		
	DB5	PRESC_MOD1	Dual-Modulus Prescaler Mode	<B5,B4>:00 8/9 <B5,B4>:01 16/17 <B5,B4>:00 32/33 <B5,B4>:00 64/65
	DB4	PRESC_MOD0		
Address Bits	**DB3**	0		
	DB2	0		
	DB1	1		
	DB0	0		

B<12,0>: This 13 bit words <DB24,DB12> controls the value of the B counter of the N divider. The valid range is from 3 to 8191.

A<5,0>: The 6 bits <DB11,DB6> control the value of the A counter. The valid range is from 0 to 63.

PRESC_MOD<1,0>: The bits <DB5,DB4> define the mode of the dual modulus prescaler according the table 4

START_LK: TRF3761 doesnt load the serial interface registers values into the dividers registers till bit DB29 of register 3 is set to 1. After TRF3761 is locked to the new frequency, bit DB29 is internally reset to 0.

TYPICAL CHARACTERISTICS

Open Loop VCO Phase Noise

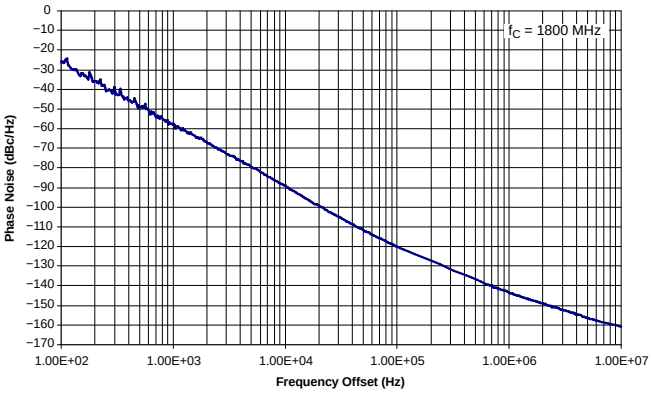


Figure 2.

Closed Loop VCO Phase Noise

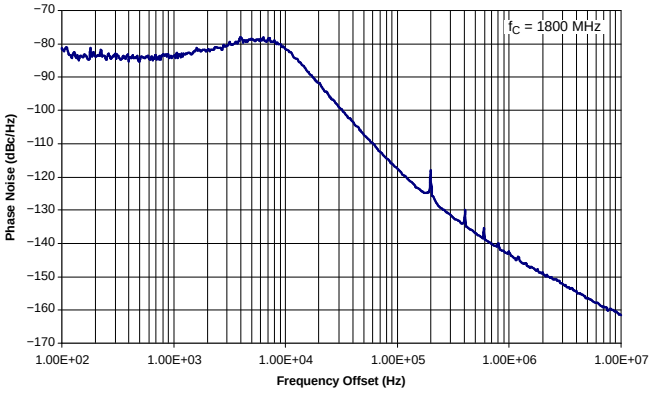


Figure 3.

Open Loop VCO Phase Noise

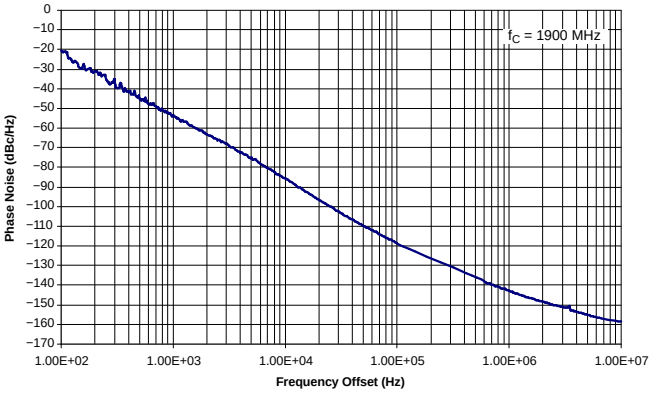


Figure 4.

Closed Loop VCO Phase Noise

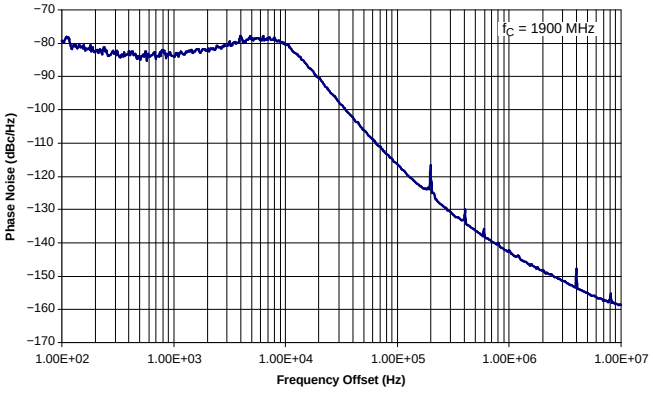


Figure 5.

Open Loop VCO Phase Noise

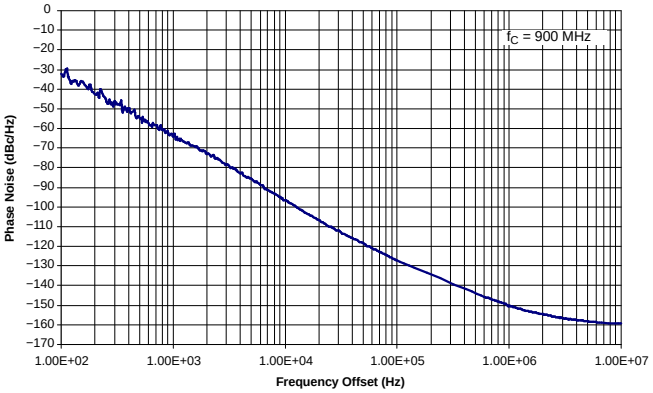


Figure 6.

Closed Loop VCO Phase Noise

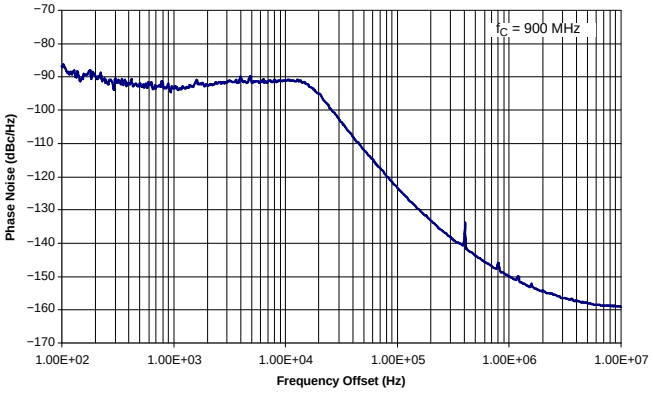


Figure 7.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

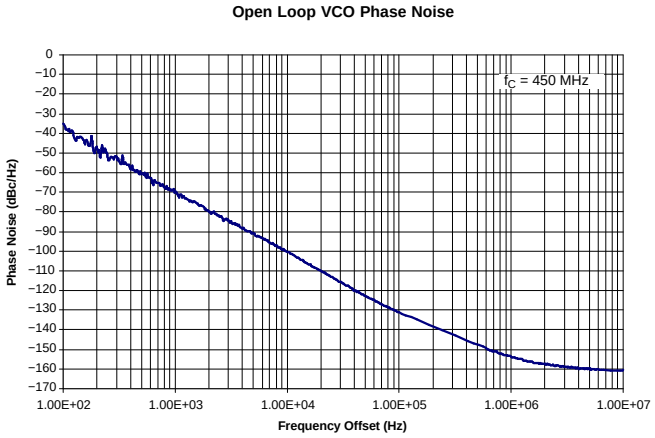


Figure 8.

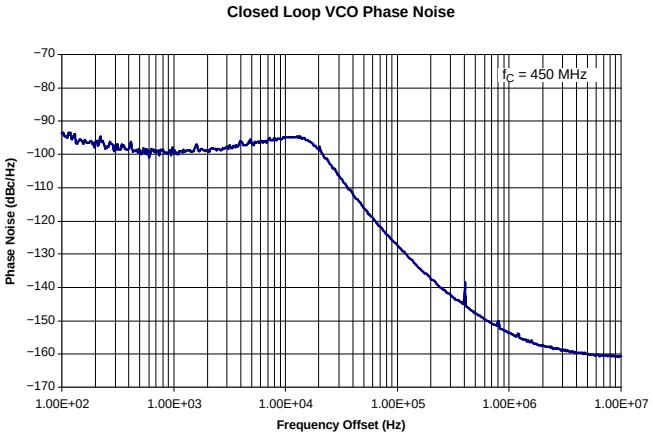


Figure 9.

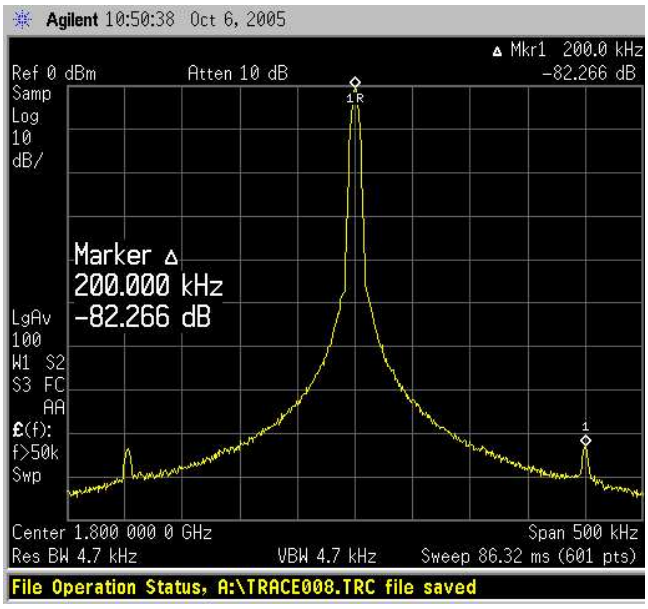


Figure 10. Direct Output: PFD Frequency Spurs

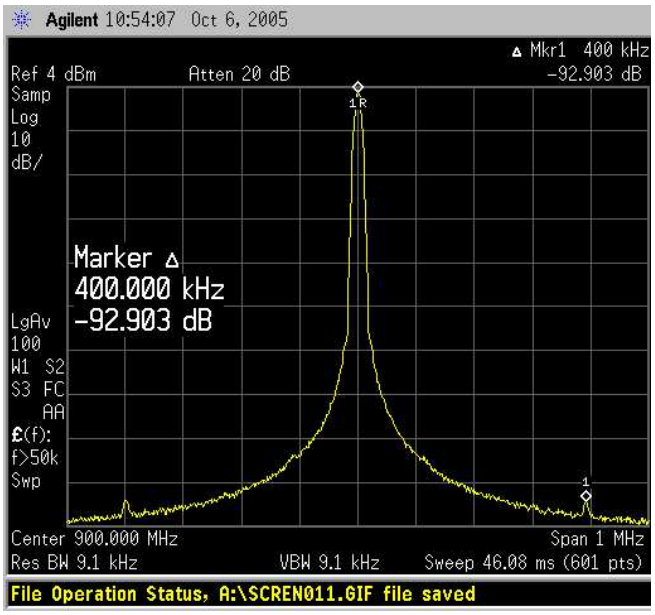


Figure 11. Divide-By-2 Output: PFD Frequency Spurs

TYPICAL CHARACTERISTICS (continued)

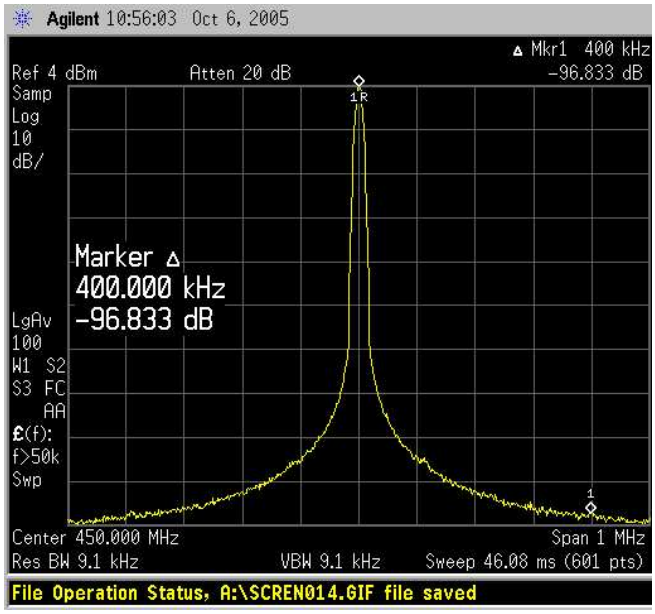


Figure 12. Divide-By-4 Output: PFD Frequency Spurs

FUNCTIONAL DESCRIPTION

VCO

TRF3761 integrates a high performance LC tank voltage controlled oscillator (VCO). For each of the devices of TRF3761 family, the inductance and capacitance of the tank are optimized to yield best phase noise performance. The VCO output is fed externally and to the prescaler through a series of very low noise buffers, that greatly reduce the effect of load pulling onto the VCO.

Divider by 2, by 4, and Output Buffer

To extend the frequency coverage the TRF3761 integrates a divider by 2 and by 4 with very low noise floor. The VCO signal is fed externally through a final open collector differential output buffer. This buffer is able to provide up to 3dBm (typical) of power into a 200 ohm differential resistive load. The open collector structure gives the flexibility to choose different loads configuration to meet different requirements.

Prescaler Stage

This stage divides down the VCO frequency before the A and B counters. This is a dual-modulus prescaler and the user can select any of the following settings: 8/9, 16/17, 32/33, and 64/65.

A and B Counter Stage

The TRF3761 includes a 6-bit A counter and a 13-bit B counter that operate on the output of the prescaler. The A counter can take values from 0 to 63, while the B counter can take values from 3 to 8191. Also, the value for the B counter has to be greater than or equal to the value for the A counter. The A and B counter with the Prescaler stage create the VCO N-divider.

R Divider

TRF3761 includes a 14-bit R divider that allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

FUNCTIONAL DESCRIPTION (continued)

Phase Frequency Detector (PFD) and Charge Pump Stage

The outputs of the R divider and the N counter are fed into the PFD stage, where the two signals are compared in frequency and phase. The TRF3761 features an anti-backlash pulse, whose width is controllable by the user through the serial programming interface. The PFD feeds the charge pump, whose output current pulses are fed into an external loop filter, which eventually produces the tuning voltage needed to control the integrated VCO to the desired frequency.

APPLICATION INFORMATION

Initial Calibration

The integrated high performance VCO requires an internal frequency calibration at power up. To perform such calibration the following procedure is recommended. After the power supply has been applied and the input reference frequency is stable, turn on TRF3761 through the chip enable pin (CHIP_EN, pin 2). Setup the device through register 1. Then the calibration can start. To initiate the calibration procedure, program register 2 as follows:

- Use bits <DB17, DB4> of register 2 to specify the input reference frequency in MHz. The value is split into integer and fraction part. For example to insert a f_{REF} of 30.72 MHz, set:
  - <DB17, DB11> (integer part) equal to 0011110 (30) and
  - <DB10,DB4> (fraction part) equal to 1001000 (72).
- Set bit DB31 of register 2 to 1 to start the calibration.

The VCO calibration will run for 5ms. During the cal procedure it won't be possible to program register 2 and 3. At the end of the calibration, bit DB31 of register 2 will be internally reset to 0.

Synthesizing a Frequency

The TRF3761 is an integer-N PLL synthesizer, whose frequency can be programmed through the SPI by setting the values for the R divider, A and B counter. For a given reference frequency (f_{REFIN}), the users choice of the R divider yields the PFD frequency (f_{PFD}), which is the step by which the resultant output frequency can be incremented or decremented. The choice of prescaler, and A and B counters yields the frequency of the internal VCO as shown below. $f_{VCO} = f_{PFD}\ N = (f_{REFIN} / R)\ (A + P\ B)$

Application Schematic

Figure 13 shows a typical application schematic for the TRF3761. In this example the output signal is taken differential using from the 2 resistive pull-up resistors of the final output buffer. A single ended and tuned load configuration is also available.

The loop filter components shown in the application schematic are typical one used for the plots shown above. Those values can be optimized differently according to the requirements of the different applications.

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

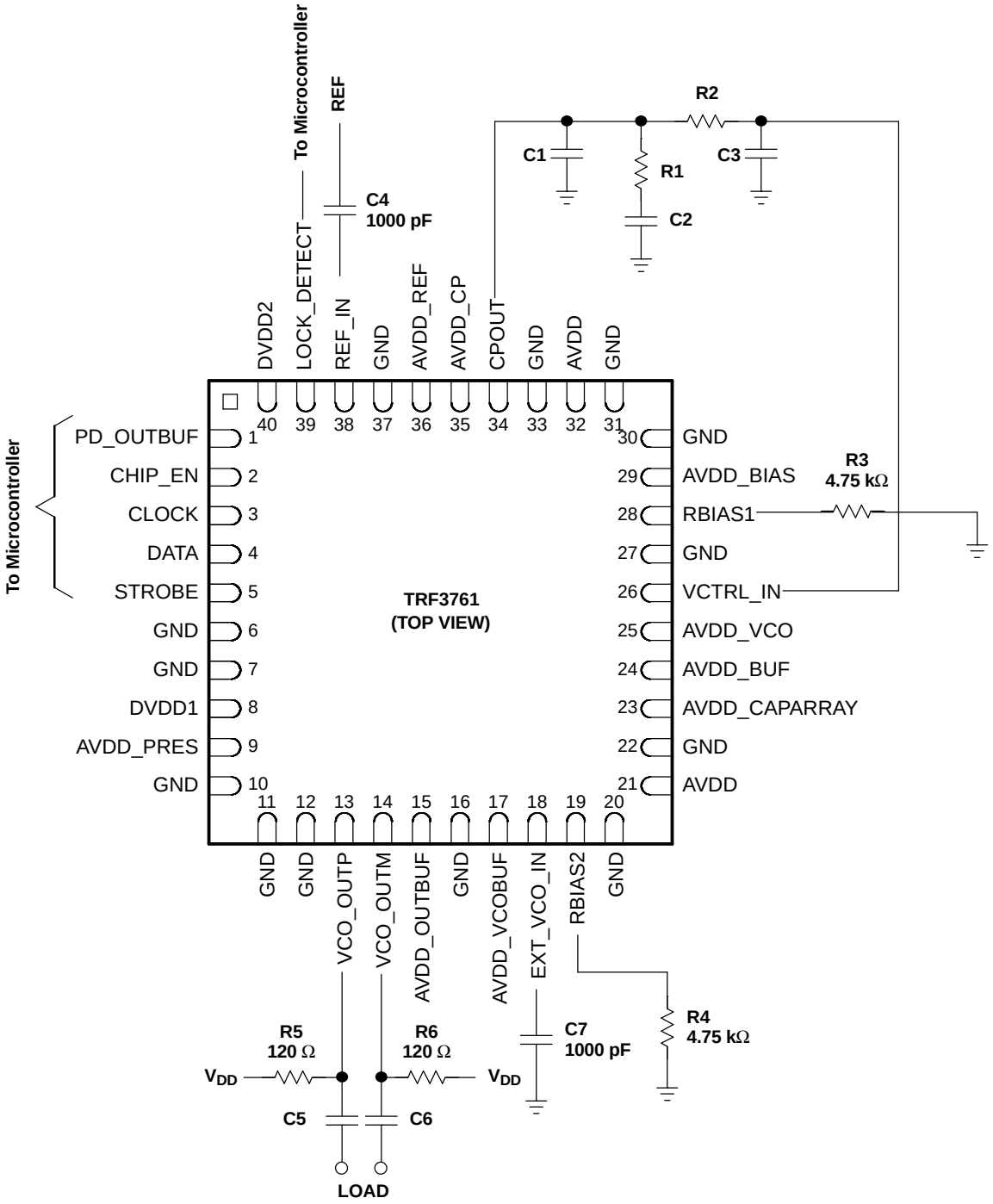


Figure 13. TRF3761 Application Schematic

PRODUCT PREVIEW

PACKAGING INFORMATION

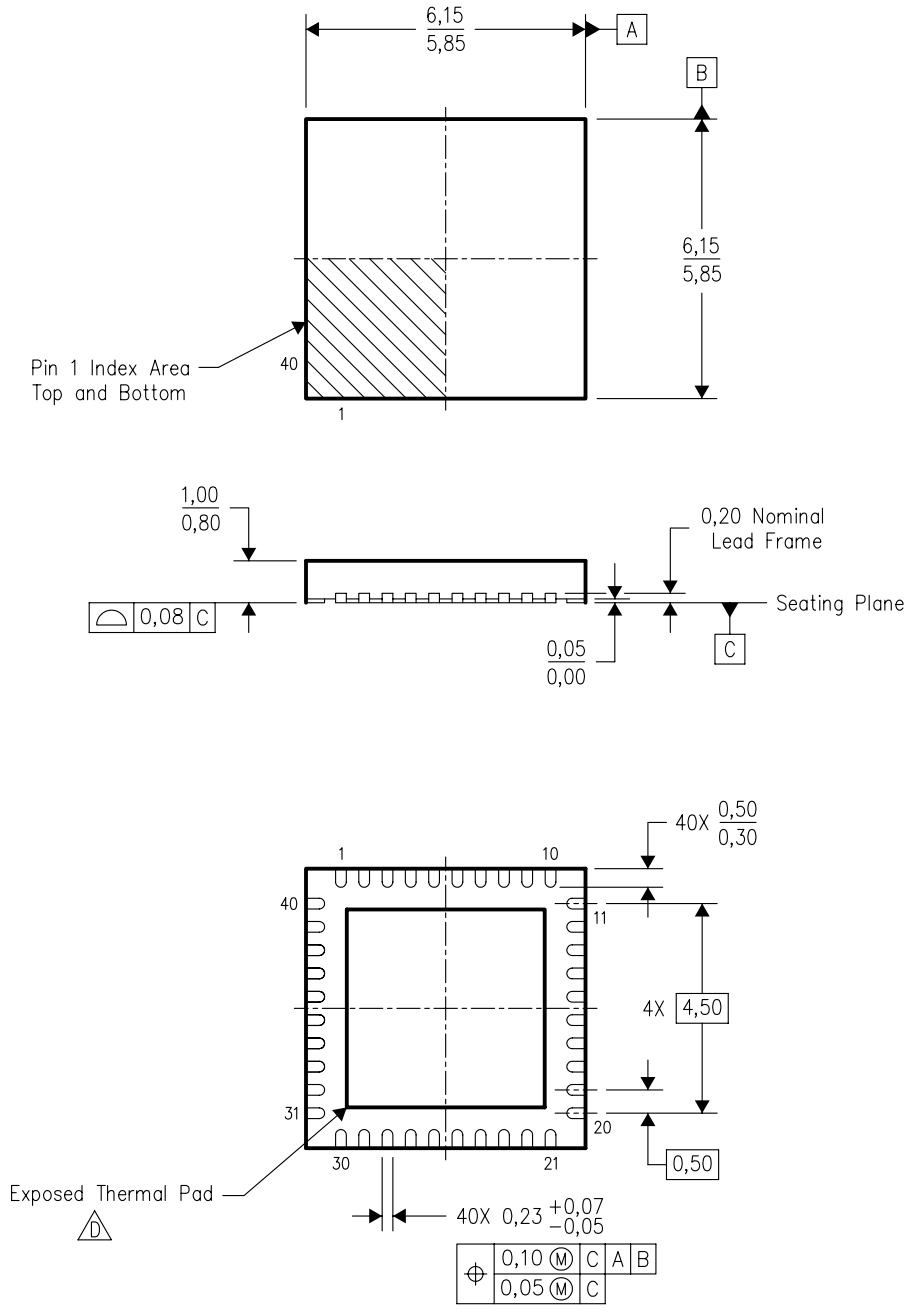
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRF3761IRHAR	PREVIEW	QFN	RHA	40	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RHA (S–PQFP–N40) PLASTIC QUAD FLATPACK



Bottom View

4204276/C 12/2004

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation VJJD–2.

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