

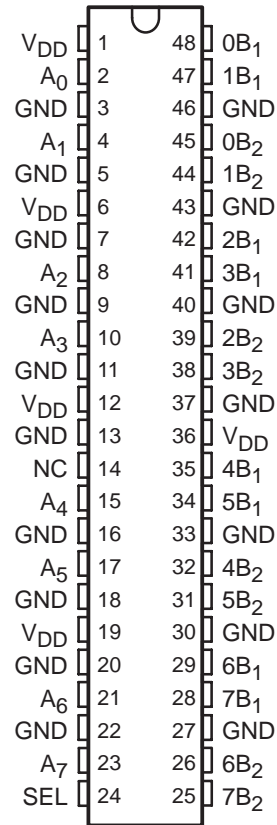
# TS3L301

## 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

SCDS178B – NOVEMBER 2004 – REVISED APRIL 2005

- **Wide Bandwidth (BW = 900 MHz Typ)**
- **Low Crosstalk ( $X_{TALK} = -41$  dB Typ)**
- **Low Bit-to-Bit Skew [ $t_{sk(o)} = 0.2$  ns Max]**
- **Low and Flat ON-State Resistance ( $r_{on} = 4 \Omega$  Typ,  $r_{on(Flat)} = 0.7 \Omega$  Typ)**
- **Low Input/Output Capacitance ( $C_{ON} = 10$  pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)**
- **$V_{DD}$  Operating Range From 3 V to 3.6 V**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **Suitable for 10/100/1000-Mbit Ethernet Signaling**
- **Applications**
  - 10/100/1000 Base-T Signal Switching
  - Differential (LVDS, LVPECL) Signal Switching
  - Digital Video Signal Routing
  - Notebook Docking Signal Routing
  - Hub and Router Signal Switching

**DGG OR DGV PACKAGE  
(TOP VIEW)**



NC – No internal connection

### description/ordering information

The TS3L301 is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input. The SEL input controls the data path of the multiplexer/demultiplexer.

The device provides a low and flat on-state resistance ( $r_{on}$ ) and an excellent on-resistance match. Low input/output capacitance, high-bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	TS3L301DGGR	TS3L301
	TVSOP – DGV	Tape and reel	TS3L301DGVR	TK301

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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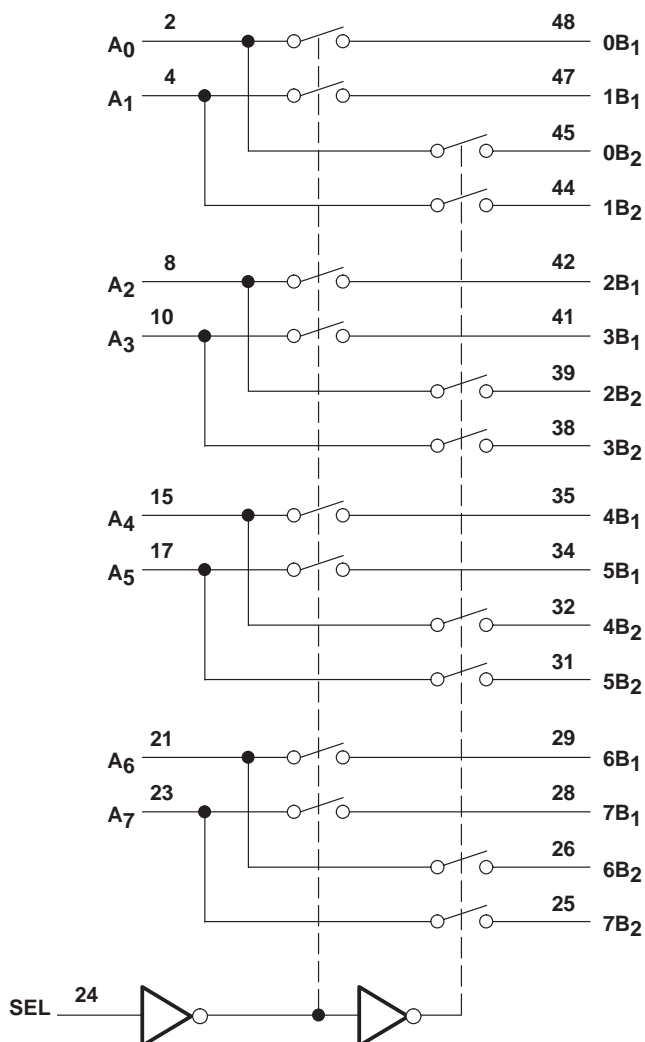
**FUNCTION TABLE**

INPUT SEL	INPUT/OUTPUT $A_n$	FUNCTION
L	$nB_1$	$A_n = nB_1$
H	$nB_2$	$A_n = nB_2$

**PIN DESCRIPTIONS**

PIN NAME	DESCRIPTION
$A_n$	Data I/Os
$nB_m$	Data I/Os
SEL	Select input

logic diagram (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{DD}$ .....	–0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) .....	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) .....	–0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ ) .....	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ ) .....	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) .....	±128 mA
Continuous current through $V_{DD}$ or GND terminals .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DGG package .....	70°C/W
DGV package .....	58°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground, unless otherwise specified.  
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .  
4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .  
5. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 6)**

	MIN	MAX	UNIT
$V_{DD}$ Supply voltage	3	3.6	V
$V_{IH}$ High-level control input voltage (SEL)	2	5.5	V
$V_{IL}$ Low-level control input voltage (SEL)	0	0.8	V
$V_{I/O}$ Input/output voltage	0	5.5	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 6: All unused control inputs of the device must be held at  $V_{DD}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

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electrical characteristics for 1000 Base-T ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V
$I_{IH}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{DD} = 0$ ,	$V_O = 0 \text{ to } 3.6 \text{ V}$ ,			1	$\mu\text{A}$
$I_{CC}$		$V_{DD} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,			250	$\mu\text{A}$
						600	$\mu\text{A}$
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$			2.5	pF
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,			3.5	pF
			Outputs open,			4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,			10	pF
			Outputs open,			10.9	pF
$r_{on}$		$V_{DD} = 3 \text{ V}$	$1.5 \text{ V} \leq V_I \leq V_{DD}$ ,			4	$\Omega$
						8	$\Omega$
$r_{on(Flat)}^\ddagger$		$V_{DD} = 3 \text{ V}$	$V_I = 1.5 \text{ V}$ and $V_{DD}$ ,			0.7	$\Omega$
$\Delta r_{on}^\S$		$V_{DD} = 3 \text{ V}$ ,	$1.5 \text{ V} \leq V_I \leq V_{DD}$ ,			0.2	$\Omega$
						1.2	$\Omega$

$V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.

† All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡  $r_{on(Flat)}$  is the difference of  $r_{on}$  in a given channel at specified voltages.

§  $\Delta r_{on}$  is the difference of  $r_{on}$  from center (A4, A5) ports to any other port.

electrical characteristics for 10/100 Base-T ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V
$I_{IH}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	SEL	$V_{DD} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{DD} = 0$ ,	$V_O = 0 \text{ to } 3.6 \text{ V}$ ,			1	$\mu\text{A}$
$I_{CC}$		$V_{DD} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,			250	$\mu\text{A}$
						600	$\mu\text{A}$
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$			2.5	pF
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,			3.5	pF
			Outputs open,			4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,			10	pF
			Outputs open,			10.9	pF
$r_{on}$		$V_{DD} = 3 \text{ V}$	$1.25 \text{ V} \leq V_I \leq V_{DD}$ ,			4	$\Omega$
						8	$\Omega$
$r_{on(Flat)}^\ddagger$		$V_{DD} = 3 \text{ V}$	$V_I = 1.25 \text{ V}$ and $V_{DD}$ ,			0.7	$\Omega$
$\Delta r_{on}^\S$		$V_{DD} = 3 \text{ V}$ ,	$1.25 \text{ V} \leq V_I \leq V_{DD}$ ,			0.2	$\Omega$
						1.2	$\Omega$

$V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.

† All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡  $r_{on(Flat)}$  is the difference of  $r_{on}$  in a given channel at specified voltages.

§  $\Delta r_{on}$  is the difference of  $r_{on}$  from center (A4, A5) ports to any other port.



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**WITH LOW AND FLAT ON-STATE RESISTANCE**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $R_L = 200\ \Omega$ ,  $C_L = 10\text{ pF}$  (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{pd}^\ddagger$	A or B	B or A		0.25		ns
$t_{PZH}$ , $t_{PZL}$	SEL	A or B	1.5		11.5	ns
$t_{PHZ}$ , $t_{PLZ}$	SEL	A or B	1		8.5	ns
$t_{sk(o)}^\S$	A or B	B or A		0.1	0.2	ns
$t_{sk(p)}^\parallel$				0.1	0.2	ns

† All typical values are at  $V_{DD} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

§ Output skew between center port (A<sub>4</sub> to A<sub>5</sub>) to any other port

¶ Skew between opposite transitions of the same output in a given device  $|t_{PHL} - t_{PLH}|$

dynamic characteristics over recommended operating free-air temperature range,  
 $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

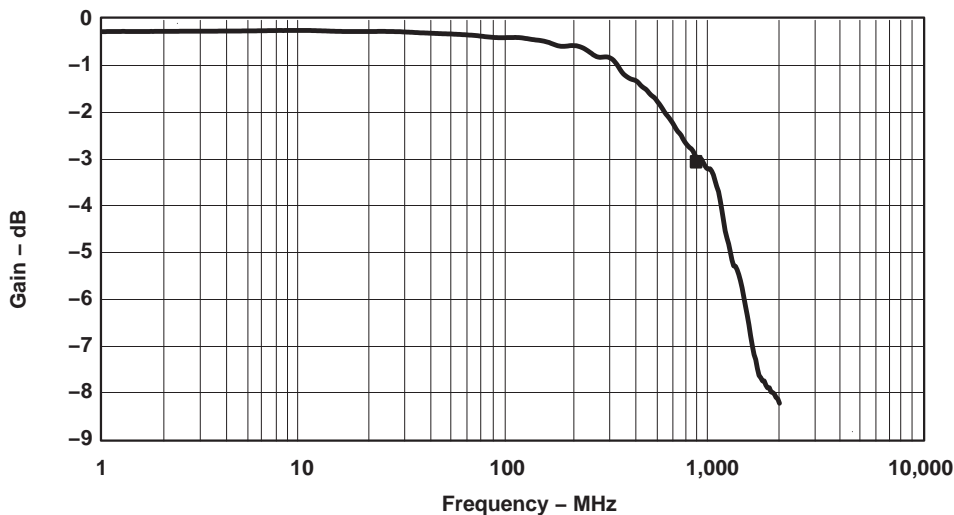
PARAMETER	TEST CONDITIONS			TYP†	UNIT
X <sub>TALK</sub>	$R_L = 100\ \Omega$ ,	$f = 250\text{ MHz}$ ,	See Figure 7	-41	dB
O <sub>IRR</sub>	$R_L = 100\ \Omega$ ,	$f = 250\text{ MHz}$ ,	See Figure 8	-39	dB
BW	$R_L = 100\ \Omega$ ,	See Figure 6		900	MHz

† All typical values are at  $V_{DD} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

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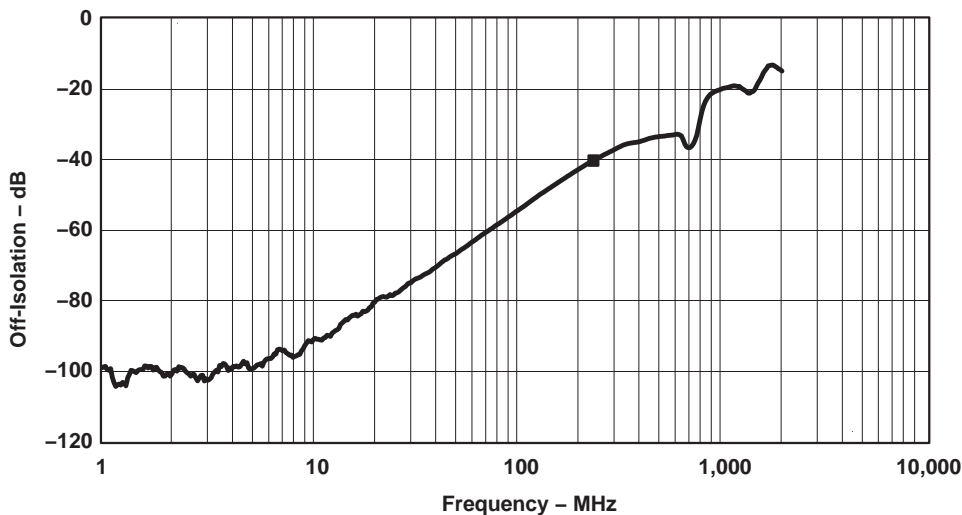
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**OPERATING CHARACTERISTICS**



■ Gain at 900 MHz, -3 dB

**Figure 1. Gain vs Frequency**



■ Off-Isolation at 250 MHz, -39 dB

**Figure 2. Off-Isolation vs Frequency**

OPERATING CHARACTERISTICS (continued)

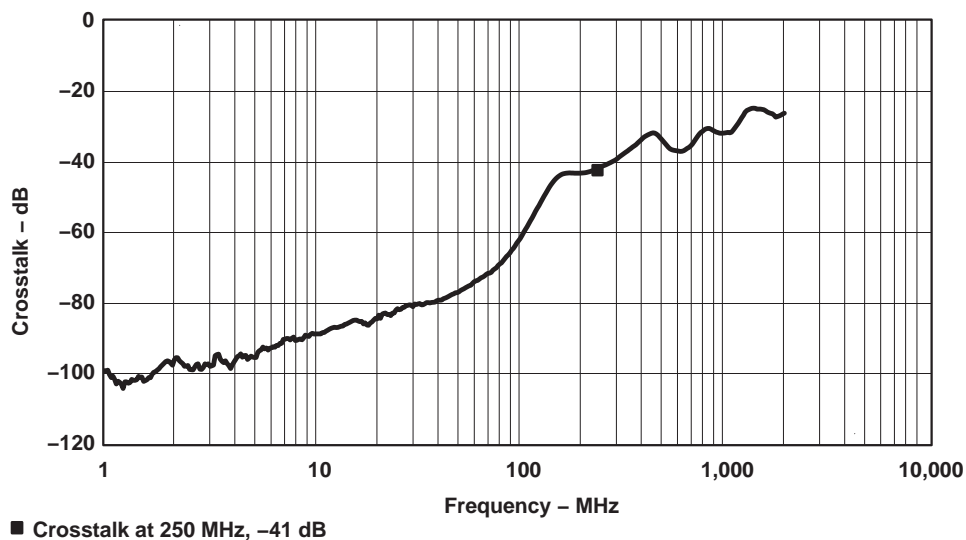
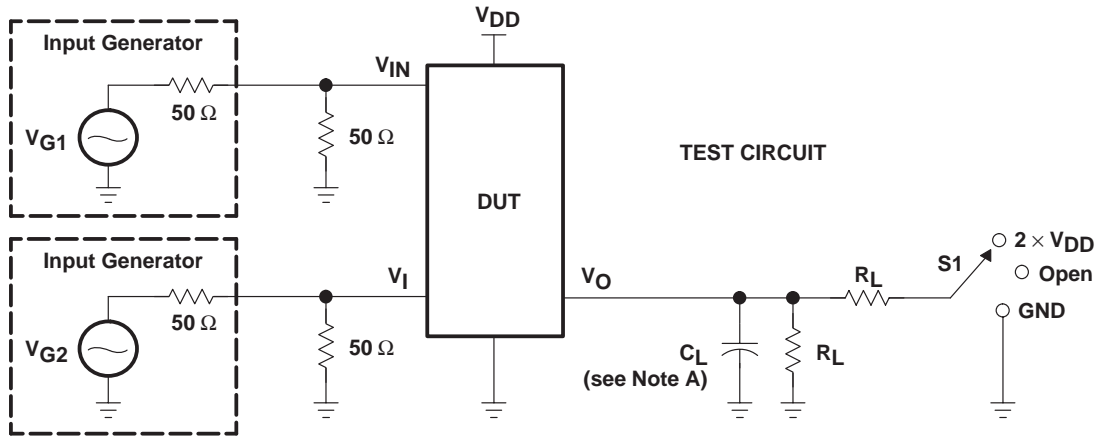


Figure 3. Crosstalk vs Frequency

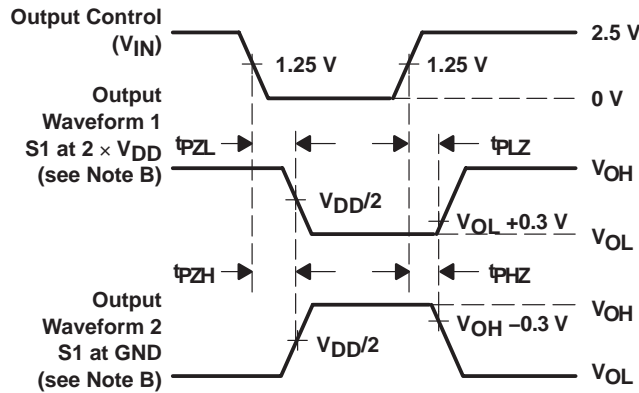
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**PARAMETER MEASUREMENT INFORMATION**  
**FOR ENABLE AND DISABLE TIMES**



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>DD</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>DD</sub>	10 pF	0.3 V



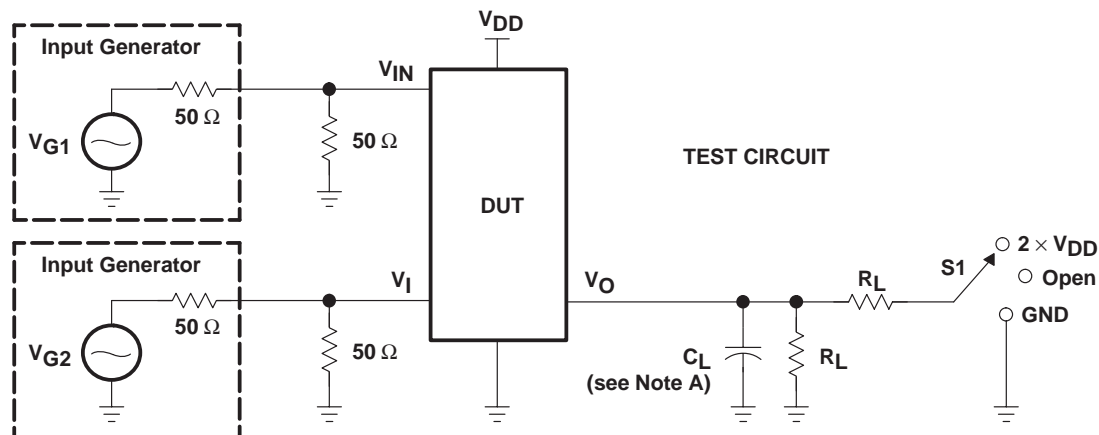
**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

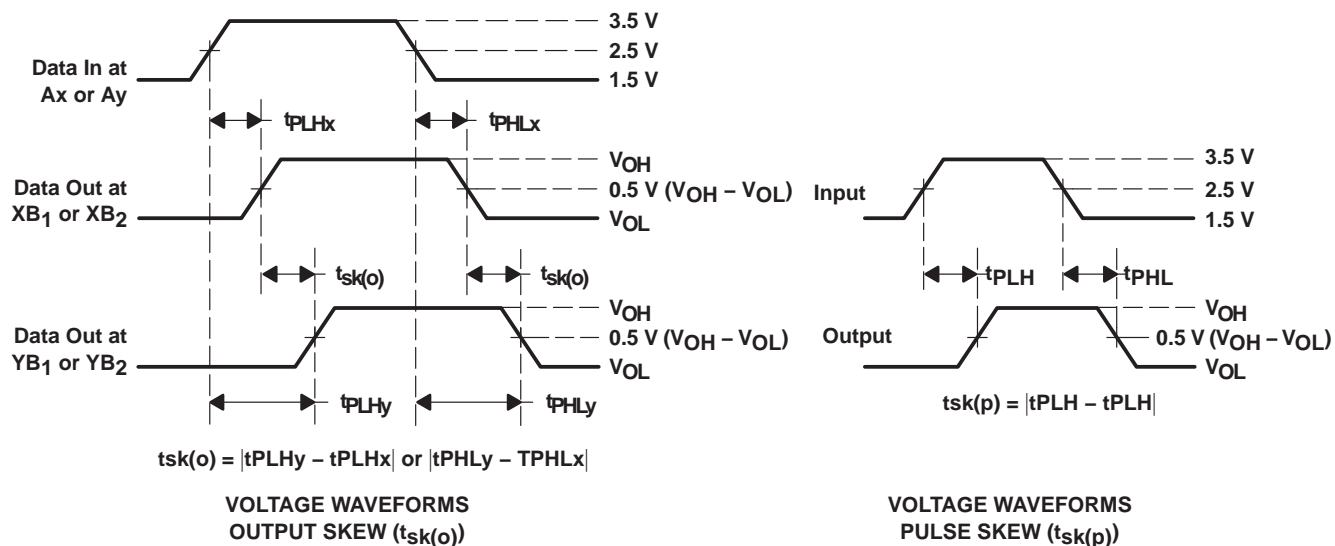
**Figure 4. Test Circuit and Voltage Waveforms**



**PARAMETER MEASUREMENT INFORMATION  
 FOR SKEW**



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF	
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF	



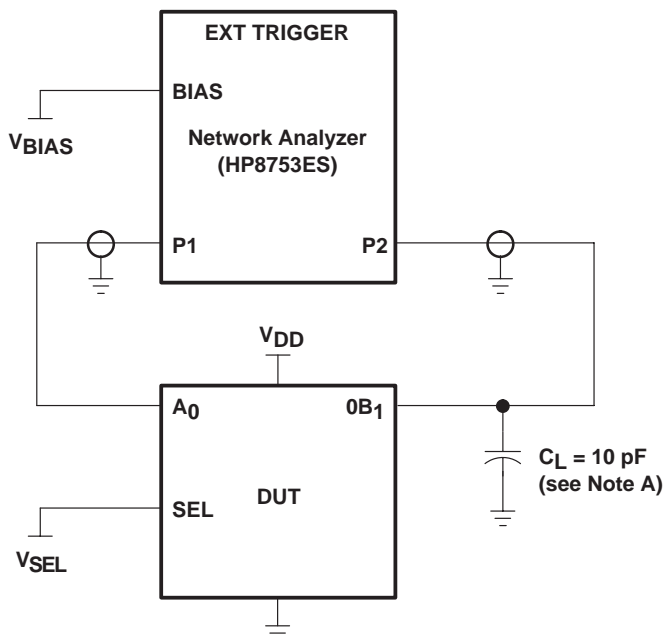
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

**Figure 5. Test Circuit and Voltage Waveforms**

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## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and jig capacitance.

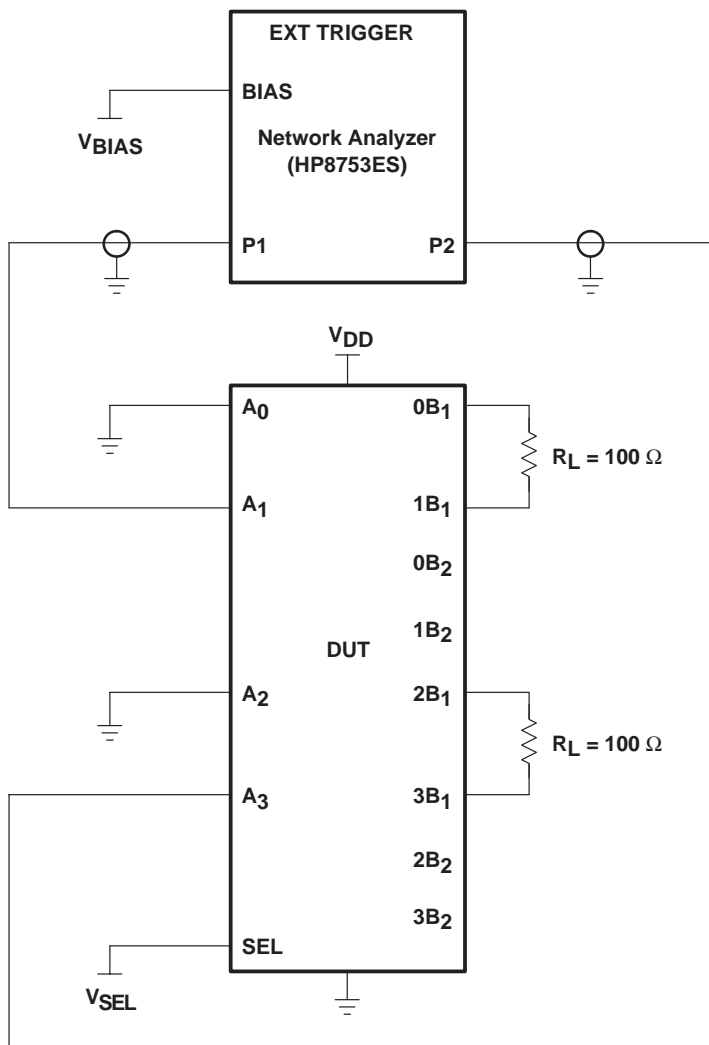
**Figure 6. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $OB_1$ . All unused analog I/O ports are left open.

### HP8753ES setup

Average = 4  
RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
ST = 2 s  
P1 = 0 dBm

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 7. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL} = 0$  and  $A_1$  is the input, the output is measured at  $A_3$ . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

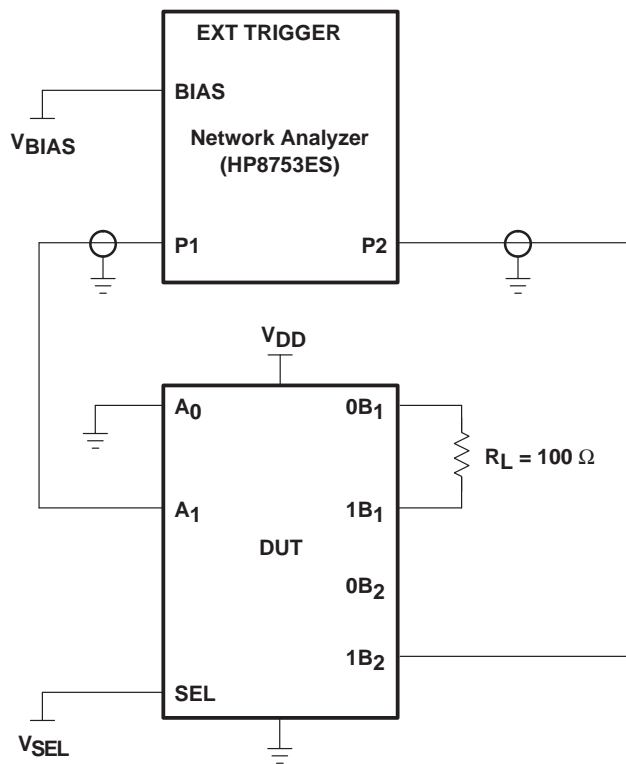
**HP8753ES setup**

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35$  V
- ST = 2 s
- P1 = 0 dBm

# TS3L301 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LOW AND FLAT ON-STATE RESISTANCE

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 8. Test Circuit for Off Isolation ( $O_{IRR}$ )**

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = GND$  and  $A_1$  is the input, the output is measured at  $1B_2$ . All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

### HP8753ES setup

Average = 4  
RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
ST = 2 s  
P1 = 0 dBm

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS3L301DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TS3L301DGVR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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