SSTU32865

1.8 V 28-bit 1:2 registered buffer with parity for DDR2 RDIMM applications

Rev. 02 — 28 September 2004 Product data sheet

1. General description

The SSTU32865 is a 1.8 V 28-bit 1:2 register specifically designed for use on two rank by four (2R × 4) and similar high-density Double Data Rate 2 (DDR2) memory modules. It is similar in function to the JEDEC-standard 14-bit DDR2 register, but integrates the functionality of the normally required two registers in a single package, thereby freeing up board real-estate and facilitating routing to accommodate high-density Dual In-line Memory Module (DIMM) designs.

The SSTU32865 also integrates a parity function, which accepts a parity bit from the memory controller, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active-LOW).

The SSTU32865 is packaged in a 160-ball, 12 × 18 grid, 0.65 mm ball pitch, thin profile fine-pitch ball grid array (TFBGA) package, which—while requiring a minimum 9 mm × 13 mm of board space—allows for adequate signal routing and escape using conventional card technology.

2. Features

- 28-bit data register supporting DDR2
- Fully compliant to JEDEC standard JESD82-9
- Supports 2 rank by 4 DIMM density by integrating equivalent functionality of two JEDEC-standard DDR2 registers (i.e. 2 × SSTU32864 or 2 × SSTU32866)
- Parity checking function across 22 input data bits
- Parity out signal
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-9 speed performance (1.8 ns max. single-bit switching propagation delay, 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports Stub Series Terminated Logic SSTL_18 data inputs
- Differential clock (CK and $\overline{\text{CK}}$) inputs
- Supports Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) switching levels on the control and $\overline{\text{RESET}}$ inputs
- Single 1.8 V supply operation
- Available in 160-ball 9 mm × 13 mm, 0.65 mm ball pitch TFBGA package

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3. Applications

- High-density (e.g. 2 rank by 4) DDR2 registered DIMMs
- DDR2 Registered DIMMs (RDIMM) desiring parity checking functionality

4. Ordering information

Table 1: Ordering information

Type number	Solder process	Package		
		Name	Description	Version
SSTU32865ET/G	Pb-free (SnAgCu solder ball compound)	TFBGA160	plastic thin fine-pitch ball grid array package; 160 balls; body 9 × 13 × 0.8 mm	SOT802-1
SSTU32865ET	SnPb solder ball compound	TFBGA160	plastic thin fine-pitch ball grid array package; 160 balls; body 9 × 13 × 0.8 mm	SOT802-1

5. Functional diagram

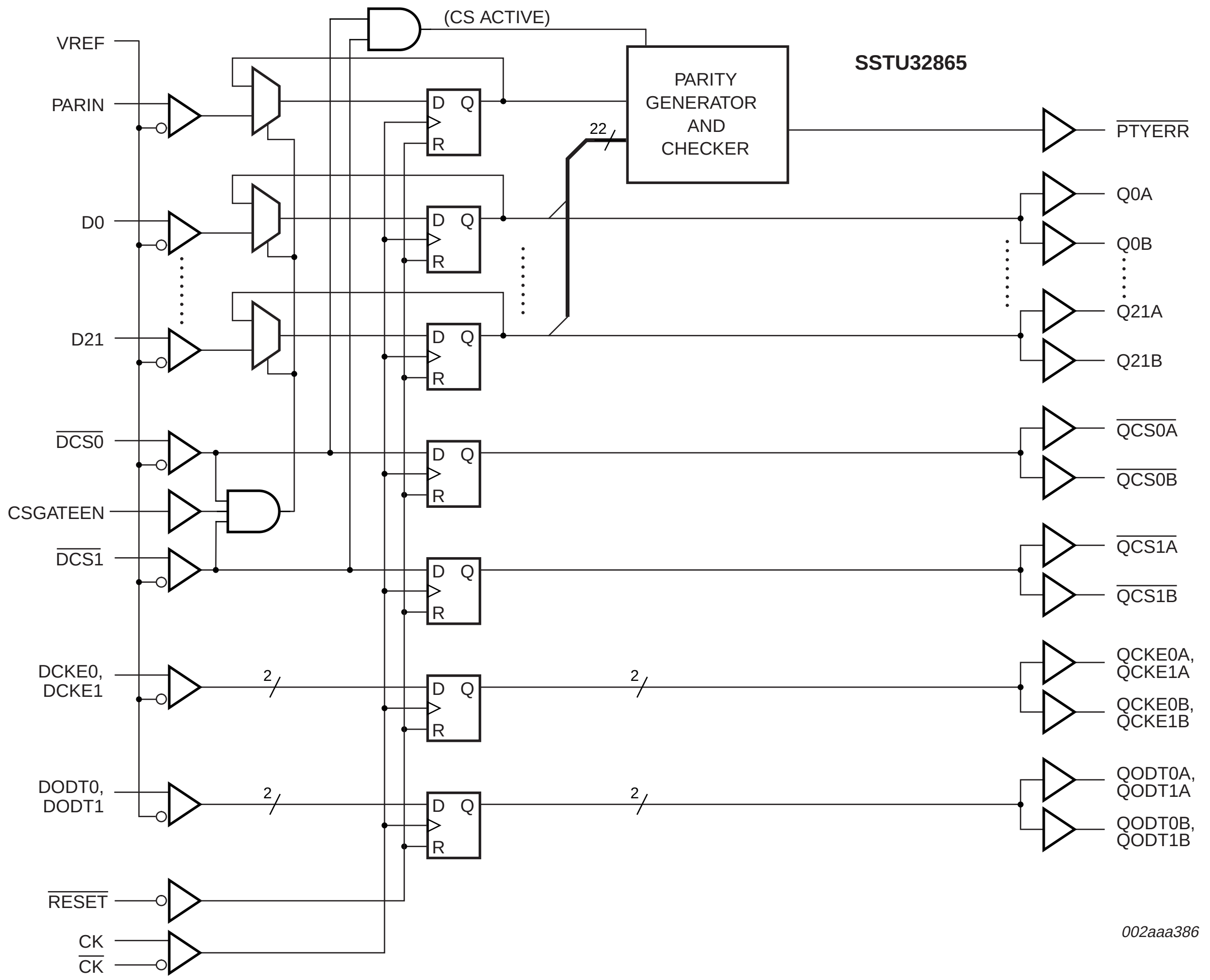

Fig 1. Functional diagram of SSTU32865

6. Pinning information

6.1 Pinning

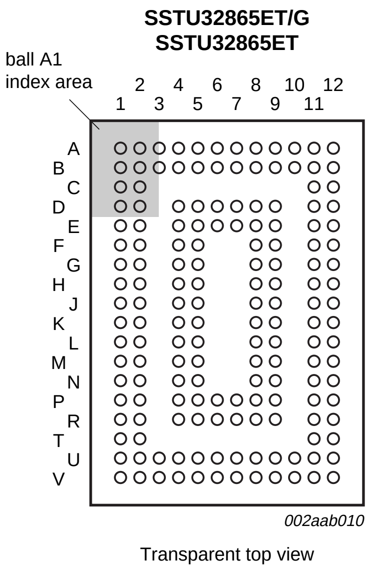

Fig 2. Pin configuration for TFBGA160

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	n.c.	PARIN	n.c.	n.c.	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	n.c.	n.c.	n.c.	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	n.c.	n.c.	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGATEEN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	$\overline{\text{DCS0}}$		GND	GND			VDDR	VDDR		$\overline{\text{QCS0B}}$	$\overline{\text{QCS0A}}$
K	$\overline{\text{CK}}$	$\overline{\text{DCS1}}$		VDDL	VDDL			GND	GND		$\overline{\text{QCS1B}}$	$\overline{\text{QCS1A}}$
L	$\overline{\text{RESET}}$	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	m.c.l.	$\overline{\text{PTYERR}}$	m.c.h.	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	m.c.l.	m.c.l.	n.c.	m.c.h.	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

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160-ball, 12 × 18 grid; top view.

An empty cell indicates no ball is populated at that grid point.

n.c. denotes a no-connect (ball present but not connected to the die).

m.c.l. denotes a pin that must be connected LOW.

m.c.h. denotes a pin that must be connected HIGH.

Fig 3. Ball mapping

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
Ungated inputs			
DCKE0, DCKE1	U1, U2	SSTL_18	DRAM function pins not associated with Chip Select.
DODT0, DODT1	T2, T1		
Chip Select gated inputs			
D0 to D21	M1, B1, B2, C1, C2, D2, D1, E1, E2, F2, M2, F1, G2, R1, L2, H2, N2, N1, G1, P1, R2, P2	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs			
$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	J2, K2	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGATEEN = HIGH) when at least one Chip Select input is LOW.
Re-driven outputs			
Q0A to Q21A	V11, F12, G12, V6, V9, H12, L12, V8, V12, N12, M12, P12, V7, V10, T12, R12, E12, A12, A10, A9, D12, A8	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Q0B to Q21B	U11, F11, G11, U6, U9, H11, L11, U8, U12, N11, M11, P11, U7, U10, T11, R11, E11, A11, B10, B9, D11, B8		
$\overline{\text{QCS0A}}$, $\overline{\text{QDS1A}}$, $\overline{\text{QCS0B}}$, $\overline{\text{QCS1B}}$	J12, K12, J11, K11		
QCKE0A, QCKE1A, QCKE0B, QCKE1B	A7, A6, B7, B6		
QODT0A, QODT1A, QODT0B, QODT1B	B12, C12, B11, C11		
Parity input			
PARIN	A3	SSTL_18	Parity input for the D0 to D21 inputs. Arrives one clock cycle after the corresponding data input.
Parity error			
$\overline{\text{PTYERR}}$	U4	open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{\text{PTYERR}}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR2 register with parity (in JEDEC definition).
Program inputs			
CSGATEEN	H1	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0 to D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0 to D21 inputs will be latched and redriven on every rising edge of the clock.

Table 2: Pin description *…continued*

Symbol	Pin	Type	Description
Clock inputs			
CK, $\overline{\mathrm{CK}}$	J1, K1	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs			
m.c.l.	U3, V2, V3		Must be connected to a logic LOW
m.c.h.	U5, V5		Must be connected to a logic HIGH.
$\overline{\mathrm{RESET}}$	L1	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{\mathrm{RESET}}$ also resets the $\overline{\mathrm{PTYERR}}$ signal.
VREF	A1, V1	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.
VDDL	D4, E4, E6, F4, G4, H4, K4, K5, N4, N5, P5, P6, R5, R6		power supply voltage
VDDR	E7, F8, F9, G8, G9, J8, J9, L8, L9, N8, N9, P7, P8		power supply voltage
GND	D5, D8, D9, E5, E8, E9, F5, G5, H5, H8, H9, J4, J5, K8, K9, L4, L5, M4, M5, M8, M9, P4, P9, R4, R7, R8, R9		ground
n.c.	A2, A4, A5, B3, B4, B5, D6, D7, V4		ball present but not connected to die

7. Functional description

7.1 Function table

Table 3: Function table (each flip-flop)

Inputs							Outputs [1]			
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CSGATEEN	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS0}$	$\overline{QCS1}$	QODTn, QCKEn
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

[1] Q_0 is the previous state of the associated output.

Table 4: Parity and standby function table

Inputs							Output
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CK	$\overline{CK}$	∑ of inputs = H (D0 to D21)	PARIN [1]	$\overline{PTYERR}$ [2] [3]
H	L	H	↑	↓	even	L	H
H	L	H	↑	↓	odd	L	L
H	L	H	↑	↓	even	H	L
H	L	H	↑	↓	odd	H	H
H	H	L	↑	↓	even	L	H
H	H	L	↑	↓	odd	L	L
H	H	L	↑	↓	even	H	L
H	H	L	↑	↓	odd	H	H
H	H	H	↑	↓	X	X	$\overline{PTYERR}_0$
H	X	X	L or H	L or H	X	X	$\overline{PTYERR}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

[1] PARIN arrives one clock cycle after the data to which it applies. All Dn inputs must be driven to a known state for parity to be calculated correctly.

[2] This condition assumes $\overline{\text{PTYERR}}$ is HIGH at the crossing of CK going HIGH and $\overline{\text{CK}}$ going LOW. If $\overline{\text{PTYERR}}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

CSGATEEN is 'don't care' for $\overline{\text{PTYERR}}$.

[3] $\overline{\text{PTYERR}}_0$ is the previous state of output $\overline{\text{PTYERR}}$.

7.2 Functional information

This 28-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32865 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going HIGH, and $\overline{\text{CK}}$ going LOW.

The device supports low-power standby operation. When the reset input ($\overline{\text{RESET}}$) is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is LOW all registers are reset, and all outputs except $\overline{\text{PTYERR}}$ are forced LOW. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTU32865 ensures that the outputs remain LOW, thus ensuring no glitches on the output.

The device monitors both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are HIGH. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is LOW, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and will force the Qn outputs LOW and the $\overline{\text{PTYERR}}$ output HIGH. If the $\overline{\text{DCSn}}$-control functionality is not desired, then the CSGATEEN input can be hardwired to ground, in which case, the setup-time requirement for $\overline{\text{DCSn}}$ would be the same as for the other Dn data inputs.

The SSTU32865 includes a parity checking function. The SSTU32865 accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the Dn inputs (with either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ active) and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active LOW).

7.3 Functional differences to SSTU32864

The SSTU32865 for its basic register functionality, signal definition and performance is based upon the industry-standard SSTU32864, but provides key operational features which differ (at least in part) from the industry-standard register in the following aspects:

7.3.1 Chip Select (CS) gating of key inputs ($\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, CSGATEEN)

As a means to reduce device power, the internal latches will only be updated when one or both of the CS inputs are active (LOW) and CSGATEEN HIGH at the rising edge of the clock. The 22 'Chip-Select-gated' input signals associated with this function include addresses (ADDR0 to ADDR15, BA0 to BA2), and RAS, CAS, WE, with the remaining signals (CS, CKE, ODT) continuously re-driven at the rising edge of every clock as they are independent of CS. The CS gating function can be disabled by tying CSGATEEN LOW, enabling all internal latches to be updated on every rising edge of the clock.

Table 5: Chip Select gating mode

Mode	Signal name	Description
Gating	CSGATEEN HIGH	Registers only re-drive signals to the DRAMs when Chip Select inputs are LOW.
Non-gating	CSGATEEN LOW	Registers always re-drive signals on every clock cycle, independent of the state of the Chip Select inputs.

7.3.2 Parity error checking and reporting

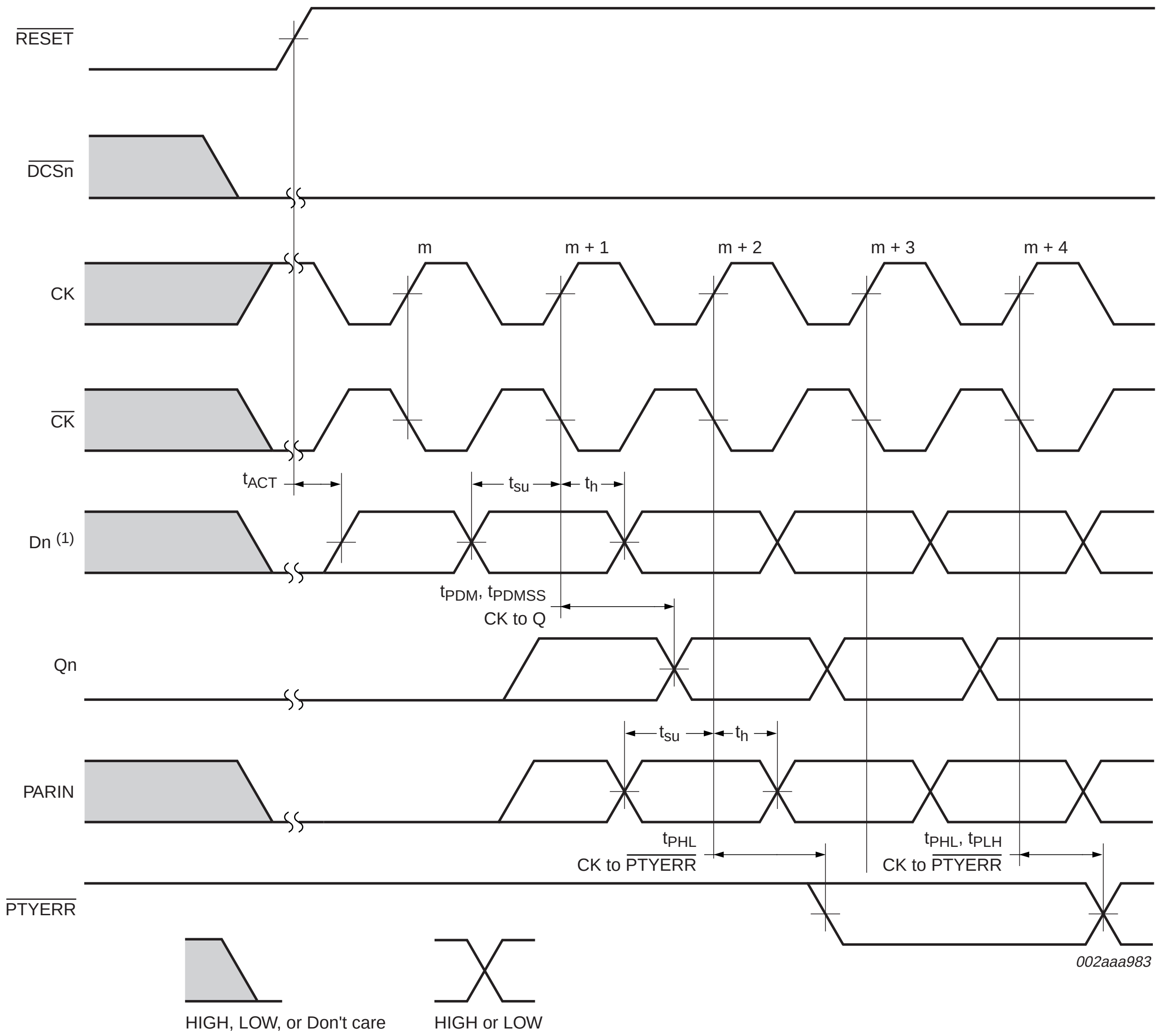
The SSTU32865 incorporates a parity function, whereby the signal received on input pin PARIN is received as parity to the register, one clock cycle later than the CS-gated inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The 22 CS-gated input signals will be latched and re-driven on the first clock, and any error will be reported one clock cycle later via the $\overline{\text{PTYERR}}$ output pin (driven LOW for two consecutive clock cycles). $\overline{\text{PTYERR}}$ is an open-drain output, allowing multiple modules to share a common signal pin for reporting the occurrence of a parity error during a valid command cycle (coincident with the re-driven signals). This output is driven LOW for two consecutive clock cycles to allow the memory controller sufficient time to sense and capture the error even. A LOW state on $\overline{\text{PTYERR}}$ indicates that a parity error has occurred.

7.3.3 Reset ($\overline{\text{RESET}}$)

Similar to the $\overline{\text{RESET}}$ pin on the industry-standard SSTU32864, this pin is used to clear all internal latches and all outputs will be driven LOW quickly except the $\overline{\text{PTYERR}}$ output, which will be floated (and will normally default HIGH by their external pull-up).

7.3.4 Power-up sequence

The reset function for the SSTU32865 is similar to that of the SSTU32864 except that the $\overline{\text{PTYERR}}$ signal is also cleared and will be held clear (HIGH) for three consecutive clock cycles.



(1) After RESET is switched from LOW to HIGH, all data and PARIN input signals must be set and held LOW for a minimum time of $t_{ACT(max)}$ to avoid false error.

Fig 4. RESET switches from LOW to HIGH

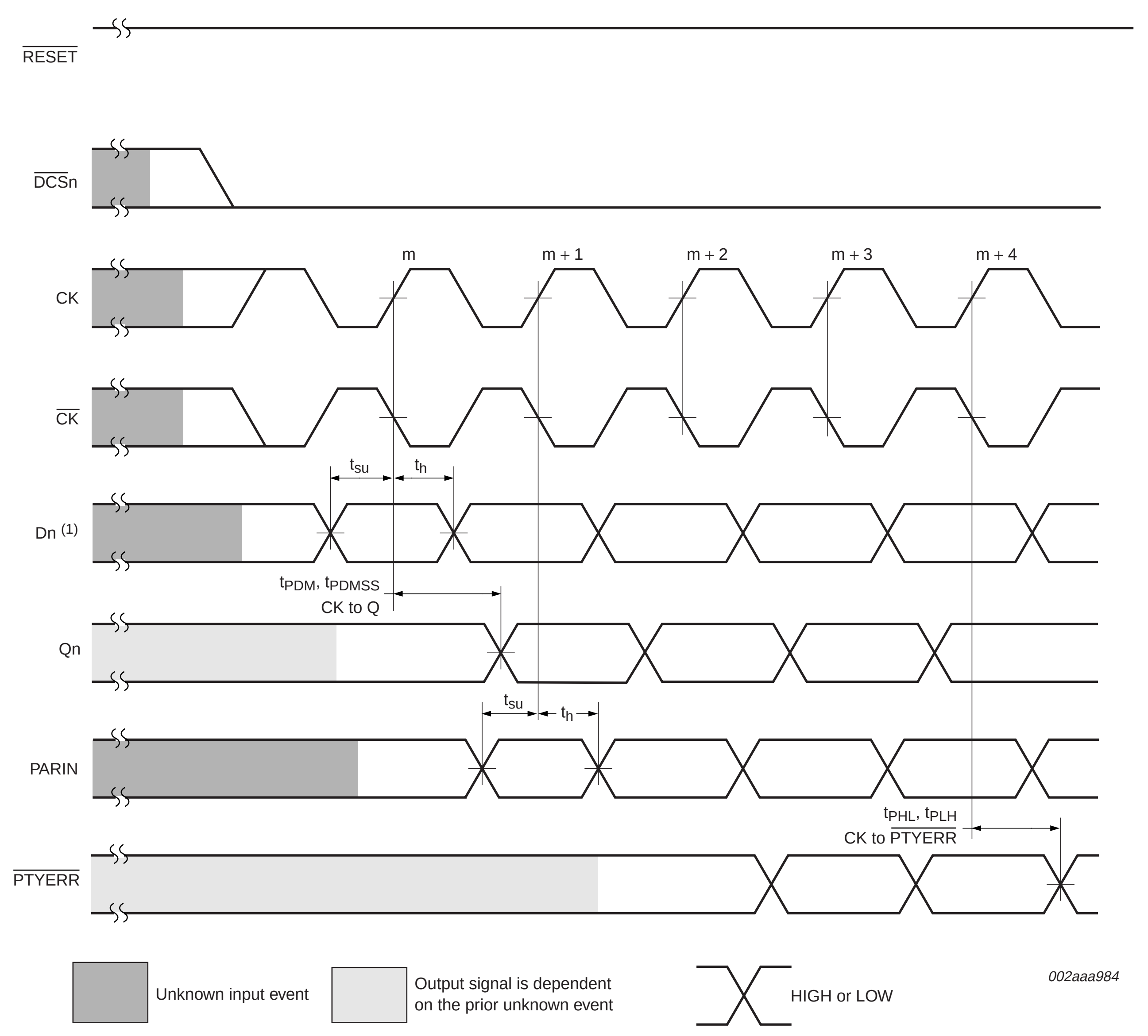
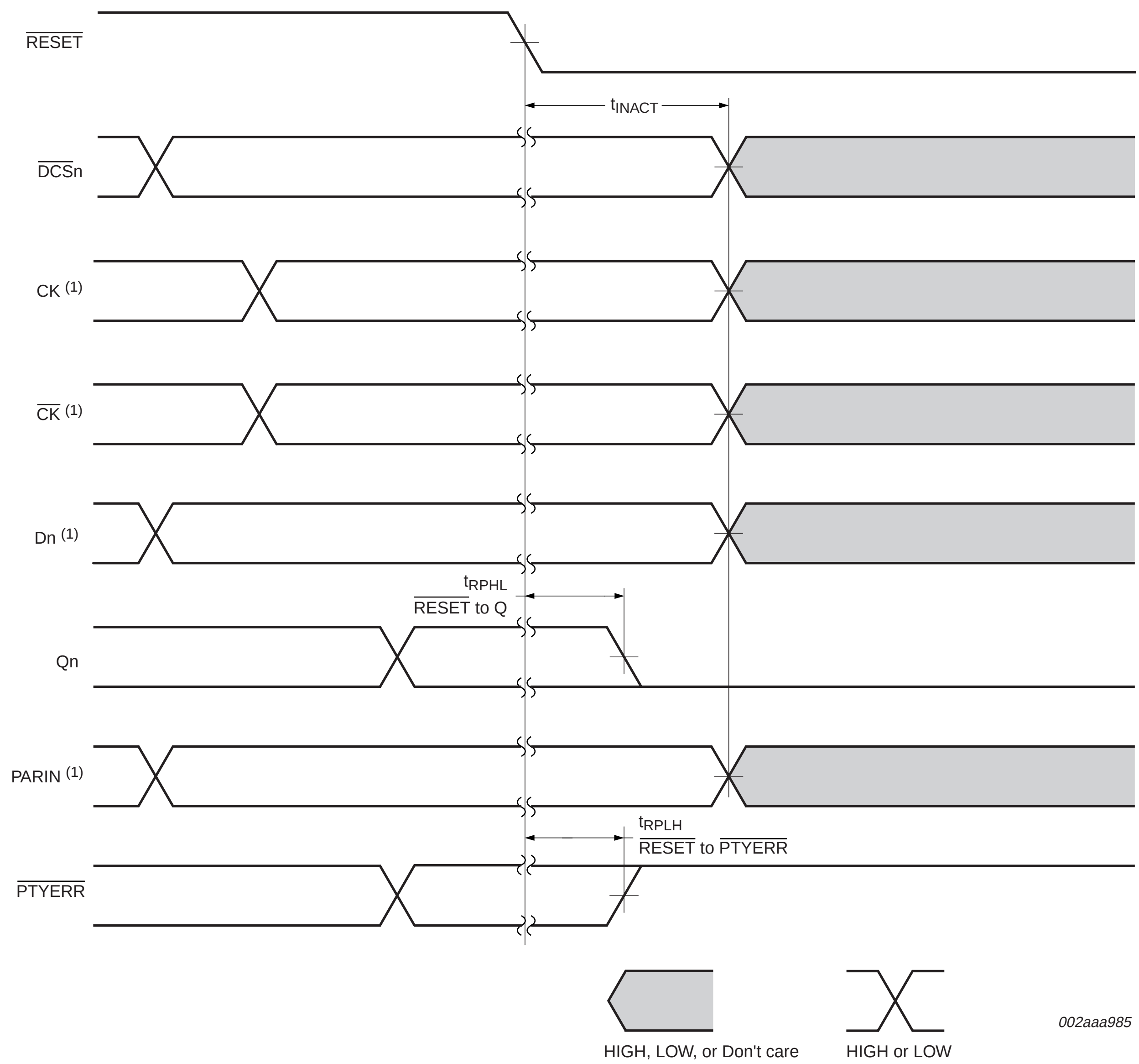
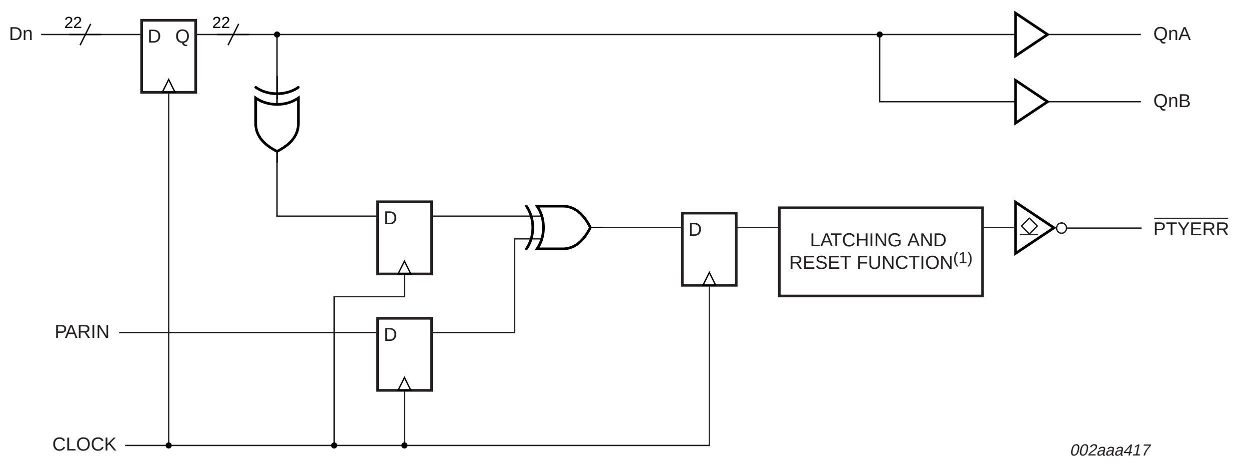


Fig 5. RESET being held HIGH



(1) After RESET is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of $t_{INACT(max)}$.

Fig 6. RESET switches from HIGH to LOW



(1) This function holds the error for two cycles. For details, see Section 7 “Functional description” and Figure 4 “RESET switches from LOW to HIGH”.

Fig 7. Parity logic diagram

8. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
V_I	receiver input voltage		[2]	–0.5	+2.5	V
V_O	driver output voltage		[2]	–0.5	V_{DD} + 0.5	V
I_{IK}	input clamp current	$V_I < 0$ V or $V_I > V_{DD}$		-	–50	mA
I_{OK}	output clamp current	$V_O < 0$ V or $V_O > V_{DD}$		-	±50	mA
I_O	continuous output current	$0 \text{ V} < V_O < V_{DD}$		-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); 1.5 kΩ; 100 pF		2	-	kV
		Machine Model (MM); 0 Ω; 200 pF		200	-	V

[1] Stresses beyond those listed under ‘absolute maximum ratings’ may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ‘recommended operating conditions’ is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	1.9	V
V_{REF}	reference voltage			$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	termination voltage			V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	input voltage			0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	data inputs (Dn)	[1]	V_{REF} + 250 mV	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	data inputs (Dn)	[1]	-	-	V_{REF} – 250 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage	data inputs (Dn)	[1]	V_{REF} + 125 mV	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	data inputs (Dn)	[1]	-	-	V_{REF} – 125 mV	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$	[2]	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$	[2]	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$		0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$		600	-	-	mV
I_{OH}	HIGH-level output current			-	-	–8	mA
I_{OL}	LOW-level output current			-	-	8	mA
T_{amb}	operating ambient temperature in free air			0	-	+70	°C

[1] The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

[2] The $\overline{RESET}$ input of the device must be held at valid logic levels (not floating) to ensure proper device operation.

10. Characteristics

Table 8: Characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_I	input current	all inputs; V_I = V_{DD} or GND; V_{DD} = 1.9 V	-	-	±5	μA
I_{DD}	static standby current	$\overline{RESET}$ = GND; V_{DD} = 1.9 V	-	-	100	μA
	static operating current	$\overline{RESET}$ = V_{DD}; V_{DD} = 1.9 V; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	40	mA
I_{DDD}	dynamic operating current per MHz, clock only	$\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.8 V	-	16	-	μA
	dynamic operating current per MHz, per each data input	$\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.8 V	-	19	-	μA
C_i	input capacitance, data inputs	V_I = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	input capacitance, CK and $\overline{CK}$	V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
	input capacitance, $\overline{RESET}$	V_I = V_{DD} or GND; V_{DD} = 1.8 V	3	-	5	pF

Table 9: Timing requirements

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clock}	clock frequency			-	-	450	MHz
t_W	pulse duration, CK, $\overline{CK}$ HIGH or LOW			1	-	-	ns
t_{ACT}	differential inputs active time		[1] [2]	-	-	10	ns
t_{INACT}	differential inputs inactive time		[1] [3]	-	-	15	ns
t_{su}	setup time, Chip Select	$\overline{DCS0}$, $\overline{DCS1}$ valid before clock switching		0.7	-	-	ns
	setup time, Data	Dn valid before clock switching		0.5	-	-	ns
	setup time, PARIN	PARIN before CK and $\overline{CK}$		0.5	-	-	ns
t_h	hold time	input to remain valid after clock switching		0.5	-	-	ns
	hold time, PARIN	PARIN after CK and $\overline{CK}$		0.5	-	-	ns

[1] This parameter is not necessarily production tested.

[2] Data inputs must be active below a minimum time of $t_{ACT(max)}$ after $\overline{RESET}$ is taken HIGH.

[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$ after $\overline{RESET}$ is taken LOW.

Table 10: Switching characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MAX}	maximum input clock frequency			450	-	-	MHz
t_{PDM}	propagation delay	CK and $\overline{CK}$ to output	[1]	1.41	-	1.8	ns
t_{LH}	LOW-to-HIGH delay	CK and $\overline{CK}$ to $\overline{PTYERR}$		1.2	-	3	ns
t_{HL}	HIGH-to-LOW delay	CK and $\overline{CK}$ to $\overline{PTYERR}$		1	-	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from $\overline{RESET}$ to $\overline{PTYERR}$		-	-	3	ns
t_{PDMSS}	propagation delay, simultaneous switching	CK and $\overline{CK}$ to output	[1] [2]	-	-	2.0	ns
t_{PHL}	propagation delay	$\overline{RESET}$ to output		-	-	3	ns

[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 11: Output edge rates

Over recommended operating conditions, unless otherwise noted.

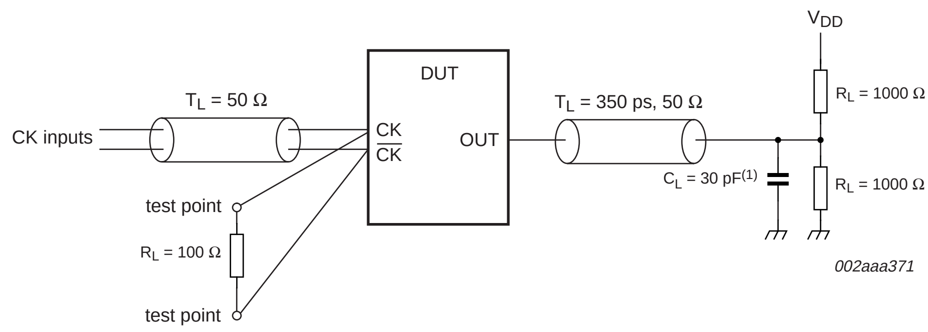
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate		1	-	4	V/ns
dV/dt_f	falling edge slew rate		1	-	4	V/ns
dV/dt_Δ	absolute difference between dV/dt_r and dV/dt_f		-	-	1	V/ns

11. Test information

11.1 Test circuit

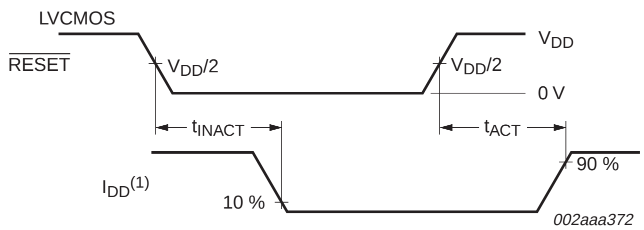
All input pulses are supplied by generators having the following characteristics: Pulse Repetition Rate (PRR) ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



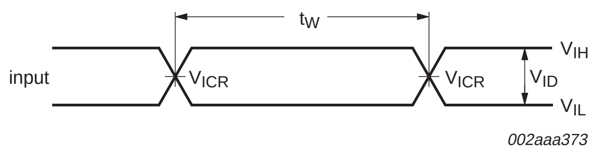
(1) C_L includes probe and jig capacitance.

Fig 8. Load circuit



(1) I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Fig 9. Voltage and current waveforms; inputs active and inactive times

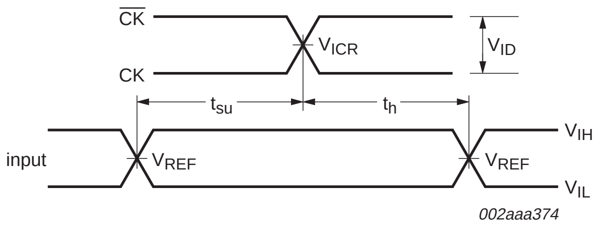


V_{ID} = 600 mV

V_{IH} = V_{REF} + 250 mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.

V_{IL} = V_{REF} – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 10. Voltage waveforms; pulse duration



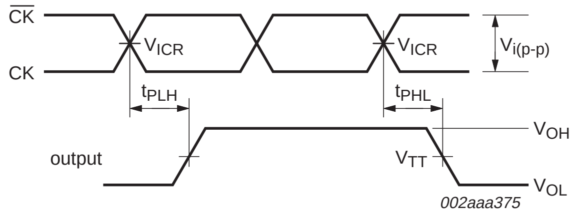
V_{ID} = 600 mV

$V_{REF} = V_{DD}/2$

$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

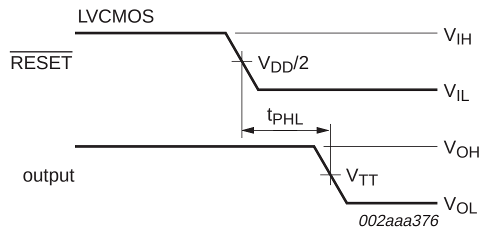
$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 11. Voltage waveforms; setup and hold times



t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 12. Voltage waveforms; propagation delay times (clock to output)



t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

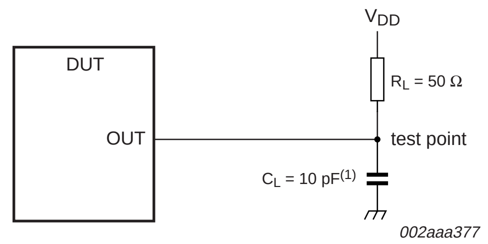
$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 13. Voltage waveforms; propagation delay times (reset to output)

11.2 Output slew rate measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 14. Load circuit, HIGH-to-LOW slew measurement

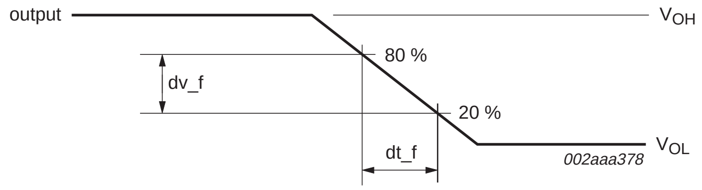
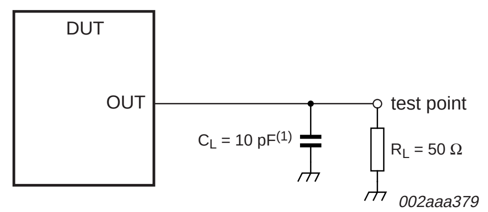


Fig 15. Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Fig 16. Load circuit, LOW-to-HIGH slew measurement

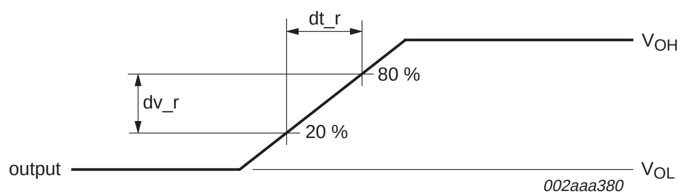
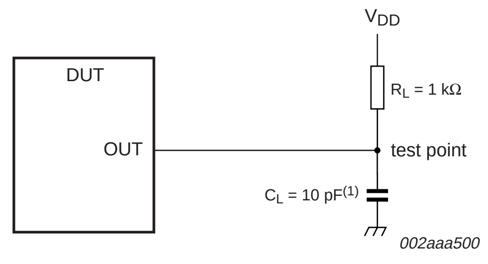


Fig 17. Voltage waveforms, LOW-to-HIGH slew rate measurement

11.3 Error output load circuit and voltage measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 18. Load circuit, error output measurements

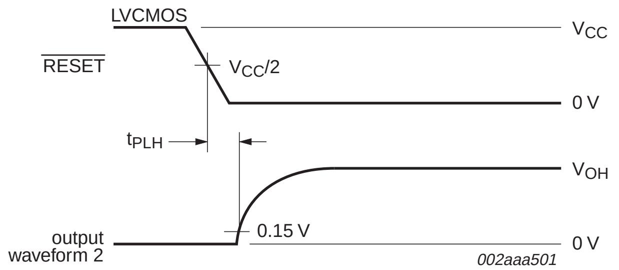


Fig 19. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to RESET input

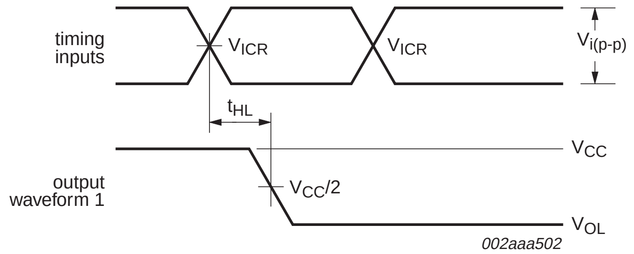


Fig 20. Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs

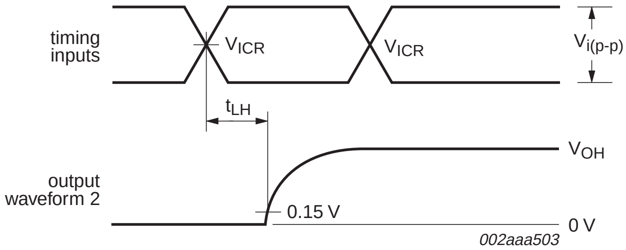
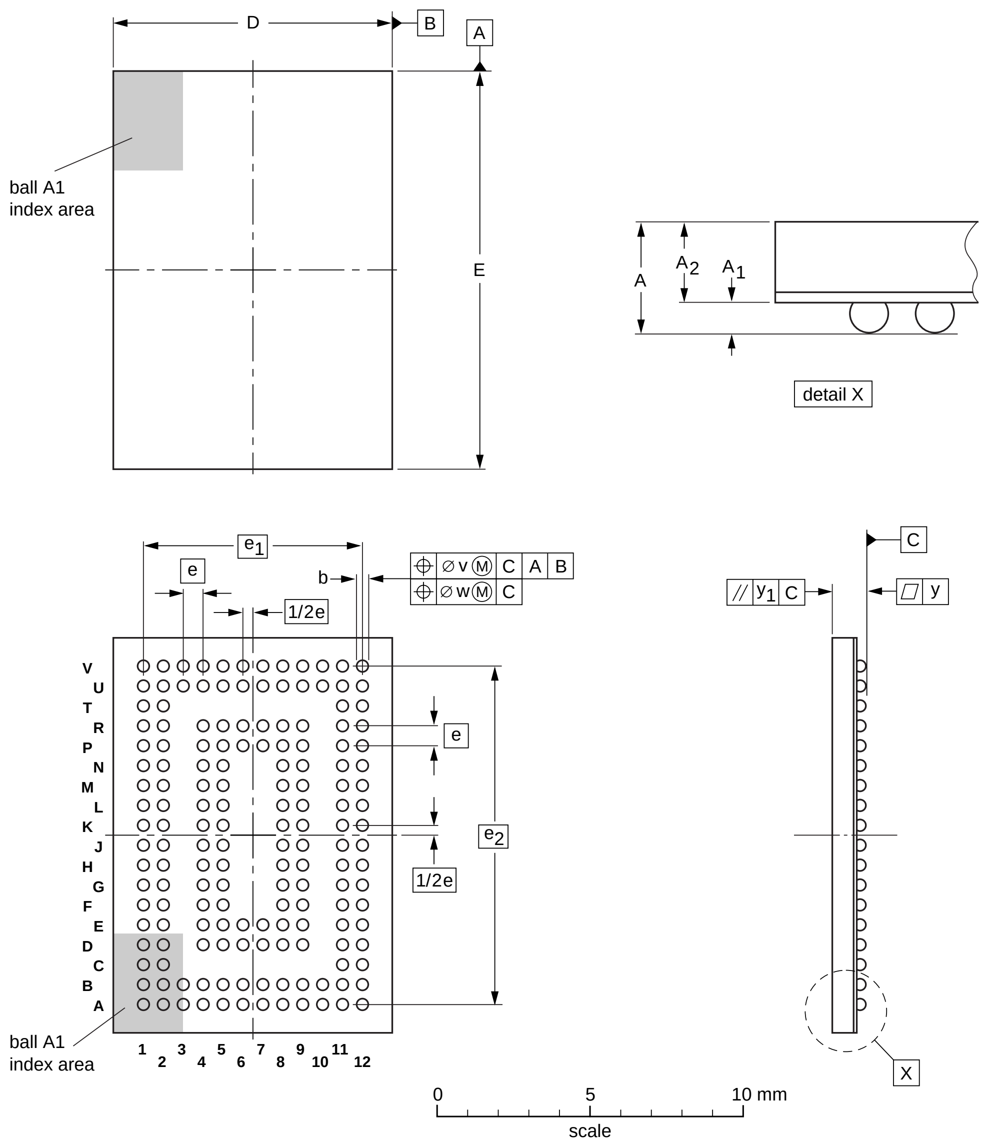


Fig 21. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

12. Package outline

TFBGA160: plastic thin fine-pitch ball grid array package; 160 balls; body 9 x 13 x 0.8 mm **SOT802-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.35 0.25	0.85 0.75	0.45 0.35	9.1 8.9	13.1 12.9	0.65	7.15	11.05	0.15	0.08	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT802-1	- - -	- - -	- - -			03-01-29

Fig 22. Package outline SOT802-1 (TFBGA160)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  – for all BGA, HTSSON..T and SSOP..T packages
  – for packages with a thickness ≥ 2.5 mm
  – for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  – larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 12: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 13: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SSTU32865_2	20040928	Product data sheet	-	9397 750 13799	SSTU32865-01

Modifications:

- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.
- Section 1 “General description”: acronym TFBGA defined.
- Section 2 “Features”: acronym SSTL defined.
- Additional features added to Section 2 “Features”
- Section 6 “Pinning information”
  - change ‘MCL’ to ‘m.c.l.’ and ‘MCH’ to ‘m.c.h.’
  - add descriptions for VDDL and VDDR in Table 2 “Pin description”
  - added Figure 2 “Pin configuration for TFBGA160”
  - added Figure 3 “Ball mapping” (replaces Table 2 “Ball mapping”)
- Table 3 “Function table (each flip-flop)” and Table 4 “Parity and standby function table” moved to Section 7.1 on page 8.
- Table 3 “Function table (each flip-flop)”: add Table note 1 and its reference at ‘Outputs’.
- Table 4 “Parity and standby function table”:
  - Table note 2: change ‘This transition assumes ...’ to ‘This condition assumes ...’.
  - Add Table note 3.
- Section 7.3.4 “Power-up sequence”: add ‘(HIGH)’ after ‘... and will be held clear’.
- Table 6 “Limiting values”:
  - Symbol V_i changed to V_I; Symbol V_o changed to V_O.
  - Symbols ESD_{HBM} and ESD_{MM} replaced with V_{esd} (added model types under “Conditions”)
- Table 7 “Recommended operating conditions”:
  - change V_{IH} (for data inputs) to $V_{IH(AC)}$ and $V_{IH(DC)}$; condition changed to ‘data inputs (Dn)’
  - change V_{IL} (for data inputs) to $V_{IL(AC)}$ and $V_{IL(DC)}$; condition changed to ‘data inputs (Dn)
  - Table note split into 2 notes; references added.
- Table 8 “Characteristics”
  - change I_{DDD} Parameter from “dynamic operating current ...” to “dynamic operating current per MHz ...”; change Unit from “µA/MHz” to “µA”.
  - change Typical value for I_{DDD} (clock only) from TBD to 16 µA
  - change Typical value for I_{DDD} (per each data input) from TBD to 19 µA
- Table 9 “Timing requirements”:
  - change symbol f_{CLOCK} to f_{clock}
  - change f_{clock} maximum value from 270 MHz to 450 MHz
  - change symbol t_{SU} to t_{su}; under ‘Conditions’, change ‘Chip Select’ to ‘$\overline{DCS0}$, $\overline{DCS1}$’.
  - change symbol t_H to t_h
- Table 10 “Switching characteristics”:
  - change f_{MAX} minimum value from 270 MHz to 450 MHz
  - change t_{PDM} maximum value from 2.15 ns to 1.8 ns
  - change t_{PDMSS} maximum value from 2.35 ns to 2.0 ns
- Section 11.1 “Test circuit”: acronym PRR defined; titles for Figure 12 and Figure 13 modified.

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SSTU32865-01	20040705	Product data	-	9397 750 10942	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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