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Digital Control Compatible Dual Low-Side ±4 Amp MOSFET Drivers with Programmable Common Current Sense

FEATURES

- Adjustable Current Limit Protection
- 3.3-V, 10-mA Internal Regulator
- DSP/µC Compatible Inputs
- Dual ±4-A TrueDrive™ High Current Drivers
- 10-ns Typical Rise and Fall Times with 2.2-nF Loads
- 20-ns Input-to-Output Propagation Delay
- 25-ns Current Sense-to-Output Propagation Delay
- Programmable Current Limit Threshold
- Digital Output Current Limit Flag
- 4.5-V to 15-V Supply Voltage Range
- Rated from -40°C to 105°C
- Lead(Pb)-Free Packaging

APPLICATIONS

- Digitally Controlled Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers

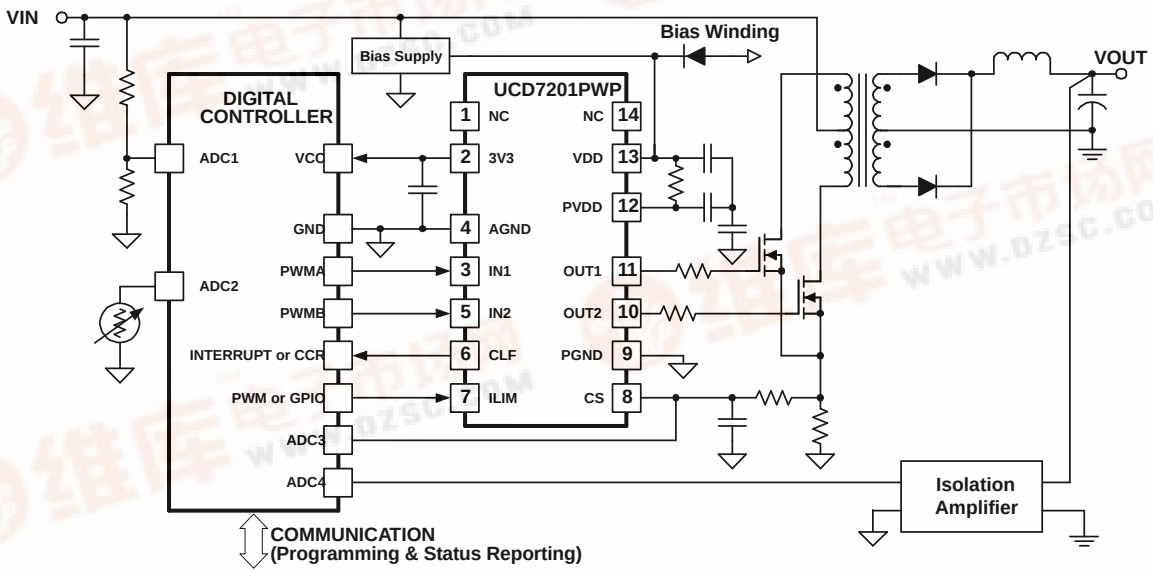
DESCRIPTION

The UCD7201 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

The UCD7201 includes dual low-side ±4-A high-current MOSFET gate drivers. It allows the digital power controllers such as UCD9110 or UCD9501 to interface to the power stage in double ended topologies. It provides a cycle-by-cycle current limit function for both driver channels, a programmable threshold and a digital output current limit flag which can be monitored by the host controller. With a fast cycle-by-cycle current limit protection, the driver can turn off the power stage in the event of an overcurrent condition.

For fast switching speeds, the UCD7201 output stages use the TrueDrive™ output architecture, which delivers rated current of ±4 A into the gate of a MOSFET during the Miller plateau region of the switching transition. It also includes a 3.3-V, 10-mA linear regulator to provide power to the digital controller.

TYPICAL APPLICATION DIAGRAM (Push-Pull Converter)



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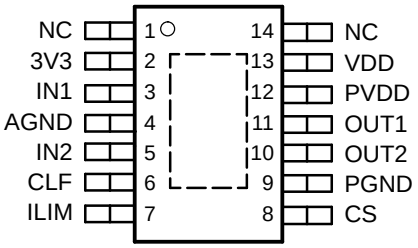
DESCRIPTION (CONT.)

For similar applications requiring direct start-up capability from higher voltages such as the 48-V telecom input line, the UCD7601 includes a 110-V high-voltage startup circuit.

The UCD7K driver family is compatible with standard 3.3-V I/O ports of DSPs, Microcontrollers, or ASICs. UCD7201 is offered in PowerPAD™ HTSSOP-14 or space-saving QFN-16 packages.

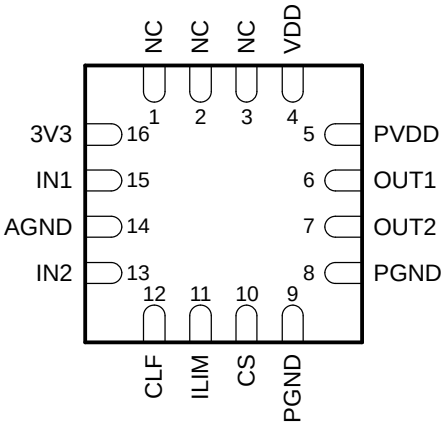
CONNECTION DIAGRAMS

PWP−14 PACKAGE
(TOP VIEW)



NC − No internal connection

RSA−16 PACKAGE
(BOTTOM VIEW)



ORDERING INFORMATION

TEMPERATURE RANGE	CURRENT SENSE LIMIT PER CHANNEL	110-V HV STARTUP CIRCUIT	PACKAGED DEVICES (1)(2)	
			PowerPAD™ HTSSOP-14 (PWP)	QFN-16 (RSA)(3)
-40°C to 105°C	Common	No	UCD7201PWP	UCD7201RSA

(1) These products are packaged in Pb-Free and Green lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) HTSSOP-14 (PWP) and QFN-16 (RSA), packages are available taped and reeled. Add R suffix to device type (e.g. UCD7201PWPR) to order quantities of 2,000 devices per reel for the PWP package and 1,000 devices per reel for the RSA packages.
(3) Contact factory for availability of QFN packaging.

PACKAGING INFORMATION

PACKAGE	SUFFIX	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING T_A = 70°C, T_J = 125°C (mW)	DERATING FACTOR, ABOVE 70°C (mW/°C)
PowerPAD™ HTSSOP- 14	PWP	2.07	37.47(1)	1470	27
QFN-16	RSA	-	-	-	-

(1) PowerPAD® soldered to the PWB (TI recommended PWB as defind in TI's application report SLMA002 pg.33) with OLFM.

ABSOLUTE MAXIMUM RATINGS(1)(2)

SYMBOL	PARAMETER		UCD7201	UNIT
V_{DD}	Supply Voltage		16	V
I_{DD}	Supply Current	Quiescent	20	mA
		Switching, T_A = 25°C, , T_J = 125°C, V_{DD} = 12 V	200	
V_{OUT}	Output Gate Drive Voltage	OUT	-1 to PVDD	V
$I_{OUT(sink)}$	Output Gate Drive Current	OUT	4.0	A
$I_{OUT(source)}$			-4.0	
	Analog Input	ISET, CS	-0.3 to 3.6	V
		ILIM	-0.3 to 3.6	
	Digital I/O's	IN, CLF	-0.3 to 3.6	
	Power Dissipation	T_A = 25°C (PWP-14 package), T_J = 125°C	2.67	W
		T_A = 25°C (QFN-16 package), T_J = 125°C	-	
T_J	Junction Operating Temperature	UCD7201	-55 to 150	°C
T_{str}	Storage Temperature		-65 to 150	
HBM	ESD Rating	Human body model	2000	V
CDM		Change device model	500	
T_{SOL}	Lead Temperature (Soldering, 10 sec)		+300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, 0.22µF from 3V3 to AGND, T_A = T_J = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION					
Supply current, OFF	V_{DD} = 4.2 V	-	200	400	µA
Supply current	Outputs not switching IN = LOW	-	1.5	2.5	mA
LOW VOLTAGE UNDER-VOLTAGE LOCKOUT					
VDD UVLO ON		4.25	4.5	4.75	V
VDD UVLO OFF		4.05	4.25	4.45	
VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY					
3V3 initial set point	T_A = 25°C, I_{LOAD} = 0	3.267	3.3	3.333	V
3V3 set point over temperature		3.234	3.3	3.366	
3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, VDD = 5 V	-	1	6.6	mV
3V3 line regulation	VDD = 4.75 V to 12 V, I_{LOAD} = 10 mA	-	1	6.6	
Short circuit current	VDD = 4.75 to 12 V	11	20	35	mA
3V3 OK threshold, ON	3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.9	
INPUT SIGNAL					
HIGH, positive-going input threshold voltage (VIT+)		1.65	-	2.08	V
LOW negative-going input threshold voltage (VIT-)		1.16	-	1.5	
Input voltage hysteresis, (VIT+ - VIT-)		0.6	-	0.8	

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, 0.22µF from 3V3 to AGND, $T_A = T_J$ = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency		-	-	2	MHz
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.51	0.55	0.58	V
ILIM maximum current limit threshold	I_{LIM} = 3.3 V	1.05	1.10	1.15	
ILIM current limit threshold	I_{LIM} = 0.75 V	0.700	0.725	0.750	
ILIM minimum current limit threshold	I_{LIM} = 0.25 V	0.21	0.23	0.25	
CLF output high level	CS > I_{LIM} , I_{LOAD} = -7 mA	2.64	-	-	
CLF output low level	CS ≤ I_{LIM}, I_{LOAD} = 7 mA	-	-	0.66	
Propagation delay from IN to CLF	IN rising to CLF falling after a current limit event	-	10	20	ns
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current		-	–1	-	uA
Propagation delay from CS to OUTx (1)	I_{LIM} = 0.5 V, measured on OUTx, CS = threshold + 60 mV	-	25	40	ns
Propagation delay from CS to CLF(1)	I_{LIM} = 0.5 V, measured on CLF, CS = threshold + 60 mV	-	25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	IN = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current (1)	VDD = 12 V, IN = high, OUTx = 5 V		4		A
Sink current (1)	VDD = 12 V, IN = low, OUTx = 5 V		4		
Source current(1)	VDD = 4.75 V, IN = high, OUTx = 0		2		
Sink current (1)	VDD = 4.75 V, IN = low, OUTx = 4.75 V		3		
Rise time, t_R	C_{LOAD}= 2.2 nF, VDD = 12 V		10	20	ns
Fall time, t_F	C_{LOAD} = 2.2 nF, VDD = 12 V		10	15	
Output with VDD < UVLO	VDD =1.0 V, I_{SINK} = 10 mA		0.8	1.2	V
Propagation delay from IN to OUT1, t_{D1}	C_{LOAD} = 2.2 nF, VDD = 12 V, CLK rising		20	35	ns
Propagation delay from IN to OUT2, t_{D2}	C_{LOAD} = 2.2 nF, VDD = 12 V, CLK falling		20	35	

(1) Ensured by design. Not 100% tested in production.

FUNCTIONAL BLOCK DIAGRAM

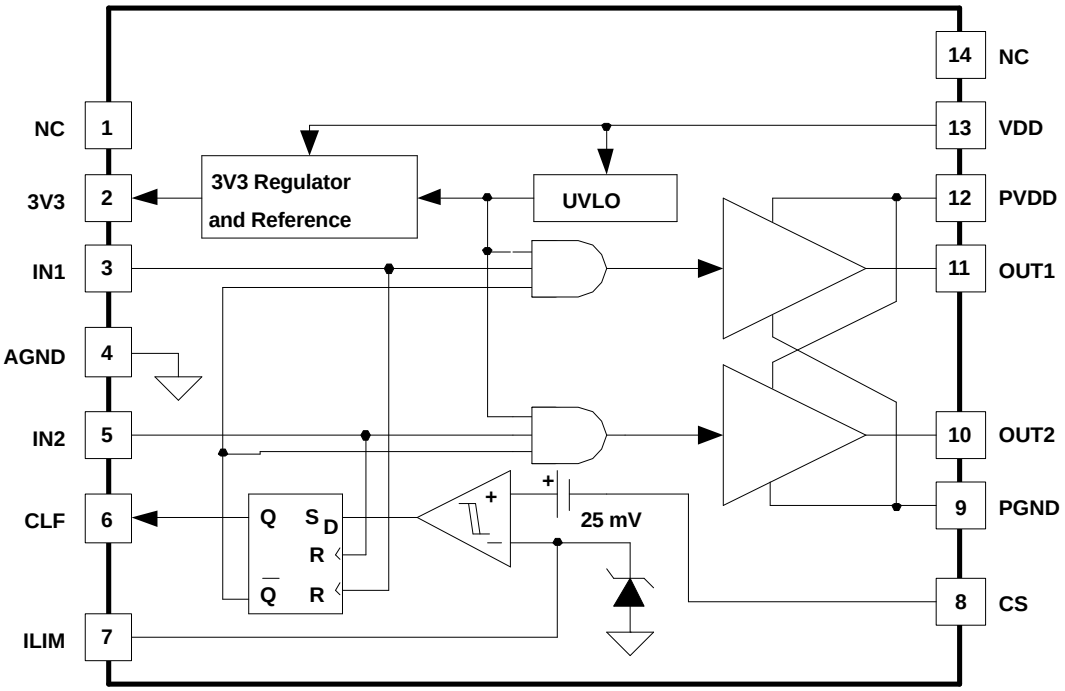
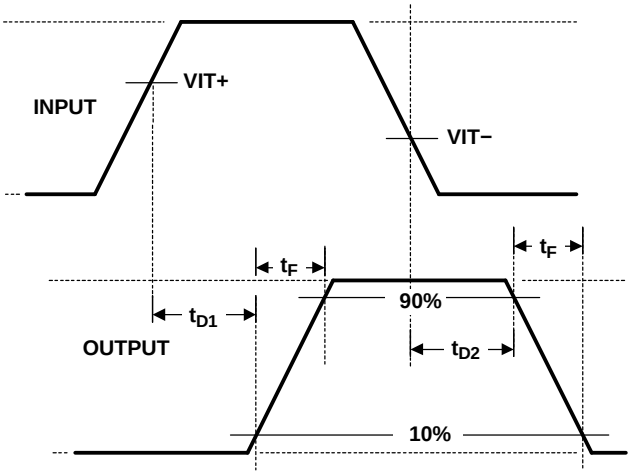


Figure 1. UCD7201

Timing Diagram



TERMINAL FUNCTIONS

UCD7201		PIN NAME	I/O	FUNCTION
HTSSOP -14 PIN #	QFN-16 PIN #			
1	-	NC	-	No Connection
2	1	3V3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place 0.22 µF of ceramic capacitance from this pin to ground.
3	2	IN1	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
4	3	AGND	-	Analog ground return.
5	4	IN2	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
6	5	CLF	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on the IN pin.
7	6	ILIM	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V. The default value while open is 0.5 V.
8	7	CS	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
9	8, 9	PGND	-	Power ground return. The pin should be connected very closely to the source of the power MOSFET.
10	10	OUT2	O	The high-current TrueDrive™ driver output.
11	11	OUT1	O	The high-current TrueDrive™ driver output.
12	12	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. The bypass capacitor for this pin should be returned to PGND.
13	13	VDD	I	Supply input pin to power the driver. The UCD7K devices accept an input range of 4.5 V to 15 V. Bypass the pin with at least 4.7 µF of capacitance, returned to AGND.
14	14, 15, 16	NC	-	No Connection.

APPLICATION INFORMATION

The UCD7201 is member of the UCD7K family of digital compatible drivers targeting applications utilizing digital control techniques or applications that require local fast peak current limit protection.

Supply

The UCD7K devices accept a supply range of 4.5 V to 15 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage supplies the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Although quiescent VDD current is low, total supply current depends on the gate drive output current required for capacitive load and switching frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$I_{OUT} = Q_G$ x f, where f is frequency.

For the best high-speed circuit performance, VDD bypass capacitors are recommended to prevent noise problems. A 4.7-µF ceramic capacitor should be located closest to the VDD and the AGND connection. In addition, a larger capacitor with relatively low ESR should be connected to the PVDD and PGND pin, to help deliver the high current peaks to the load. The capacitors should present a low impedance characteristic for the expected current levels in the driver application. The use of surface mount components for all bypass capacitors is highly recommended.

Reference / External Bias Supply

All devices in the UCD7K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place 0.22-µF of ceramic capacitance between the 3V3 pin to the AGND pin.

Input Pin

The input pins are high impedance digital inputs capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt Trigger comparator which isolates the internal circuitry from any external noise.

If limiting the rise or fall times to the power device is desired then an external resistance may be added between the output of the driver and the load device, which is generally the gate of a power MOSFET.

Current Sensing and Protection

A very fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.

The current limit threshold may be set to any value between 0.25 V and 1.0 V by applying the desired threshold voltage to the current limit (ILIM) pin. If the ILIM pin is left floating, the internal current limit threshold will be 0.5 volts. When the CS level is greater than the I_{LIM} voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on either of the IN pins.

When the CS voltage is below I_{LIM}, the driver output follows the PWM input. The CLF digital output flag can be monitored by the host controller to determine when a current limit event occurs and to then apply the appropriate algorithm to obtain the desired current limit profile (i.e. straight time, fold back, hickup or latch-off).

A benefit of this local protection feature is that the UCD7K devices can protect the power stage if the software code in the digital controller becomes corrupted. If the controller's PWM output stays high, the local current sense circuit turns off the driver output when an over-current event occurs. The system would then likely go into retry mode because most DSP and microcontrollers have on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD7K's local current limit comparator provides the required fast protection for the power stage.

The CS threshold is 25 mV below the I_{LIM} voltage. If the user attempts to command zero current while the CS pin is at ground the CLF flag will latch high until the IN pin receives a pulse. At start-up it is necessary to ensure that the ILIM pin will always be greater than the CS pin for the handshaking to work as described below. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag will be latched high and the digital controller must poll the UCD7K device, by sending it a narrow IN pulse. If a fault condition is not present the IN pulse will reset the CLF signal to low indicating that the UCD7K device is ready to process power pulses.

Handshaking

The UCD7K family of devices have a built-in hand-shaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD7K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device will process input drive signals. The micro-controller should monitor the CFL flag at start-up and wait for the CLF flag to go LOW before sending power pulses to the UCD7K device.

Driver Output

The high-current output stage of the UCD7K device family is capable of supplying ±4-A peak current pulses and swings to both PVDD and PGND. The driver outputs follow the state of the IN pin provided that the VDD and 3V3 voltages are above their respective under-voltage lockout threshold.

The drive output utilizes Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pullup pulldown circuits with bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD7K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [1]

Drive Current and Power Requirements

The UCD7K family of drivers can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device.

Reference [1] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = CV^2 \times f$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged.

With V_{DD} = 12 V, C_{LOAD} = 2.2 nF, and f = 300 kHz, the power loss can be calculated as:

$$P = 2.2\ \text{nF} \times 12^2 \times 300\ \text{kHz} = 0.095\ \text{W}$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.095\ \text{W}}{12\ \text{V}} = 7.9\ \text{mA}$$

Operational Waveforms

Figure 24 shows the circuit performance achievable with the output driving a 10-nF load at 12-V V_{DD}. The input pulsewidth (not shown) is set to 200 ns to show both transitions in the output waveform. Note the linear rising and falling edges of the switching waveforms. This is due to the constant output current characteristic of TrueDrive™ stage as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD7K family of drivers is available in PowerPAD™ TSSOP and QFN/DFN packages to cover a range of application requirements. Both have an exposed pad to enhance thermal conductivity from the semiconductor junction.

As illustrated in Reference [2], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the T_{JC} down to 2.07°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPad™ should be connected to the quiet ground of the circuit.

Circuit Layout Recommendations

In a power driver operating at high frequency, it is critical to minimize stray inductance to minimize overshoot/undershoots and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. It is advantageous to connect the driver device close to the MOSFETs. It is recommended that the PGND and the AGND pins be connected to the PowerPad™ of the package with a thin trace. It is critical to ensure that the voltage potential between these two pins does not exceed 0.3 V. The use of schottky diodes on the outputs to PGND and PVDD is recommended when driving gate transformers.

Additional Application Circuits

Figure 2 shows the UCD7201 in a half-bridge converter design. The digital controller is performing the output voltage compensation and all supervisory functions. The isolation amplifier is made up of a linear opto-coupler configured for a gain of 1/10, so the output voltage is transformed to a level comparable with the ADC of the digital controller.

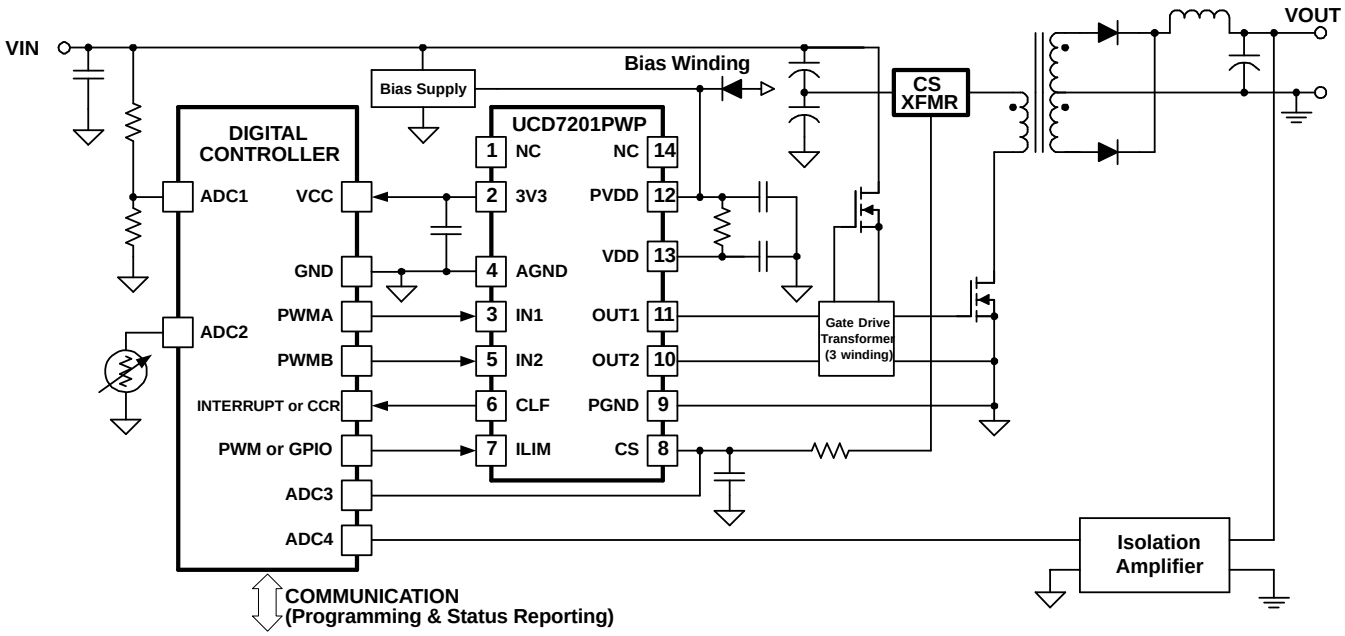


Figure 2. Half-Bridge Converter

Figure 3 shows the UCD7201 in an analog only implementation of an intermediate bus converter. The ILIM pin of the UCD7201 is exponentially increased at start-up, which minimizes overshoot on the output voltage. The UCC28089 is a push-pull controller with fixed dead-time. The UCC28089 operates at a fixed duty cycle close to 100% so the circuit acts like a DC transformer linearly transforming the input voltage via the turns ratio of the transformer.

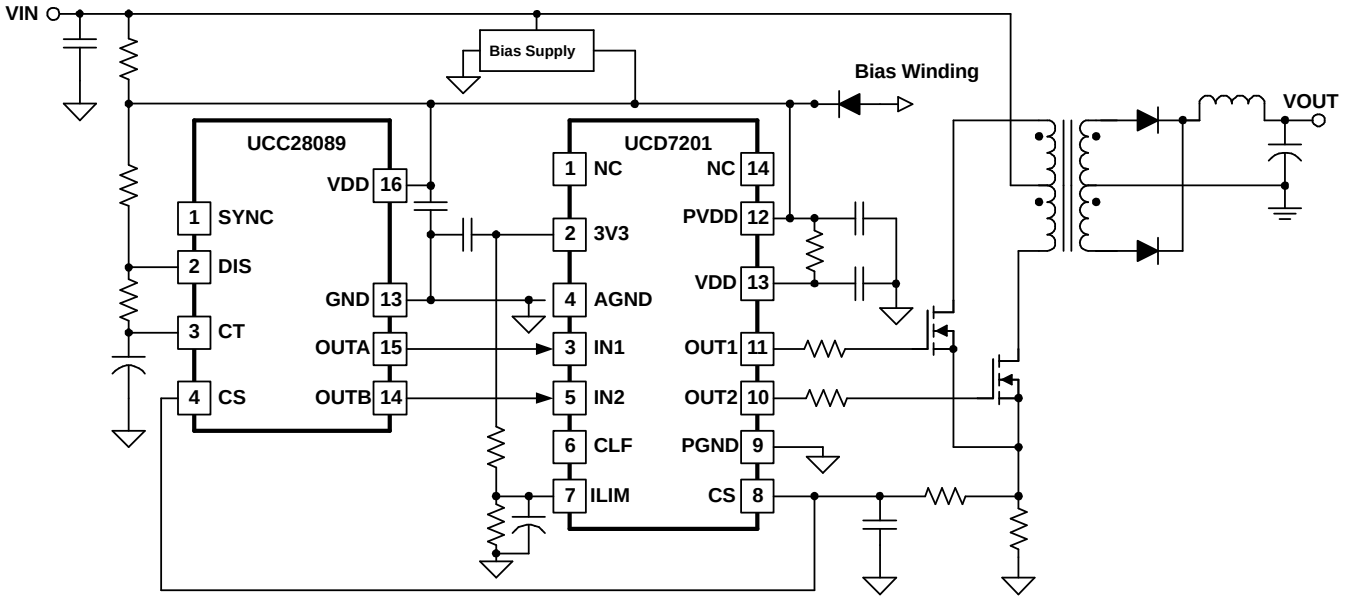


Figure 3. Intermediate Bus Converter

Typical Characteristics

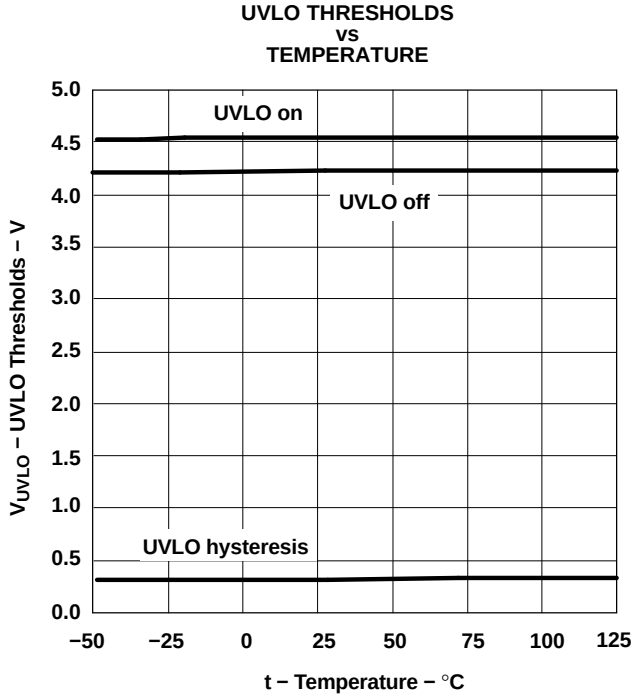


Figure 4.

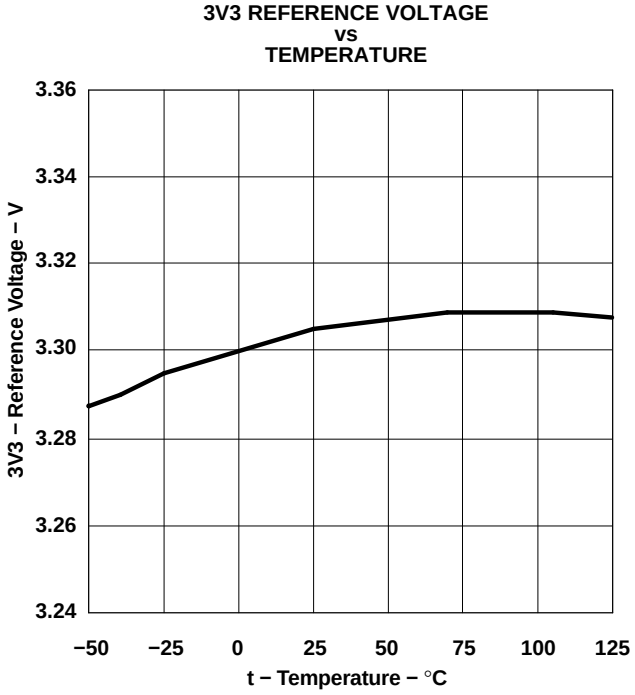


Figure 5.

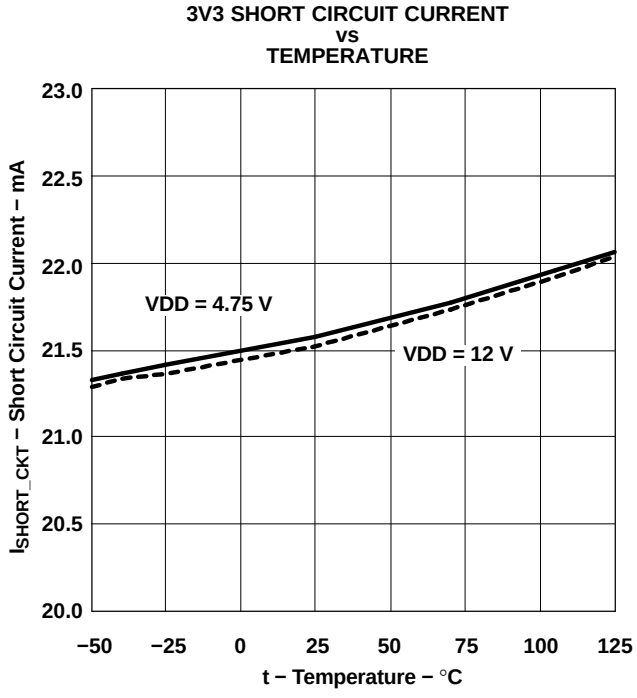


Figure 6.

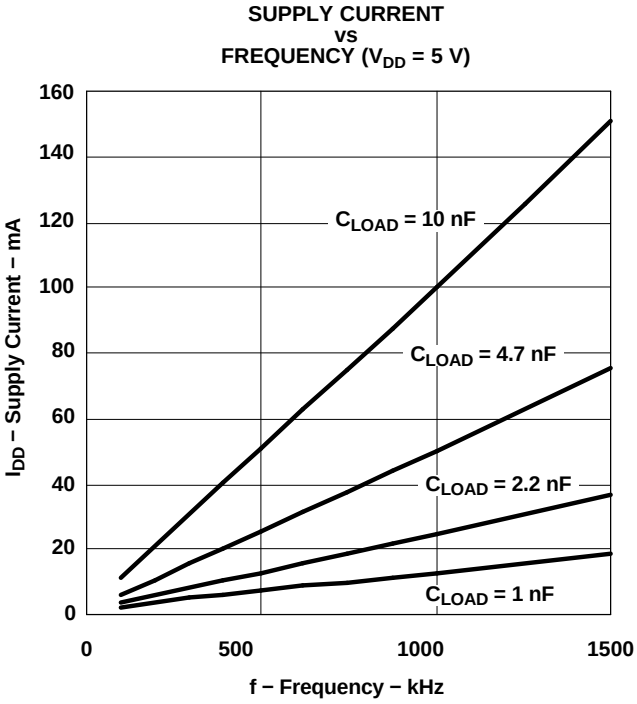


Figure 7.

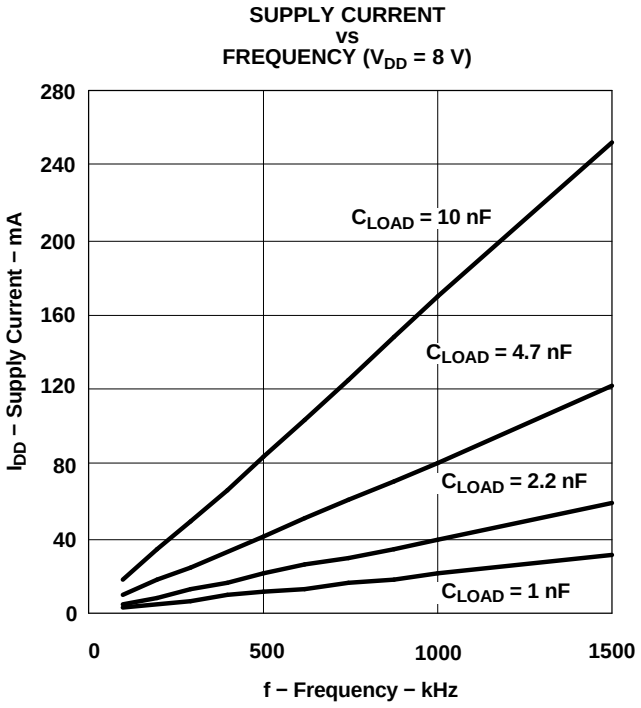
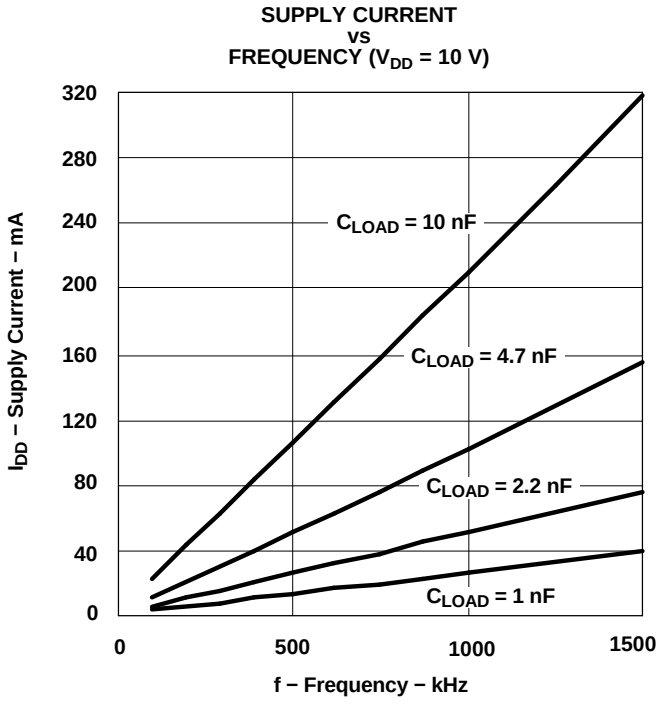


Figure 8.



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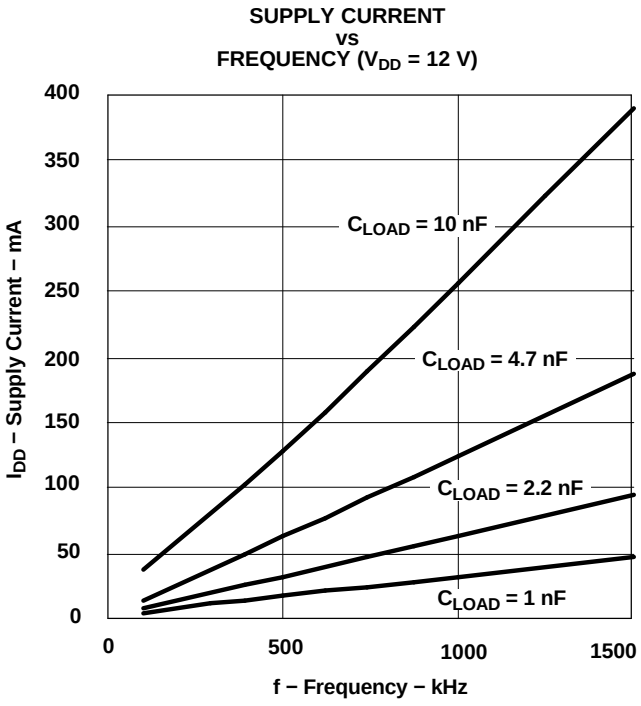

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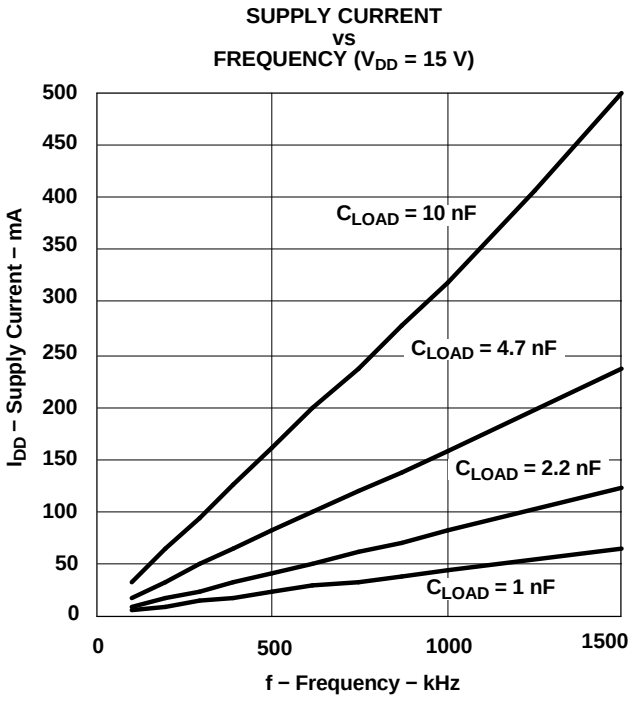

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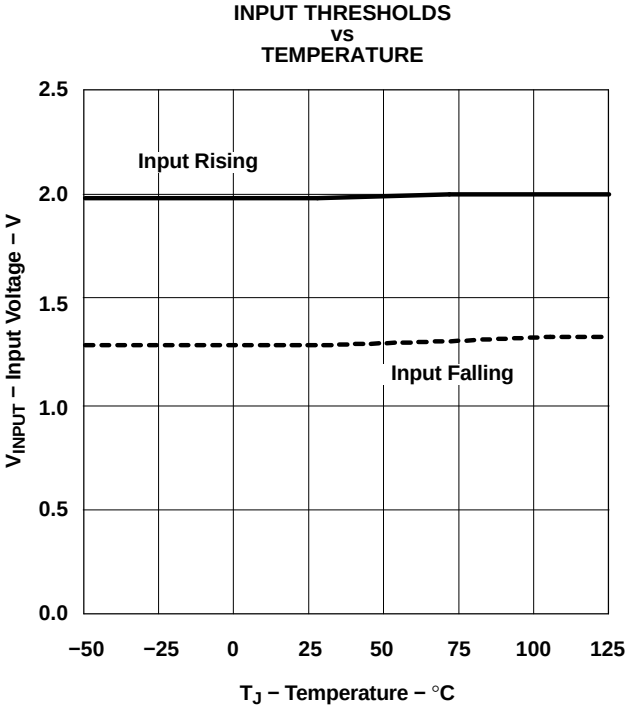

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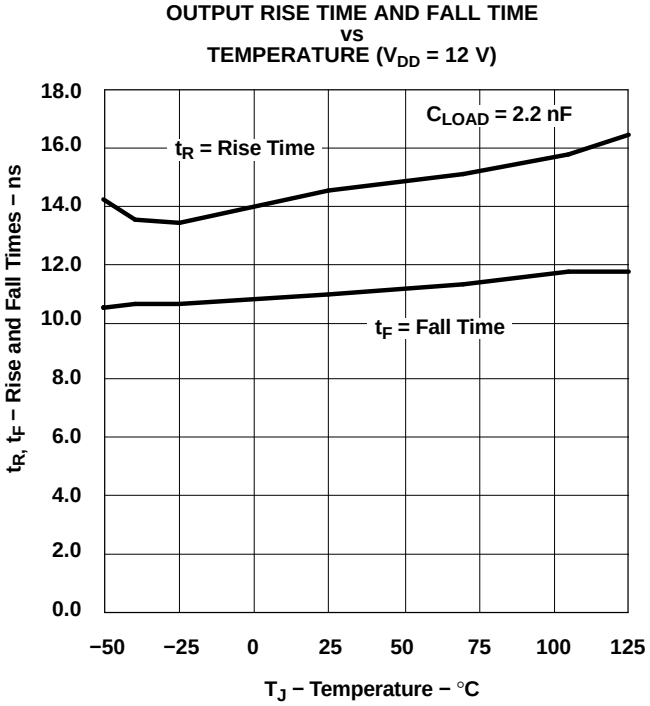

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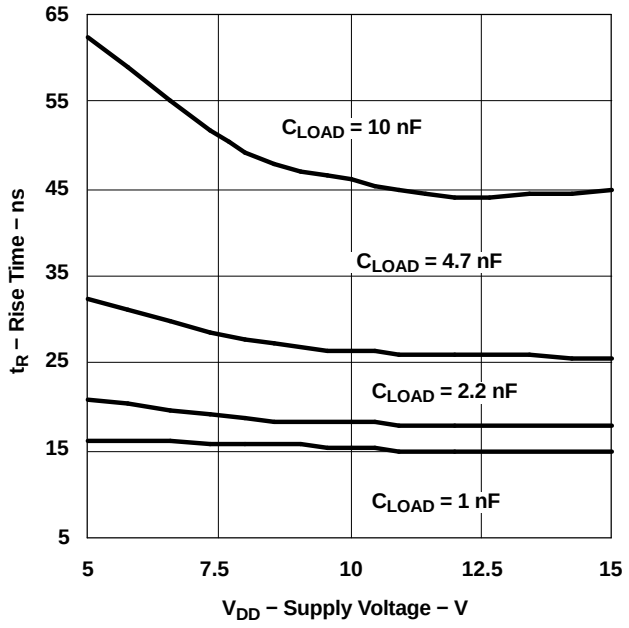

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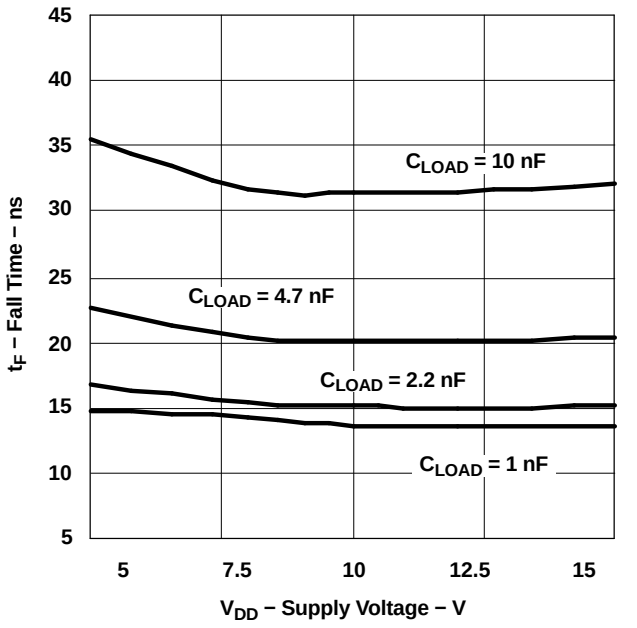


Figure 15.

IN to OUTx PROPAGATION DELAY RISING
vs
SUPPLY VOLTAGE

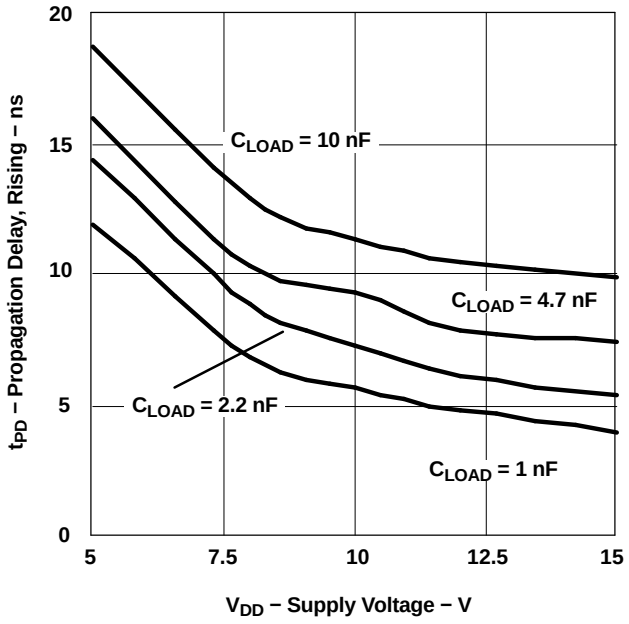


Figure 16.

IN to OUTx PROPAGATION DELAY FALLING
vs
SUPPLY VOLTAGE

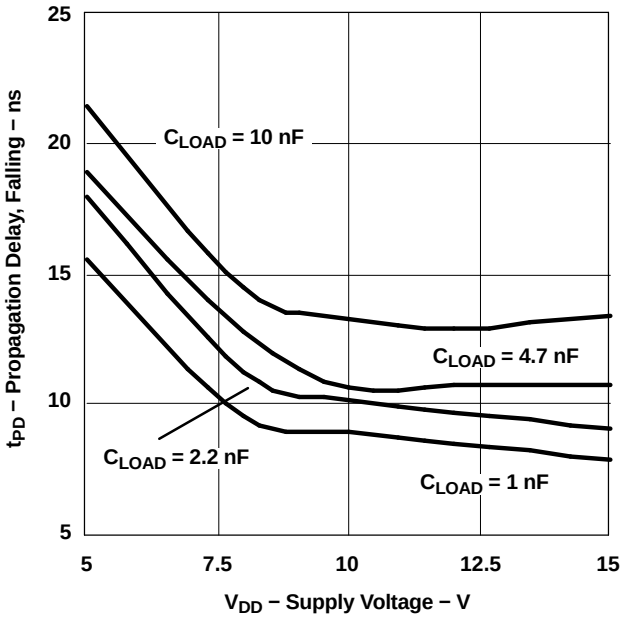


Figure 17.

DEFAULT CURRENT LIMIT THRESHOLD
vs
TEMPERATURE

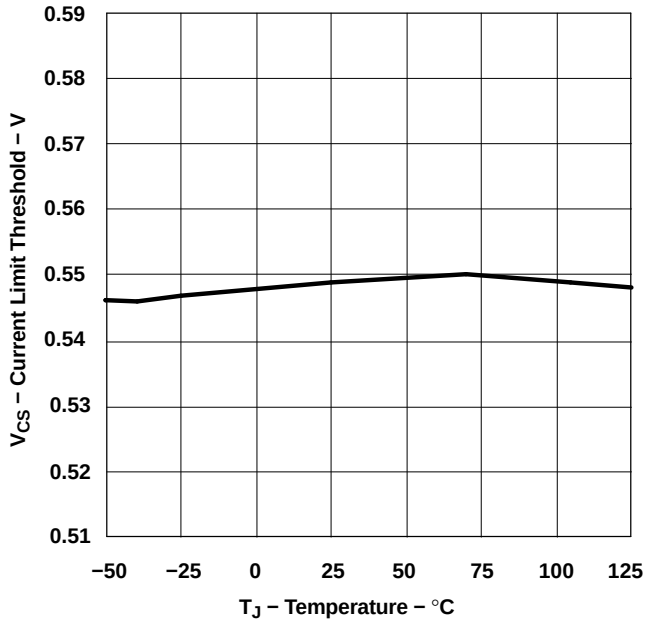


Figure 18.

CS TO OUTx PROPAGATION DELAY
vs
TEMPERATURE

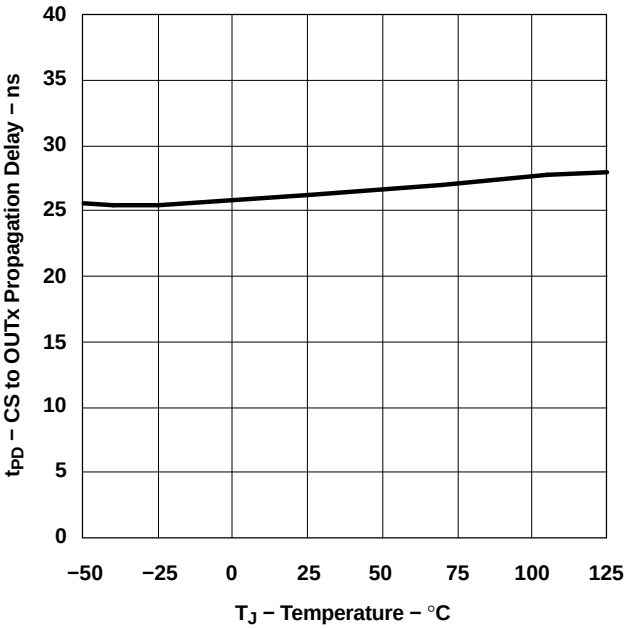


Figure 19.

CS TO CLF PROPAGATION DELAY
vs
TEMPERATURE

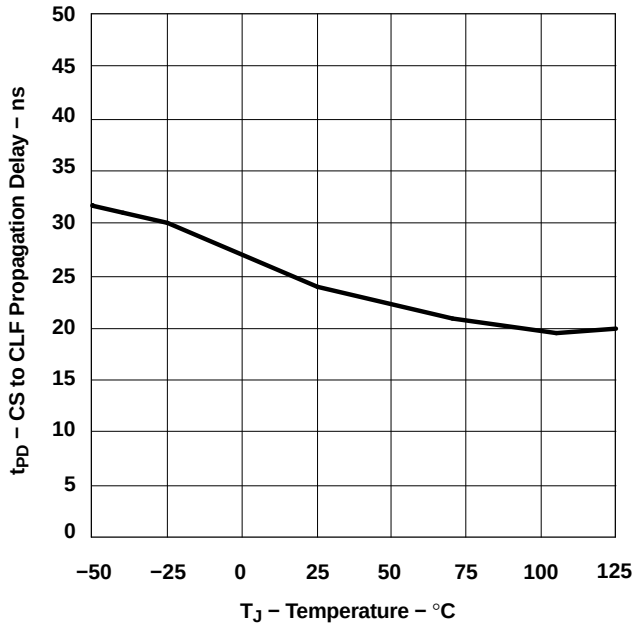


Figure 20.

IN TO OUT PROPAGATION DELAY
vs
TEMPERATURE

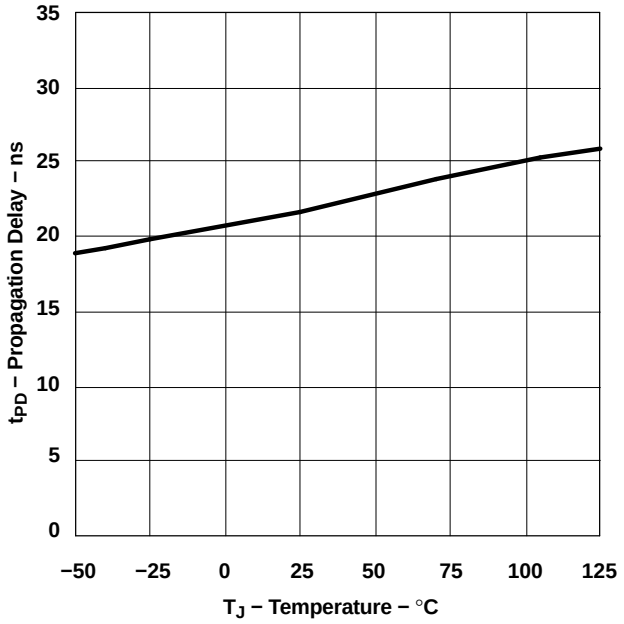
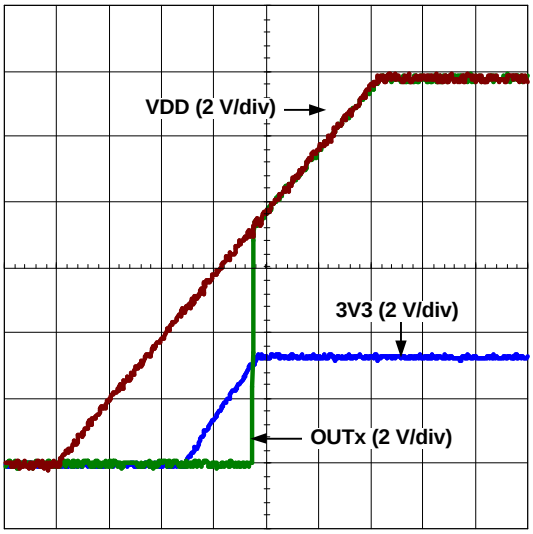


Figure 21.

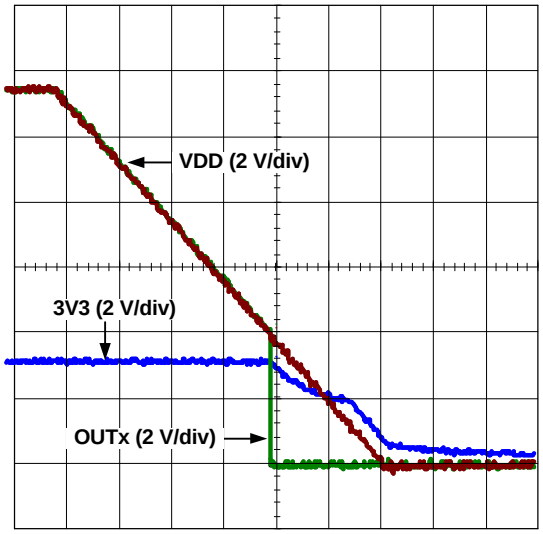
START-UP BEHAVIOR AT V_{DD} = 12 V (INPUT TIED TO 3V3)



t – Time – 40 μs/div

Figure 22.

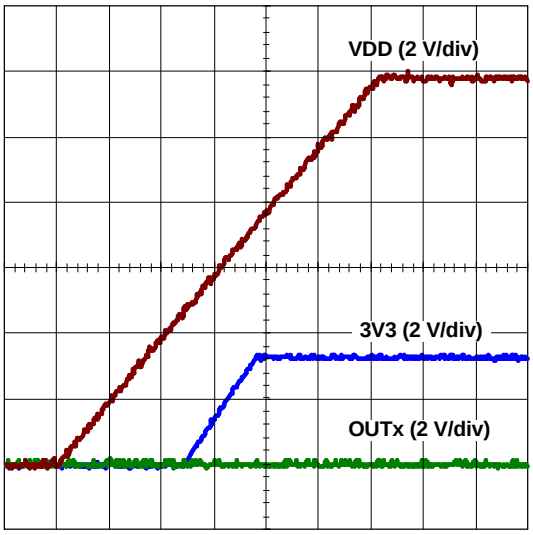
SHUT DOWN BEHAVIOR AT V_{DD} = 12 V (INPUT TIED TO 3V3)



t – Time – 40 μs/div

Figure 23.

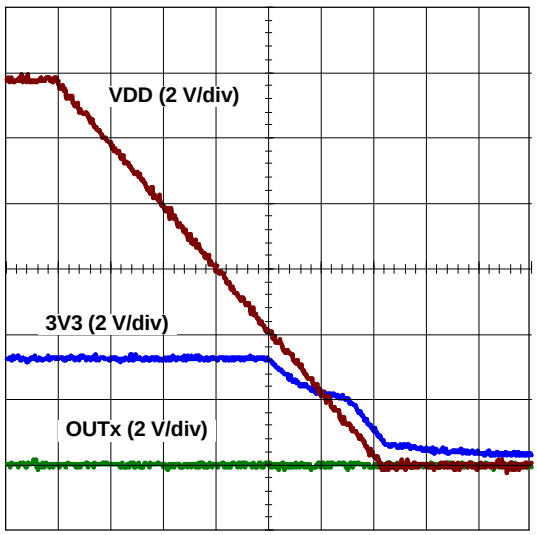
START-UP BEHAVIOR AT V_{DD} = 12 V (INPUT SHORTED TO GND)



t – Time – 40 μs/div

Figure 24.

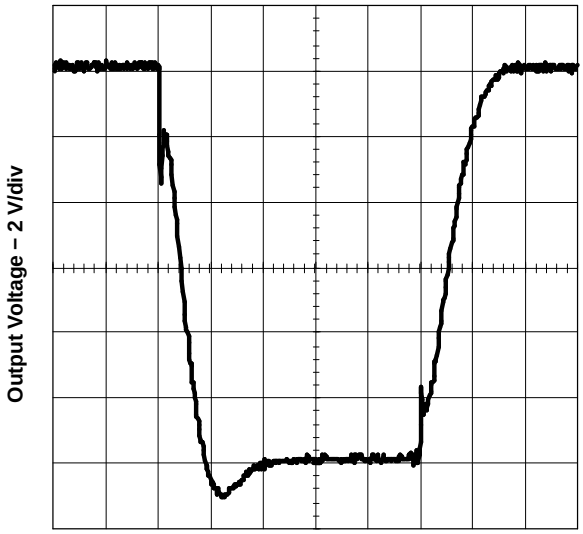
SHUT DOWN BEHAVIOR AT V_{DD} = 12 V (INPUT SHORTED TO GND)



t – Time – 40 μs/div

Figure 25.

OUTPUT RISE AND FALL TIME (V_{DD} = 12 V, C_{LOAD} = 10 nF)



t – Time – 40 ns/div

Figure 26.

REFERENCES

1. Power Supply Seminar SEM-1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
2. Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002
3. Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004

RELATED PRODUCTS

TEMPERATURE RANGE	CURRENT SENSE LIMIT PER CHANNEL	FEATURES
UCD7100	Single Low Side ±4-A Driver with Independent CS	3V3, CS(1)(2)
UCD7200	Dual Low Side ±4-A Drivers with Independent CS	3V3, CS(1)(2)
UCD7230	±4-A Synchronous Buck Driver with CS	3V3, CS(1)(2)
UCD7500	Single Low Side ±4-A Driver with CS and 110-V High Voltage Startup	3v3, CS, HVS110 (1)(2)(3)
UCD7600	Dual Low Side ±4-A Drivers with Independent CS and 110-V High Voltage Startup	3V3, CS, HVS110 (1)(2)(3)
UCD7601	Dual Low Side ±4-A Drivers with Common CS and 110-V High Voltage Startup	3V3, CCS, HVS110 (1)(4)(3)
UCD9110	Digital Power Controller for High Performance Single-loop Applications	
UCD9501	Digital Power Controller for High Performance Multi-Loop Applications	

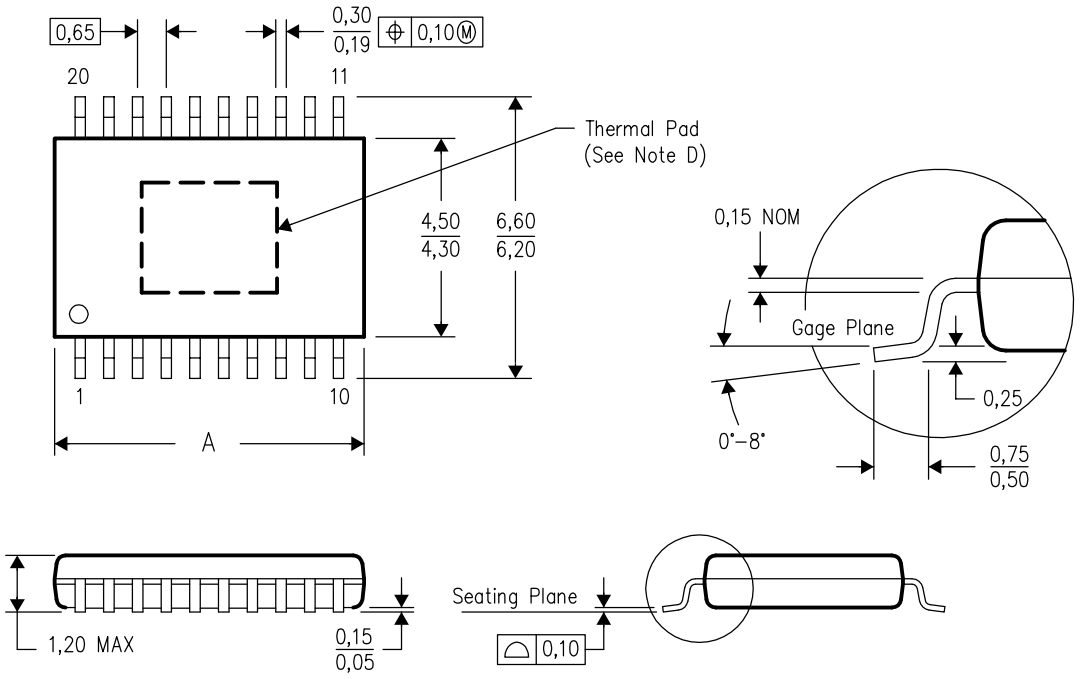
(1) 3V3 = 3.3-V linear regulator.
(2) CS = current sense and current limit function.
(3) HVS110 = 110-V high voltage startup circuit.
(4) CCS = Common current sense and current limit function.

REVISION HISTORY

DATE	REVISION	CHANGE DESCRIPTION
3/4/05	SLUS645	Initial release of preliminary datasheet.
4/1/05	SLUS645A	Updated packaging information.
7/14/05	SLUS645B	Initial release of production datasheet. Updated specification and application information.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



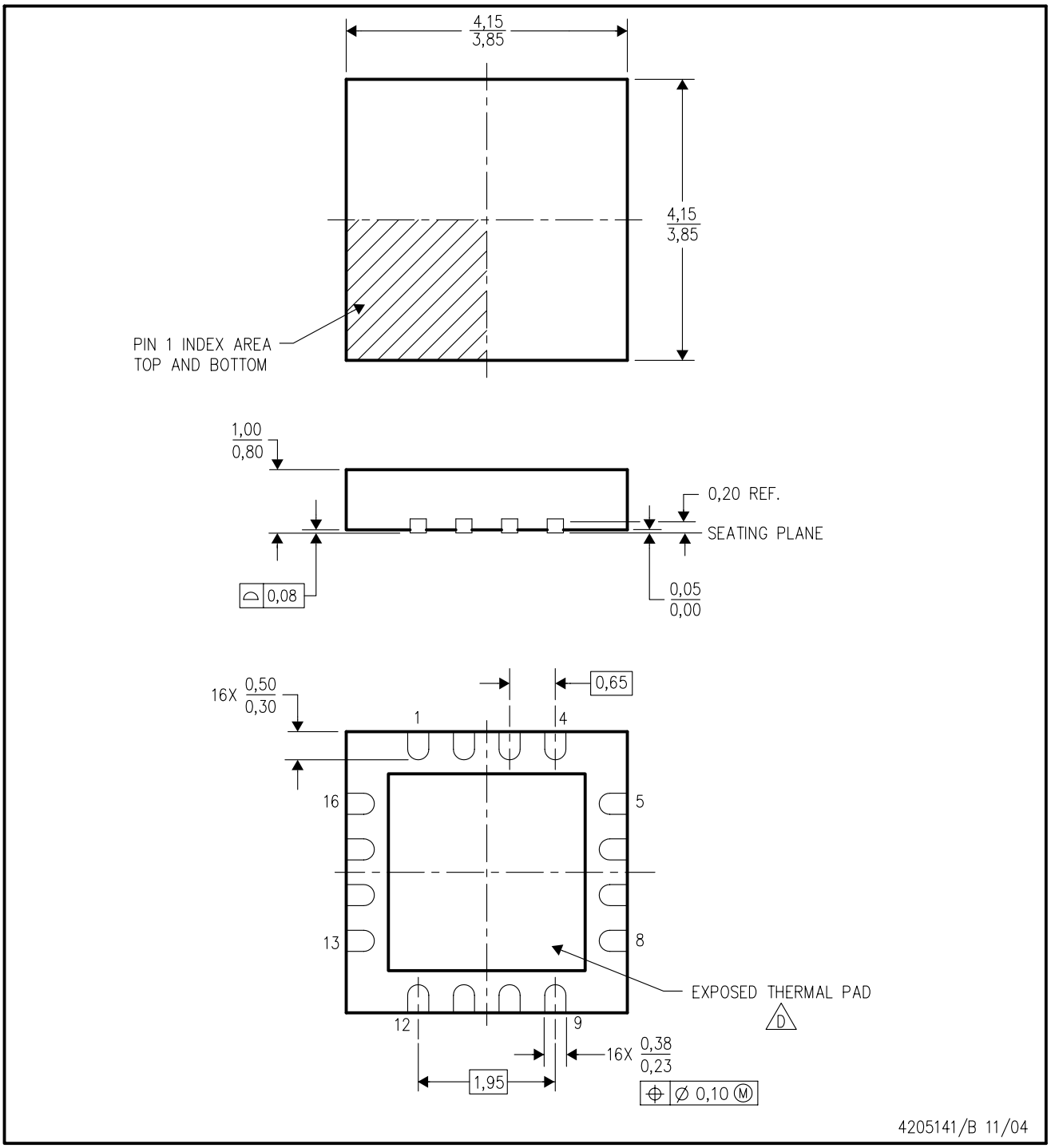
DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

RSA (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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