DIGITALLY MANAGED PUSH-PULL ANALOG PWM CONTROLLERS

FEATURES

- For Digitally Managed Power Supplies Using μCs or the TMS320 ™ DSP Family
- Voltage or Peak Current Mode Control with Cycle-by-Cycle Current Limiting
- Clock input from Digital Controller to set Operating Frequency and Max Duty Cycle
- Analog PWM Comparator
- 2-MHz Switching Frequency
- 110-V Input Startup Circuit and Thermal Shutdown (UCD8620)
- Internal Programmable Slope Compensation
- 3.3-V, 10-mA Linear Regulator
- DSP/μC Compatible Inputs
- Dual ±4-A TrueDrive™ High Current Drivers
- 10-ns Typical Rise and Fall Times with 2.2-nF
- 25-ns Input-to-Output Propagation Delay
- 25-ns Current Sense-to-Output Propagation Delay
- Programmable Current Limit Threshold
- Digital Output Current Limit Flag
- 4.5-V to 15.5-V Supply Voltage Range
- Rated from -40°C to 105°C

APPLICATIONS

- Digitally Managed Switch Mode Power Supplies
- Push-Pull, Half-Bridge, or Full-Bridge Converters
- Battery Chargers

DESCRIPTION

The UCD8220 and UCD8620 are members of the UCD8K family of analog pulse-width modulator devices to be used in digitally managed power supplies using a microcontroller or the TMS320™ DSP family.

UCD8220 and UCD8620 are double-ended PWM controllers configured with push-pull drive logic. The UCD8620 has a 110-V high-voltage startup circuit which can directly start up the controller from a 48-V telecom input line.

Systems using UCD8K devices close the PWM feedback loop with traditional analog methods, but the UCD8K controllers include circuitry to interpret a time-domain digital pulse train. The pulse train contains the operating frequency and maximum duty cycle limit which are used to control the power supply operation. This eases implementation of a converter with high level control features without the added complexity or possible PWM resolution limitations of closing the control loop in the discrete time domain.

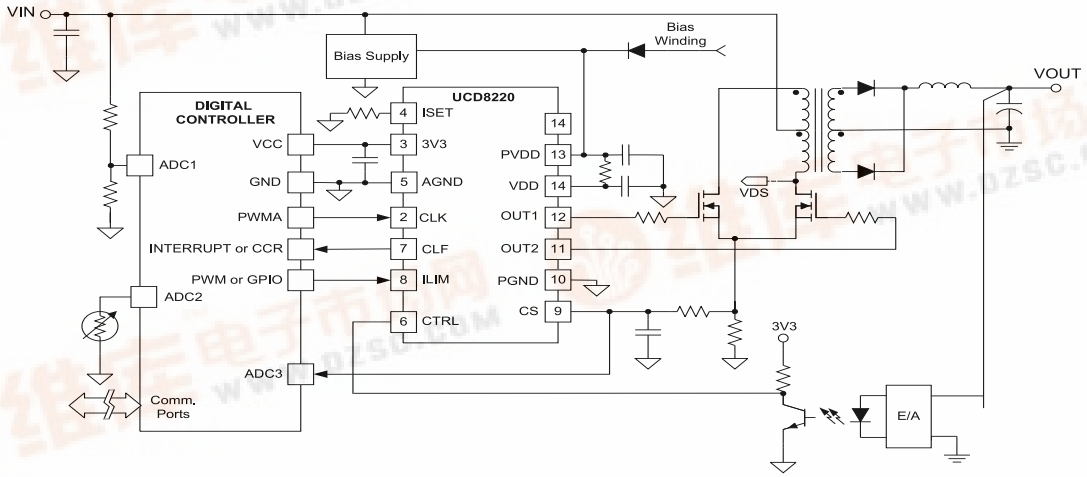


Figure 1. UCD8220 Typical Simplified Push-Pull Converter Application Schematic

DESCRIPTION (continued)

The UCD8220 and UCD8620 can be configured for either peak current mode or voltage mode control. They provide a programmable current limit function and a digital output current limit flag which can be monitored by the host controller to set the current limit operation. For fast switching speeds, the output stages use the TrueDrive™ architecture, which delivers rated current of ±4 A into the gate of a MOSFET. Finally they also include a 3.3-V, 10-mA linear regulator to provide power to the digital controller or act as a reference in the system.

The UCD8K controller family is compatible with the standard 3.3-V I/O ports of UCD9K digital power controllers, DSPs, Microcontrollers, or ASICs and is offered in PowerPAD™ HTSSOP and QFN packages.

SIMPLIFIED APPLICATION DIAGRAMS

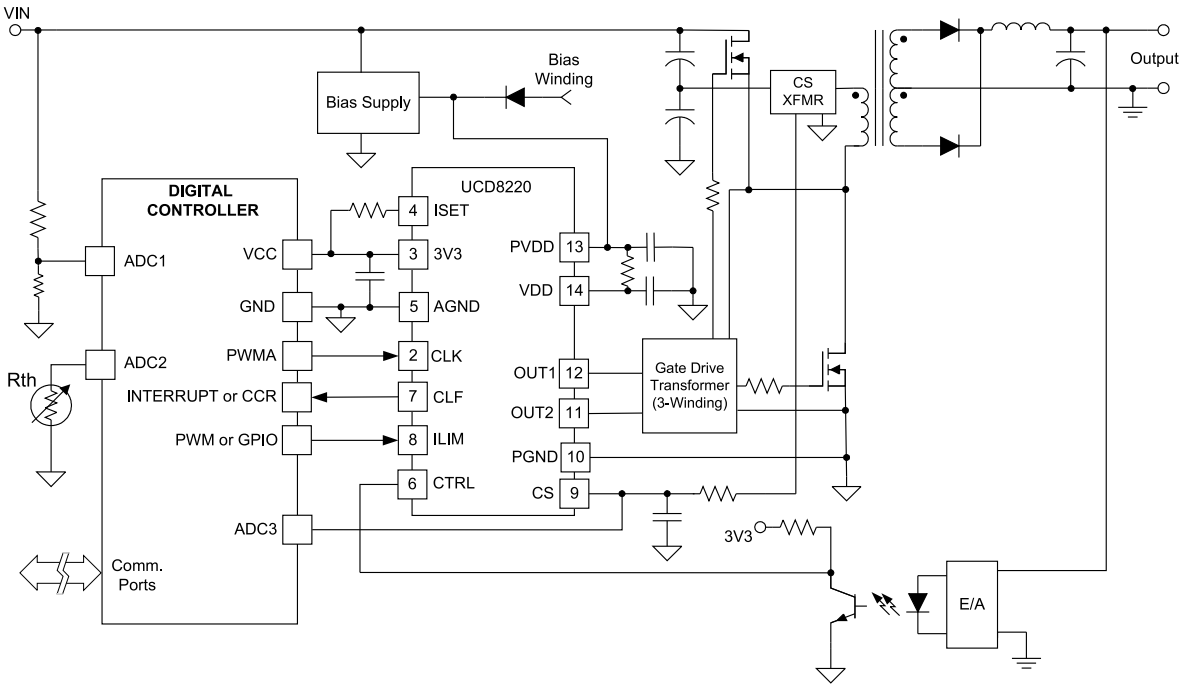


Figure 2. UCD8220 Typical Simplified Half-Bridge Converter Application Schematic

SIMPLIFIED APPLICATION DIAGRAMS (continued)

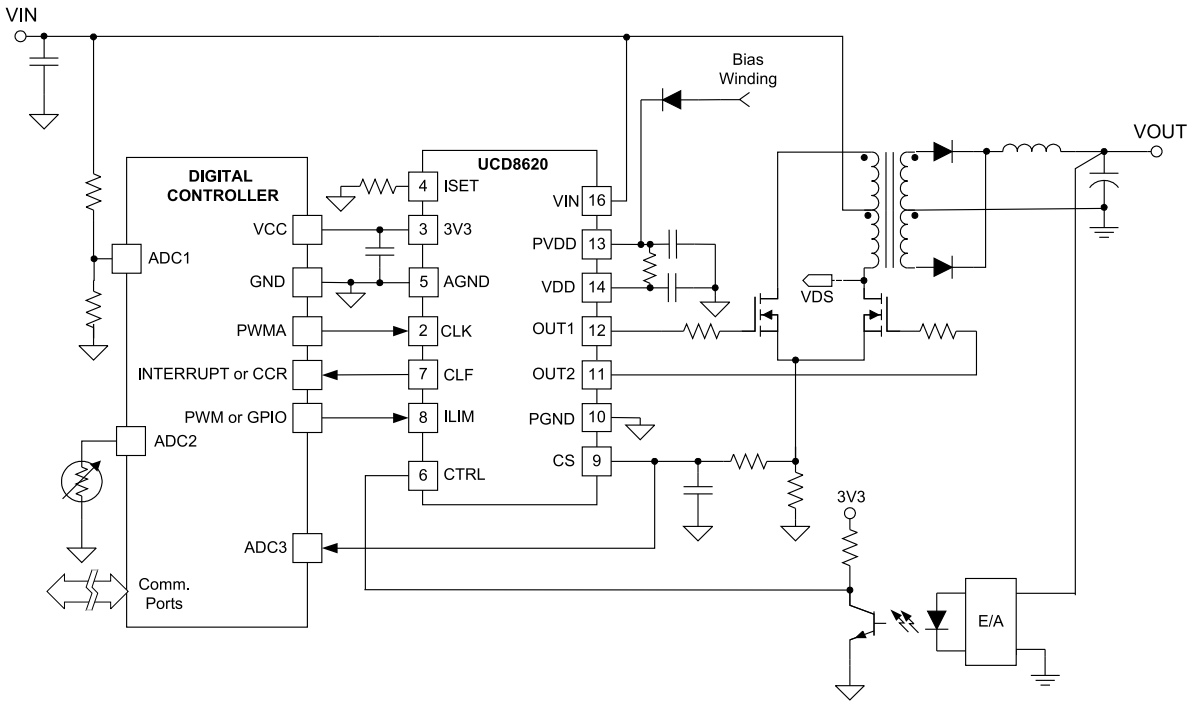


Figure 3. UCD8620 Typical Simplified Push-Pull Converter Application Schematic

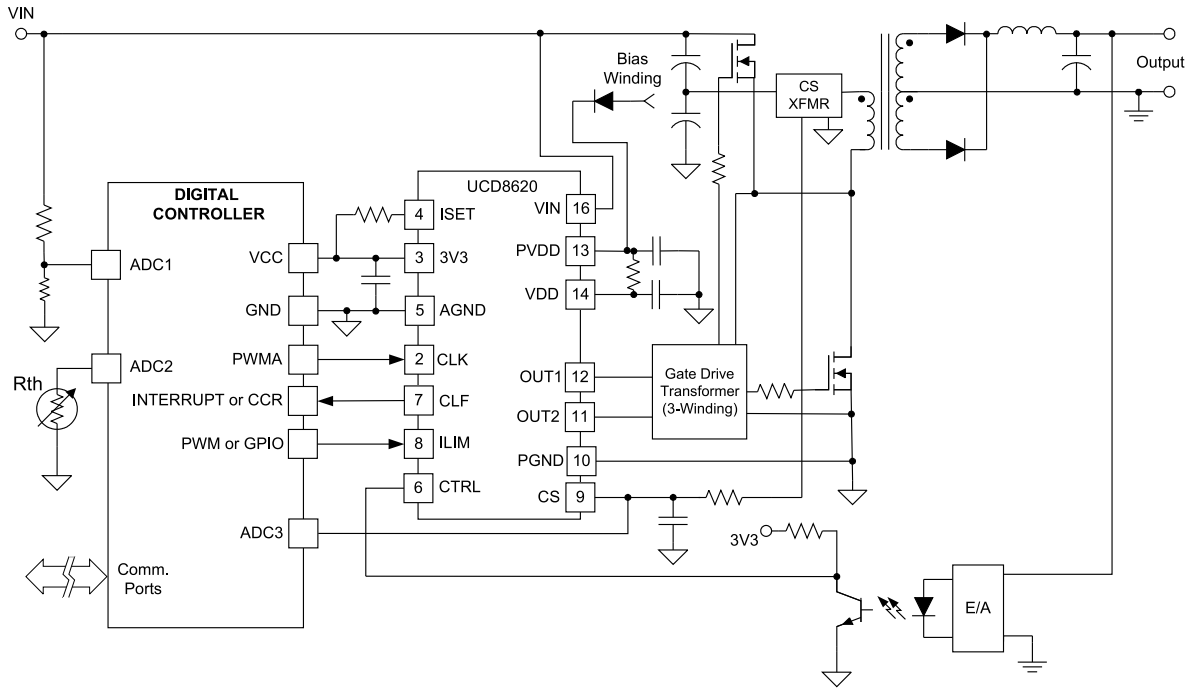
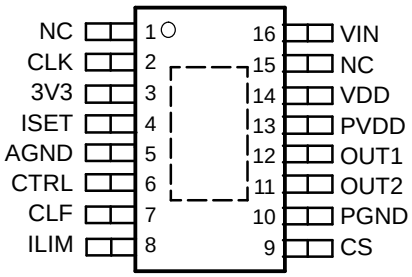


Figure 4. UCD8620 Typical Simplified Half-Bridge Converter Application Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

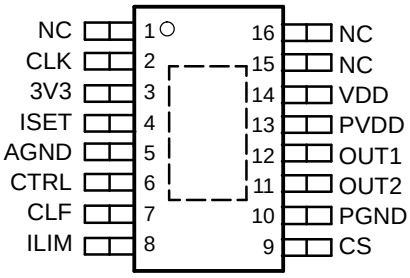
CONNECTION DIAGRAMS

HTSSOP PACKAGE (PWP −16)
UCD8620 (TOP VIEW)



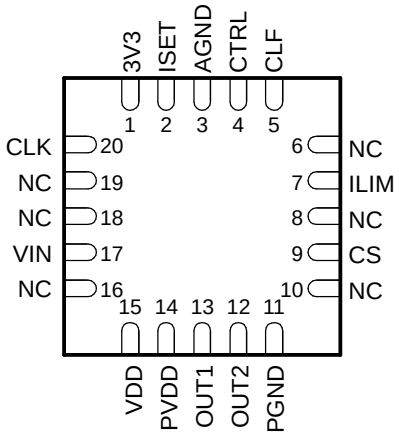
NC − No internal connection

HTSSOP PACKAGE (PWP −16)
UCD8220 (TOP VIEW)

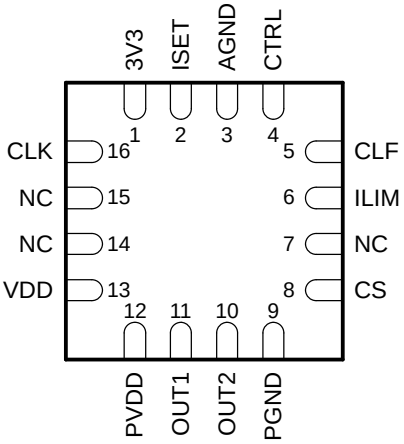


NC − No internal connection

QFN PACKAGE (RGW−20)
UCD8620 (BOTTOM VIEW)



QFN PACKAGE (RSA−16)
UCD8220 (BOTTOM VIEW)



ORDERING INFORMATION

TEMPERATURE RANGE	110-V HV STARTUP CIRCUIT	PACKAGED DEVICES(1)(2)(3)		
		PowerPAD™ HTSSOP-16 (PWP)	QFN-16 (RSA)(4)	QFN-20 (RGW)
-40°C to 105°C	No	UCD8220PWP	UCD8220RSA	-
	Yes	UCD8620PWP(5)	-	UCD8620RGW

(1) HTSSOP-16 (PWP), QFN-16 (RSA), and QFN-20 (RGW) packages are available taped and reeled. Add R suffix to device type (e.g. UCD8620PWPR) to order quantities of 2,000 devices per reel for the PWP package and 1,000 devices per reel for the RSA and RGW packages.
(2) These products are packaged in Pb-Free and Green lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(4) Contact factory for availability of QFN packaging.
(5) Product preview stage of development.

PACKAGING INFORMATION

PACKAGE	SUFFIX	θ_{JC}(°C/W)	θ_{JA}(°C/W)	POWER RATING T_A = 70°C, T_J = 125°C (mW)	RATING FACTOR ABOVE 70°C (mW/°C)
PowerPad™ MSSOP-16	PWP	2.07	37.47(1)	1470	27
QFN-16	RSA	-	-	-	-
QFN-20	RGW	-	-	-	-

(1) PowerPad™ soldered to the PWB with TI recommended PWB as defined in TI's Application Report (TI Literature Number SLMA002) with OLFM.

ABSOLUTE MAXIMUM RATINGS(1)(2)

SYMBOL	PARAMETER		UCD8x20	UNIT
V_I	Input Line Voltage	UCD8620 only	110	V
V_{DD}	Supply Voltage		16	
I_{DD}	Supply Current	Quiescent	20	mA
		Switching, T_A = 25°C, T_J = 125°C, V_{DD} = 12 V	200	
V_O	Output Gate Drive Voltage	OUT	-1 to PVDD	V
$I_{O(sink)}$	Output Gate Drive Current	OUT	4.0	A
$I_{O(source)}$			-4.0	
	Analog Input	ISET, CS, CTRL, ILIM	-0.3 to 3.6	V
	Digital I/O's	CLK, CLF	-0.3 to 3.6	
	Power Dissipation	T_A = 25°C (PWP-16 package)	2.67	W
		T_A = 25°C (QFN-16 package)	-	
		T_A = 25°C (QFN-20 package)	-	
T_J	Junction Operating Temperature	UCD8220	-55 to 150	°C
		UCD8620	-55 to 130	
T_{stg}	Storage Temperature		-65 to 150	
HBM	ESD Rating(3)	Human body model	2000	V
CDM		Change device model	500	
	Lead Temperature (Soldering, 10 sec)		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
(3) Tested to JEDEC standard EIA/JESD22 - A114-B.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to AGND, 1 µF from PVDD to PGND, 0.22-µF capacitor from 3V3 to AGND, $T_A = T_J$ = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY SECTION						
Supply current, OFF	V_{DD} = 4.2 V	UCD8620		500	800	µA
		UCD8220		300	500	
Supply current, ON	(UCD8620), outputs not switching, CLK = low		2		3	mA
	(UCD8220), outputs not switching, CLK = low		2		3	
LOW VOLTAGE UNDERVOLTAGE LOCKOUT (UCD8220 only)						
V_{DD} UVLO ON			4.25	4.5	4.75	V
V_{DD} UVLO OFF			4.05	4.25	4.45	
V_{DD} UVLO hysteresis			150	250	350	mV
110-V HIGH VOLTAGE UNDERVOLTAGE LOCKOUT AND JFET CONTROL (UCD8620 ONLY)						
V_{DD} UVLO ON			12.5	13	13.5	V
V_{DD} UVLO OFF			7	7.5	8	
JFET turn-off threshold (V_{START_JFET})	No switching, JFET on at startup		12.5	13	13.5	
JFET turn-on threshold	No switching		11.5	12	12.5	
JFET on/off hysteresis				1		
High voltage JFET current	V_{DD} < 5 V, VIN = 18 V to 76 V		3	5	8	mA
	V_{DD} = 12 V, VIN = 18 V to 76 V			10		
Thermal shutdown, OFF (1)	V_{DD} = 5 V to 12 V		130	145	160	°C
Thermal shutdown, ON (1)	V_{DD} > 5 V		110	125	140	
REFERENCE / EXTERNAL BIAS SUPPLY						
3V3 initial set point	T_A = 25°C, I_{LOAD} = 0		3.267	3.3	3.333	V
3V3 set point over temperature			3.234	3.3	3.366	
3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, VDD = 5 V		-	1	6.6	mV
3V3 line regulation	VDD = 4.75 V to 12 V, I_{LOAD} = 10 mA		-	1	6.6	
Short circuit current	VDD = 4.75 to 12 V		11	20	35	mA
3V3 OK threshold, ON	3.3 V rising		2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling		2.7	2.8	2.9	
CLOCK INPUT (CLK)						
HIGH, positive-going input threshold voltage (VIT+)			1.65	-	2.08	V
LOW negative-going input threshold voltage (VIT-)			1.16	-	1.5	
Input voltage hysteresis, (VIT+ - VIT-)			0.6	-	0.8	
Frequency	OUTx = 1 MHz		-	-	2	MHz
Minimum allowable off time (1)					20	ns
SLOPE COMPENSATION (ISET)						
ISET Voltage	V_{ISET} , 3V3 = 3.3 V, +/-2%		1.78	1.84	1.90	V
m, V_{SLOPE} (I-Mode)	R_{ISET} = 6.19 kΩ to AGND, CS = 0.25 V, CTRL = 2.5 V		1.48	2.12	2.76	V/µs
	R_{ISET} = 100 kΩ to AGND, CS = 0.25 V, CTRL = 2.5 V		0.099	0.142	0.185	
	R_{ISET} = 499 kΩ to AGND, CS = 0.25 V, CTRL = 2.5 V		0.019	0.028	0.037	
m, V_{SLOPE} (V-Mode)	R_{ISET} = 4.99 kΩ to 3V3, CTRL = 2.5 V		1.44	2.06	2.68	
	R_{ISET} = 100 kΩ to 3V3, CTRL = 2.5 V		0.079	0.114	0.148	
	R_{ISET} = 402 kΩ to 3v3, CTRL = 2.5 V		0.019	0.027	0.035	

(1) Ensured by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to AGND, 1 µF from PVDD to PGND, 0.22-µF capacitor from 3V3 to AGND, $T_A = T_J$ = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISET resistor range	Current mode control; R_{ISET} connected to AGND	6.19		499	kΩ
ISET resistor range	Voltage mode control; R_{ISET} connected to 3V3	4.99		402	
ISET current range	Voltage mode control with Feed-Forward; R_{ISET} connected to VIN	3.7		300	µA
PWM					
PWM offset at CTRL input	3V3 = 3.3 V +/-2%	0.45	0.51	0.6	V
CTRL buffer gain (1)	Gain from CTRL to PWM comparator input		0.5		V/V
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.466	0.5	0.536	V
ILIM maximum current limit threshold	ILIM = 3.3 V	0.975	1.025	1.075	V
ILIM current limit threshold	ILIM = 0.75 V	0.700	0.725	0.750	
ILIM minimum current limit threshold	ILIM = 0.25 V	0.21	0.23	0.25	V
CLF output high level	CS > ILIM , I_{LOAD} = -7 mA	2.64	-	-	V
CLF output low level	CS ≤ ILIM, I_{LOAD} = 7 mA	-	-	0.66	
Propagation delay from CLK to CLF	CLK rising to CLF falling after a current limit event	-	15	25	ns
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current		-	–1	-	µA
Propagation delay from CS to OUTx	ILIM = 0.5 V, measured on OUTx, CS = threshold + 60 mV	-	25	40	ns
Propagation delay from CS to CLF	ILIM = 0.5 V, measured on CLF, CS = threshold + 60 mV	-	25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	CLK = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current (2)	V_{DD} = 12 V, CLK = high, OUTx = 5 V	-	4	-	A
Sink current (2)	V_{DD} = 12 V, CLK = low, OUTx = 5 V	-	4	-	
Source current (2)	V_{DD} = 4.75 V, CLK = high, OUTx = 0	-	2	-	
Sink current (2)	V_{DD} = 4.75 V, CLK = low, OUTx = 4.75 V	-	3	-	
Rise time, t_R	C_{LOAD} = 2.2 nF, V_{DD} = 12 V	-	10	20	ns
Fall time, t_F	C_{LOAD} = 2.2 nF, V_{DD} = 12 V	-	10	15	
Output with V_{DD} < UVLO	V_{DD} = 1.0 V, I_{SINK} = 10 mA	-	0.8	1.2	V
Propagation delay from CLK to OUTx	C_{LOAD} = open, V_{DD} = 12 V, CLK rising, t_{D1}	-	25	35	ns
	C_{LOAD} = open, V_{DD} = 12 V, CLK falling, t_{D2}		25	35	

(2) Ensured by design. Not 100% tested in production.

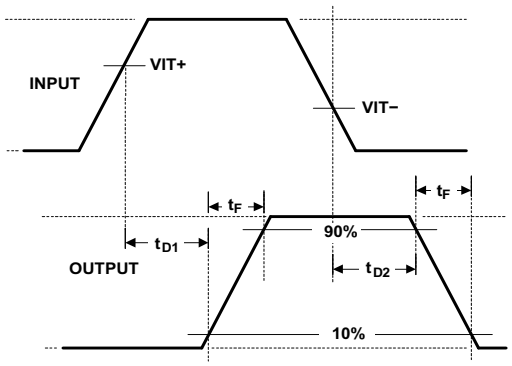


Figure 5. Timing Diagram

FUNCTIONAL BLOCK DIAGRAMS

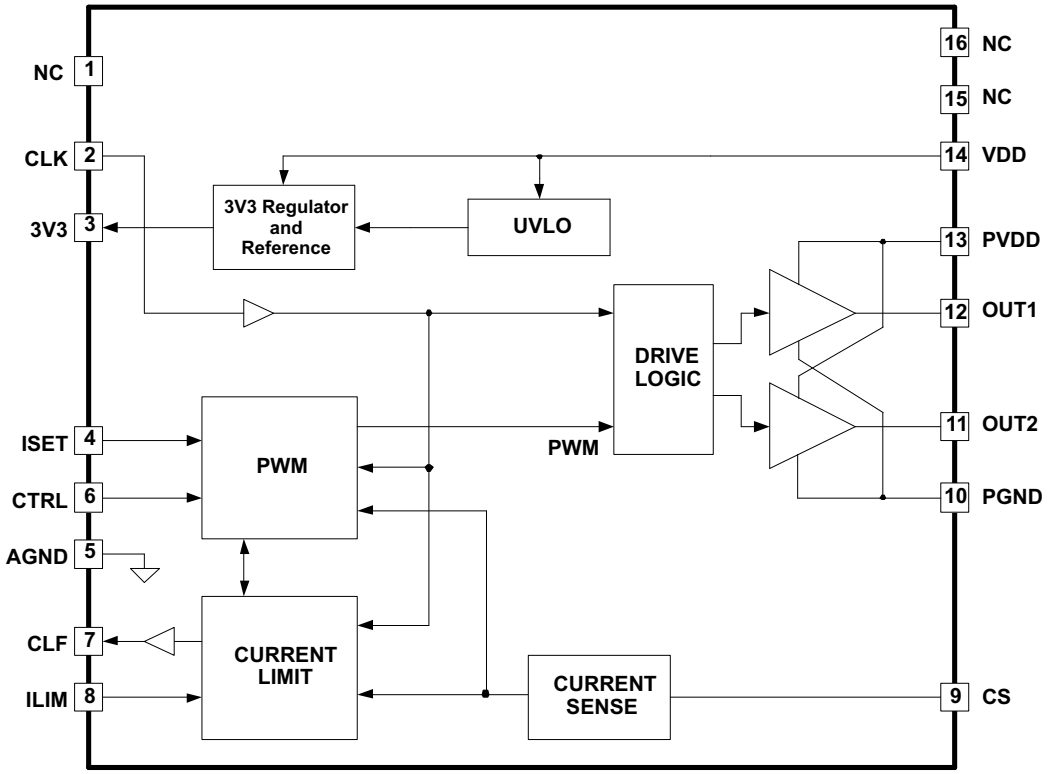


Figure 6. UCD8220

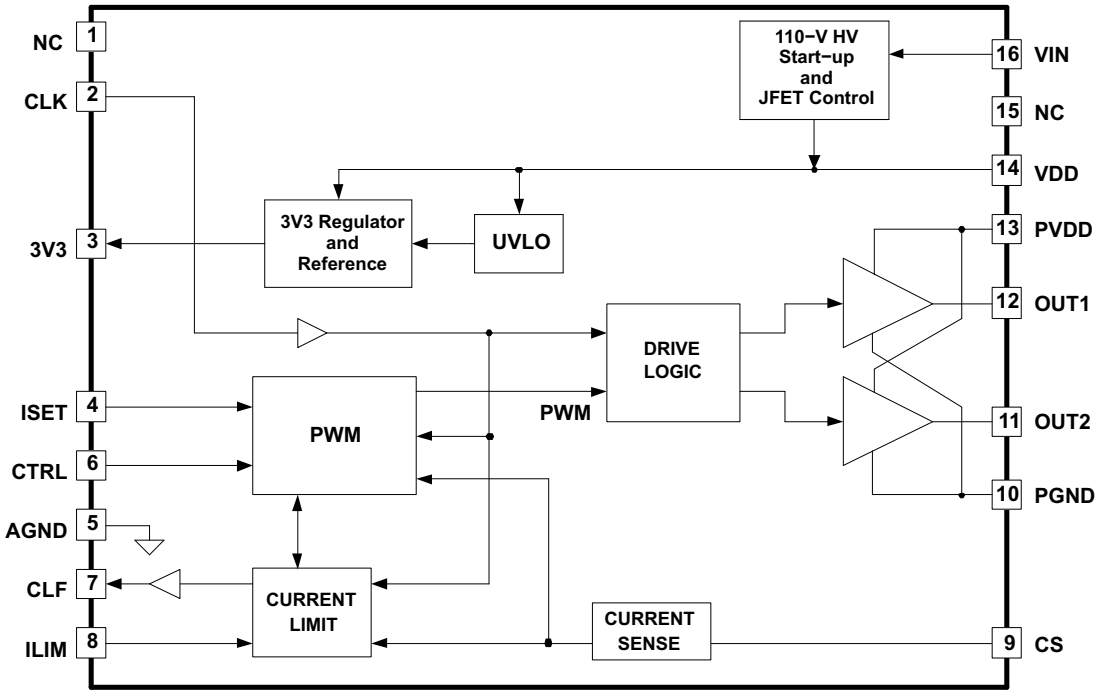


Figure 7. UCD8620

TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER				I/O	FUNCTION
	UCD8220		UCD8620			
	HTSSOP-16 (PWP)	QFN-16 (RSA)	HTSSOP-16 (PWP)	QFN-20 (RGW)		
CLK	2	16	2	20	I	Clock. Input pulse train contains operating frequency and maximum duty cycle limit. This pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry CLK 2 16 2 20 I from any external noise.
CLF	7	5	7	5	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on the CLK pin. This signal is also used for the start-up handshaking between the Digital controller and the analog controller
ISET	4	2	4	2	I	Pin for programming the current used to set the amount of slope compensation in Peak-Current Mode control or to set the frequency in voltage mode control.
3V3	3	1	3	1	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place 0.22 μF of ceramic capacitance from this pin to analog ground.
AGND	5	3	5	3	-	Analog ground return
ILIM	8	6	8	7	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V. The default value while open is 0.5 V.
CTRL	6	4	6	4	I	Input for the error feedback voltage from the external error amplifier. This input is multiplied by 0.5 and routed to the negative input of the PWM comparator
NC	1, 15, 16	7, 14, 15	1, 15	6, 8, 10, 16, 18, 19	-	No connection.
CS	9	8	9	9	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
PGND	10	9	10	11	-	Power ground return. This pin should be connected close to the source of the power MOSFET.
OUT2	11	10	11	12	O	The high-current TrueDrive™ driver output.
OUT1	12	11	12	13	O	The high-current TrueDrive™ driver output.
PVDD	13	12	13	14		Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. The bypass capacitor for this pin should be returned to PGND.
VDD	14	13	14	15	I	Supply input pin to power the control circuitry. Bypass the pin with at least 4.7 μF of capacitance, returned to AGND.
VIN	-	-	16	17	I	Input to the internal start-up circuitry rated to 110 V. This pin connects directly to the input power rail.

TYPICAL CHARACTERISTICS

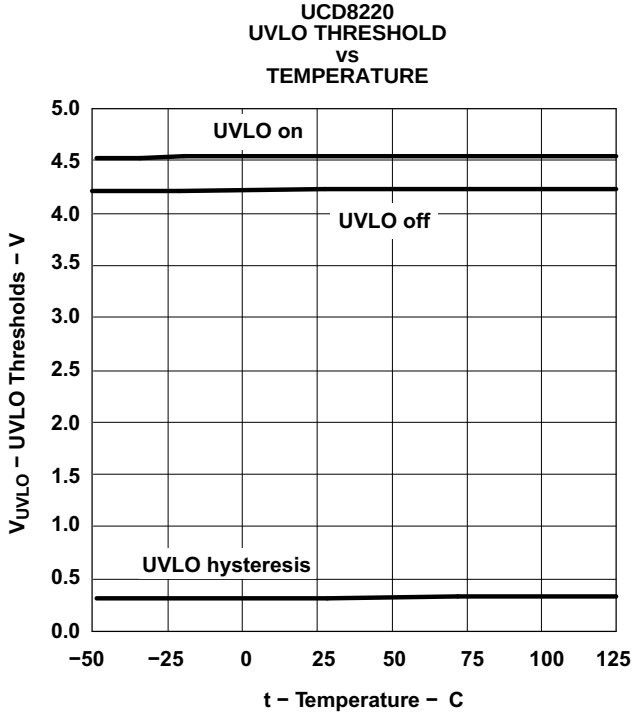


Figure 8.

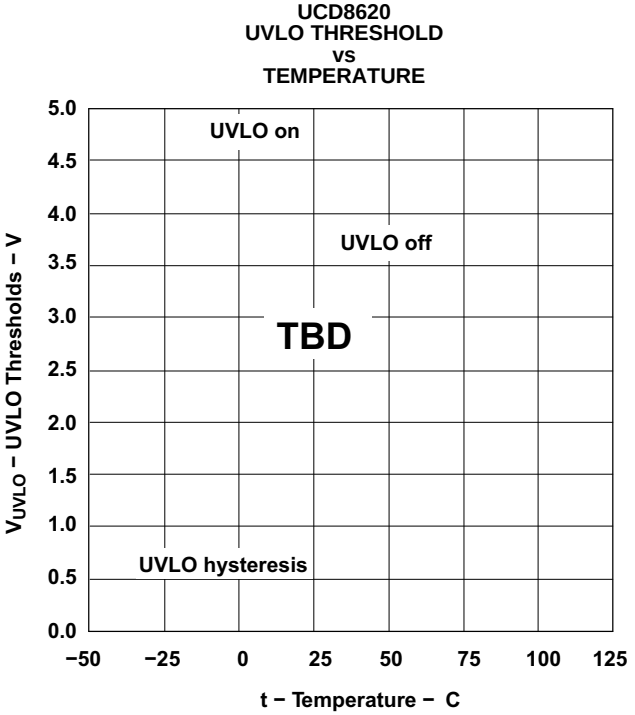


Figure 9.

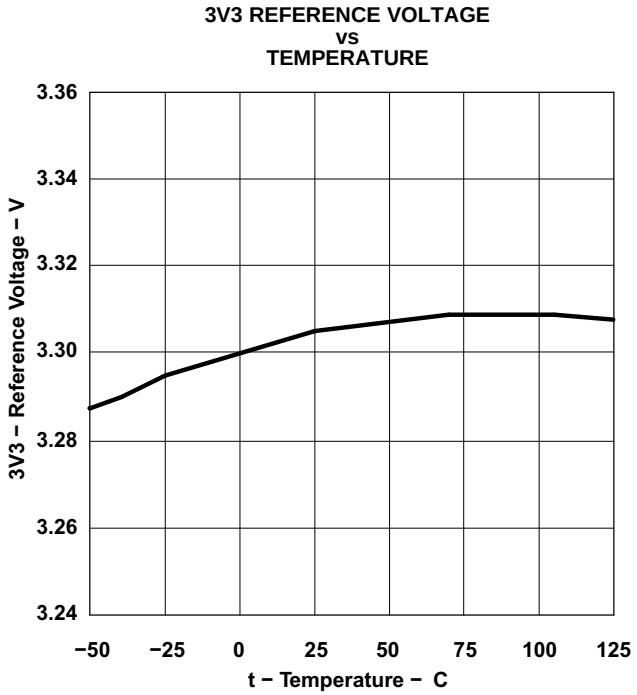


Figure 10.

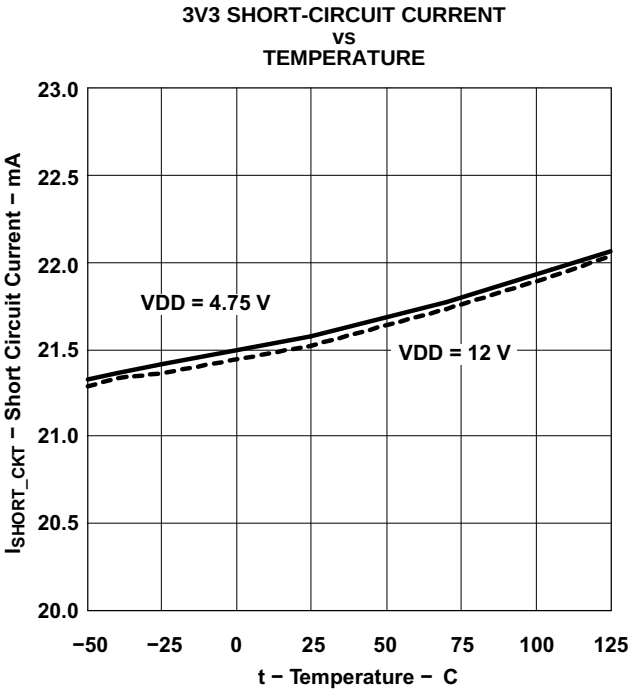


Figure 11.

TYPICAL CHARACTERISTICS (continued)

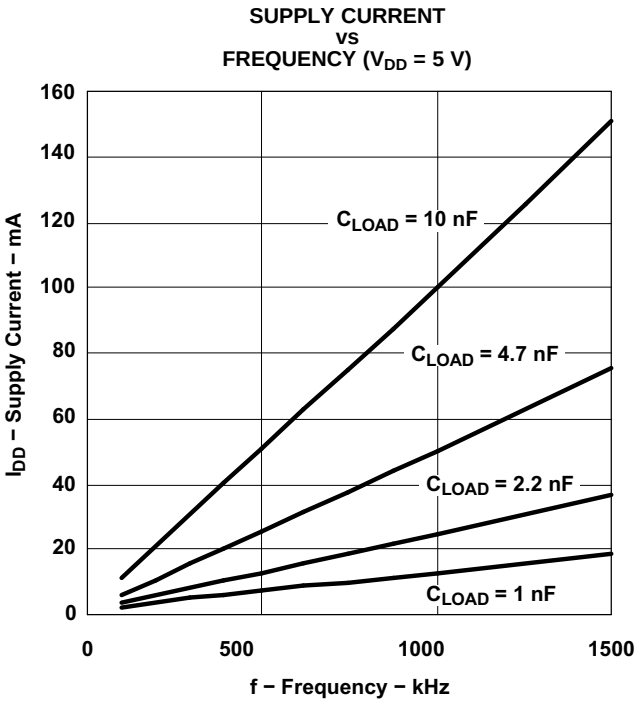


Figure 12.

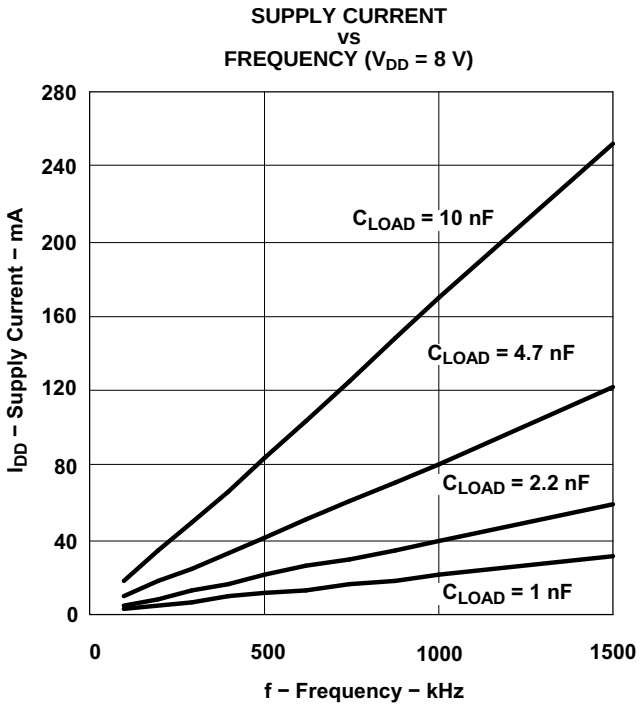


Figure 13.

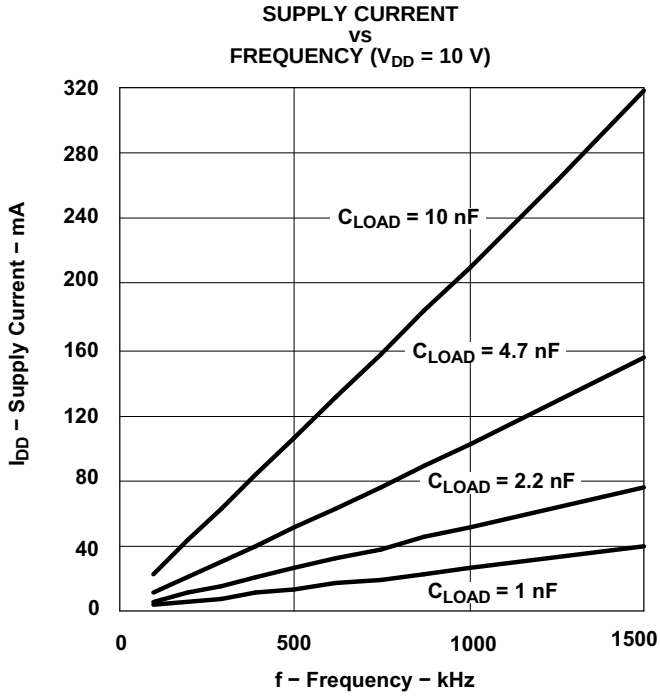


Figure 14.

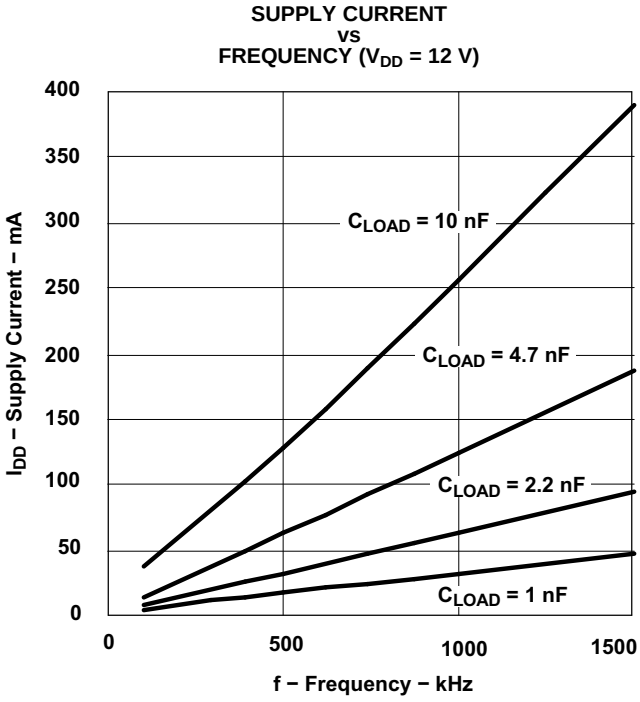


Figure 15.

TYPICAL CHARACTERISTICS (continued)

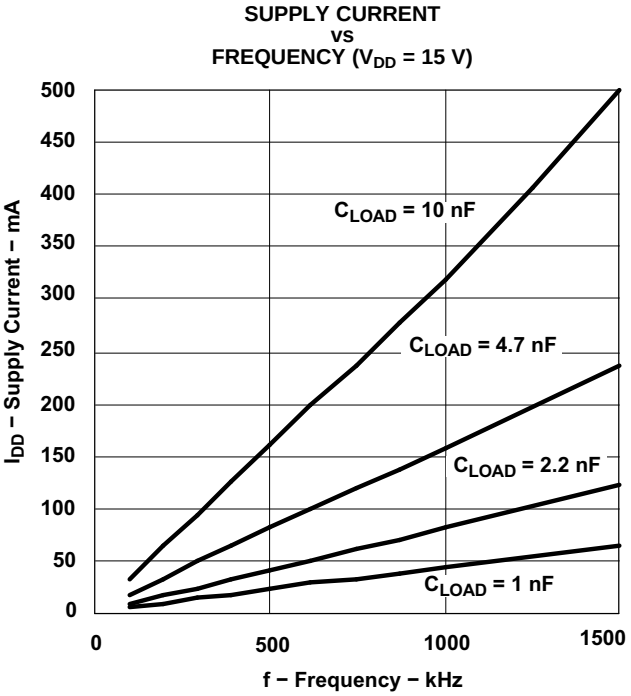


Figure 16.

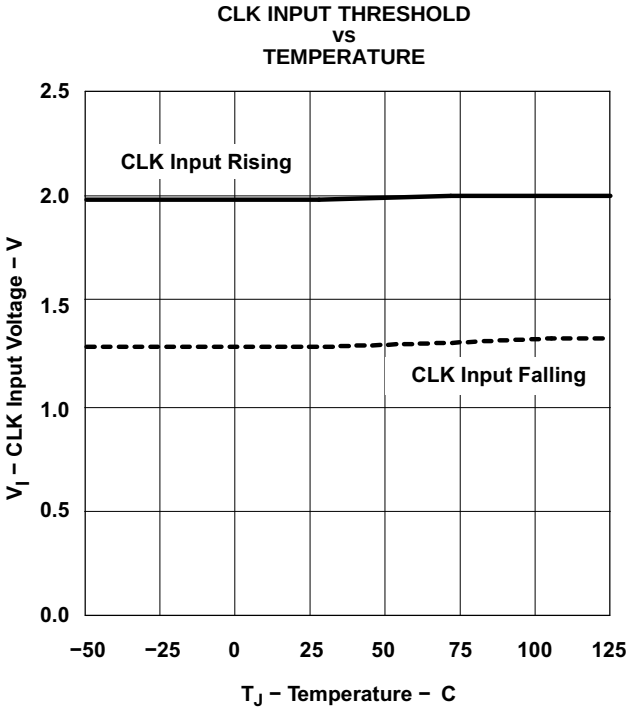


Figure 17.

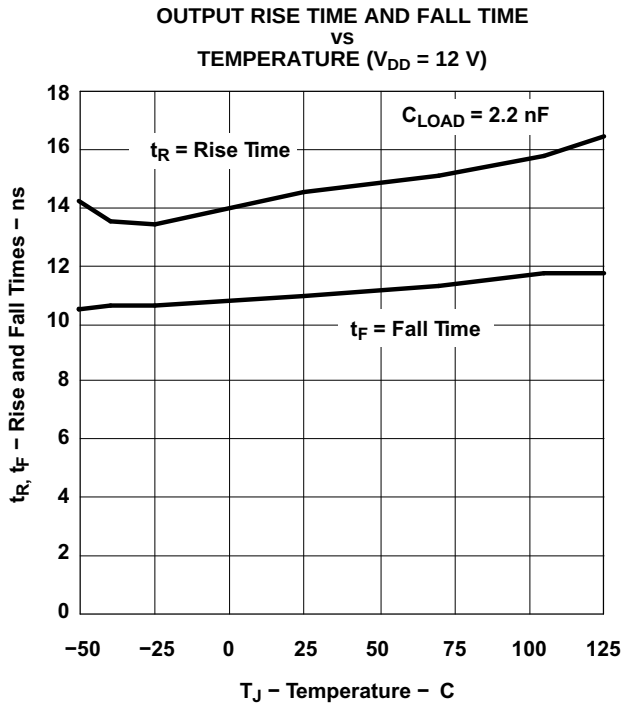


Figure 18.

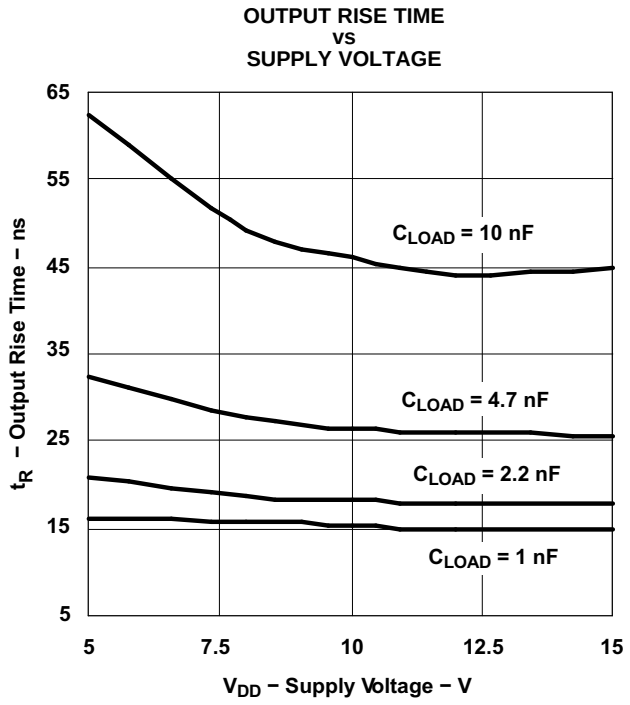


Figure 19.

TYPICAL CHARACTERISTICS (continued)

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

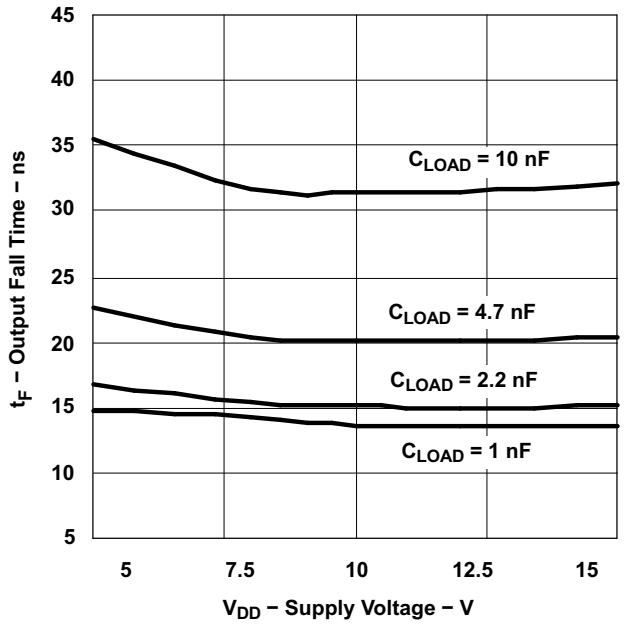


Figure 20.

CLK to OUTx PROPAGATION DELAY RISING
vs
SUPPLY VOLTAGE

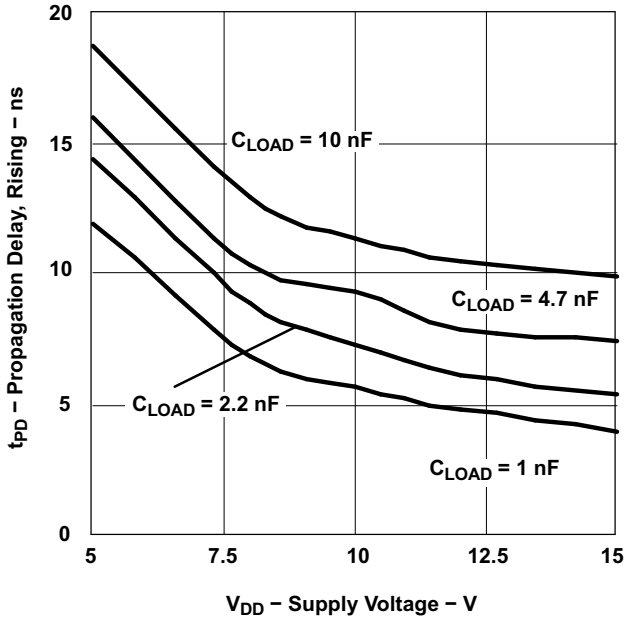


Figure 21.

CLK TO OUTx PROPAGATION DELAY FALLING
vs
SUPPLY CURRENT

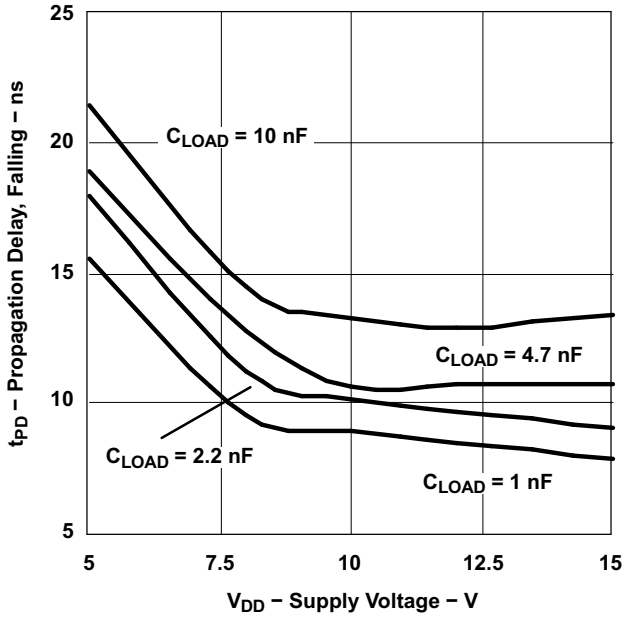


Figure 22.

DEFAULT CURRENT LIMIT THRESHOLD
vs
TEMPERATURE

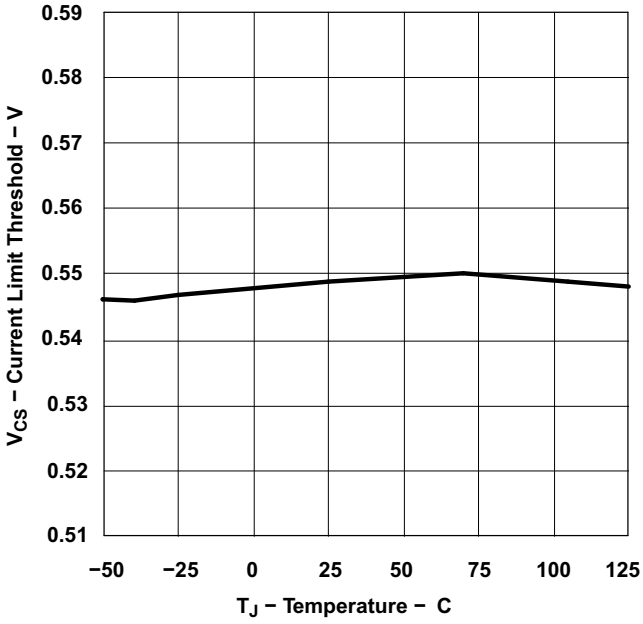


Figure 23.

TYPICAL CHARACTERISTICS (continued)

CS TO OUTx PROPAGATION DELAY
vs
TEMPERATURE

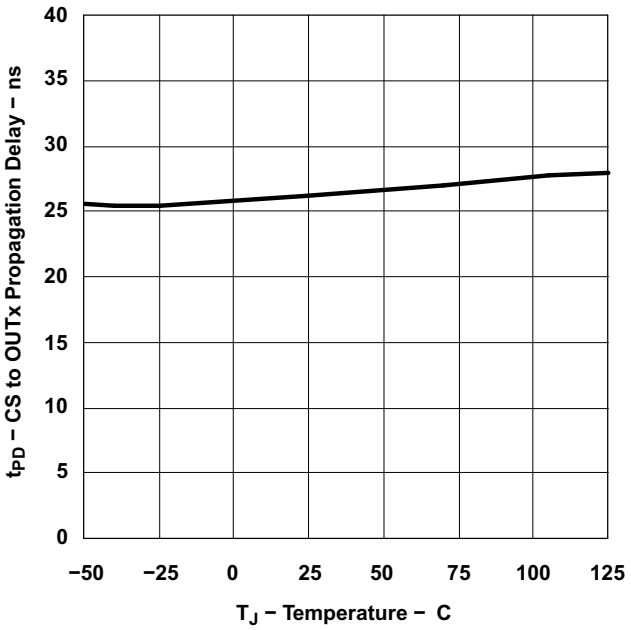


Figure 24.

CS TO CLF PROPAGATION DELAY
vs
TEMPERATURE

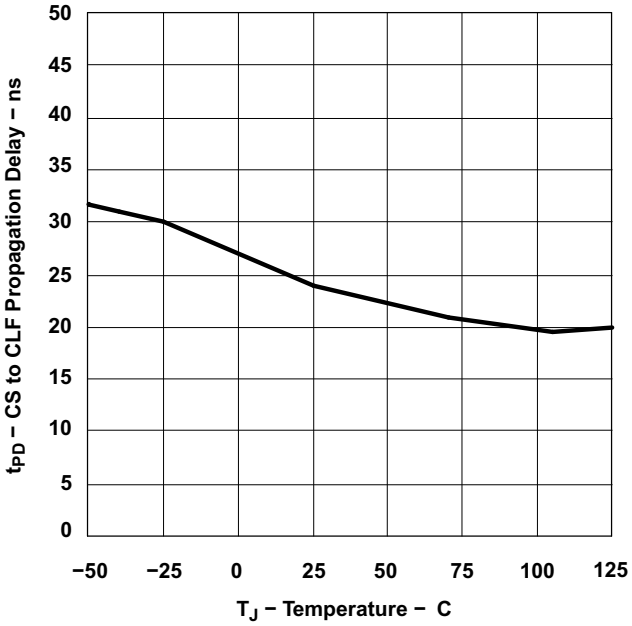


Figure 25.

CLK TO OUT PROPAGATION DELAY
vs
TEMPERATURE

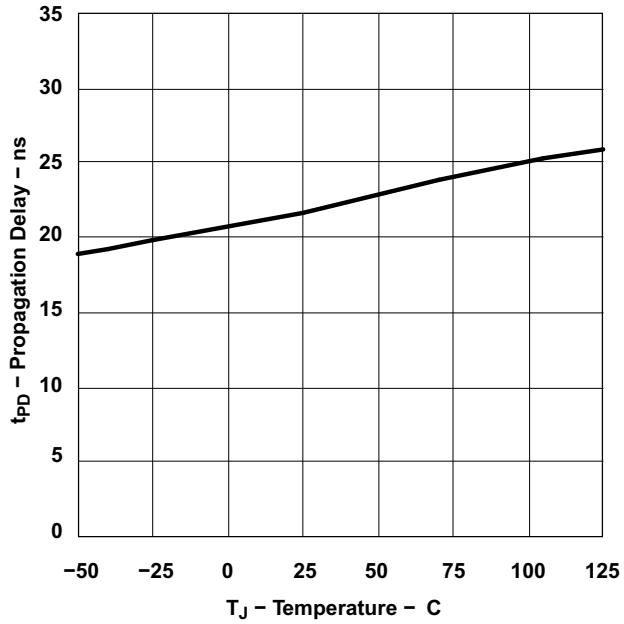


Figure 26.

UCD8220
START-UP BEHAVIOR AT V_{DD} = 12 V

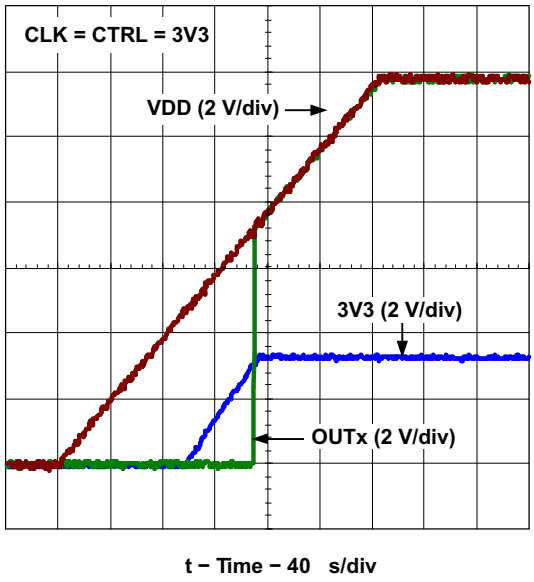
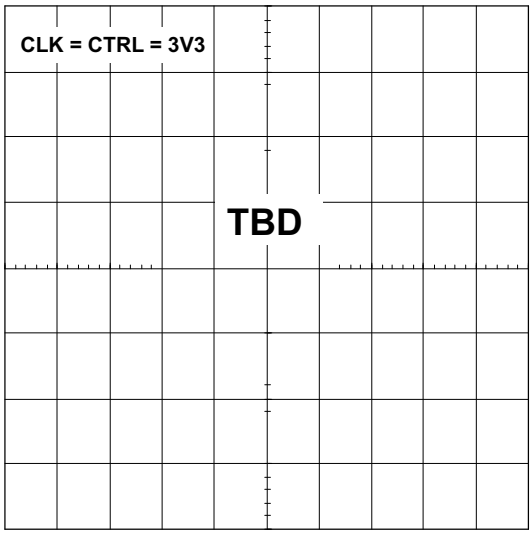


Figure 27.

TYPICAL CHARACTERISTICS (continued)

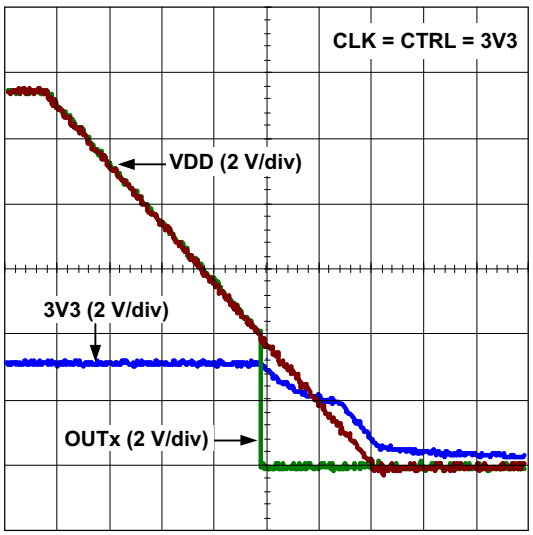
UCD8620
START-UP BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 28.

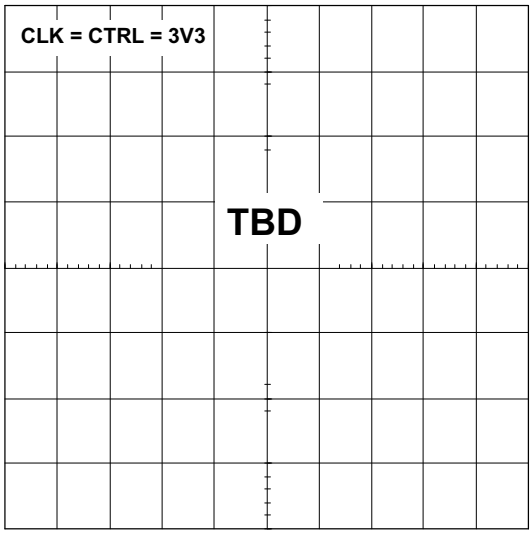
UCD8220
SHUT-DOWN BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 29.

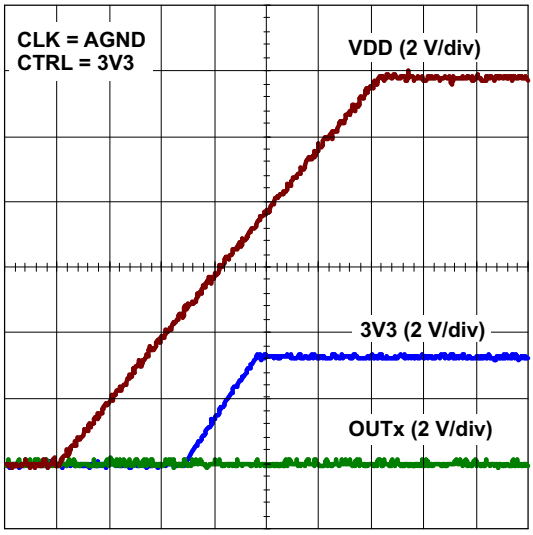
UCD8620
SHUT-DOWN BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 30.

UCD8220
START-UP BEHAVIOR AT V_{DD} = 12 V

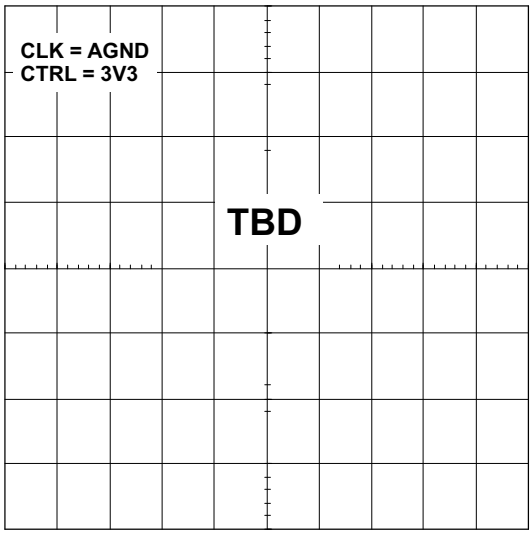


t − Time − 40 s/div

Figure 31.

TYPICAL CHARACTERISTICS (continued)

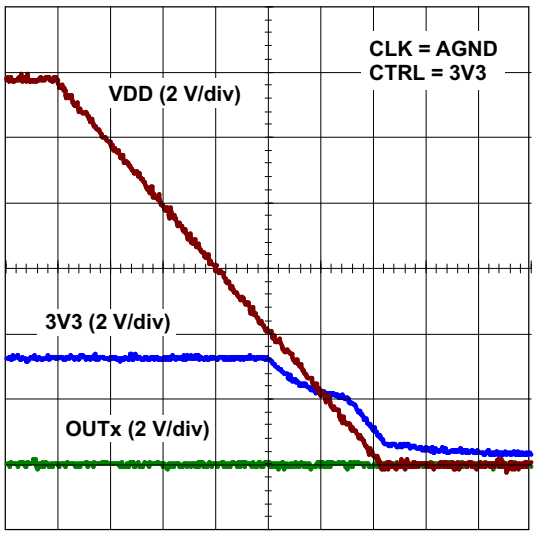
UCD8620
START-UP BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 32.

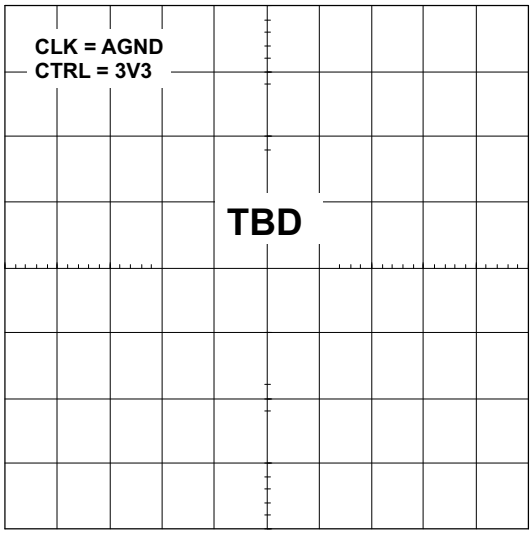
UCD8220
SHUT-DOWN BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 33.

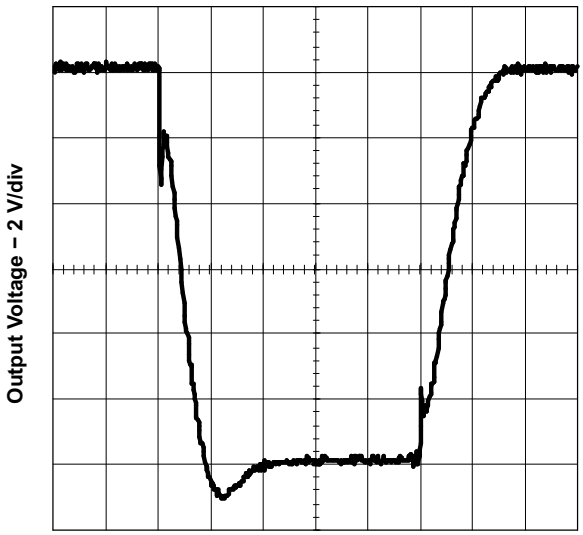
UCD8620
SHUT-DOWN BEHAVIOR AT V_{DD} = 12 V



t − Time − 40 s/div

Figure 34.

OUTPUT RISE AND FALL TIME
(V_{DD} = 12 V, C_{LOAD} = 10 nF)



t − Time − 40 ns/div

Figure 35.

TYPICAL CHARACTERISTICS (continued)

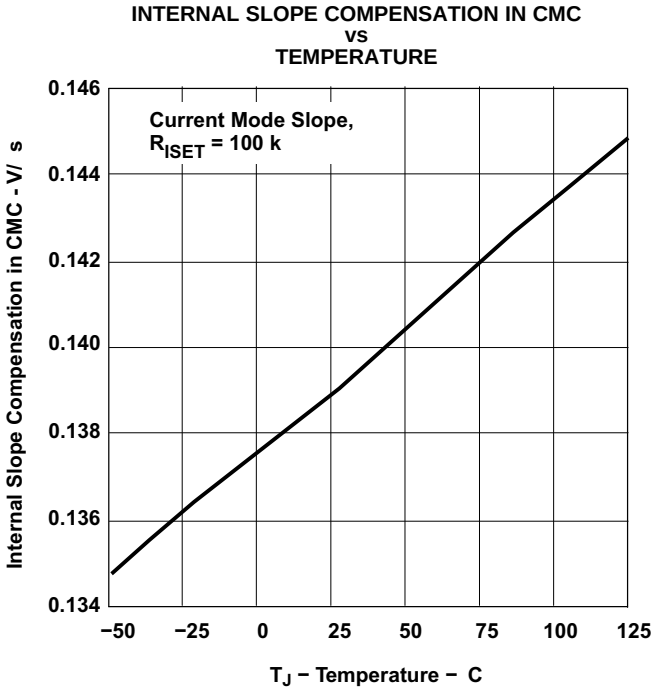


Figure 36.

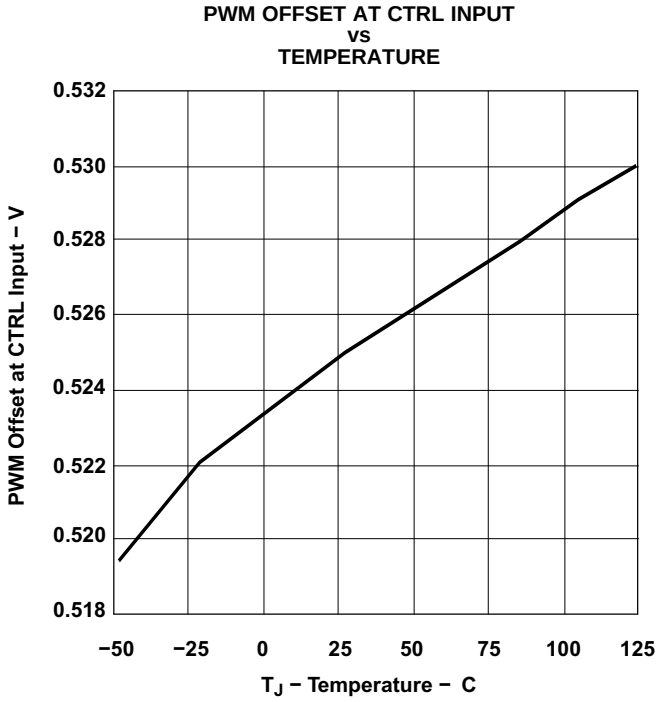


Figure 37.

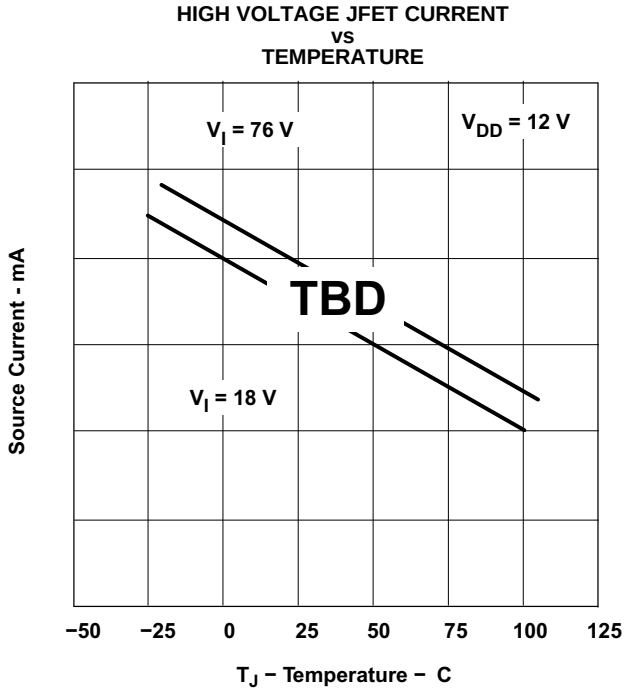


Figure 38.

APPLICATION INFORMATION

Introduction

The UCD8220 and UCD8620 are digitally managed analog PWM controllers configured with push-pull drive logic. The UCD8620 has a 110-V high-voltage startup circuit which can directly start up the controller from a 48-V telecom input line.

In systems using UCD8K devices, the PWM feedback loop is closed using the traditional analog methods, but the UCD8K controllers include circuitry to interpret a time-domain digital pulse train from a digital controller. The pulse train contains the operating frequency and maximum duty cycle limit and hence controls the power supply operation. This eases implementing a converter with high-level control features without the added complexity or digital PWM resolution limitations encountered when closing the voltage control loop in the discrete time domain.

The UCD8220 and UCD8620 can be configured for either peak current mode or voltage mode control. They provide a programmable current limit function and a digital output current limit flag which can be monitored by the host controller. For fast switching speeds, the output stages use the TrueDrive™ output architecture, which delivers rated current of ±4 A into the gate of a MOSFET during the Miller plateau region of the switching transition. Finally they also include a 3.3-V, 10-mA linear regulator to provide power for the digital controller.

The UCD8620 includes circuitry and features to ease implementing a converter that is managed by a microcontroller or a digital signal processor. Digitally managed power supplies provide software programmability and monitoring capability of the power supply operation including:

- Switching frequency
- Synchronization
- D_{MAX}
- V x S clamp
- Input UVLO start/stop voltage
- Input OVP start/stop voltage
- Soft-start profile
- Current limit operation
- Shutdown
- Temperature shutdown

CLK Input Time-Domain Digital Pulse Train

While the loop is closed in the analog domain, the UCD8K devices are managed by a time-domain digital pulse train from a digital controller. The pulse train, shown as CLK in Figure 39, contains the operating frequency and maximum duty cycle limit and hence controls the power supply operation as listed above. The pulse train uses a Texas Instruments communication protocol which is a proprietary communication system that provides handles for control of the power supply operation through software programming. The rising edge of the CLK signal represents the switching frequency. Figure 39 depicts the operation of the UCD8K device in one of 5 modes. At the time when the internal signal *REF OK* is low, the UCD8K device is not ready to accept CLK inputs. Once the *REF OK* signal goes high, then the device is ready to process inputs. While the CLK input is low, the outputs are disabled and the CLK signal is used as an enable input. Once the Digital controller completes its initialization routine and verifies that all voltages are within their operating range, then it starts the soft-start procedure by slowly ramping up the duty cycle of the CLK signal, while maintaining the desired switching frequency. The duty cycle continues to increase until it reaches steady-state where the analog control loop takes over and regulates the output voltage to the desire set point. During steady state, the maximum duty cycle can be set using a volt second product calculation in order to protect the primary of the power transformer from saturation during transients. When the power supply enters current limit, the outputs are quickly turned off, and the CLF signal is set high in order to notify the digital controller that the last power pulse was truncated because of an overcurrent event. The benefit of this technique is in the flexibility it offers. The software is now in charge of the response to overcurrent events. In typical analog designs, the power supply response to overcurrent is hardwired in the silicon. With this method, the user can configure the response differently for different applications. For example, the software can be configured to latch-off the power supply in response the first overcurrent event, or to allow a fixed number of current limit events, so that the supply is capable of starting up into a capacitive load. The user can also configure the supply to enter into *hiccup* mode immediately or after a certain number of current limit events. As described later in this data sheet, the current limit threshold can be varied in time to create unique current limit profiles. For example, the current limit set point can be set high for a predefined number of cycles to blow a manual fuse, and can be reduced down to protect the system in the event of a faulty fuse.

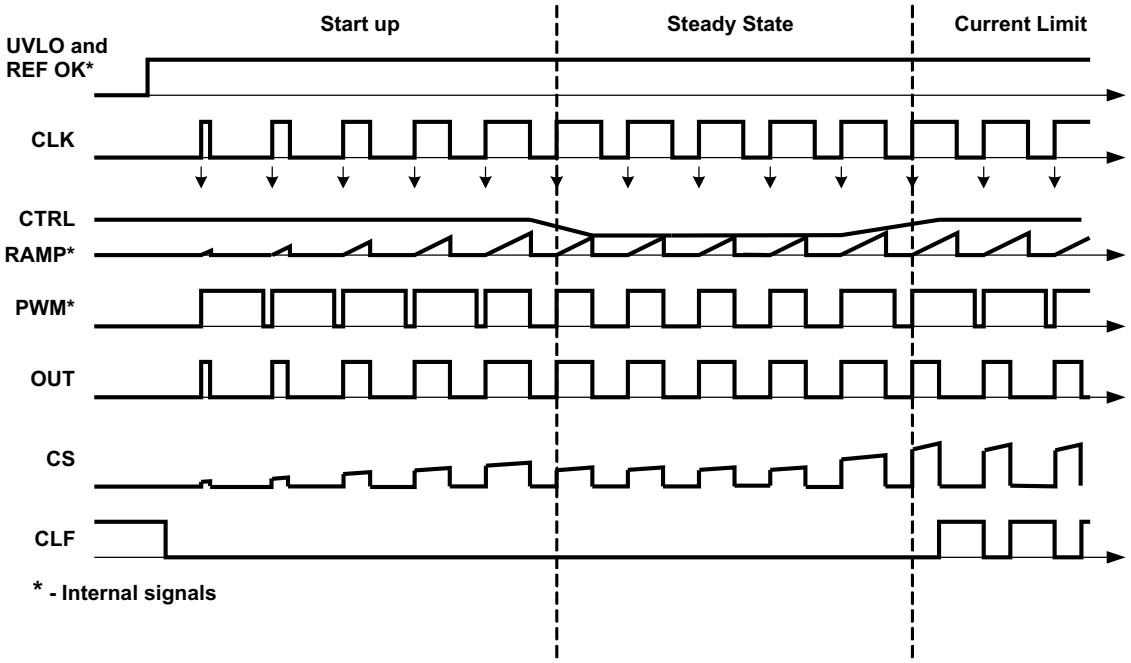
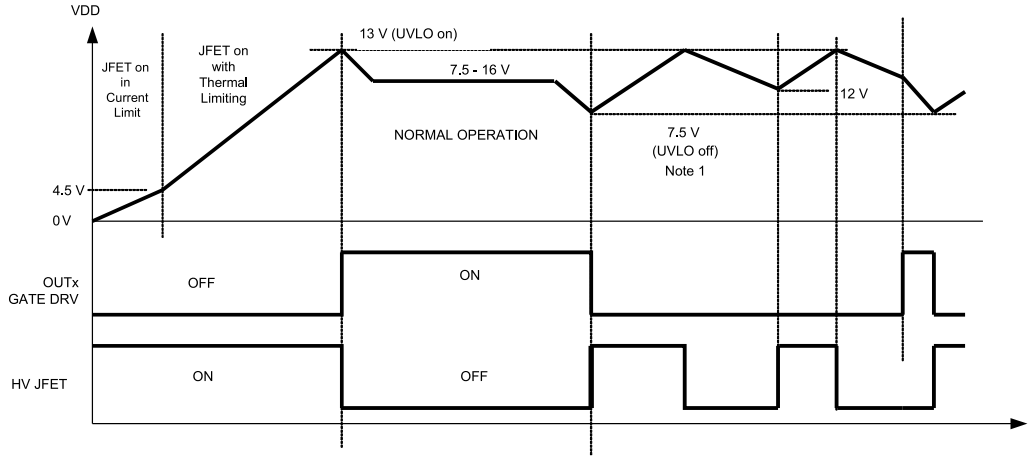


Figure 39. UCD8220 and UCD8620 Timing and Circuit Operation Diagram

JFET Operation (UCD8620 Only)

The UCD8620 digitally managed push-pull analog PWM Controller contains a 110-V start-up JFET to simplify the start-up and standby power requirements for systems with digital controllers. The JFET circuit has two operating modes. When the VDD voltage is less than 5 V, the circuit is limited to 5 mA of source current into VDD. The VDD reaches 5 V, the circuit switches into temperature protection mode and provides 10 mA until the temperature of the die exceeds 145°C. Figure 40 shows the operation of the JET circuitry during various operating conditions. At start-up, the JFET is on and charges up the VDD capacitor. Once the VDD voltage reaches its UVLO of 13 V, the JFET turns off and the outputs are allowed to switch. The JFET remains off provided the outputs are switching and the VDD voltage stays above 7.5 V. If the VDD voltage drops below 7.5 V while the outputs are switching, the outputs are immediately disabled, and the JFET is switched back on. It then attempts to charge the VDD voltage back up to 13 V. Once the VDD voltage reaches 13 V, the outputs are enabled again and allowed to switch. If the CLK input is not switched by the digital controller, then the VDD voltage decays to 12 V, and the JFET turns on again. This charges the VDD capacitor back to 13 V where the cycle repeats until the input voltage drops to a point where the VDD voltage can no longer be maintained. Figure 41 shows the graph of available source current as a function of input and VDD voltage.



(1) For VDD to go below 12 V, the input supply must be dropping out.

Figure 40. UCD8620 JFET Operation Waveforms

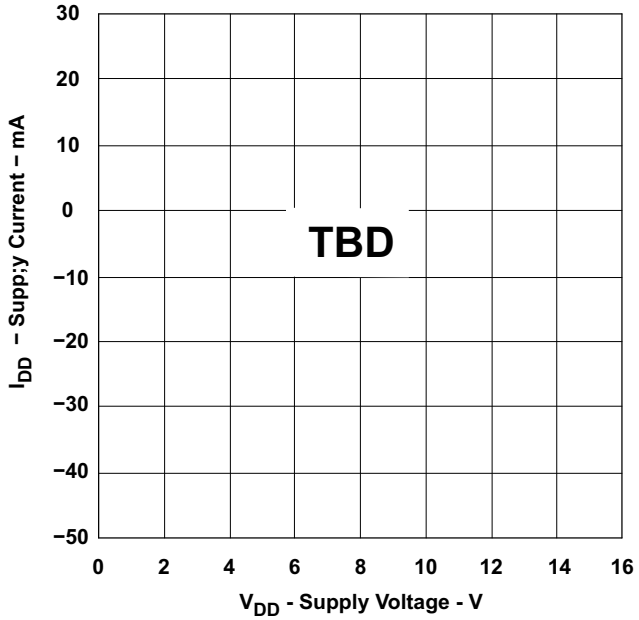


Figure 41. UCD8620 Supply Current vs Supply Voltage

Supply

The UCD8K devices accept an input range of 4.5 V to 15.5 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage must supply the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Reference / External Bias Supply

All devices in the UCD8K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place 0.22-µF of ceramic capacitance between the 3V3 pin and the AGND pin.

Current Sensing and Protection

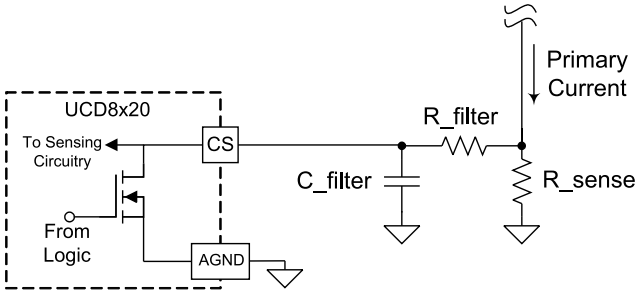


Figure 42. Current Sense Filter

A fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.Figure 43 shows various methods for setting the ILIM threshold.

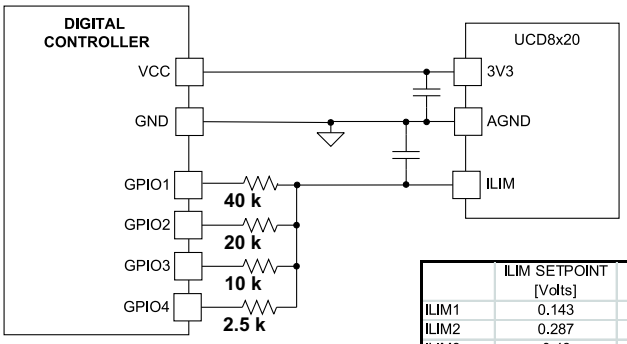
The current limit threshold may be set to any value between 0.25 V and 1 V by applying the desired threshold voltage to the current limit (ILIM) pin. If the ILIM pin is left floating, the internal current limit threshold is 0.5 V. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD8K device receives the next rising edge on the CLK pin.

When the CS voltage is below ILIM, the driver output follows the PWM command. The CLF digital output flag is monitored by the host controller to determine when a current limit event occurs, and to then apply the appropriate algorithm to obtain the desired current limit profile (i.e. straight line, fold back, hickup, or latch-off).

A benefit of this local protection feature is that the UCD8620 devices protects the power stage if the software code in the digital controller becomes corrupted. If the controller's PWM output stays high, the local current sense circuit turns off the driver output when an overcurrent event occurs. The system then goes into retry mode because most DSP and microcontrollers have an on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD87K's local current limit comparator provides the required fast protection for the power stage.

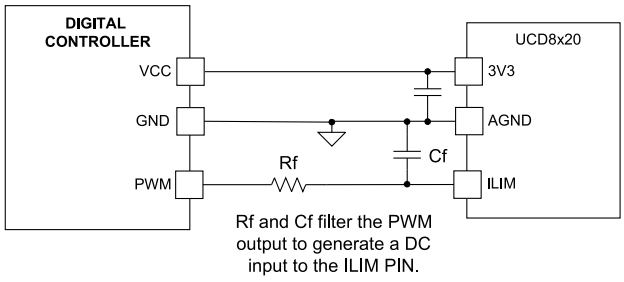
The CS threshold is 25 mV below the ILIM voltage. If the user attempts to command zero current while the CS pin is at ground, the CLF flag latches high until the CLK pin receives a pulse. At start-up, it is necessary to ensure that the ILIM pin is always greater than the CS pin for the handshaking to work. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag is latched high and the digital controller must poll the UCD8620 device, by sending it a narrow CLK pulse. If a fault condition is not present, the CLK pulse resets the CLF signal to low indicating that the UCD8620 device is ready to process power pulses.

a) GPIO outputs

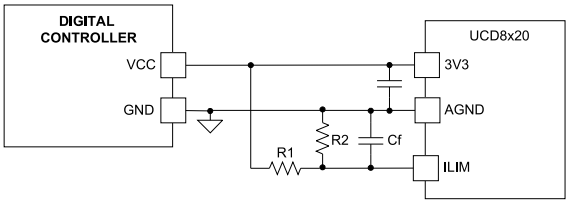


	ILIM SETPOINT [Volts]	GPIO3	GPIO2	GPIO1	GPIO4
ILIM1	0.143	0	0	1	0
ILIM2	0.287	0	1	0	0
ILIM3	0.43	0	1	1	0
ILIM0	0.5	OPEN	OPEN	OPEN	OPEN
ILIM4	0.574	1	0	0	0
ILIM5	0.717	1	0	1	0
ILIM6	0.861	1	1	0	0
ILIM7	1.004	1	1	1	0

b) PWM output



c) Resistor divider



d) internal set point

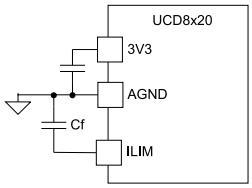


Figure 43. ILIM Settings

Selecting the ISET Resistor for Voltage Mode Control

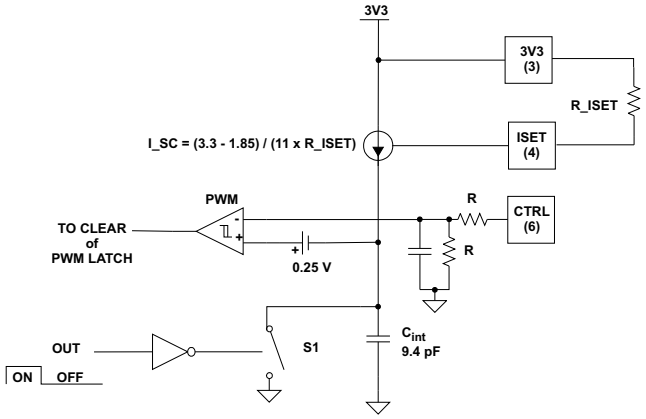


Figure 44. UCD8x20 Configured in Voltage Mode Control with an Internal Timing Capacitor

When the ISET resistor is configured as shown in Figure 44 with the ISET resistor connected between the ISET pin and the 3V3 pin, the device is set-up for voltage mode control. For purposes of voltage loop compensation the, voltage ramp is 1.4 V from the valley to the peak. See Equation 1 for selecting the proper resistance for a desired clock frequency.

$$R\_ISET = \frac{(3.3 - 1.85) \times 10^{12}}{11 \times 1.4 \times fclk \times 1000 \times 9.4} \quad (1)$$

Where:

fclk = Desired Clock Frequency in Hz.

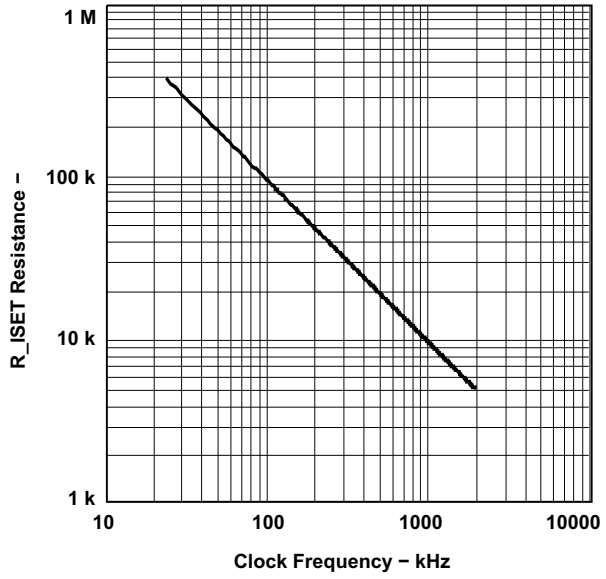


Figure 45. ISET Resistance vs Clock Frequency

Figure 45 shows the nominal value of resistance to use for a desired clock frequency. Note that for the UCD8220 and the UCD8620 controllers, which have two outputs controlled by Push-Pull logic, the output ripple frequency is equal to the clock frequency; and each output switches at half the clock frequency.

Selecting the ISET Resistor for Voltage Mode Control with Voltage Feed forward

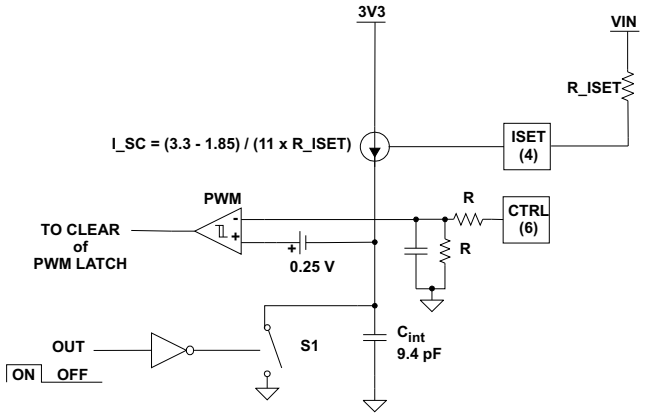


Figure 46. UCD8x20 Configured in Voltage Mode Control with Voltage Feed Forward

When the ISET resistor is configured as shown in Figure 46 with the ISET resistor connected between the ISET pin and the input voltage, VIN, the device is configured for voltage mode control with voltage feed forward. For the purposes of voltage loop compensation, the voltage ramp is 1.4 x Vin/Vin_max Volts from the valley to the peak. See Equation 2 for selecting the proper resistance for a desired clock frequency and input voltage range.

$$R\_ISET = \frac{(Vin\_max - 1.85) \times 10^{12}}{11 \times 1.4 \times fclk \times 9.4} \quad (2)$$

Where:

fclk = Desired Clock Frequency in Hz.

For a general discussion of the benefits of Voltage Mode Control with Voltage feed forward, see Reference [5].

Selecting the ISET Resistor for Peak Current Mode Control with Internal Slope Compensation

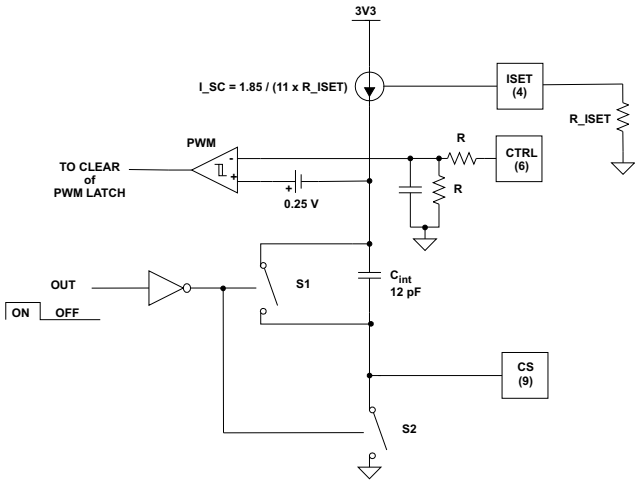


Figure 47. UCCD8x20 Configured in Peak Current Control with Internal Slope Compensation

When the ISET resistor is configured as shown in Figure 47 with the ISET resistor connected between the ISET pin and AGND, the device is configured for peak current mode control with internal slope compensation. The voltage at the ISET pin is 1.85 volts so the internal slope compensation current, I_SC, being fed into the internal slope compensation capacitor is equal to 1.85 / (11x R_ISET). The voltage slope at the PWM comparator input which is generated by this current is equal to:

$$\text{SLOPE} = \frac{1.85 \times 10^6}{11 \times \text{R\_ISET} \times 12} \text{ V/ s} \quad (3)$$

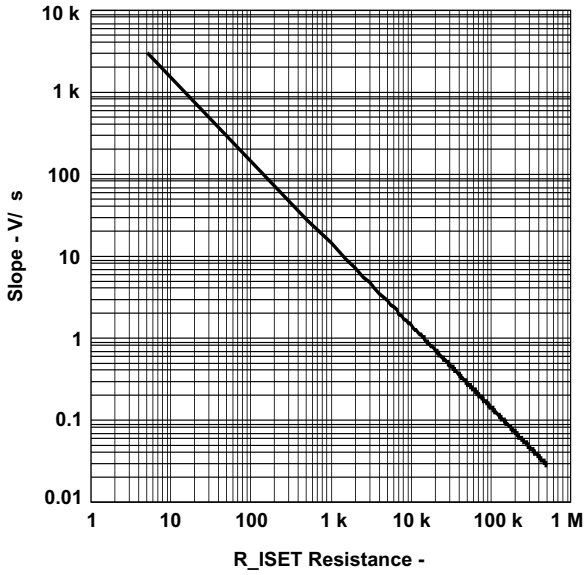


Figure 48. Slope vs RISET Resistance

The amount of slope compensation required depends on the design of the power stage and the output specifications. A general rule is to add an up-slope equal to the down slope of the output inductor.

Handshaking

The UCD8K family of devices have a built-in handshaking feature to facilitate efficient start-up of the digitally managed power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD8K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device processes the CLK signals. The digital controller should monitor the CFL flag at start-up and wait for the CLF flag to go LOW before sending CLK pulses to the UCD8K device.

Driver Output

The high-current output stage of the UCD8K device family is capable of supplying ±4-A peak current pulses and swings to both PVDD and PGND.

The drive output uses the Texas Instruments TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pull-up/pull-down circuits with bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD8K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [2].

Drive Current and Power Requirements

The UCD8620 family of controllers contains drivers which can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High-peak current is required to turn on a MOSFET. Then, to turn off a MOSFET, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device.

Reference [2] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2 \quad (4)$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = CV^2 \times 1 \quad (5)$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged.

With V_{DD} = 12 V, C_{LOAD} = 2.2 nF, and f = 300 kHz, the power loss can be calculated as:

$$P = 2.2\ nF \times 12^2 \times 300\ kHz = 0.095\ W \quad (6)$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.095\ W}{12\ V} = 7.9\ mA \quad (7)$$

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD8K family of drivers is available in PowerPAD™ TSSOP and QFN/DFN packages to cover a range of application requirements. Both have an exposed pad to enhance thermal conductivity from the semiconductor junction.

As illustrated in Reference [3], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the θ_{JA} down to 37.47°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [4].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPAD™ should be connected to the quiet ground of the circuit.

Circuit Layout Recommendations

In a MOSFET driver operating at high frequency, it is critical to minimize stray inductance to minimize overshoot/undershoot and ringing. The low output impedance of the drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. It is advantageous to connect the driver device close to the MOSFETs. It is recommended that the PGND and the AGND pins be connected to the PowerPAD™ of the package with a thin trace. It is critical to ensure that the voltage potential between these two pins does not exceed 0.3 V. The use of schottky diodes on the outputs to PGND and PVDD is recommended when driving gate transformers.

REFERENCES

1. Power Supply Seminar SEM-1600 Topic 6: A Practical Introduction to Digital Power Supply Control, by Laszlo Balogh, Texas Instruments Literature No. SLUP224
2. Power Supply Seminar SEM–1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
3. Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002
4. Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004
5. Power Supply Seminar SEM-300 Topic 2, "Closing the Feedback Loop", by Lloyd Dixon Jr., Texas Instruments, (Literature Number SLUP068)

RELATED PRODUCTS

PRODUCT	DESCRIPTION	FEATURES
UCD9501	Digital Power Controller for High Performance Multi-loop Applications	
MSP430F1232	Microcontroller	

REVISION HISTORY

DATE	REVISION	CHANGE DESCRIPTION
03/05	SLUS652	Initial release.
08/05	SLUS652A	Extensive changes throughout
09/05	SLUS652B	Extensive changes throughout

PACKAGE OPTION ADDENDUM

23-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCD8220PWP	PREVIEW	HTSSOP	PWP	16	90	TBD	Call TI	Call TI
UCD8220PWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI
UCD8220RSA	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI
UCD8220RSAR	PREVIEW	QFN	RSA	16	3000	TBD	Call TI	Call TI
UCD8620PWP	PREVIEW	HTSSOP	PWP	16	90	TBD	Call TI	Call TI
UCD8620PWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI
UCD8620RGWR	PREVIEW	QFN	RGW	20	3000	TBD	Call TI	Call TI
UCD8620RGWT	PREVIEW	QFN	RGW	20	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PACKAGE OPTION ADDENDUM

3-Oct-2005

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCD8220PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCD8220PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCD8220RSA	PREVIEW	QFN	RSA	16	250	TBD	Call TI	Call TI
UCD8220RSAR	PREVIEW	QFN	RSA	16	3000	TBD	Call TI	Call TI
UCD8620PWP	PREVIEW	HTSSOP	PWP	16	90	TBD	Call TI	Call TI
UCD8620PWPR	PREVIEW	HTSSOP	PWP	16	2000	TBD	Call TI	Call TI
UCD8620RGWR	PREVIEW	QFN	RGW	20	3000	TBD	Call TI	Call TI
UCD8620RGWT	PREVIEW	QFN	RGW	20	250	TBD	Call TI	Call TI

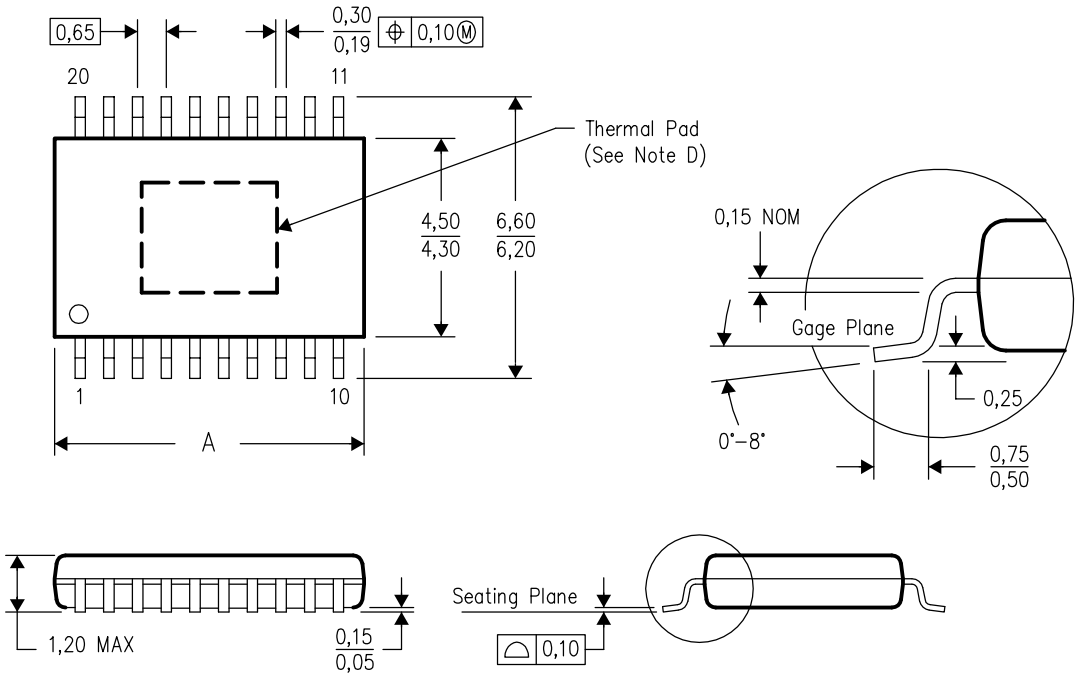
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



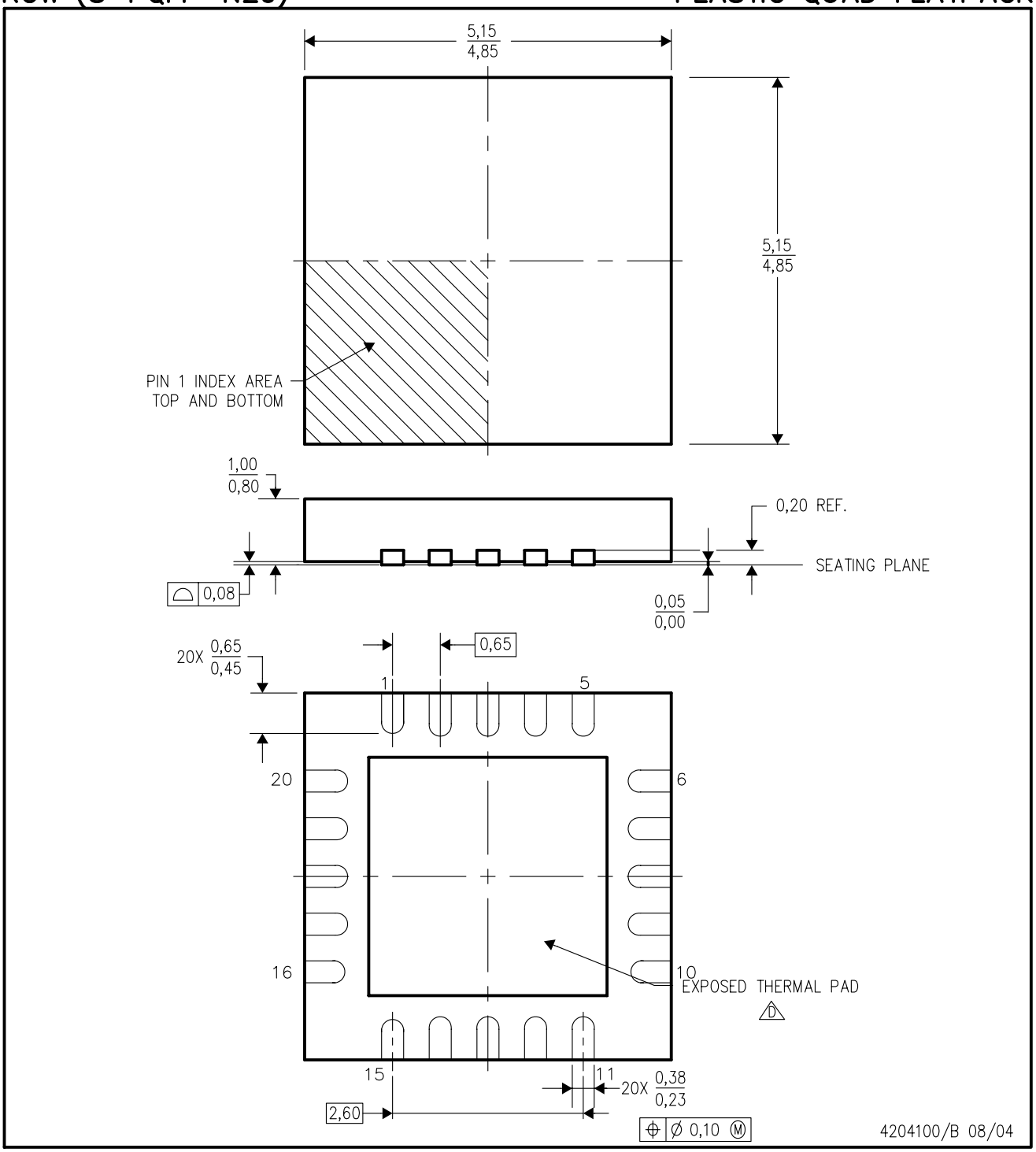
DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

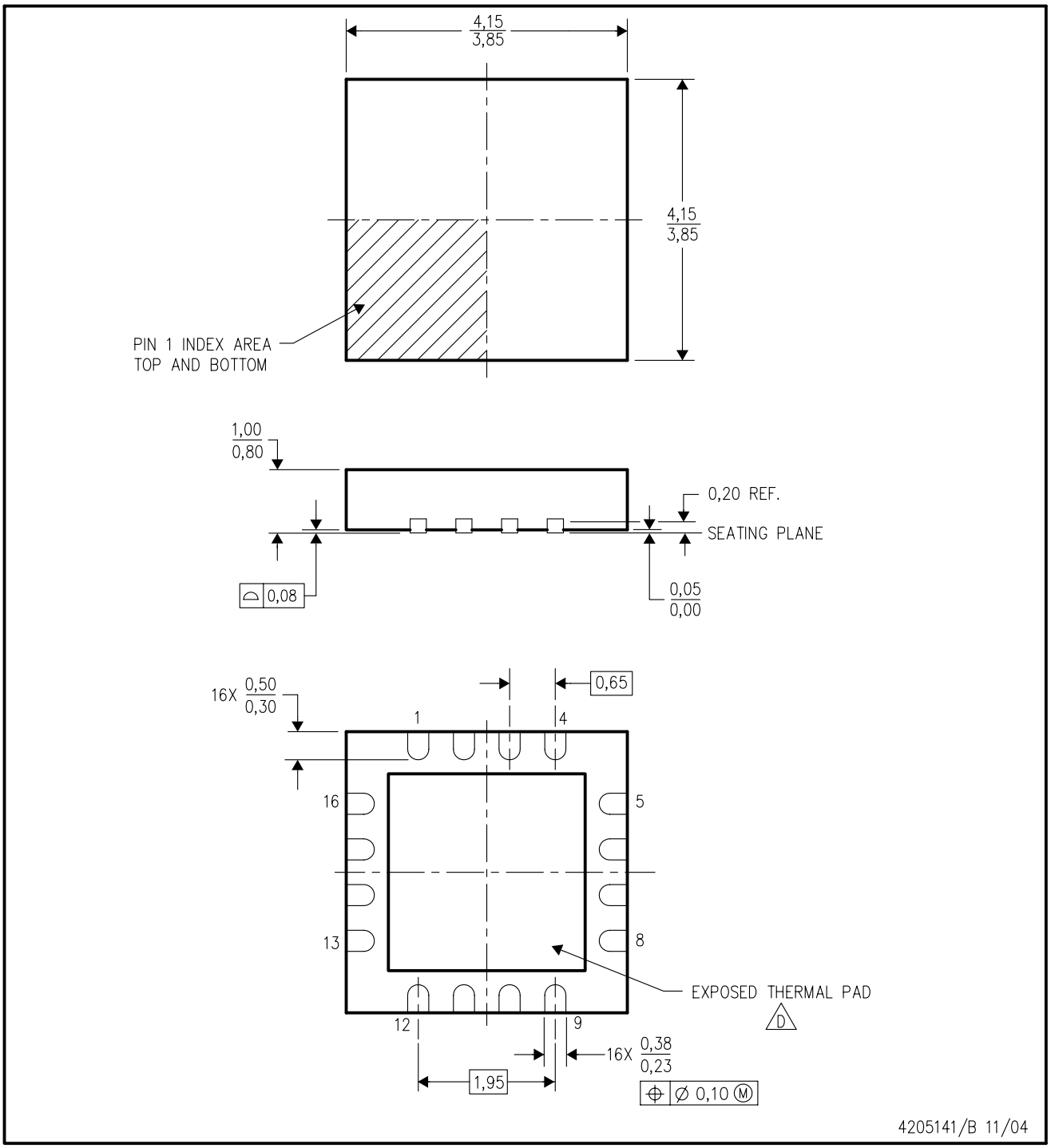
PowerPAD is a trademark of Texas Instruments.

RGW (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

RSA (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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