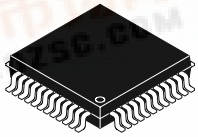
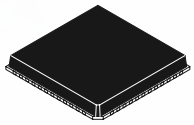
TEXAS INSTRUMENTS





SLES020 – DECEMBER 2001

CCD SIGNAL PROCESSOR FOR DIGITAL CAMERAS

FEATURES

- **CCD Signal Processing:**
  - **Correlated Double Sampling (CDS)**
  - **Programmable Black Level Clamping**
- **Programmable Gain Amplifier (PGA) –6-dB to 42-dB Gain Ranging**
- **12-Bit Digital Data Output:**
  - **Up to 28-MHz Conversion Rate**
  - **No Missing Codes**
- **77-dB Signal-To-Noise Ratio**
- **Portable Operation:**
  - **Low Voltage: 2.7 V to 3.6 V**
  - **Low Power: 94 mW (Typ) at 3 V**
  - **Stand-By Mode: 6 mW**

APPLICATIONS

- **DSC, DVC, Security Camera**

DESCRIPTION

The VSP2272 device is a complete mixed-signal processing IC for digital cameras providing signal conditioning and analog-to-digital conversion for the output of a charge-coupled device (CCD) array. The primary CCD channel provides correlated double sampling (CDS) to extract the video information from the pixels, –6-dB to 42-dB gain range with digital control for varying illumination conditions, and black level clamping for an accurate black level reference. Input signal clamping and offset correction of the input CDS are also performed. The stable gain control is linear in dB. Additionally, the black level is quickly recovered after gain change.

The VSP2272Y device is available in a 48-lead LQFP package and the VSP2272M device is available in a 48-lead P-VQFN package. Both devices operate from a single 3-V/3.3-V supply.

AVAILABLE OPTIONS

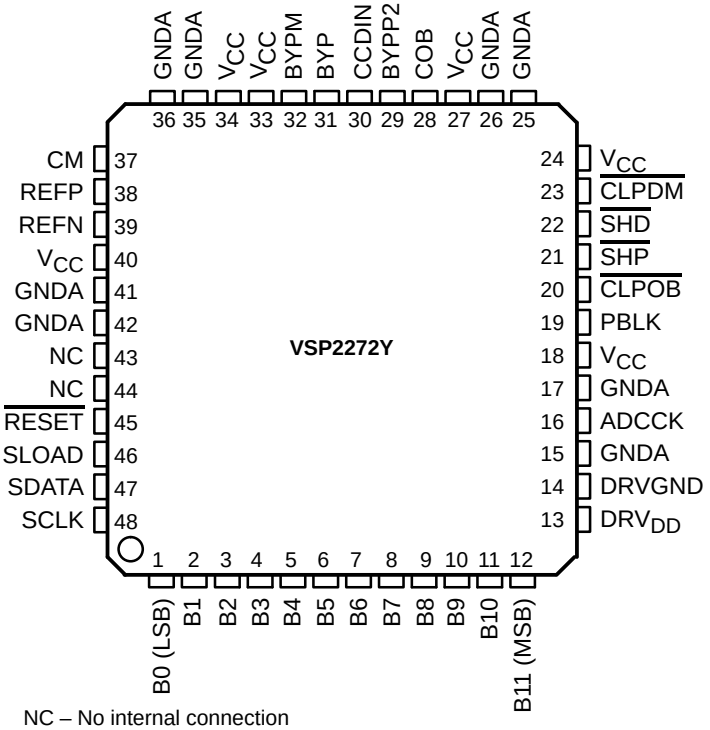
PRODUCT	PACKAGE	PACKAGE OUTLINE DESIGNATOR†	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER‡	TRANSPORT MEDIA
VSP2272Y	48-Lead LQFP	PT	–25°C to 85°C	VSP2272Y	VSP2272Y	250-piece tray
VSP2272Y	48-Lead LQFP	PT	–25°C to 85°C	VSP2272Y	VSP2272Y/2K	Tape and reel
VSP2272M	48-Lead P-VQFN	RGN	–25°C to 85°C	VSP2272M	VSP2272M	250-piece tray
VSP2272M	48-Lead P-VQFN	RGN	–25°C to 85°C	VSP2272M	VSP2272M/2K	Tape and reel

† A detailed drawing and a dimension table are located at the end of the data sheet.

‡ Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2,000 devices per reel). Ordering 2,000 pieces of the VSP2272Y/2K device will get a single 2,000-piece tape and reel.

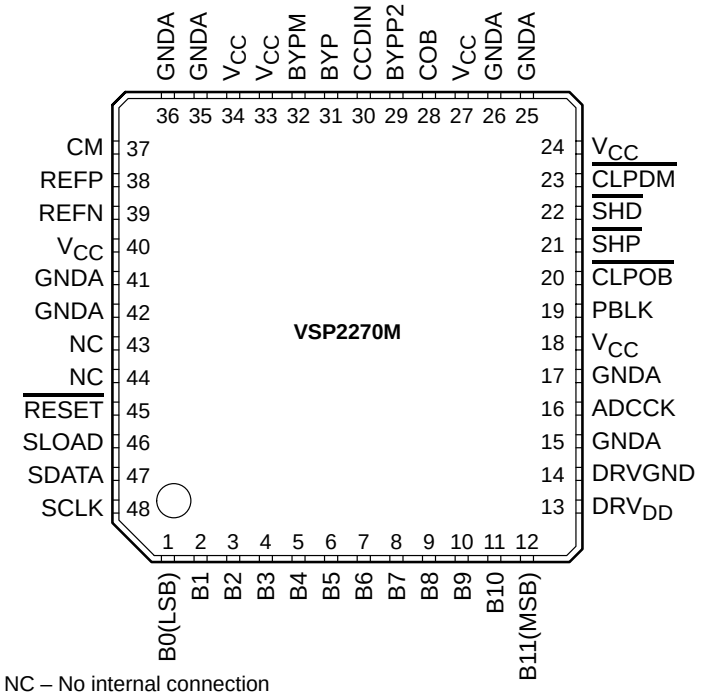
pin assignments

PT PACKAGE
(TOP VIEW)



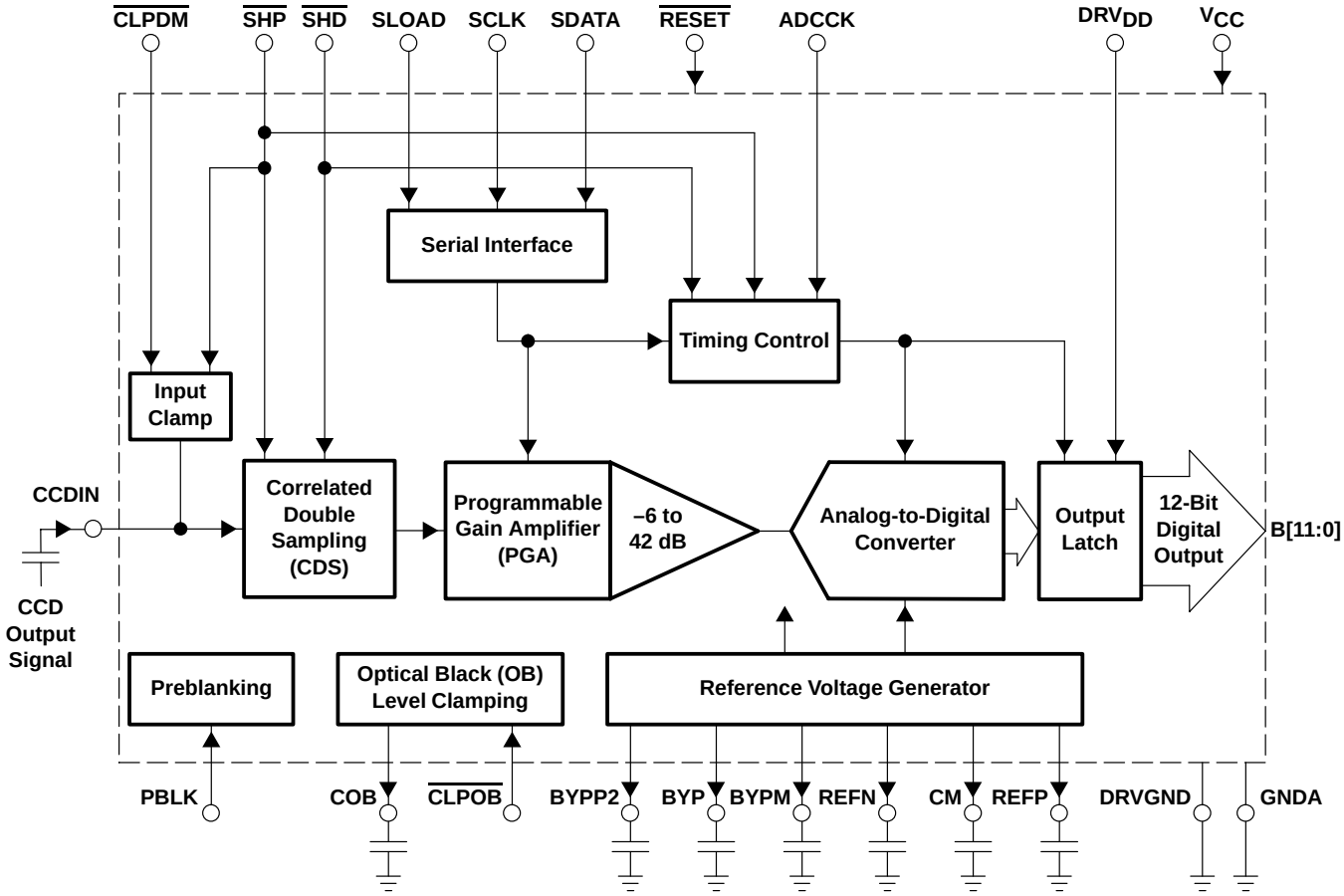
NC – No internal connection

RGN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



Terminal Functions

TERMINAL NO.	TERMINAL NAME	TYPE (see Note 1)	DESCRIPTION
1	B0 (LSB)	DO	A/D converter output, bit 0 (LSB)
2	B1	DO	A/D converter output, bit 1
3	B2	DO	A/D converter output, bit 2
4	B3	DO	A/D converter output, bit 3
5	B4	DO	A/D converter output, bit 4
6	B5	DO	A/D converter output, bit 5
7	B6	DO	A/D converter output, bit 6
8	B7	DO	A/D converter output, bit 7
9	B8	DO	A/D converter output, bit 8
10	B9	DO	A/D converter output, bit 9
11	B10	DO	A/D converter output, bit 10
12	B11 (MSB)	DO	A/D converter output, bit 11 (MSB)
13	DRV_{DD}	P	Power supply for digital output
14	DRVGND	P	Digital ground for digital output
15, 17. 25, 26 35, 36, 41, 42	GNDA	P	Analog ground
16	ADCCK	DI	Clock for digital output buffer
18, 24, 27, 33, 34, 40	V_{CC}	P	Analog power supply
19	PBLK	DI	Preblanking: High = Normal operation mode Low = Preblanking mode: digital outputs are all 0s
20	$\overline{CLPOB}$	DI	Optical black clamp pulse (default = active low) (see Note 5)
21	$\overline{SHP}$	DI	CDS reference level sampling pulse (default = active low) (see Note 5)
22	$\overline{SHD}$	DI	CDS data level sampling pulse (default = active low) (see Note 5)
23	$\overline{CLPDM}$	DI	Dummy pixel clamp pulse (default = active low) (see Note 5)
28	COB	AO	Optical black clamp loop reference (bypass to ground) (see Note 2)
29	BYPP2	AO	Internal reference P (bypass to ground) (see Note 3)
30	CCDIN	AI	CCD signal input
31	BYP	AO	Internal reference C (bypass to ground) (see Note 4)
32	BYPM	AO	Internal reference N (bypass to ground (see Note 3)
37	CM	AO	A/D converter common mode voltage (bypass to ground) (see Note 4)
38	REFP	AO	A/D converter positive reference (bypass to ground) (see Note 4)
39	REFN	AO	A/D converter negative reference (bypass to ground) (see Note 4)
43, 44	NC		Must be left open
45	$\overline{RESET}$	DI	Asynchronous system reset (active low)
46	SLOAD	DI	Serial data latch signal (triggered at the rising edge)
47	SDATA	DI	Serial data input
48	SCLK	DI	Clock for serial data shift (triggered at the rising edge)

NOTES: 1. Designators in TYPE: P: power supply and ground, DI: digital input, DO: digital output, AI: analog input, AO: analog output
2. Must be connected to ground with a bypass capacitor. The recommended value is 0.1 μF to 0.22 μF, however it depends on the application environment. Refer to the *optical black level clamp loop* section for details.
3. Must be connected to ground with a bypass capacitor. The recommended value is 400 pF to 1000 pF, however it depends on the application environment. Refer to the *voltage reference* section for details.
4. Must be connected to ground with a bypass capacitor (0.1 μF). Refer to the *voltage reference* section for details.
5. Refer to the *serial interface* section for details.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{CC}, DRV_{DD} . . . . . 4 V
Supply voltage differences: V_{CC} . . . . . ±0.1 V
Ground voltage differences: GNDA, DRV_{DD} . . . . . ±0.1 V
Digital input voltage . . . . . –0.3 V to 5.3 V
Analog input voltage . . . . . –0.3 V to V_{CC} + 0.3 V
Input current (any leads except supplies) . . . . . ±10 mA
Operating temperature . . . . . –25°C to 85°C
Storage temperature . . . . . –55°C to 125°C
Junction temperature . . . . . 150°C
Lead temperature (soldering, 5 sec) . . . . . 260°C
Package temperature (IR reflow, peak, 10 sec) . . . . . 235°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics all specifications at T_A = 25°C, V_{CC} = 3 V, DRV_{DD} = 3 V, conversion rate (f_{ADCCK}) = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VSP2272Y, VSP2272M			UNIT
			MIN	TYP	MAX	
Resolution				12		Bits
Maximum conversion rate			28			MHz
DIGITAL INPUTS						
	Logic family			TTL		
V_{T+}	Input low-to-high threshold voltage			1.7		V
$V_{T–}$	Input high-to-low threshold voltage			1		V
I_{IH}	Input logic high current	V_I = 3 V			±20	µA
I_{IL}	Input logic low current	V_I = 0 V			±20	µA
	ADCCK clock duty cycle			50%		
	Input capacitance			5		pF
	Maximum input voltage		– 0.3		5.3	V
DIGITAL OUTPUTS						
	Logic family			CMOS		
	Logic coding			Straight binary		
V_{OH}	Output logic high voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Output logic low voltage	I_{OL} = 2 mA			0.4	V
	Additional output data delay	J[1:0] = 00		0		ns
		J[1:0] = 01		5		
		J[1:0] = 10		10		
		J[1:0] = 11		13		
REFERENCE						
	Positive reference voltage			1.75		V
	Negative reference voltage			1.25		V
ANALOG INPUT (CCDIN)						
	Input signal level for full-scale out	PGA gain = 0 dB	900			mV
	Input capacitance			15		pF
	Input limit		–0.3		3.3	V

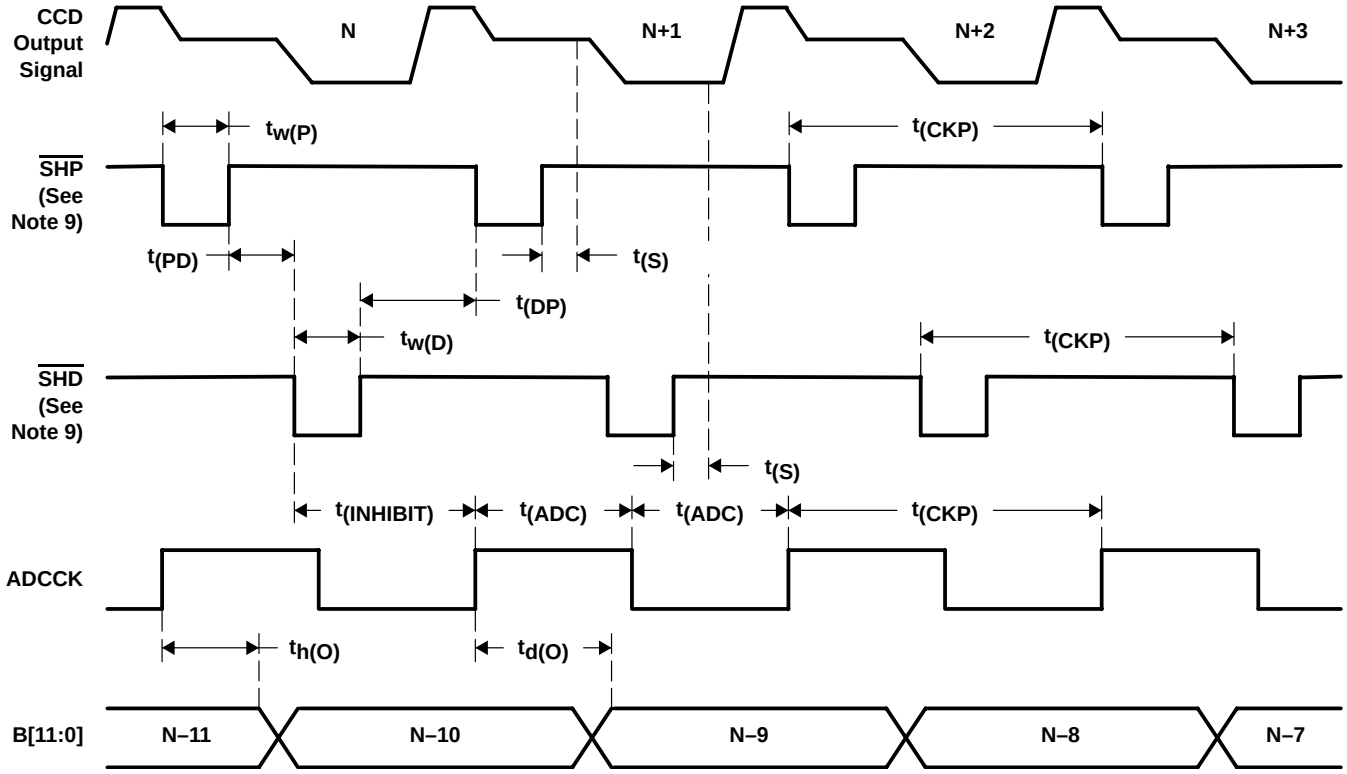
electrical characteristics all specifications at T_A = 25°C, V_{CC} = 3 V, DRV_{DD} = 3 V, conversion rate (f_{ADCCK}) = 20 MHz (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	VSP2272Y, VSP2272M			UNIT
			MIN	TYP	MAX	
TRANSFER CHARACTERISTICS						
DNL	Differential nonlinearity	PGA gain = 0 dB		±0.5		LSB
INL	Integral nonlinearity	PGA gain = 0 dB		±1		LSB
	No missing codes			Assured		
	Step response settling time	Full-scale step input		1		pixel
	Overload recovery time	Step input from 1.8 V to 0 V		2		pixels
	Data latency			9 (fixed)		Clock Cycles
	Signal-to-noise ratio (see Note 1)	Grounded input capacitor, PGA gain = 0 dB		77		dB
		Grounded input capacitor, gain = 24 dB		53		
	CCD offset correction range		–180		200	mV
CDS						
	Reference sample settling time	Within 1 LSB, driver impedance = 50 Ω			8.9	ns
	Data sample settling time	Within 1 LSB, driver impedance = 50 Ω			8.9	ns
INPUT CLAMP						
	Clamp-on resistance			400		Ω
	Clamp level			1.5		V
PROGRAMMABLE GAIN AMPLIFIER (PGA)						
	Gain control resolution			10		Bits
	Maximum gain	Gain code = 1111111111		42		dB
	High gain	Gain code = 1101001000		34		
	Medium gain	Gain code = 1000100000		20		
	Low gain	Gain code = 0010000000		0		
	Minimum gain	Gain code = 0000000000		–6		
	Gain control error			±0.5		
OPTICAL BLACK CLAMP LOOP						
	Control DAC resolution			10		Bits
	Optical black clamp level	Programmable range of clamp level	2		242	LSB
		OBCLP level at CODE = 1000		130		
	Minimum output current for control DAC	COB pin		±0.15		µA
	Maximum output current for control DAC	COB pin		±153		µA
	Loop time constant	C_{COB} = 0.1 µF		40.7		µs
	Slew rate	C_{COB} = 0.1 µF, Saturated output current of control DAC		1530		V/s
POWER SUPPLY						
	Supply voltage	V_{CC}, DRV_{DD}	2.7	3	3.6	V
	Power dissipation	Normal operation mode: No load		94		mW
		Stand-by mode: f_{ADCCK} = Does not apply		6		
TEMPERATURE RANGE						
	Operating temperature		–25		85	°C
θ_{JA}	Thermal resistance	VSP2272Y: 48-lead LQFP		100		°C/W
		VSP2272M: 48-lead P-VQFN		107		

NOTE 1: SNR = 20 log (full-scale voltage / rms noise)

timing specification

VSP2272 CDS

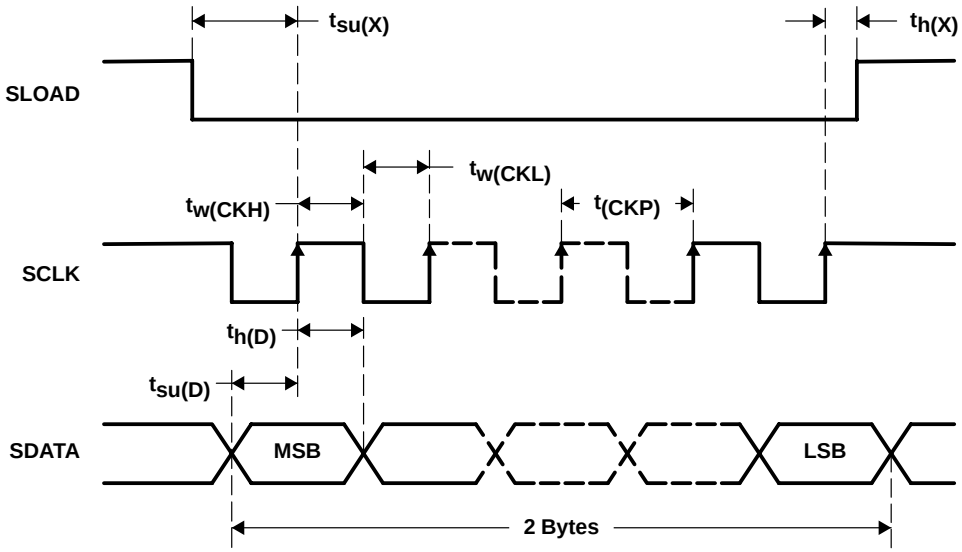


SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	35			ns
$t_{(ADC)}$	ADCCK high/low pulse width	17			ns
$t_{w(P)}$	SHP pulse width	8			ns
$t_{w(D)}$	SHD pulse width	8			ns
$t_{(PD)}$	SHP trailing edge to SHD leading edge (see Note 9)	8			ns
$t_{(DP)}$	SHD trailing edge to SHP leading edge (see Note 9)	8			ns
$t_{(S)}$	Sampling delay		3		ns
$t_{(INHIBIT)}$	Inhibited clock period	20			ns
$t_{h(O)}$	Output hold time	2			ns
$t_{d(O)}$	Output delay (no load)			22	ns
DL	Data latency, normal operation mode		9 (fixed)		Clock Cycles

NOTES: 9. The description and the timing diagrams in this data sheet are all based on the polarity of active low (default value).
10. The user can select the active polarity (active low or active high) through the serial interface, refer to the *serial interface* section for details.
11. Output hold time is specified at additional output delay = 0 ns, refer to the *serial interface* section for details.

timing specifications (continued)

VSP2272 serial interface



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(CKP)}$	Clock period	100			ns
$t_{w(CKH)}$	Clock high pulse width	40			ns
$t_{w(CKL)}$	Clock low pulse width	40			ns
$t_{su(D)}$	Data setup time	30			ns
$t_{h(D)}$	Data hold time	30			ns
$t_{su(X)}$	SLOAD to SCLK setup time	30			ns
$t_{h(X)}$	SCLK to SLOAD hold time	30			ns

NOTES: 12. Data shift operation must decode at the rising edges of SCLK while SLOAD is low. Two bytes of input data are loaded to the parallel latch in the VSP2272 device at the rising edge of SLOAD.

13. When the input serial data is longer than 2 bytes (16 bits), the last 2 bytes become effective and the former bits are lost.

PRINCIPLES OF OPERATION

introduction

The VSP2272 device is a complete mixed-signal IC that contains all the key features associated with the processing of CCD imager output signals in a video camera, a digital still camera, security camera, or similar applications. A simplified block diagram is shown on page 3 of this data sheet. The VSP2272 device includes correlated double sampler (CDS), programmable gain amplifier (PGA), analog-to-digital converter (ADC), input clamp, optical black (OB) level clamp loop, serial interface, timing control, and reference voltage generator.

An off-chip emitter follower buffer is recommended between the CCD output and the VSP2272 CCDIN input. The PGA gain control, the clock polarity setting, and the operation mode can be selected through the serial interface. All parameters are reset to their default values when pin 45 ($\overline{\text{RESET}}$) goes low asynchronously from the clocks.

correlated double sampler (CDS)

The output signal of a CCD imager is sampled twice during one pixel period; once at the reference interval and again at the data interval. Subtracting these two samples extracts the video information of the pixel and removes any noise that is common—or correlated—to both intervals. Thus, the CDS reduces the reset noise and the low frequency noises that are present on the CCD output signal. Figure 1 shows the simplified block diagram of the CDS and input clamp.

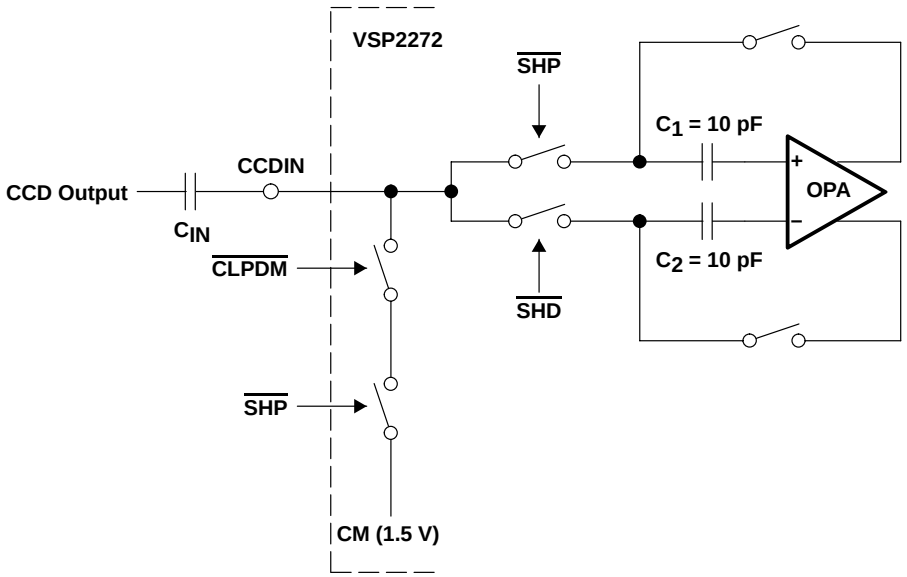


Figure 1. Simplified Block Diagram of CDS and Input Clamp

The CDS is driven through an off-chip coupling capacitor C_{IN}. AC-coupling is strongly recommended because the dc level of the CCD output signal is usually too high (several volts) for the CDS to work properly. A 0.1-µF capacitor is recommended for C_{IN}, but it depends on the application environment.

Also, an off-chip emitter follower buffer is recommended to drive more than 10 pF, because the 10-pF sampling capacitor and a few pF of stray capacitance can be seen at the input pin. The analog input signal range at pin 30 (CCDIN) is 1 Vp-p, and the appropriate common mode voltage for the CDS is around 0.5 to 1.5 V.

PRINCIPLES OF OPERATION

correlated double sampler (CDS) (continued)

The reference level is sampled during the SHP active period, and the voltage level is held by the sampling capacitor C_1 at the trailing edge of SHP. The data level is sampled during the SHD active period, and the voltage level is held by the sampling capacitor C_2 at the trailing edge of SHD. Then, the switched-capacitor amplifier performs the subtraction of these two levels.

The user can select the active polarity of SHP/SHD (active high or active low) through the serial interface; refer to the *serial interface* section for details. The default polarity of SHP/SHD is *active low*. Upon power on, this value is not defined. For this reason, it must be set to the appropriate value by using the serial interface, and reset to the default value by strobing pin 45 ($\overline{\text{RESET}}$). The description and the timing diagrams in this data sheet are all based on active low polarity (default value).

input clamp and dummy pixel clamp

The buffered CCD output is capacitively coupled to the VSP2272 device. The input clamp restores the dc component of the input signal that was lost with the ac-coupling and establishes the desired dc bias point for the CDS. Figure 1 also shows a simplified block diagram of the input clamp. The input level is clamped to the internal reference voltage CM (1.5 V) during the dummy pixel interval. Specifically, when both CLPDM and SHP are active, the dummy clamp function becomes active. If the dummy pixels and/or the CLPDM pulse are not available in your system, the CLPOB pulse can be used in place of the CLPDM pulse, as long as the clamping takes place during black pixels. In this case, both the CPLDM (active at the same timing as CLPOB) and SHP signals become active during the optical black pixel interval; then the dummy clamp function becomes active.

The user can select the active polarity of CLPDM and SHP (active high or active low) through the serial interface, refer to the *serial interface* section for details. The default value of CLPDM and SHP is active low. Upon power on, this value is not defined. For this reason, it must be set to the appropriate value by using the serial interface, and reset to the default value by strobing pin 45 ($\overline{\text{RESET}}$). The description and the timing diagrams in this data sheet are all based on active low polarity (default value).

high performance analog-to-digital converter (ADC)

The analog-to-digital converter (ADC) utilizes a fully differential and pipelined architecture. This ADC is well suited for low voltage operation, low power consumption requirements, and high-speed applications. Twelve-bit resolution with no missing code is assured.

The VSP2272 device includes the reference voltage generator for the ADC. Positive reference voltage, pin 38 (REFP), negative reference voltage, pin 39 (REFN), and common-mode voltage, pin 37 (CM) must be bypassed to the ground with a 0.1-µF ceramic capacitor. Do not use these voltages elsewhere in the system. They affect the stability of these reference levels, which causes ADC performance degradation. Also, these are analog output pins. Do not apply external voltages.

programmable gain amplifier (PGA)

Figure 2 shows the characteristics of the PGA gain. The PGA provides a gain range of –6 dB to 42 dB, which is linear in dB. The gain is controlled by a digital code with 10-bit resolution, and it can be set through the serial interface, refer to the *serial interface* section for details. The default value of the gain control code is 128 (PGA gain = 0 dB).

Upon power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, and reset to the default value by strobing pin 45 ($\overline{\text{RESET}}$).

PRINCIPLES OF OPERATION

optical black (OB) level clamp loop

To extract the video information correctly, the CCD signal must be referenced to a well-established optical black (OB) level. The VSP2272 device has an auto-calibration loop to establish the OB level, using the optical black pixel output from the CCD imager. The input signal level of the OB pixels is identified as the real OB level, and the loop must be closed while CLPOB is active. During the effective pixel interval, the reference level of the CCD output signal is clampled to the OB level by the OB level clamp loop. To determine the loop time constant, a required off-chip capacitor must be connected to pin 28 (COB). The time constant T is given the following equation:

$$T = \frac{C}{\left(16384 \times I_{min}\right)}$$

where, C is the capacitor value connected to pin 28 (COB). I_{min} is the minimum current (0.15 μA) of the control DAC in the OB level clamp loop, and 0.15 μA is equivalent to 1 LSB of the DAC output current. When C is 0.1 μF, the time constant T is 40.7 μs. The slew rate SR is given the following equation:

$$SR = \frac{I_{max}}{C}$$

where, C is the capacitor value connected to pin 28 (COB). I_{max} is the maximum current (153 μA) of the control DAC in the OB level clamp loop, and 153 μA is equivalent to 1023 LSB of the DAC output current.

Generally, the OB level clampling at high-speed causes clamp noise or white streak noise. However, the noise is reduced by making C large. On the other hand, a large C requires a much longer time to restore from the stand-by mode or right after the power goes ON. Therefore, 0.1 μF to 0.22 μF is considered the reasonable value range for C. However, the value depends on the application environment. Make careful adjustments by the trial and error method.

The OB clamp level (the pedestal level) is programmable through the serial interface, refer to the *serial interface* section for details. Table 1 shows the relationship between input code and the OB clamp level.

The user can choose the active polarity of CLPOB (active high or active low) through the serial interface, refer to the *serial interface* section for details. The default value of CLPOB is active low. Upon power on, this value is unknown. For this reason, it must be set to the appropriate value by using the serial interface, and reset to the default value by strobing pin 45 ($\overline{\text{RESET}}$). The description and the timing diagrams in this data sheet are all based on a polarity of active low (default value).

PRINCIPLES OF OPERATION

Table 1. Programmable OB Clamp Level

INPUT CODE	OB CLAMP LEVEL, LSBS OF 12 BITS
0000	2 LSB
0001	18 LSB
0010	34 LSB
0011	50 LSB
0100	66 LSB
0101	82 LSB
0110	98 LSB
0111	114 LSB
1000 (Default)	130 LSB
1001	146 LSB
1010	162 LSB
1011	178 LSB
1100	194 LSB
1101	210 LSB
1110	226 LSB
1111	242 LSB

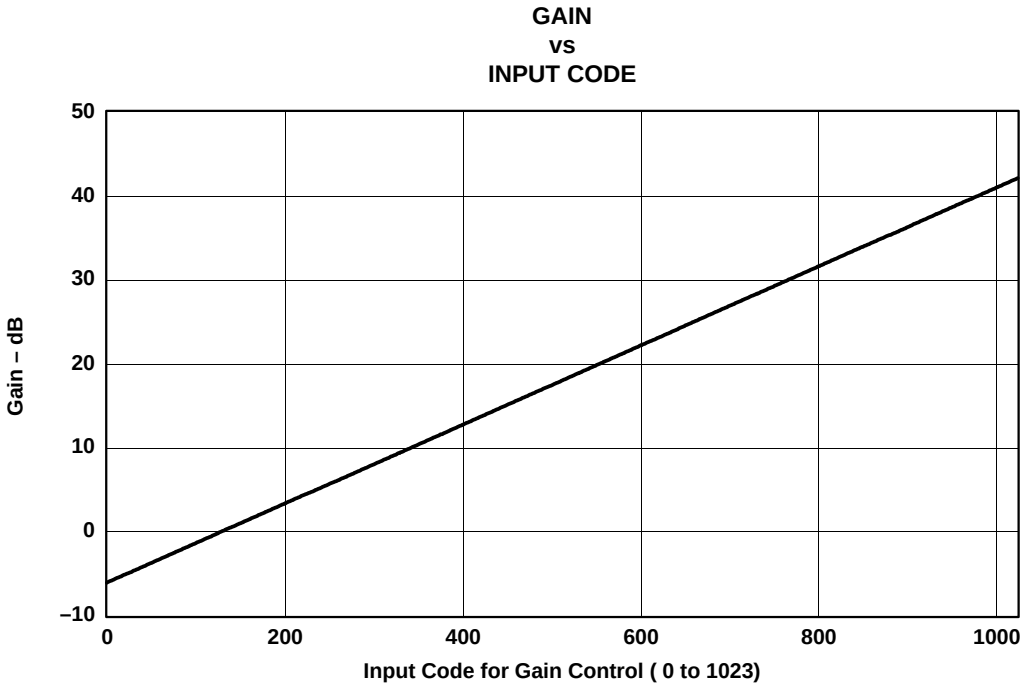


Figure 2. The Characteristics of PGA Gain

PRINCIPLES OF OPERATION

preblanking and data latency

The VSP2272 device has an input blanking (or preblanking) function.

When pin 19 (PBLK) goes low, the digital outputs go to all 0s at the 11th rising edge of ADCCK counting from PBLK.

In this mode, the digital output data comes out on the rising edge of ADCCK with a delay of 11 clock cycles (data latency is 11). This is different from the preblanking mode, in which the digital output data comes out on the rising edge of ADCCK with a delay of 9 clock cycles (data latency is 9).

If the input voltage is higher than the supply rail by 0.3 V, or lower than the ground rail by 0.3 V, then protection diodes are turned on to prevent the input voltage from going further. Such a high signal swing, which may cause damage to the VSP2272 device, must be avoided.

stand-by mode

For the purpose of saving power, the VSP2272 device can be put into the stand-by mode (or power down mode) through the serial interface when the device is not in operation. Refer to the *serial interface* section for details. In this mode, all the function blocks are disabled and the digital outputs are all 0s. Current consumption drops to 2 mA.

As all bypass capacitors discharge during this mode, a substantial time (usually of the order of 200 ms to 300 ms) is required to restore the device from the stand-by mode.

additional output delay control

The VSP2272 device can control the delay time of output data by setting the register through the serial interface. In some cases, the transition of output data affects analog performance. Generally, this is avoided by adjusting the timing of ADCCK. In case ADCCK timing cannot be adjusted, this output delay control is effective in reducing the influence of transient noise. Refer to the *serial interface* section for details.

voltage reference

All reference voltages and bias currents needed by the VSP2272 device are generated by internal bandgap circuitry. The CDS and the ADC mainly use three reference voltages, positive reference, pin 38 (REFP), negative reference, pin 39 (REFN), and common-mode voltage, pin 37 (CM). All REFP, REFN, and CM voltages must be heavily decoupled with appropriate capacitors (for example: 0.1-µF ceramic capacitor). Do not use these voltages elsewhere in the system. They affect the stability of these reference levels, which causes ADC performance degradation. These are analog output pins. Do not apply external voltages.

Pins 29 (BYPP2), 31 (BYP), and 32 (BYPM) are also reference voltages to be used in the analog circuit. Pin 31 must be connected to ground with a 0.1-µF ceramic capacitor. The capacitor values for pins 29 and 32 affect the step response. For many applications, 400 pF to 1000 pF is a reasonable value.

Depending on the application environment, TI recommends careful adjustment by the trial-and-error method. Pins 29 (BYPP2), 31 (BYP), and 32 (BYPM) must be heavily decoupled with the appropriate capacitors. Do not use these voltages elsewhere in the system. They affect the stability of these reference levels, which causes performance degradation. These are analog output pins. Do not apply external voltages.

PRINCIPLES OF OPERATION

serial interface

The serial interface has a 2-byte shift register and various parallel registers to control all the digitally programmable features of the VSP2272 device. Writing to these registers is controlled by the signals at pins 46 (SLOAD), 48 (SCLK), 47 (SDATA), and 45 ($\overline{\text{RESET}}$). To enable the shift register, SLOAD must be pulled low. SDATA is the serial data input, and SCLK is the shift clock. The data at SDATA is taken into the shift register at the rising edge of SCLK. The data length must be 2 bytes.

After the 2-byte shift operation, the data in the shift register is transferred to the parallel latch at the rising edge of SLOAD. In addition to the parallel latch, there are several registers dedicated to the specific features of the device, and they are synchronized with ADCCK clock. It takes 5 or 6 clock cycles for the data in the parallel latch to be written to those registers. Thus, to complete the data updates requires 5 or 6 clock cycles after the parallel latching by the rising edge of SLOAD.

Serial interface data format is shown in Table 2.

Table 2. Serial Interface Data Format

	MSB															LSB
REGISTERS	**TEST**	**A2**	**A1**	**A0**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C0
PGA gain	0	0	0	1	0	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
OB clamp level	0	0	1	0	0	0	0	0	0	0	0	0	O3	O2	O1	O0
Clock polarity	0	0	1	1	0	0	0	0	0	0	0	0	0	P2	P1	P0
Output delay	0	1	0	0	0	0	0	0	0	0	0	0	0	0	J1	J0
Reserved	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
Reserved	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
Reserved	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
Reserved	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Don't care

C0: Operation Mode, Normal/Stand-by

Serial interface and registers are always active, independent from the operation mode.

C0 = operation mode for the entire device without serial interface and registers. (C0 = 0 active, C0 = 1 stand-by)

G[9:0]: The Characteristics of PGA Gain (refer to Figure 2)

O[3:0]: Programmable OB Clamp Level (refer to Table 1)

P[2:0]: Clock Polarity

P0 = polarity for CLPDM
(P0 = 0 active low, P0 = 1 active high)
P1 = for CLPOB
(P0 = 0 active low, P0 = 1 active high)
P2 = for SHP/SHD
(P0 = 0 active low, P0 = 1 active high)

J[1:0]: Additional Output Delay Control

Control additional output data delay time.

PRINCIPLES OF OPERATION

serial interface (continued)

Table 3. Output Delay Control

J1	J0	OUTPUT DATA DELAY TIME
0	0	Additional delay = 0 ns
0	1	Additional delay = 5 ns (typical)
1	0	Additional delay = 10 ns (typical)
1	1	Additional delay = 13 ns (typical)

Upon power on, these values are not defined. These registers must be set to an appropriate value by using the serial interface, and reset to the default values by strobing pin 45 ($\overline{\text{RESET}}$).

Default values are:

C[0] = 0:	Normal operation mode
G[9:0] = 0010000000:	PGA gain = 0 dB
O[3:0] = 1000:	OB clamp level = 130 LSB
P[2:0] = 000:	$\overline{\text{CLPDM}}$, $\overline{\text{CLPOB}}$, $\overline{\text{SHP}}$/$\overline{\text{SHD}}$ are all active low. [The description and the timing diagrams in this data sheet are all based on a polarity of active low (default value).]
J[1:0] = 00:	Additional output delay = 0 ns

timing

The CDS and the ADC are operated by SHP/SHD, and their derivative timing clocks generated by the on-chip timing generator. The digital output data is synchronized with ADCCK. The timing relationship among the CCD signal, SHP/SHD, ADCCK, and the output data is shown in the VSP2272 CDS timing specifications.

CLPOB activates the black level clamp loop during the OB pixel interval. CLPDM activates the input clamping during the dummy pixel interval. If the CLPDM pulse is not available in your system, the CLPOB pulse can be used in place of CLPDM, as long as the clamping takes place during black pixels, refer to the *input clamp and dummy pixel clamp* section for details. When activating CLPOB and CLPDM on the same timing, the black level may shift a few LSB on high gain. In this case, OB offset correction by the system is needed.

The clock polarities of SHP/SHD, CLPOB, and CLPDM can be independently set through the serial interface, refer to the *serial interface* section for details. The description and the timing diagrams in this data sheet are all based on active low polarity (default value). In order to keep a stable and accurate OB clamp level, CLPOB must not be activated during the PBLK active period.

Refer to the *preblanking and data latency* section for details.

In the stand-by mode, all of ADCCK, SHP, SHD, CLPOB, and CLPDM are internally masked and pulled high.

power supply, grounding and device decoupling recommendations

The VSP2272 device incorporates a very high precision and high-speed ADC and analog circuitry that are vulnerable to any extraneous noise from the rails or elsewhere. For this reason, although the VSP2272 device has analog and digital supply pins, it must be treated as an analog component, and all supply pins except for DRV_{DD} must be powered by the only analog supply of the system. This will ensure the most consistent results, since digital power lines often carry a high level of wide band noise that would otherwise be coupled into the device and degrade the achievable performance.

PRINCIPLES OF OPERATION

power supply, grounding and device decoupling recommendations (continued)

Proper grounding, short lead length, and the use of ground planes are also very important for high frequency designs. Multilayer PC boards are recommended for the best performance, since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. Join the analog and digital ground pins of the VSP2272 device together at the device and connect them only to the analog ground of the system.

The driver stage of the digital outputs (B[11:0]) is supplied through a dedicated supply at pin 13 (DRV_{DD}), and it must be separated from the analog supply (V_{CC}) at pins 18, 24, 27, 33, 34, and 40 completely or at least with a ferrite bead. Keep the capacitive loading on the output data lines (pins 1–12) as low as possible (typically less than 15 pF). Larger capacitive loads demand higher charging current surges that can feed back into the analog portion of the VSP2272 device and affect the performance. Use external buffers or latches to provide the added benefit of isolating the VSP2272 device from any digital noise activities on the data lines.

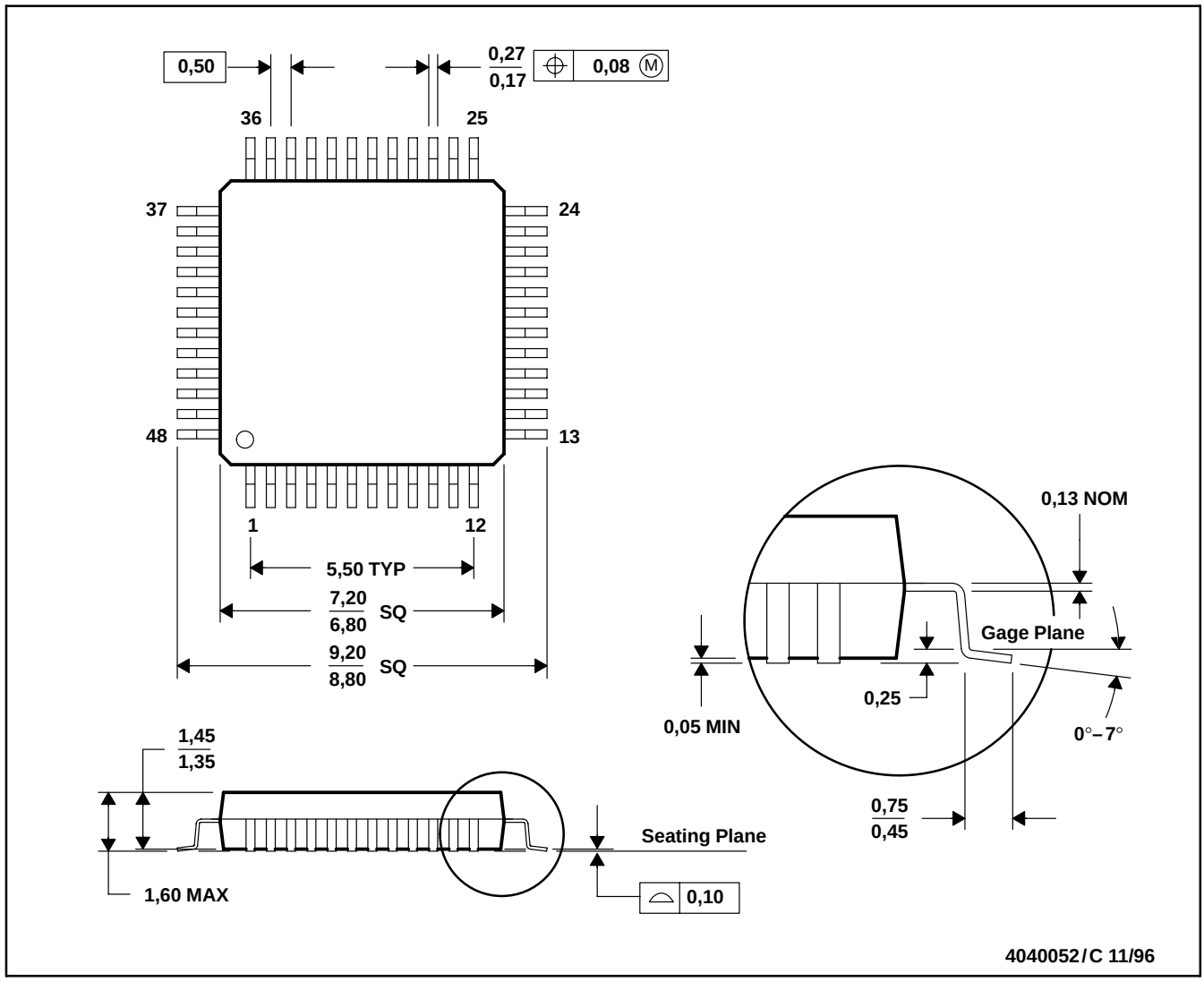
Resistors in series with each data line may help minimize the surge current. Values in the range of 100 Ω to 200 Ω limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances as the output levels change from low to high or high to low. Because of the high operation speed, the converter also generates high frequency current transients and noises that are fed back into the supply and reference lines.

This requires the supply and reference pins be sufficiently bypassed. In most cases, 0.1-μF ceramic chip capacitors are adequate to decouple the reference pins. Supply pins must be decoupled to the ground plane with a parallel combination of tantalum (1 μF to 22 μF) and ceramic (0.1 μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual pin. Pin 13 (DRV_{DD}) must be decoupled to the proximity of pin 14 (DRVGND).

Pay special attention to the bypassing of pins 28 (COB), 29 (BYPP2), and 32 (BYPM), since these capacitor values determine important analog performance of the device.

MECHANICAL DATA

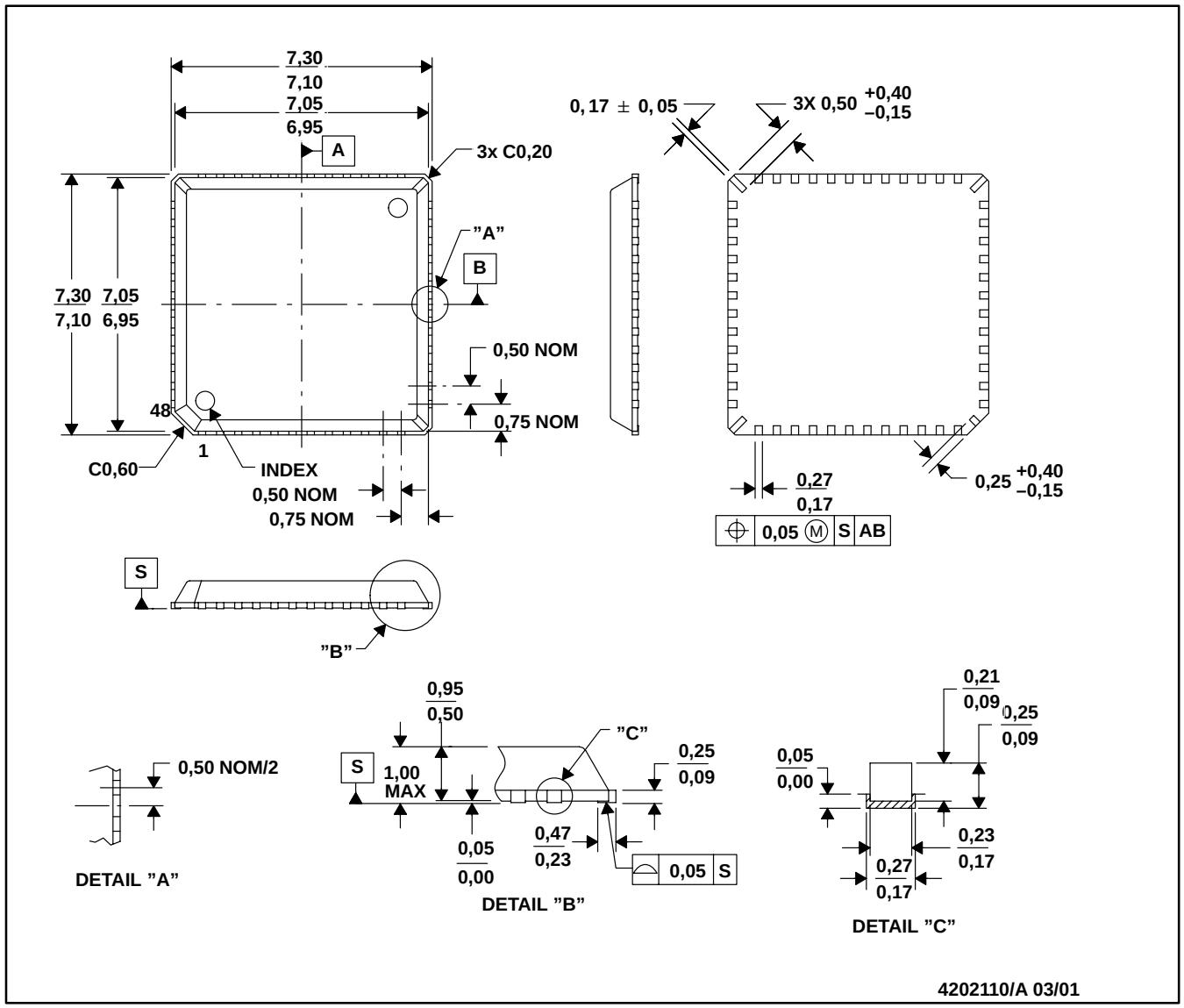
PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

MECHANICAL DATA

RGN (S-PQFP-N48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. These dimensions include package bend.

PACKAGE OPTION ADDENDUM

8-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VSP2272M	ACTIVE	QFN	RGN	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP2272M/2K	ACTIVE	QFN	RGN	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP2272Y	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
VSP2272Y/2K	ACTIVE	LQFP	PT	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265