



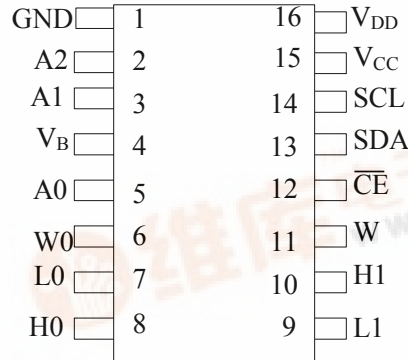
# DS1808 Dual Log Digital Potentiometer

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## FEATURES

- Two 32-position log-tapers
- 60dB attenuation range:
  - 1dB per step (12 taps)
  - 2dB per step (12 taps)
  - 3dB per step (8 taps)
  - 90dB low-end attenuation
- 2-Wire Interface Control
- Power Supply: Dual  $\pm 12V$
- Maximum Voltage Across Potentiometers:  $\pm 12V$
- Standard Resistance Value: 45k $\Omega$
- Packages: 16-Pin SOIC
- Operating Temperature: -40°C to +85°C

## PIN ASSIGNMENT



16-Pin SOIC (150-mil)

## ORDERING INFORMATION

DS1808Z-050      16-Pin SOIC    -40°C to +85°C 45k $\Omega$

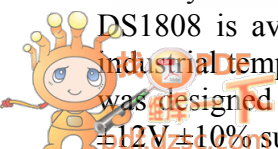
DS1808Z-050/T&R    16-Pin SOIC    -40°C to +85°C 45k $\Omega$

## PIN DESCRIPTION

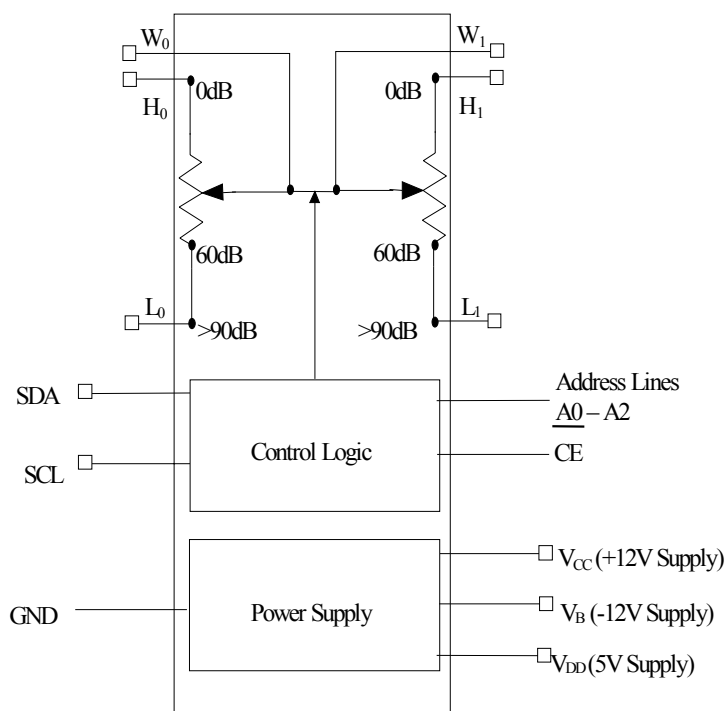
- V<sub>CC</sub>      - +12V Supply
- V<sub>B</sub>      - -12V Supply (substrate bias)
- V<sub>DD</sub>     - 5V Digital Supply
- H<sub>0</sub>, H<sub>1</sub>   - High-end Terminals
- L<sub>0</sub>, L<sub>1</sub>   - Low-end Terminals
- W<sub>0</sub>, W<sub>1</sub> - Wiper Terminals
- SDA      - 2-Wire Serial Data Input/Output
- SCL      - 2-Wire Clock Input
- /CE      - 2-Wire Interface Enable
- GND      - Ground
- A0, A1, A2 - Address Pins

## DESCRIPTION

The DS1808 is a dual-channel, digitally controlled, log-taper potentiometer. Each potentiometer is comprised of 32 wiper terminal positions plus a mute position. The device has three accessible potentiometer terminals that include the high-side terminal (H), the low-side terminal (L), and the wiper terminal (W). The resolution of the DS1808 is shown in Figure 8 and represents 1dB per step for the first 12 taps, 2dB per step for the next 12 taps and 3dB per step for the bottom 8 taps, providing a total attenuation range of 60dB. The mute position of the DS1808 provides greater than 90dB of attenuation. The wiper position on the resistor ladder is selected via a 6-bit register, whose value is controlled by the industry-standard 2-wire interface. The interface consists of two control signals: SDA and SCL. The DS1808 is available in a standard 45k $\Omega$  resistor value. The DS1808 is specified to operate over the industrial temperature range (-40°C to +85°C) and is available in the 16-pin SOIC package. The DS1808 was designed for low-cost, stereo volume control applications. The device is specified to operate from  $\pm 12V \pm 10\%$  supplies and accept a maximum input signal range of  $\pm 12V$ .



## DS1808 BLOCK DIAGRAM Figure 1



### PIN DESCRIPTIONS

**V<sub>CC</sub>** – Power Supply Terminal. This pin acts as the positive rail. The DS1808 will support positive supply voltages ranging from 5 to 13.2 volts. When  $V_{CC} - V_B$  is less than 8 volts the series wiper resistance will increase up to 1k $\Omega$ . The value of  $V_{DD}$  should never exceed  $V_{CC}$ .

**V<sub>B</sub>** – Substrate Bias Supply. This pin acts as a negative rail. The DS1808 will support negative voltages ranging from 0 to -13.2 volts. When  $V_{CC} - V_B$  is less than 8 volts the series wiper resistance will increase up to 1k $\Omega$ .

**V<sub>DD</sub>** – DC Supply Terminal. 5V DC voltage supply. The value of  $V_{DD}$  should never exceed  $V_{CC}$ .

**GND** – Ground Terminal.

**SDA** – 2-wire serial data interface. The serial data pin is for serial data transfer to and from the DS1808. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces.

**SCL** – 2-wire serial clock interface. The serial clock input is used to clock data into the DS1808 on rising edges and clock data out on falling edges.

**/CE** – Port Enable Pin. When active ( $/CE=0$ ), the port inputs **SDA** and **SCL** are recognized by the device. If inactive ( $/CE=1$ ), the port input pins **SDA** and **SCL** are disabled making 2-wire communication impossible.

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**A0, A1, A2** – Address Inputs. These input pins specify the address of the device when used in a multi-dropped configuration. Up to eight individual DS1808s may be addressed on a single 2-wire bus.

**H0, H1** – These are the high-end terminals of the potentiometers. For both potentiometers, it is not required that these terminals be connected to a potential greater than the low-end terminal of the potentiometer. Voltage applied to the high end of the potentiometers cannot exceed the power supply voltage,  $V_{CC}$ , or go below  $V_B$ .

**L0, L1** – These are the low-end terminals of the potentiometers. It is not required that these terminals be connected to a potential less than the high-end terminals of the pot. Voltage applied to the low end of the potentiometers cannot exceed the power-supply voltage,  $V_{CC}$ , or go below  $V_B$ .

**W0, W1** – Wiper of the Potentiometer. This pin is the wiper terminal of the potentiometer. Voltage applied to either wiper terminal cannot exceed the power-supply voltage,  $V_{CC}$ , or go below  $V_B$ .

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## OPERATION

The DS1808 is a dual-channel, digitally controlled, logarithmic potentiometer. Each potentiometer has three accessible terminals, which include H, L, and W. Between each resistor element is a tap-point that is multiplexed to the wiper terminal, W. A block diagram of the DS1808 is shown in Figure 1.

### Potentiometer Characteristics

The DS1808 is a volatile device and always powers-up with the wiper positions set to the mute position (33-decimal) with 90-dB of signal attenuation. The resistor section of the DS1808 is composed of two 32-position resistor arrays that provide a logarithmic attenuation. The resistor section of the DS1808 provides a typical 50k $\Omega$  end-to-end resistance between the H terminal and the L terminal. The wiper terminal will have a total possible 34 tap positions. The 34<sup>th</sup> position is considered the mute position and will provide attenuation in excess of 90dB.

The potentiometers of the DS1808 are closely matched and provide excellent tracking. Interchannel matching for the device is specified to provide less than 0.5dB. Tap-to-tap tolerances for the device are specified to provide less than 0.5dB.

### Power Supplies

The DS1808 is designed to be powered from dual  $\pm 12V$  supplies. The maximum input signal that can be placed across the potentiometer sections is  $\pm 12V$ . The device can also be powered using a single +12V power source. When using the device in a single supply configuration,  $V_B$  is set to 0V and the maximum potentiometer input signals are restricted to single supply voltage rails.

### Controlling the Potentiometers

All writing and reading to the potentiometers is done with the industry standard 2-wire interface, which includes pins SDA and SCL.

## 2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions. The DS1808 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: /CE, SDA, SCL, A0, A1, A2. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 7.

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## 2-WIRE SERIAL PROTOCOL

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus not busy:** Both data and clock lines remain high.

**Start data transfer:** A change in the state of the data line from high to low while the clock is high defines a start condition.

**Stop data transfer:** A change in the state of the data line from low to high while the clock line is high defines the stop condition.

**Data valid:** The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between start and stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9<sup>th</sup> bit.

Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1808 works in both modes.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an “acknowledge” after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the stop condition.

1. The following occurs when data is transferred from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. The following occurs when data is transferred from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” can be returned.

The master device generates all serial clock pulses and the start and stop conditions. A transfer is ended with a stop condition or with a repeated start condition. Since a repeated start condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1808 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. Start and stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.
2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1808 while the serial clock is input on SCL. Start and stop conditions are recognized as the beginning and end of a serial transfer.
3. Slave Address: command/control byte is the first byte received following the start condition from the master device. The command/control byte consists of a 4-bit control code. For the DS1808, this is set as 0101 binary for read/write operations. The next three bits of the command/control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight devices is to be accessed. When reading or writing the DS1808, the device select bits must match the device select pins (A2, A1, A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1, a read operation is selected, and when set to a 0, a write operation is selected.

Following the START condition, the DS1808 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the **0101** control code, the appropriate device address bits, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

## COMMAND AND PROTOCOL

The command and protocol structure of the DS1808 allows the user to read from or write to the potentiometer(s). Additionally, the 2-wire command/protocol structure of the DS1808 will support eight different devices and a maximum of 16 channels that can be uniquely controlled. The command structures for the device are presented in Figures 3, 4, 5, and 6. Potentiometer data values and command/control values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the acknowledgement.

## READING THE DS1808

As shown in Figure 4, the DS1808 provides one read command operation. This operation allows the user to read both potentiometers. To initiate a read operation, the R/W bit of the command/control byte is set to 1. Communication to read the DS1808 begins with a start condition, which is issued by the master device. The command/control byte from the master device will follow the start condition. Once the command/control byte has been received by the DS1808, the part will respond with an acknowledge.

When the master has received the acknowledge from the DS1808, the master can then begin to receive wiper data. The value of the wiper of potentiometer-0 will be the first returned from the DS1808. It will then be followed by the value of potentiometer-1. Once the 8-bits of potentiometer-0 have been transmitted, the master will need to issue an acknowledge, unless it is the only byte to be read, in which case the master issues a 'not acknowledge.' If desired, the master may stop the communication transfer at this point by issuing the stop condition. However, if the value of the remaining potentiometer is needed, transfer can continue by clocking the 8 bits of the potentiometer-1 value, followed by a not acknowledge.

## WRITING TO THE DS1808

A data flow diagram of the DS1808 is shown in Figure 5. The DS1808 has one write command that is used to change the position of the wiper(s). All write operations begin with a START from the master, followed by a command/control byte. The R/W bit should be written to 0b, which initiates a write command. Once the command/control byte has been issued and the master receives the ACKNOWLEDGE from the DS1808, potentiometer wiper data is transmitted to the DS1808 by the master device.

Figure 2

### 2-WIRE DATA TRANSFER OVERVIEW

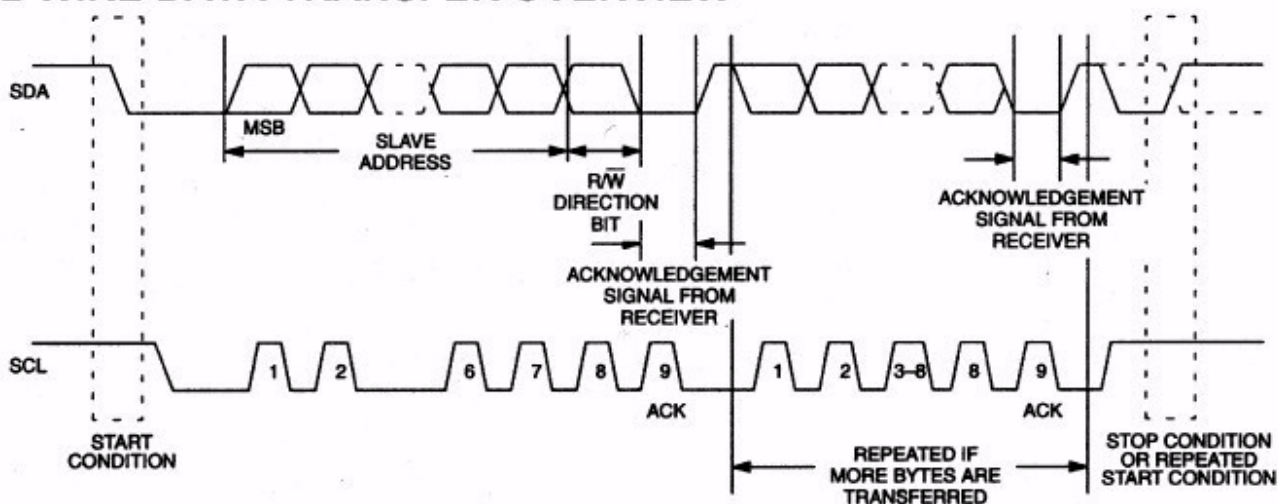


Figure 3

### COMMAND/CONTROL BYTE

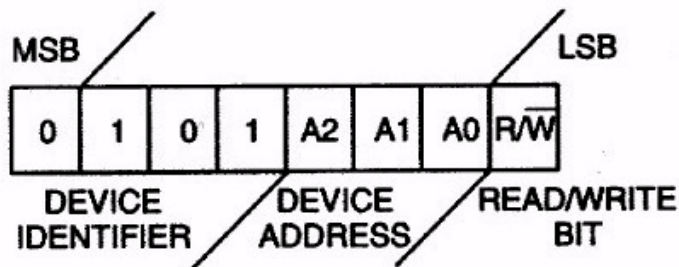
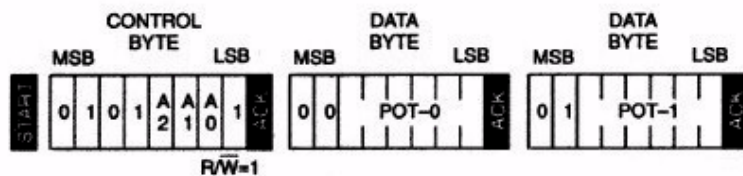


Figure 4

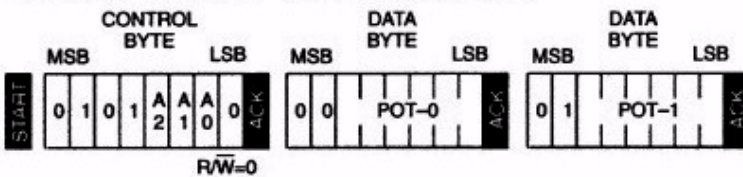
### 2-WIRE READ PROTOCOL



POTENTIOMETER DATA BYTES ARE READ IN THE ORDER INDICATED.

Figure 5

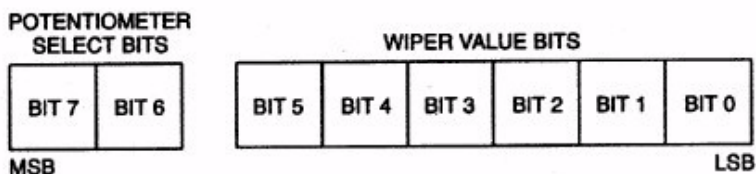
### 2-WIRE WRITE PROTOCOLS



POTENTIOMETER DATA BYTES CAN BE LOADED IN ANY ORDER.

Figure 6

### WIPER REGISTER CONFIGURATION

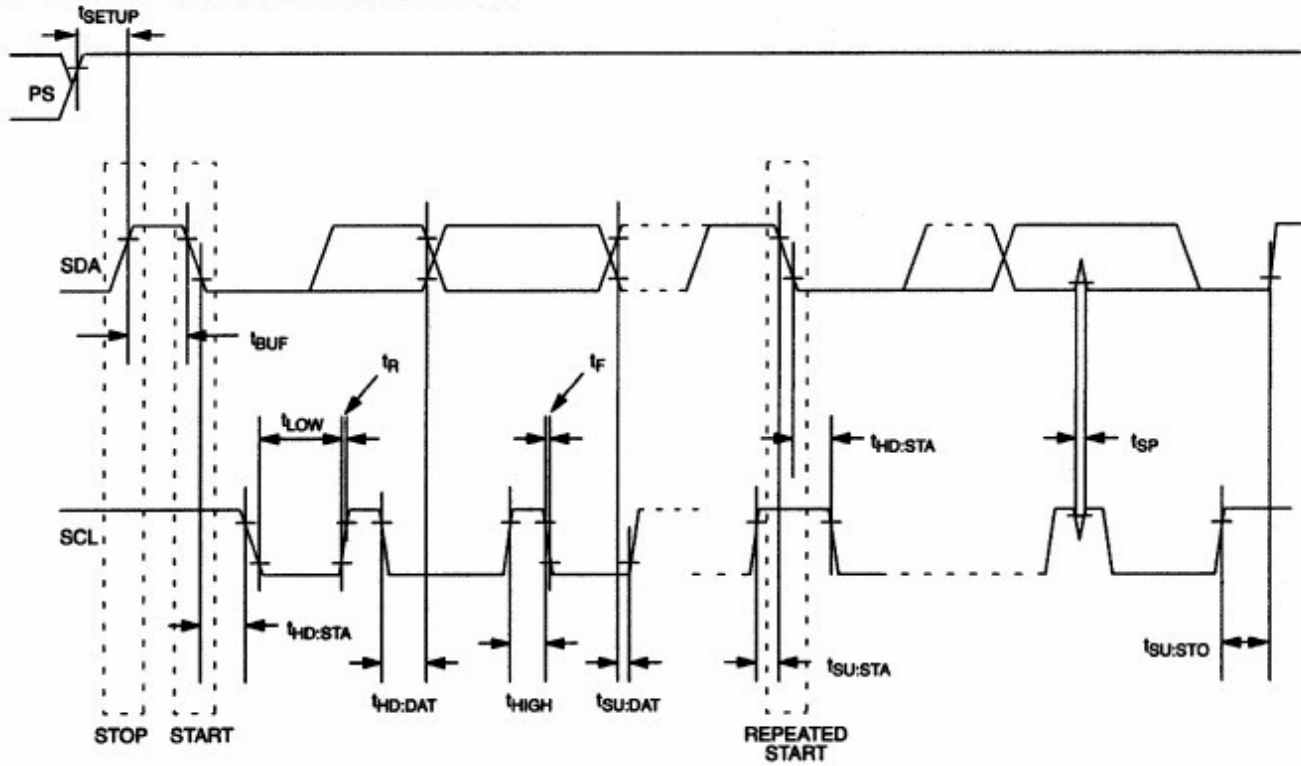


BITS 7, 6  
 00 – POTENTIOMETER-0 SELECT  
 01 – POTENTIOMETER-1 SELECT



Figure 7

## 2-WIRE TIMING DIAGRAM



**TAP/ATTENUATION TABLE** Figure 8

<b>TAP POSITION</b>	<b>ATTENUATION (dB)</b>
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	14
14	16
15	18
16	20
17	22
18	24
19	26
20	28
21	30
22	32
23	34
24	36
25	39
26	42
27	45
28	48
29	51
30	54
31	57
32	60
33	90

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on All Pins (except /CE, SDA, SCL, A0, A1, and A2) Relative to Ground  
 Voltage on Pins /CE, SDA, SCL, A0, A1, and A2  
 Operating Temperature  
 Storage Temperature  
 Soldering Temperature

$V_B - 0.3V$  to  $V_{CC} + 0.3V$   
 $GND - 0.3V$  to  $V_{DD} + 0.3V$   
 $-40^{\circ}C$  to  $+85^{\circ}C$   
 $-55^{\circ}C$  to  $+125^{\circ}C$   
 See J-STD-020A specification

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Analog Supply Voltage	$V_{CC}$	+4.5		+13.2	V	1, 3
Substrate Bias Voltage	$V_B$	-13.2		0	V	3
Digital Supply Voltage	$V_{DD}$	4.5		5.5	V	3
Resistor Inputs	L,H,W	$V_B$		$V_{CC}$	V	

**DC ELECTRICAL CHARACTERISTICS**

(-40°C to +85°C/ $V_{CC}$ ,  $V_B = \pm 5V$  to  $\pm 13.2V$ / $V_{DD} = 4.5V$  to  $5.5V$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	$I_{CC}$				2	mA	12, 13
Input Leakage	$I_{LI}$		-1		+1	$\mu A$	
Input Logic 1	$V_{IH}$		$0.7V_{DD}$		$V_{DD} + 0.3V$	V	2
Input Logic 0	$V_{IL}$		GND-0.3		0.8	V	2
Power Up Time (Port Active)	$t_{PU}$				1	ms	
Standby Current ( $V_{CC}$ , $V_B$ )	$I_{STBY}$	$\pm 8V$ $\pm 12V$			15 25	$\mu A$	4
Active Supply Current ( $V_B$ )					2.0	mA	12, 13

**ANALOG RESISTOR CHARACTERISTICS**(-40°C to +85°C/ $V_{CC}$ ,  $V_B = \pm 5V$  to  $\pm 13.2V$ / $V_{DD} = 4.5V$  to  $5.5V$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistance			-20		+20	%	
Total Resistance				45k $\Omega$			
Absolute Linearity			-0.5		+0.5	LSB	9
Relative Linearity			-0.25		+0.25	LSB	10
Interchannel Matching			-0.5		+0.5	dB	
-3 dB Cutoff frequency	$f_{cutoff}$			5		MHz	
Output Noise (20Hz to 20kHz, Grounded Input, Tap = -6dB)				2.2		$\mu V_{RMS}$	
Total Harmonic Distortion	THD+N			0.001		%	
Interchannel Isolation (20Hz to 20kHz, Grounded Input, Tap = -6dB)				-100		dB	
Mute Position				-90		dB	
Wiper Resistance	$R_W$			300	600	$\Omega$	
Wiper Current	$I_W$				1	mA	
Resistor Inputs	L,H,W		$V_B$		$V_{CC}$	V	
Temperature Coefficient				750		ppm/ $^{\circ}C$	11

**CAPACITANCE**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$				10	pF	

**AC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C,  $V_{DD}=4.5V$  to 5.5V)

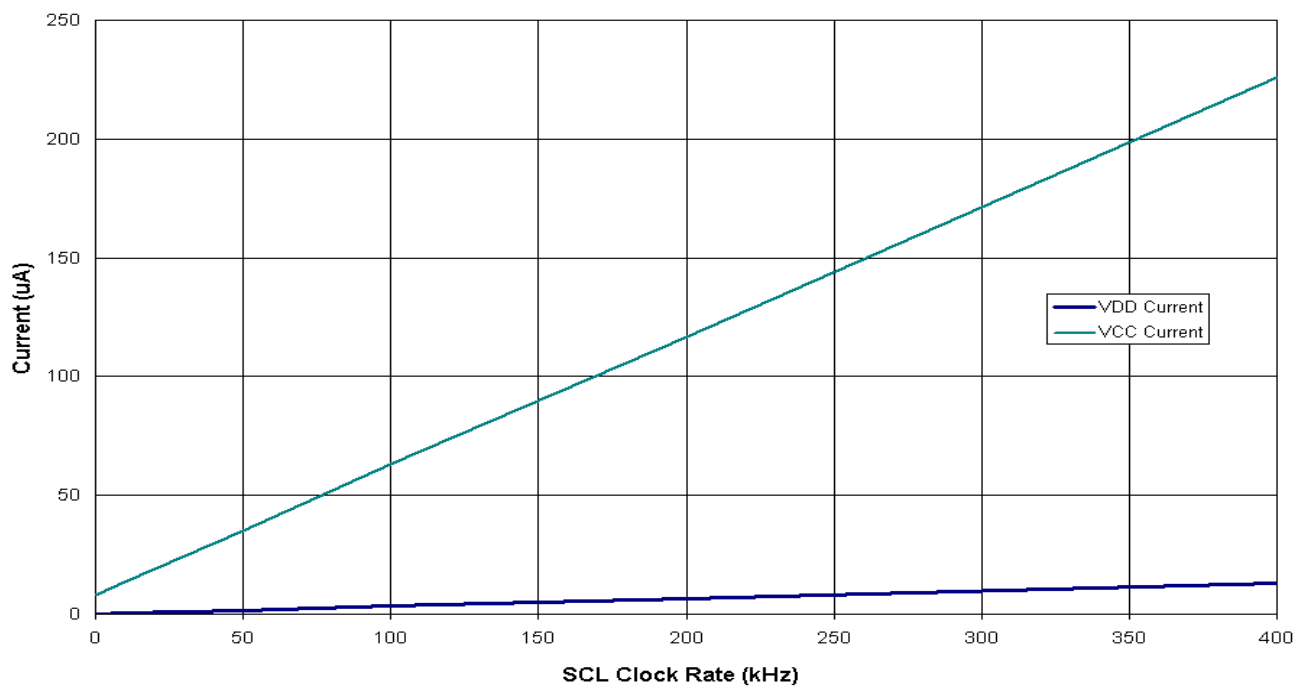
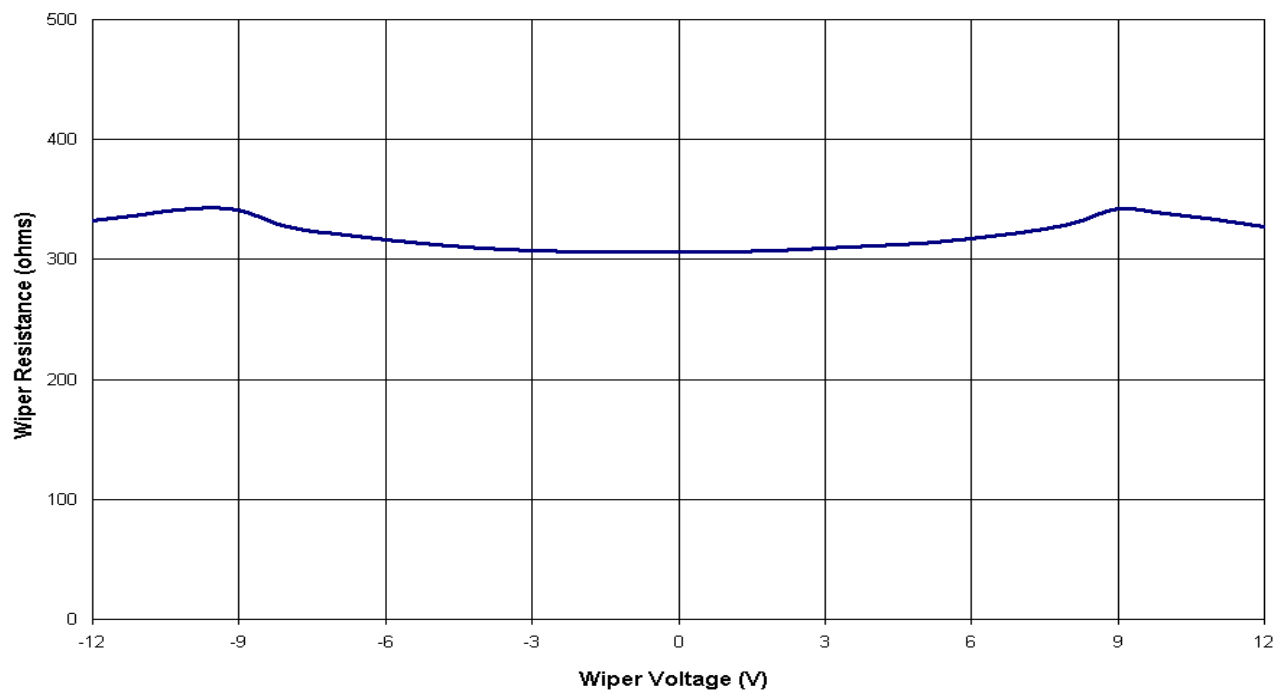
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	$f_{SCL}$	Fast Mode Standard Mode	0 0		400 100	kHz	5
Bus Free Time Between STOP and START	$t_{BUF}$		1.3 4.7			$\mu s$	5
Hold Time (repeated) START Condition	$t_{HD:STA}$		0.6 4.0			$\mu s$	6, 5
Low Period of SCL Clock	$t_{LOW}$		1.3 4.7			$\mu s$	5
High period of SCL Clock	$t_{HIGH}$		0.6 4.0			$\mu s$	5
Data Hold Time	$t_{HD:DAT}$		0 0		0.9	$\mu s$	5,7
Data Set-Up Time	$t_{SU:DAT}$		100 250			ns	5
Start Set-Up Time	$t_{SU:STA}$		0.6 4.7			$\mu s$	5
Rise Time of Both SDA and SCL Signals	$t_R$		20+0.1 $C_B$		300 1000	ns	8
Fall Time of Both SDA and SCL Signals	$t_F$		20+0.1 $C_B$		300 300	ns	8
Set-Up Time for STOP Condition	$t_{SU:STO}$		0.6 4.0			$\mu s$	
Capacitive Load for Each Bus Line	$C_B$				400	pF	8

**NOTES:**

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if  $V_{CC}$  is switched off.
3. The value of  $V_{DD}$  should never exceed  $V_{CC}$ , including during power-ups.  $V_{CC}$  must be applied before either  $V_{DD}$  or  $V_B$ .  $V_{DD}$  and  $V_B$  can then follow in any order.
4.  $I_{STBY}$  specified for  $V_{DD}$  equal to 5.0V. Control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5V of ground or  $V_{DD}$  for the corresponding inactive state.
5. A fast mode device can be used in a standard mode system, but the requirement  $t_{SU:DAT} > 250\text{ns}$  must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250\text{ns}$  before the SCL line is released.
6. After this period, the first clock pulse is generated.
7. The maximum  $t_{HD:DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
8.  $C_B$  – Total capacitance of one bus line in picofarads, timing referenced to  $(0.9)(V_{DD})$  and  $(0.1)(V_{DD})$ .
9. Absolute linearity is used to measure expected wiper voltage as determined by wiper position.
10. Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions.
11. When used as a rheostat or variable resistor the resistance temperature coefficient is:  $750\text{ppm}/^\circ\text{C}$ . When used as a voltage divider or potentiometer, the output voltage temperature coefficient approaches  $30\text{ppm}/^\circ\text{C}$ .
12.  $I_{CC}$  specified with SDA pin open.
13. Maximum  $I_{CC}$  is dependent on clock rates.

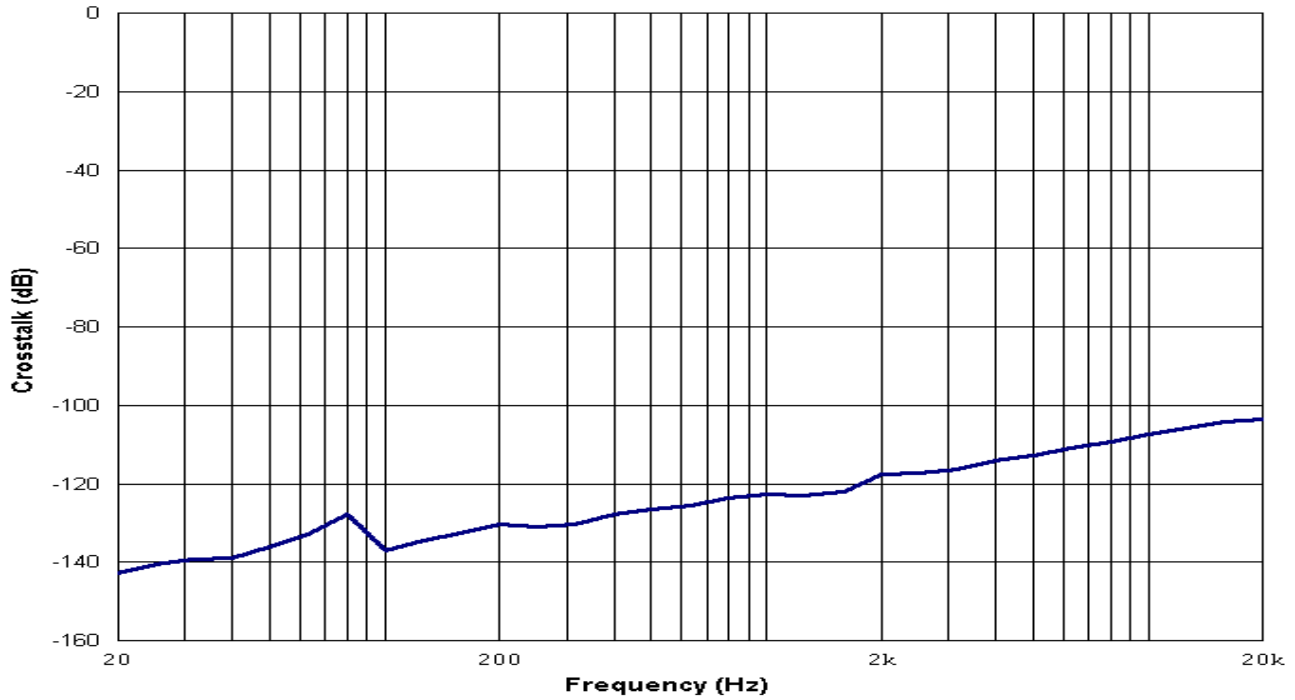
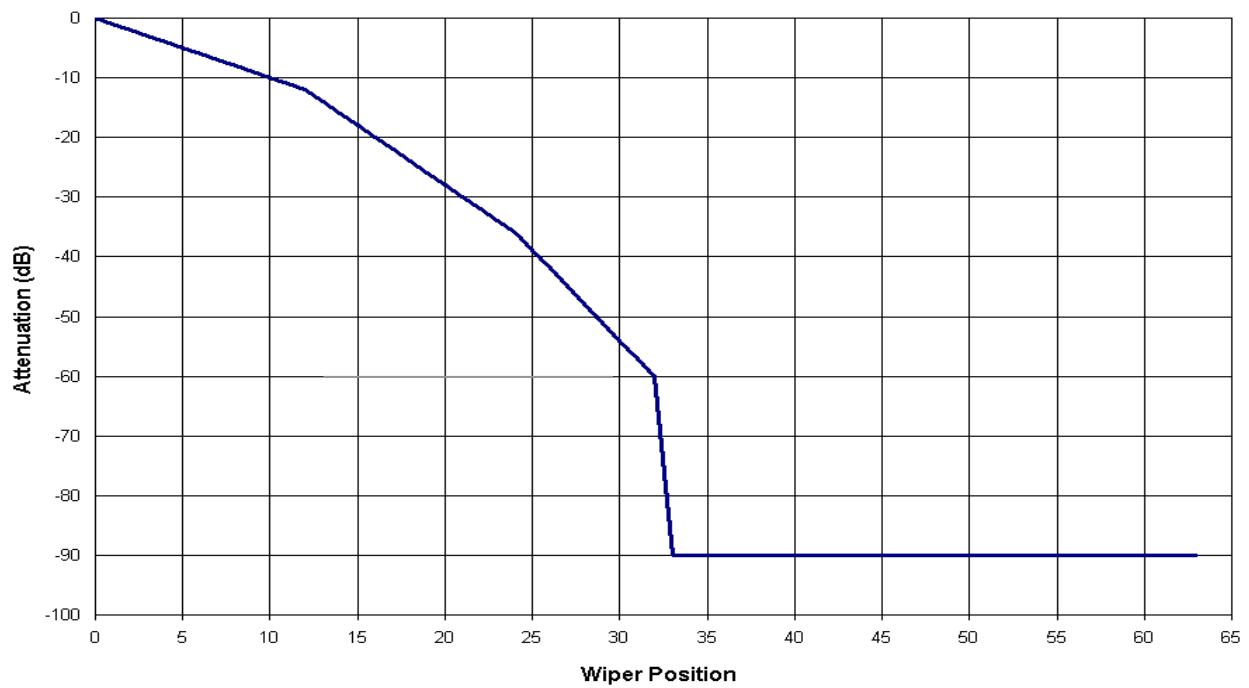
**TYPICAL OPERATING CHARACTERISTICS**

( $V_{CC} = 12V$ ,  $V_B = -12V$ ,  $V_{DD} = 5V$ ,  $T = +25^{\circ}C$ , unless otherwise specified.)

**Current vs. SCL Clock Rate****Wiper Resistance vs. Voltage**

**TYPICAL OPERATING CHARACTERISTICS (cont.)**

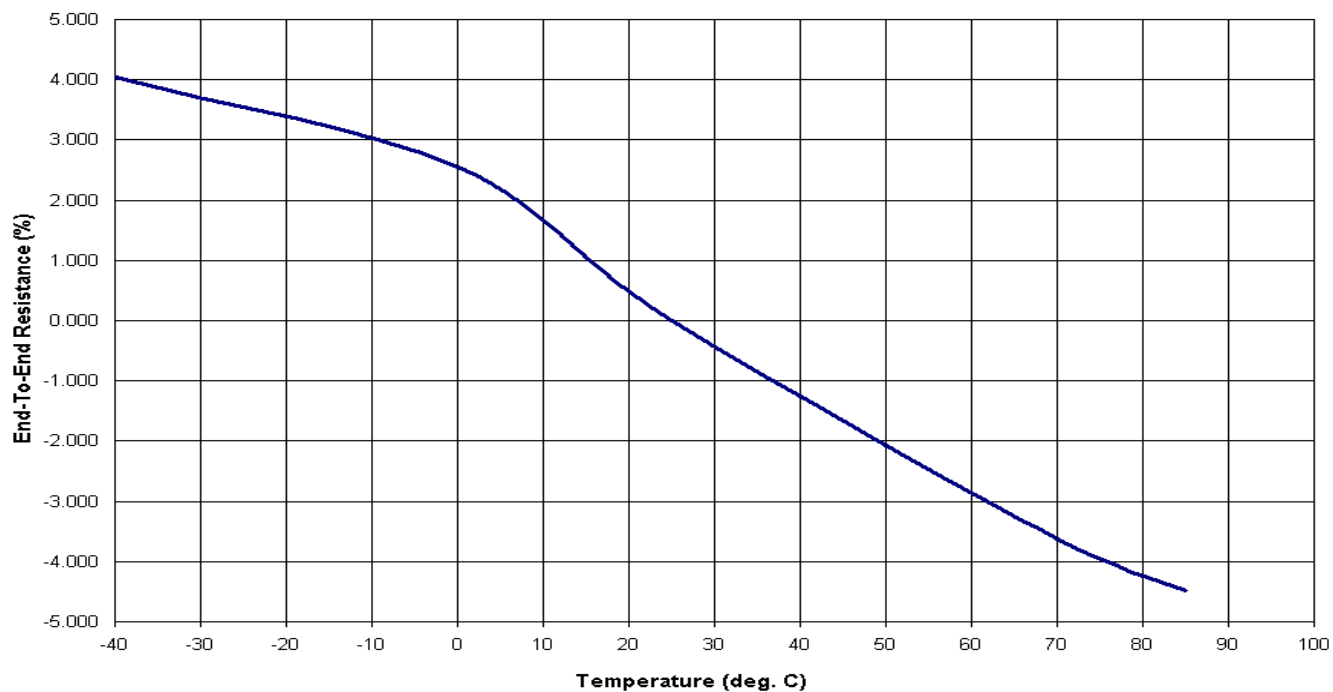
( $V_{CC} = 12V$ ,  $V_B = -12V$ ,  $V_{DD} = 5V$ ,  $T = +25^{\circ}C$ , unless otherwise specified.)

**Crosstalk vs Frequency****Attenuation vs. Wiper Position**



**TYPICAL OPERATING CHARACTERISTICS (cont.)**

( $V_{CC} = 12V$ ,  $V_B = -12V$ ,  $V_{DD} = 5V$ ,  $T = +25^{\circ}C$ , unless otherwise specified.)

**End-To-End Resistance vs. Temperature****THD+N vs Frequency**