1:4 Low Additive Jitter LVDS Buffer With Divider

Check for Samples: CDCLVD1213

FEATURES

- **1:4 Differential Buffer**
- **Low Additive Jitter: <300 fs RMS in 10-kHz to 20-MHz**
- **Low Output Skew of 20 ps (Max)**
- **Selectable Divider Ratio 1, /2, /4**
- **Universal Input Accepts LVDS, LVPECL, and CML**
- **4 LVDS Outputs, ANSI EAI/TIA-644A Standard Compatible**
- **Clock Frequency up to 800 MHz**
- **2.375 V–2.625 V Device Power Supply**
- **Industrial Temperature Range: –40°C to 85°C**
- **Packaged in 3 mm × 3 mm 16-Pin QFN (RGT)**
- **ESD Protection Exceeds 3 kV HBM, 1 kV CDM**

APPLICATIONS

- **Telecommunications/Networking**
- **Medical Imaging**
- **Test and Measurement Equipment**
- **Wireless Communications**
- **General Purpose Clocking**

DESCRIPTION

The CDCLVD1213 clock buffer distributes an input clock to 4 pairs of differential LVDS clock outputs with low additive jitter for clock distribution. The input can either be LVDS, LVPECL, or CML.

The CDCLVD1213 contains a high performance divider for one output (QD) which can divide the input clock signal by a factor of 1, 2, or 4.

The CDCLVD1213 is specifically designed for driving 50 Ω transmission lines. The part supports a fail safe function. The device incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in 2.5 V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD1213 is packaged in small 16-pin, 3-mm × 3-mm QFN package.

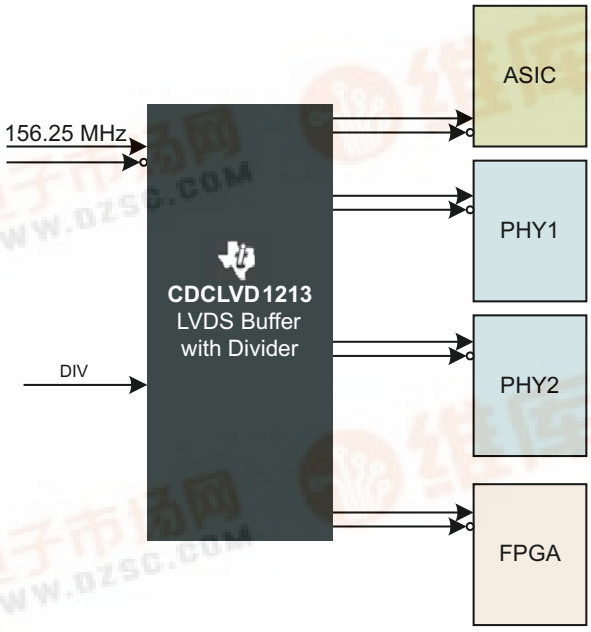


Figure 1. Application Example

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

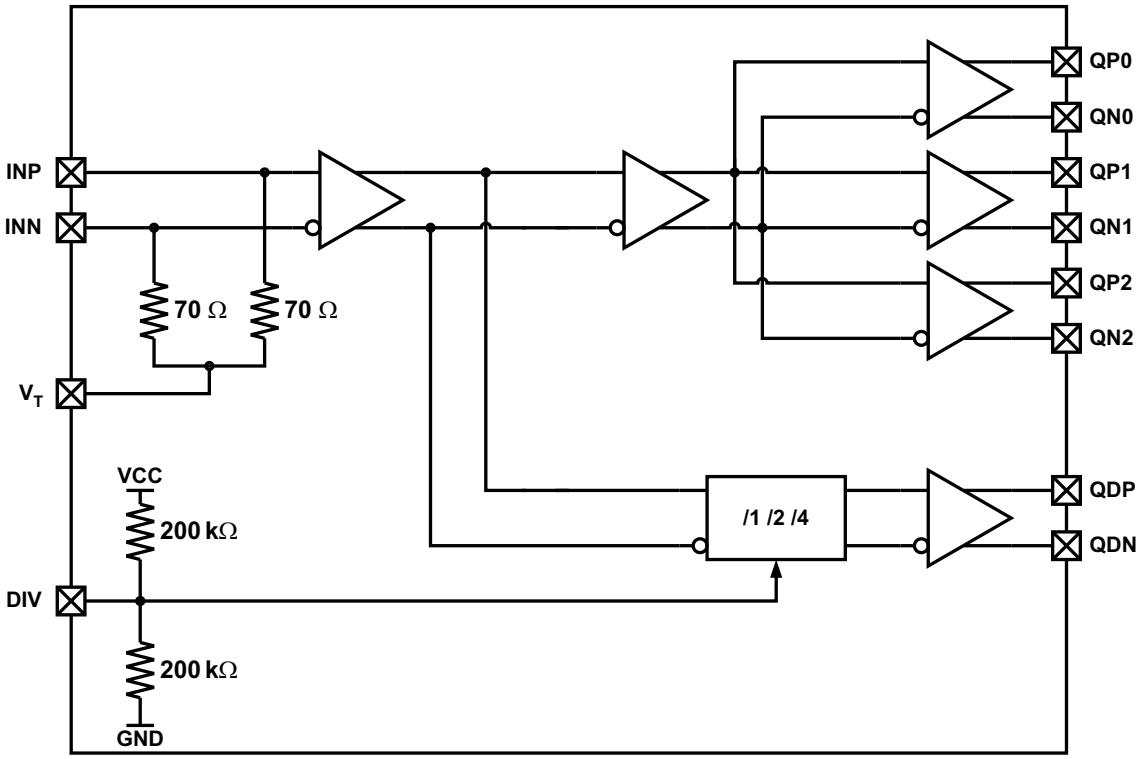
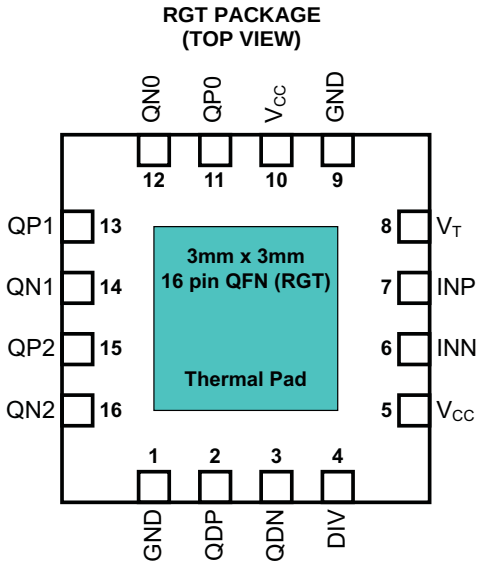


Figure 2. CDCLVD1213 Block Diagram



PIN DESCRIPTIONS

CDCLVD1213 Pin Descriptions

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{CC}	5, 10	Power	2.5 V supply for the device
GND	1, 9	Ground	Device ground
INP, INN	7, 6	Input	Differential input pair
V_T	8	Input	Input for threshold voltage
QDP, QDN	2,3	Output	Differential divided LVDS output pair
QP0, QN0	11,12	Output	Differential LVDS output pair no. 0
QP1, QN1	13,14	Output	Differential LVDS output pair no. 1
QP2, QN2	15,16	Output	Differential LVDS output pair no. 2
DIV	4	Input with an internal 200kΩ pull-up and pull-down	Divider selection – selects divider ratio for QD output; (See Table 1)
Thermal Pad			See thermal management recommendations

Table 1. Divider Selection Table

DIV	DIVIDER RATIO
0	/1
open	/2
1	/4

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).(1)

	VALUE	UNIT
Supply voltage range, V_{CC}	–0.3 to 2.8	V
Input voltage range, V_I	–0.2 to V_{CC} +0.2	V
Output voltage range, V_O	–0.2 to V_{CC}+0.2	V
Driver short circuit current , I_{OSD}	See Note(2)	
Electrostatic discharge (Human Body Model 1.5 kΩ, 100 pF)	>3000	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The output can handle the permanent short.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

	MIN	TYP	MAX	UNIT
Device supply voltage, V_{CC}	2.375	2.5	2.625	V
Ambient temperature, T_A	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		CDCLVD1213 RGT(16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	51.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	85.4	
θ_{JB}	Junction-to-board thermal resistance	20.1	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	19.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIVIDER CONTROL INPUT (DIV) CHARACTERISTICS						
Vd_{I3}	3-State	Open		$0.5\times V_{CC}$		V
Vd_{IH}	Input high voltage		$0.7\times V_{CC}$			V
Vd_{IL}	Input low voltage				$0.2\times V_{CC}$	V
Id_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			30	µA
Id_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–30	µA
$R_{pull(DIV)}$	Input pull-up/ pull-down resistor			200		kΩ
DIFFERENTIAL INPUTS (INP, INN) CHARACTERISTICS						
f_{IN}	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	V_{ICM} = 1.25 V	0.3		1.6	V_{PP}
V_{ICM}	Input common-mode voltage range		1		V_{CC} – 0.3	V
R_{IN}	Input termination	INP, INN to V_T, DC		70		Ω
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20% to 80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS OUTPUT CHARACTERISTICS						
$\|V_{OD}\|$	Differential output voltage magnitude	$V_{IN, DIFF, PP}$ = 0.3V, R_L = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude		–15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP}$ = 0.6V, R_L = 100 Ω	–15		15	mV
I_{OS}	Short-circuit output current	V_{OD} = 0 V			±24	mA
V_{OS}	Output ac common mode	$V_{IN, DIFF, PP}$ = 0.6V, R_L = 100 Ω		25	70	mV_{PP}
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.3 V		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK, O}$	Output skew (1)				20	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75V/ns 10 kHz – 20 MHz			0.3	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%,100 Ω, 5 pF	50		300	ps
I_{CCSTAT}	Static supply current	Outputs unterminated, f = 0 Hz		17	28	mA
I_{CC100}	Supply current	All outputs, R_L = 100 Ω, f = 100 MHz		40	58	mA
I_{CC800}	Supply current	All outputs, R_L = 100 Ω, f = 800 MHz		60	85	mA

(1) Undivided outputs only.

Typical Additive Phase Noise Characteristics for 100 MHz Clock

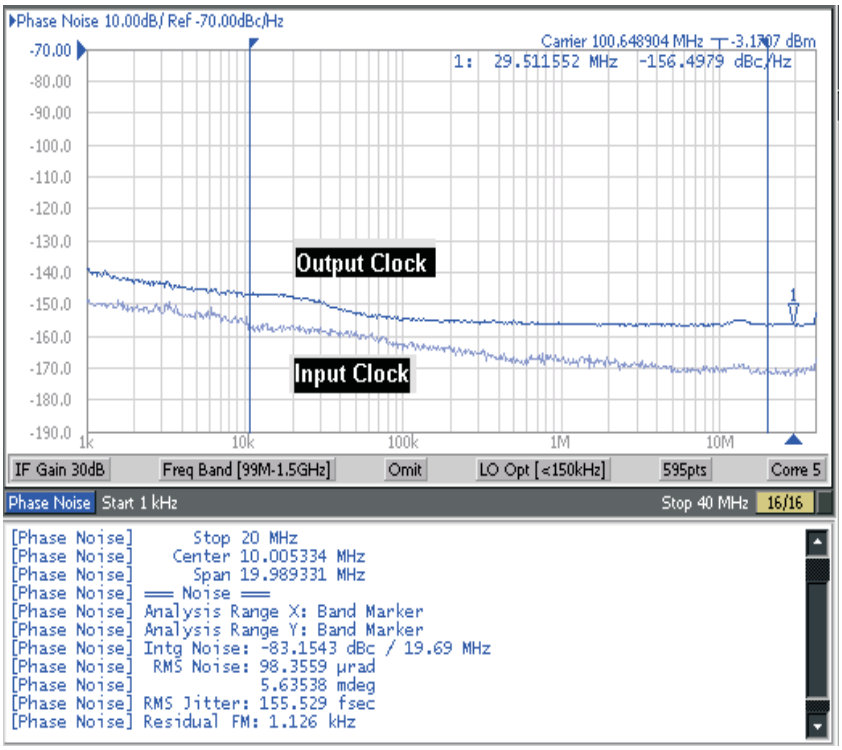
PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-138		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

TYPICAL CHARACTERISTICS

INPUT CLOCK AND OUTPUT CLOCK PHASE NOISES
vs
FREQUENCY FROM THE CARRIER (T_A = 25°C and V_{CC} = 2.5V)



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

Figure 3. 100 MHz Input and Output Phase Noise Plot

Differential Output Voltage
vs
Frequency

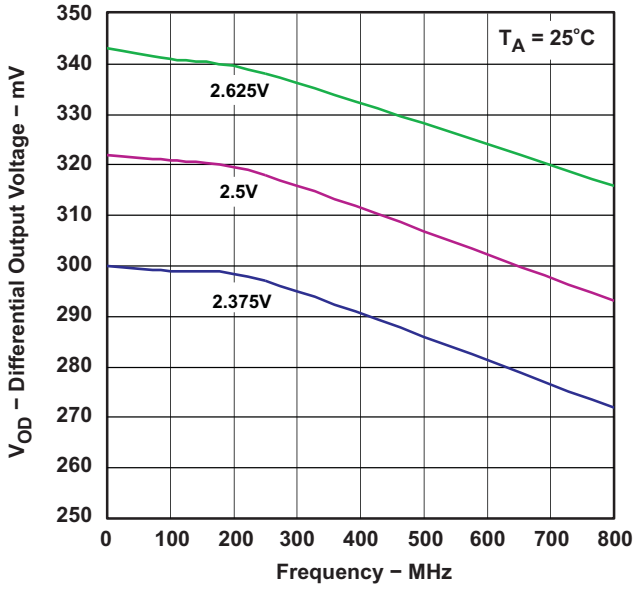


Figure 4.

TEST CONFIGURATIONS

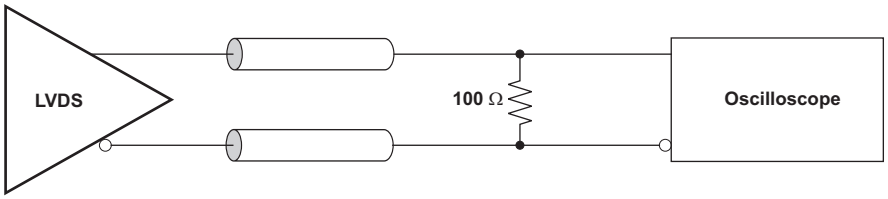


Figure 5. LVDS Output DC Configuration During Device Test

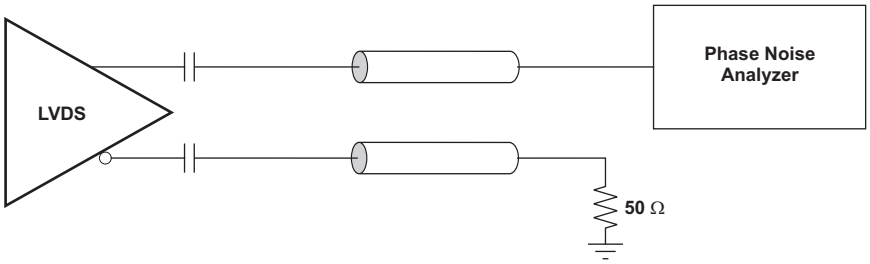


Figure 6. LVDS Output AC Configuration During Device Test

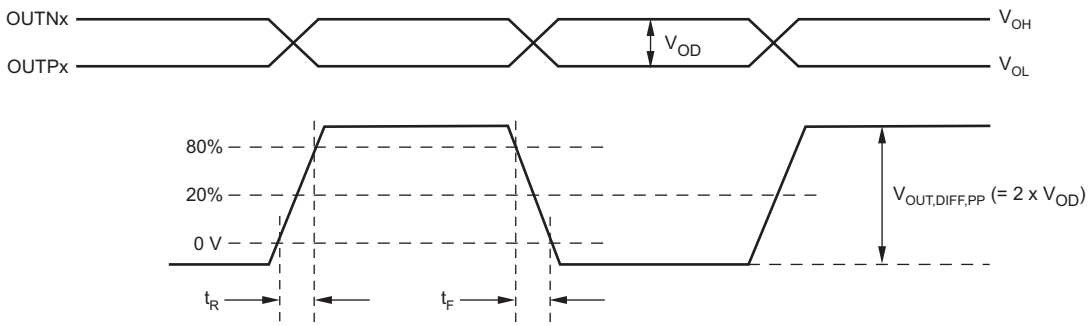
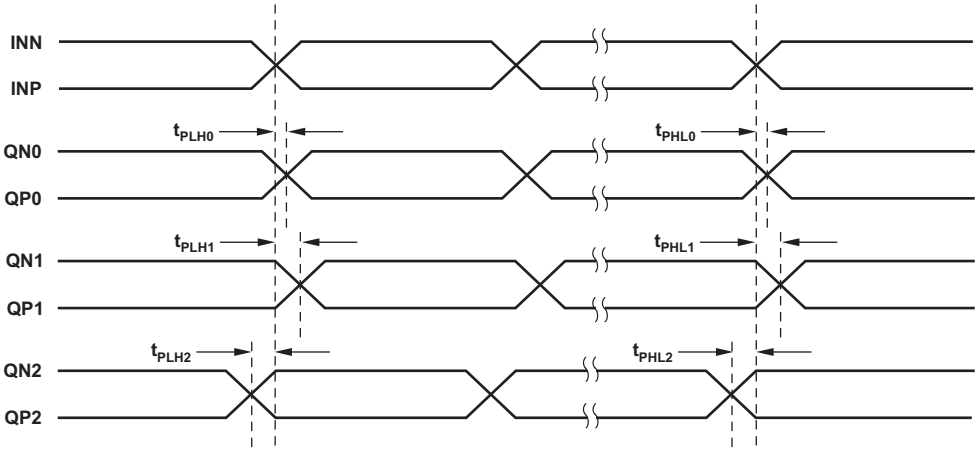


Figure 7. Output Voltage and Rise/Fall Time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2).

(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2).

Figure 8. Output and Part-to-Part Skew

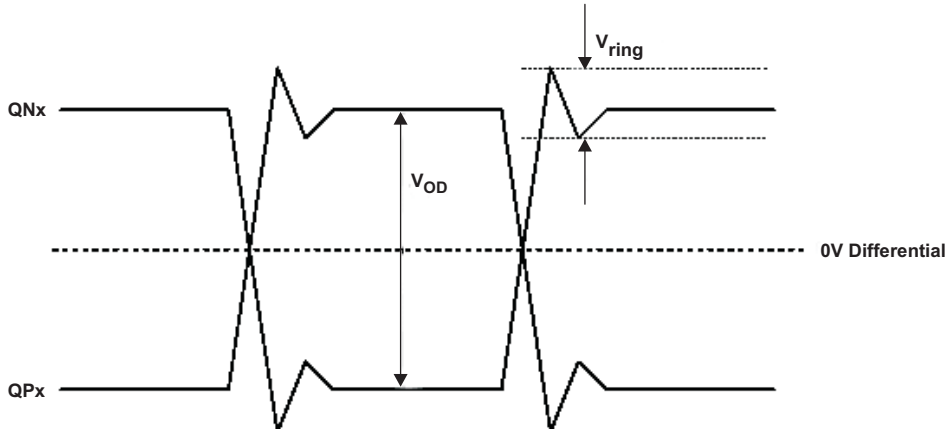


Figure 9. Output Overshoot and Undershoot

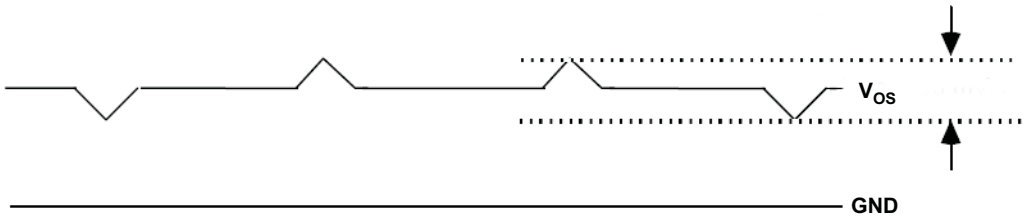


Figure 10. Output AC Common Mode

APPLICATION INFORMATION

THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to the package. Figure 11 shows a recommended land and via pattern.

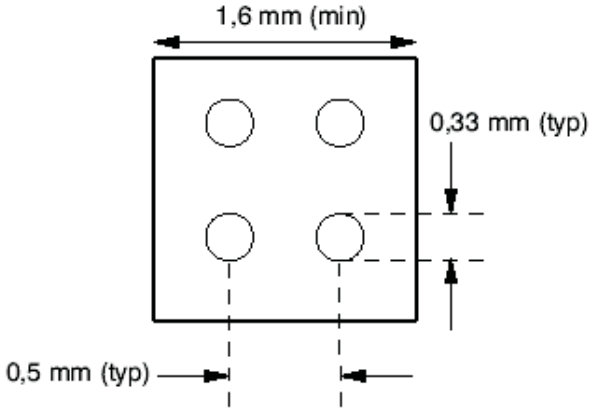


Figure 11. Recommended PCB Layout

POWER-SUPPLY FILTERING

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 µF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

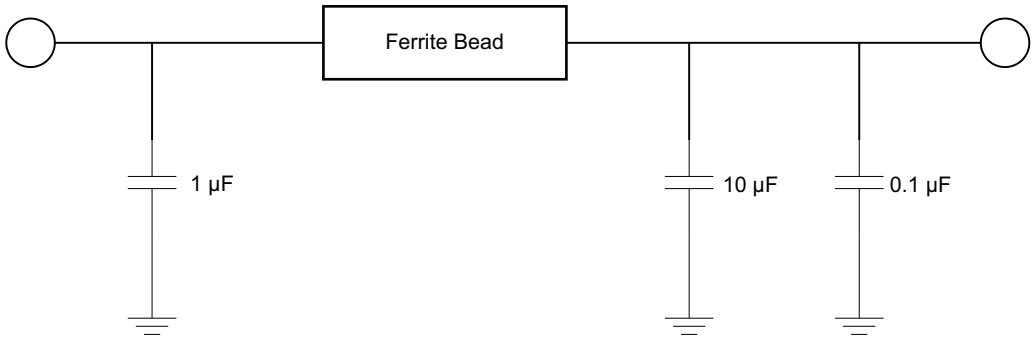


Figure 12. Power-Supply Decoupling

LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resister close to the receiver. If the receiver is internally biased, ac-coupling should be used. If the LVDS receiver has internal 100 Ω termination, external termination is not required.

Unused outputs can be left open without connecting any traces to the output pins.

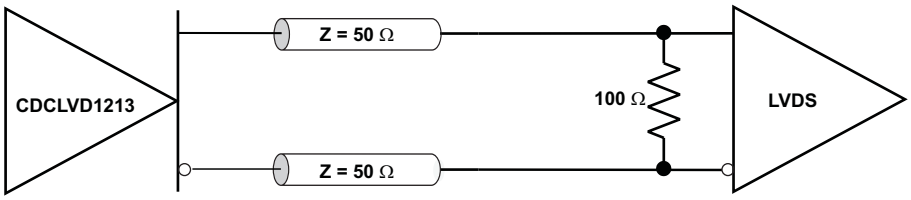


Figure 13. Output DC Termination

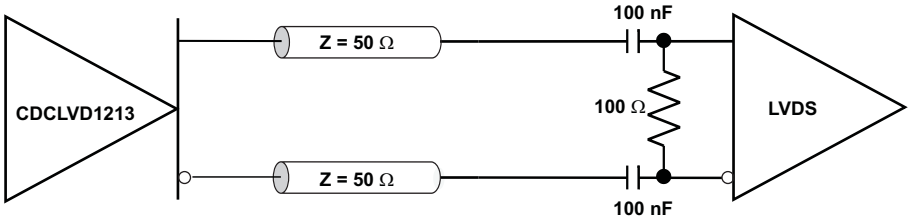


Figure 14. Output AC Termination (With Receiver Internally Biased)

INPUT TERMINATION

The CDCLVD1213 input has internal 140 Ω terminations, and an external 350 Ω resistor is required for a 50 Ω transmission line. It can be interfaced with LVDS, LVPECL, or CML drivers. LVDS input can be connected directly, dc or ac coupled. With ac coupling, external bias (V_{CC}/2) must be provided to V_T pin.

Figure 16 illustrates how to connect CML input to CDCLVD1213 input buffer. The input does not have internal biasing, so external biasing (V_{CC}/2 to V_T) is required for ac coupling. If the CML output swing is >1.6 V_{PP}, then signal swing needs to be reduced to meet $V_{IN, DIF, PP} \leq 1.6\ V_{PP}$.

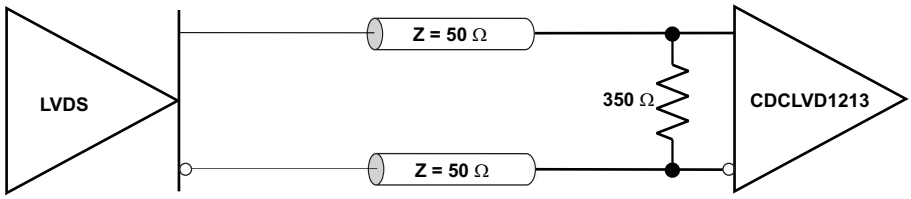


Figure 15. LVDS Clock Driver Connected to CDCLVD1213 Input

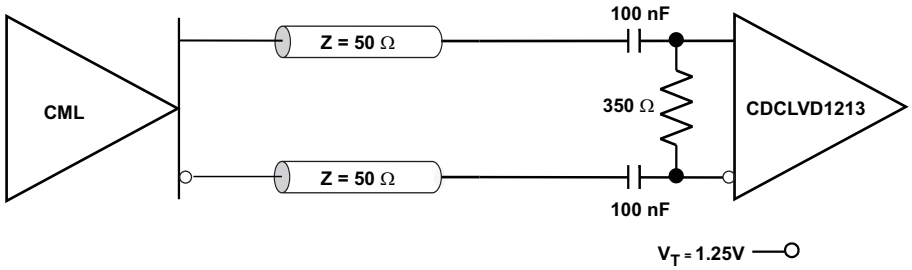


Figure 16. CML Clock Driver Connected to CDCLVD1213 Input

Figure 17 shows how to connect LVPECL input to the CDCLVD1213 input buffer. The input does not have internal biasing, so external biasing (V_{CC}/2 to V_T) is required for ac coupling. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 Vpp.

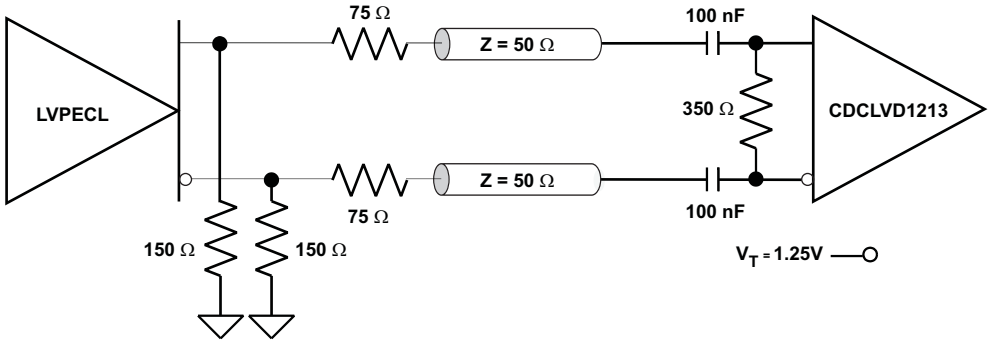


Figure 17. LVPECL Clock Driver Connected to CDCLVD1213 Input

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
CDCLVD1213RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
CDCLVD1213RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

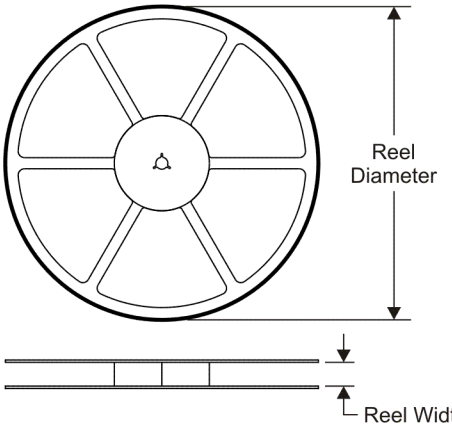
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

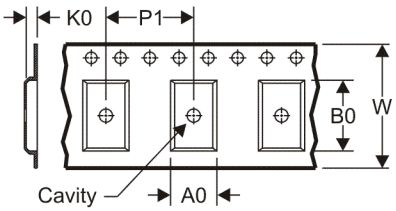
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

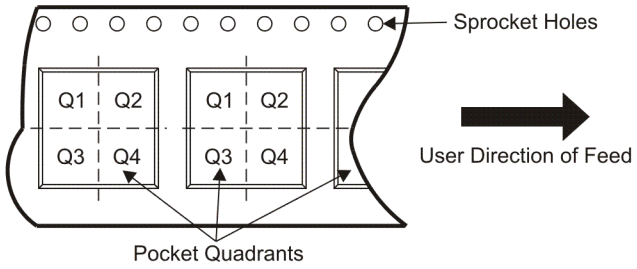


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

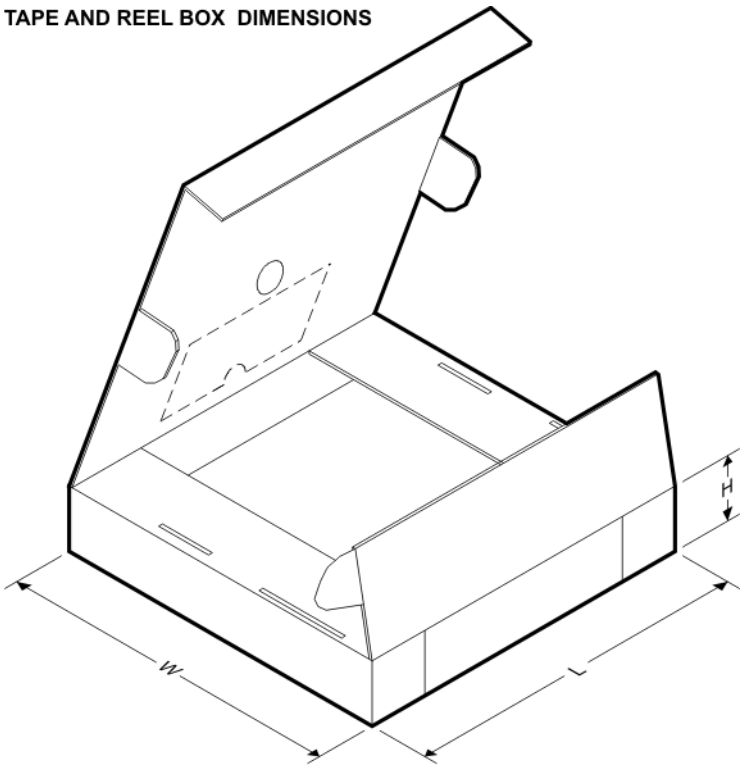
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD1213RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
CDCLVD1213RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

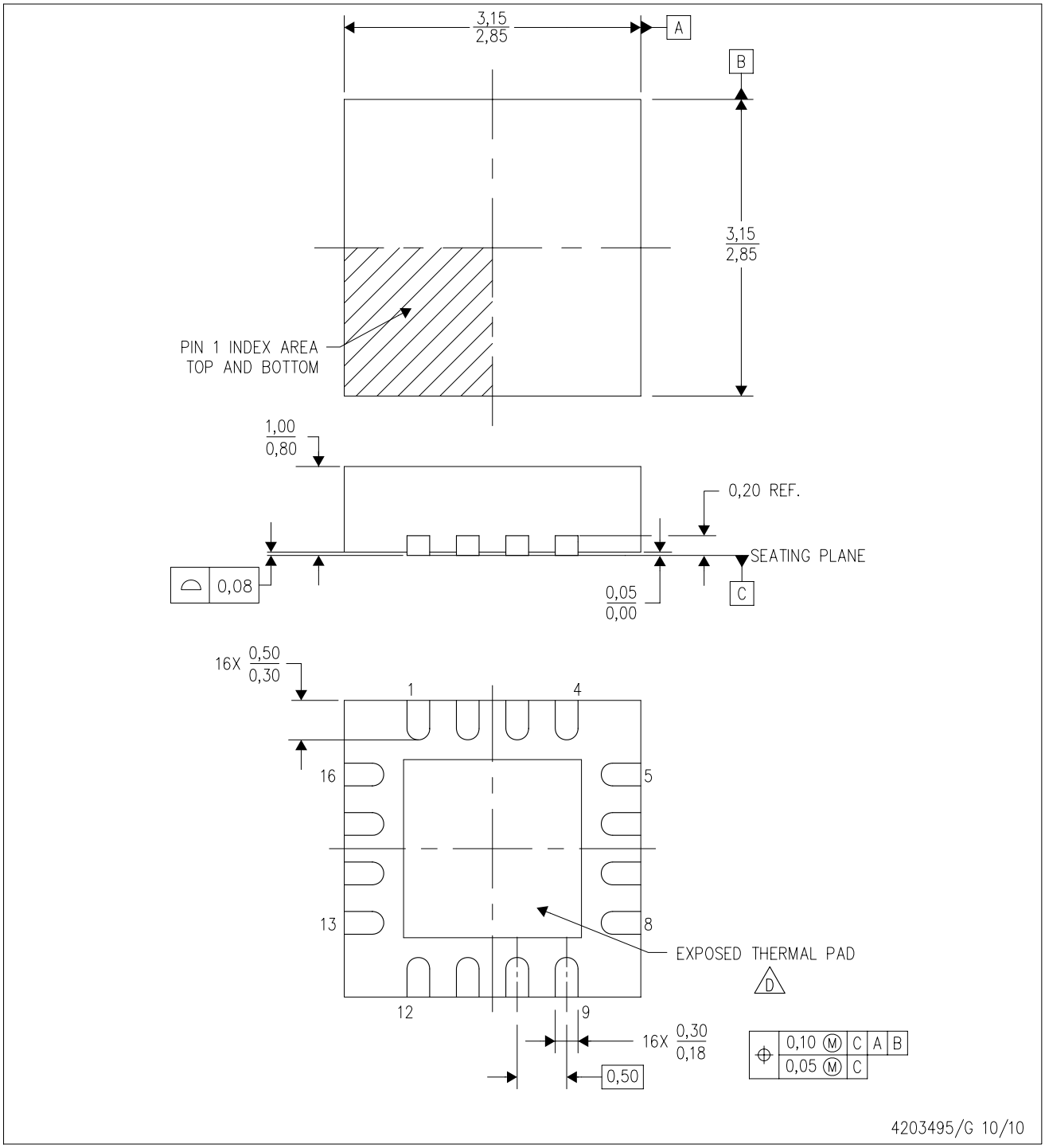
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD1213RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
CDCLVD1213RGTT	QFN	RGT	16	250	340.5	333.0	20.6

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

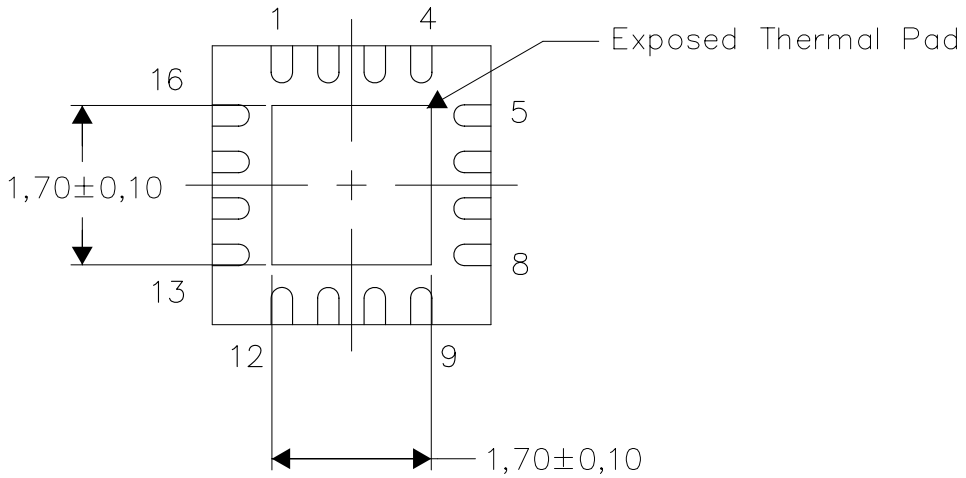
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



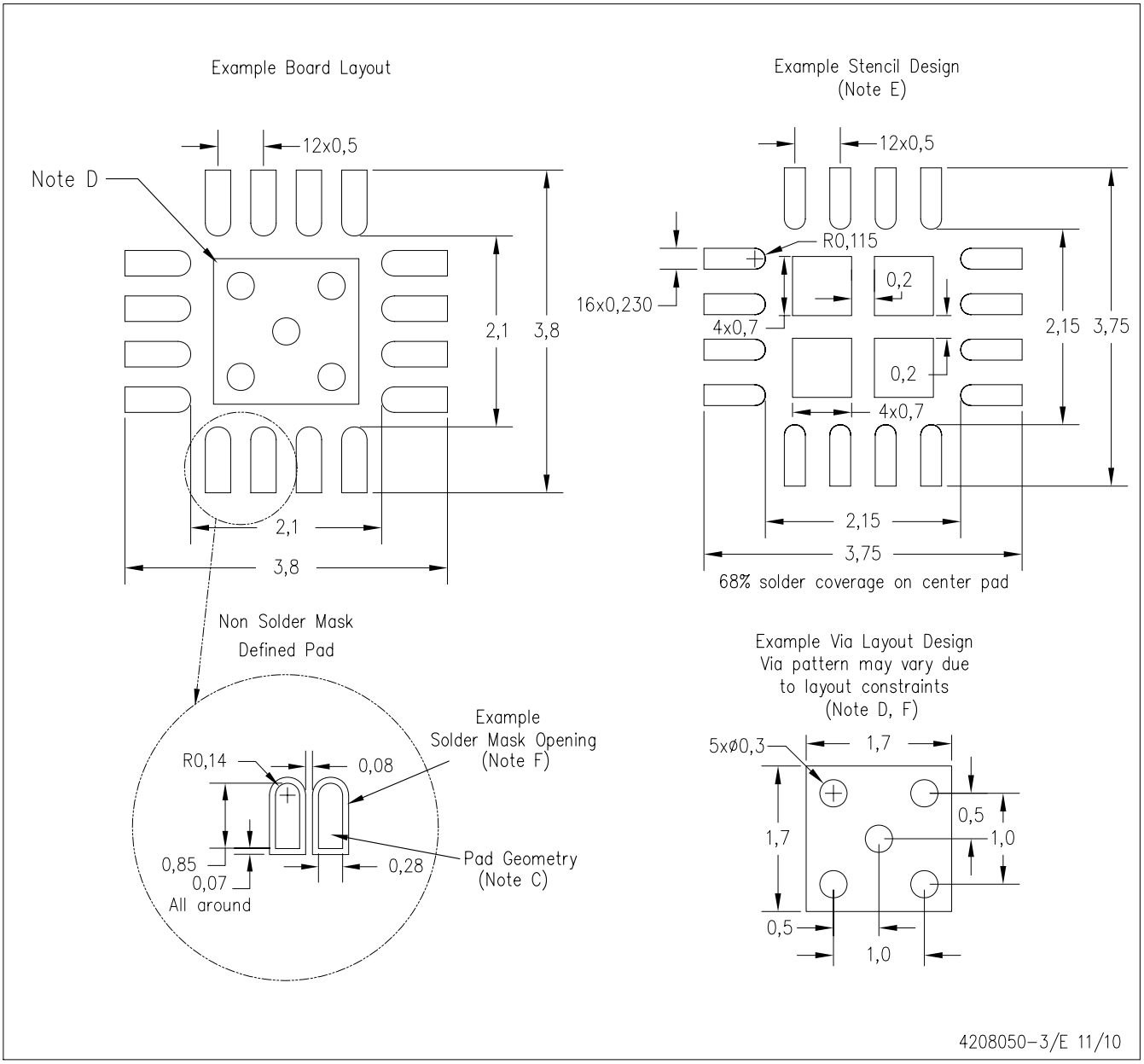
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/0 11/10

NOTE: A. All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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