June 1992
Edition 3.3A

FUJITSU

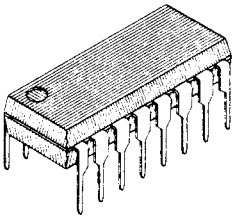
DATA SHEET

MB88301A

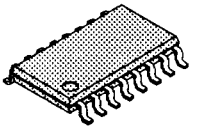
NMOS 1-Channel, 13-Bit and 3-Channel, 6-Bit D/A Converter

The Fujitsu MB88301A is a pulse width modulation (PWM) type digital-to-analog converter (DAC). It is designed for interface with Fujitsu's MB8840, MB8850, and MB88500 series of 4-bit single-chip microcomputers and other 4-bit and 8-bit microprocessors.

The MB88301A has four conversion outputs, one 13-bit resolution output, and three 6-bit resolution outputs. All outputs generate positive pulses of varying pulse widths. The pulse widths vary in proportion to the digital data programmed by the processor in the internal data register. With the connection of external filter circuits to the outputs, the MB88301A provides an excellent, easy-to-configure DAC.



Plastic DIP
(DIP-16P-M02)

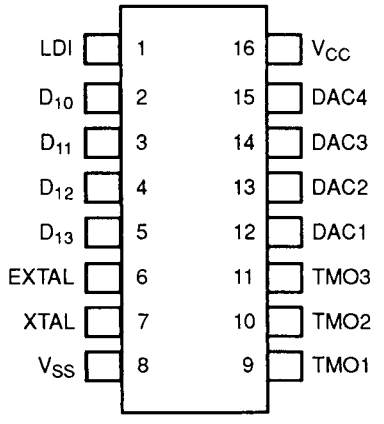


Plastic SOP
(FPT-16P-M02)

- Pulse width modulation D/A converter
- 4-bit parallel address/data loading
- Four on-chip pulse width modulators:
  – 1-channel x 13-bit resolution
  – 3-channel x 6-bit resolution
- On-chip 4 MHz clock generator with an external crystal or ceramic resonator
- Clock cycle time/clock frequency:
  – 0.25 µs/4 MHz for 13-bit resolution
  – 0.50 µs/2 MHz for 6-bit resolution
- Three synchronization clock outputs:
  – 2 MHz clock output (4 MHz divided by 2)
  – 15.625 kHz clock output (4 MHz divided by 2^8)
  – 488 Hz clock output (4 MHz divided by 2^{13})
- Single buffered conversion outputs
- High-voltage open-drain conversion outputs
- Wide operating temperature range: –30°C to +70°C
- Power supply: Single +5 V
- Inputs/outputs: TTL compatible
- Package and ordering information:
  – 16-pin plastic DIP, order as MB88301AP
  – 16-pin plastic SOP, order as M88301APF

Pin Assignment

TOP VIEW



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — LOGIC SYMBOL

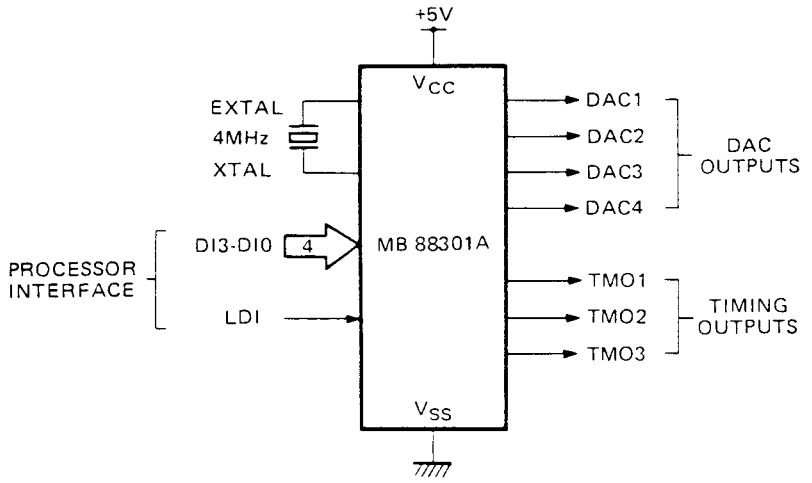
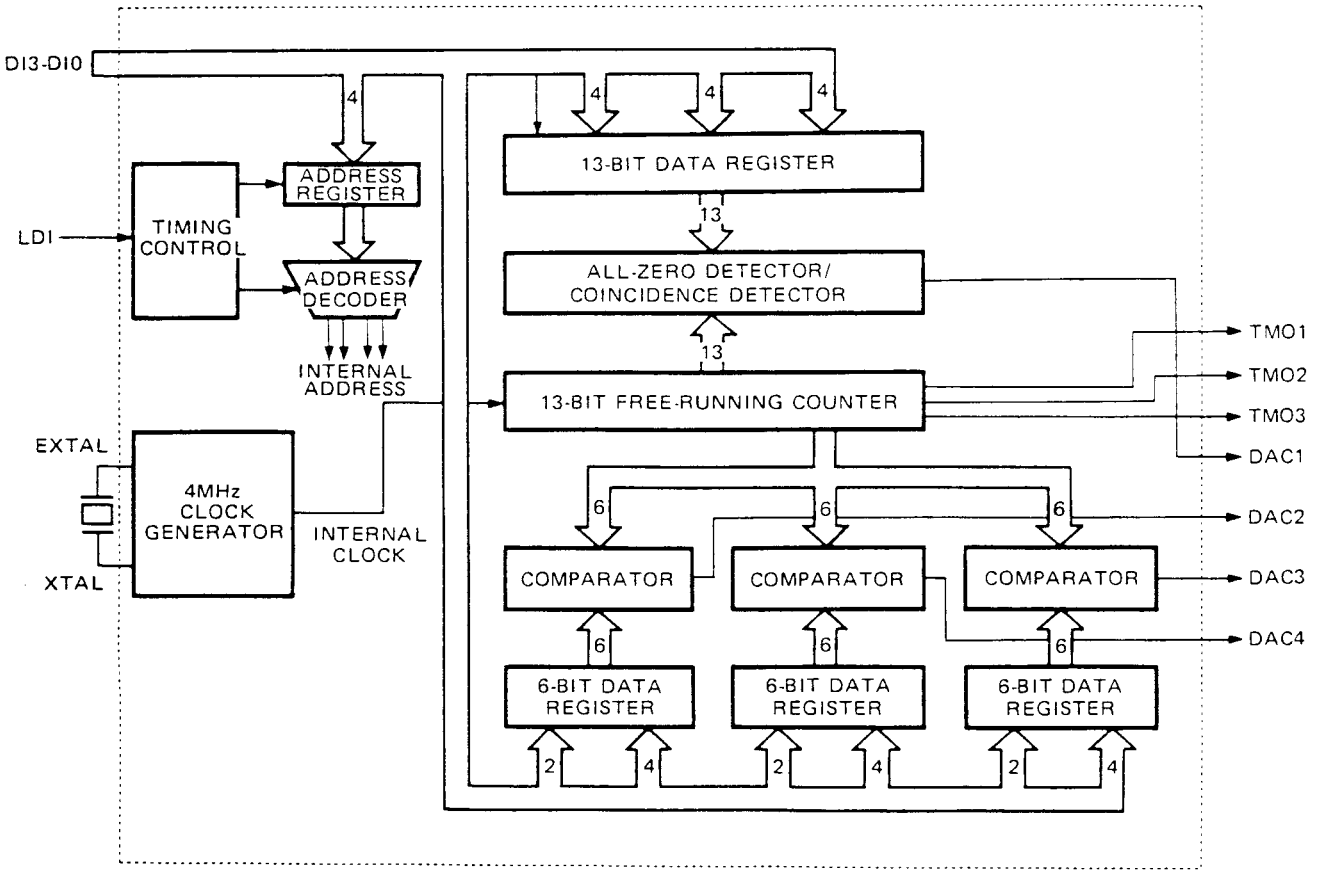


Fig. 2 — BLOCK DIAGRAM



PIN DESCRIPTION

The MB88301A has two interfaces. One is the processor interface, D3-D0 and LDI, which is used by the processor to load the MB88301A device with address and data. The second is the DAC/TIMING interface, DAC4-DAC1 and TM03-TM01, which is used to connect with the user-designed external low-pass filter.

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Function
V_{CC}	16	–	+5V power supply pin.
V_{SS}	8	–	Ground pin.
XTAL	7	–	External 4MHz crystal or ceramic resonator pins for the on-chip clock generator.
EXTAL	6	–	
DI3-DI0	5 to 2	I	4-bit parallel address/data input: The address/data format is that DI3 is the most significant bit (MSB) and that DI0 is the least significant bit (LSB). These inputs are TTL compatible. MSB LSB DI3 | DI2 | DI1 | DI0
LDI	1	I	Write strobe input for a 4-bit address/data: At the leading edge of LDI, a 4-bit address on the ID3 to ID0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs are written into the internal data register designated by the address latched at the leading edge. This input is TTL compatible.
DAC1-DAC4	12 to 15	O	Pulse width modulator outputs (DAC outputs): DAC1: 13-bit resolution (one channel) DAC2-DAC4: 6-bit resolution (three channels) All four outputs are high-voltage open drain.
TMO1-TMO3	9 to 11	O	Synchronization clock outputs (Timing outputs): TMO1: 2MHz (4MHz divided by 2) TMO2: 15.625kHz (4MHz divided by 2^8) TMO3: 488Hz (4MHz divided by 2^{13}) All three clocks have a duty ratio of approximately 50%, and are TTL compatible.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MB88301A is a pulse width modulation (PWM) type digital-to-analog converter (DAC). It converts digital data programmed by the processor in the internal data register (13-bit or 6-bit write-only register) into positive pulses. The width of these pulses is proportional to the value of the programmed data, and the cycle time of the pulses is defined by the resolution value (6 or 13 bits). The MB88301A has four conversion outputs: channel 1 is a 13-bit resolution output DAC1, and channels 2 thru 4 are 6-bit resolution outputs DAC2 to DAC4. The converted waveform appears at each DAC output. A user-designed external low-pass filter connected to the DAC output eliminates AC components from the output waveform and converts the wave form into a DC voltage proportional to the pulse width.

DIGITAL DATA INPUT

Fig. 3 shows the input timing of digital data to be converted: Digital data to define the width of the positive pulse is written into the 13-bit and 6-bit internal data registers through the DI3 to DI0 4-bit address/data inputs using the write strobe input LDI. At the leading edge of LDI, a 4-bit address on the DI3 to DI0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs is loaded into the internal data register designated by the address register.

Fig. 4 shows the address/data format: DI3 is the most significant bit (MSB) and DI0 is the least significant bit (LSB).

Fig. 5 shows the internal data register address map: The whole space size is 10 words. Addresses #0 to #3, addresses #4 and #5, addresses #6 and #7, and addresses #8 and #9 are assigned to DAC1, DAC2, DAC3 and DAC4, respectively. Fig. 6 shows the internal data register format: To the DAC1 data register, three 4-bit and one 1-bit digital data must be written. To the DAC2 to DAC4 data registers, one 4-bit and one 2-bit digital data must be written.

Fig. 3 — ADDRESS/DATA INPUT TIMING

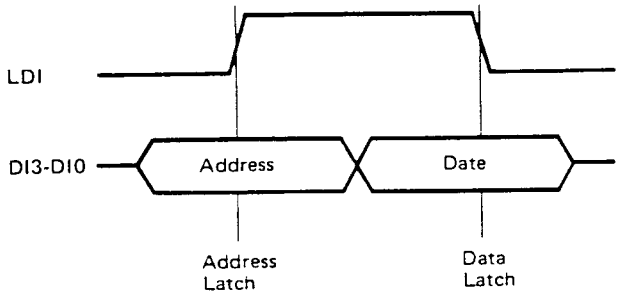


Fig. 4 — ADDRESS/DATA FORMAT

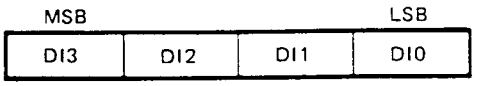


Fig. 5 — INTERNAL DATA REGISTER ADDRESS MAP

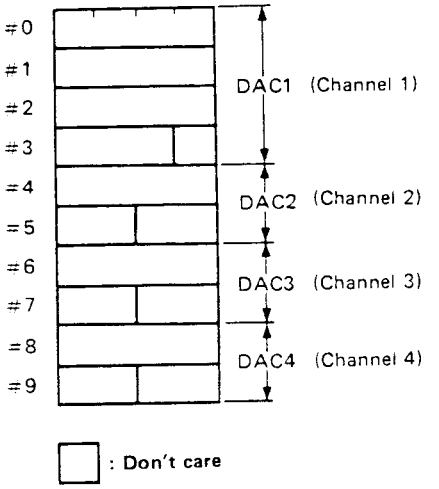
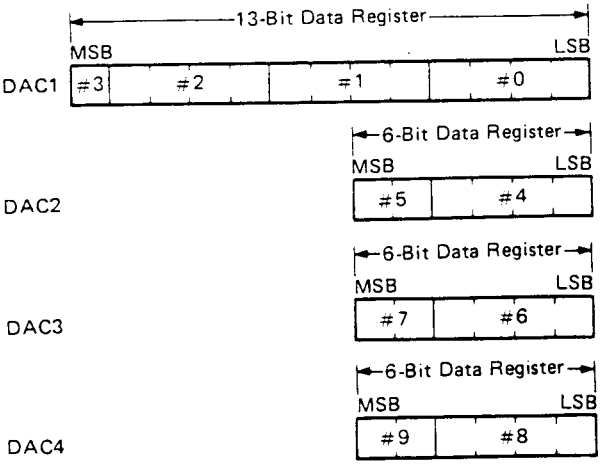


Fig. 6 — INTERNAL DATA REGISTER FORMAT



FUNCTIONAL DESCRIPTION (Continued)

PULSE WIDTH MODULATION/DAC OUTPUT WAVEFORM

13-bit Resolution D/A Converter: DAC1

Fig. 7 shows the configuration of the 13-bit resolution pulse width modulator. The on-chip clock generator provides a 4MHz clock for the 13-bit free-running counter. When all bits of the counter are zero, the all-zero detector sets the output R-R-S flip-flop. The coincidence detector compares the counter with the data register. When they match, the coincidence detector resets the output flip-flop. The waveform appearing at the DAC1 output depends on the data register value, shown in Fig. 8.

Fig. 7 — 13-BIT PULSE WIDTH MODULATOR CONFIGURATION

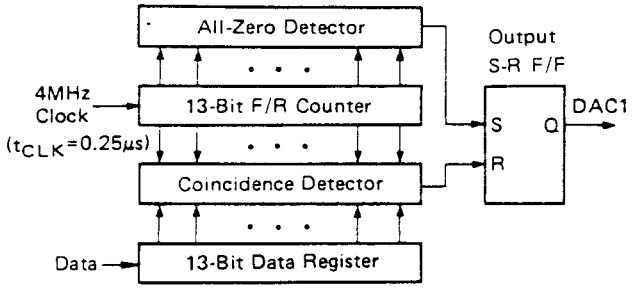
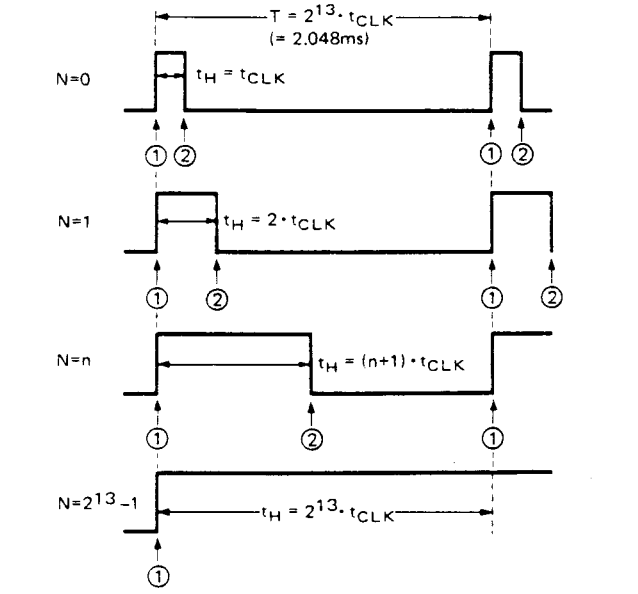


Fig. 8 — DAC1 OUTPUT WAVEFORM



NOTES:
- N : DATA REGISTER VALUE ($0 \leq N \leq 2^{13}-1$)
- T : PULSE CYCLE TIME ($T = 2^{13} \cdot t_{CLK} = 2.048ms$)
- t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
- t_{CLK} : COUNTER CLOCK CYCLE TIME ($t_{CLK} = 1/4MHz = 0.25\mu s$)
- ① : COUNTER IS ZERO.
- ② : COUNTER MATCHES DATA REGISTER.

6-Bit Resolution D/A Converters: DAC2 to DAC4

Fig. 9 shows the configuration of the 6-bit resolution pulse width modulator. The 2MHz clock that is the output of Bit 1 (of the 13-bit free-running counter) drives the 6-bit free-running counter. This 6-bit counter is also part of the 13-bit counter (Bits 2 to 7). The comparator compares the counter with the data register every cycle. When the counter value is equal to or less than the data register value, the comparator outputs a high level at the DAC output. When the counter value exceeds the data register value, the comparator outputs a low level at the DAC output. This produces the waveforms at the DAC2, DAC3, and DAC4 outputs as shown in Fig. 10.

Fig. 9 — 6-BIT PULSE WIDTH MODULATOR CONFIGURATION

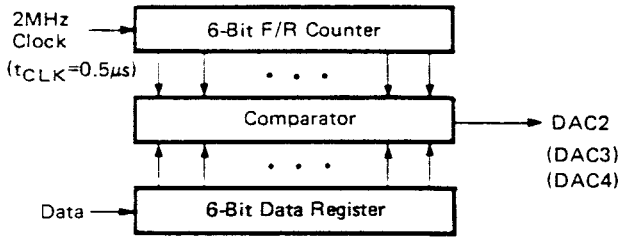
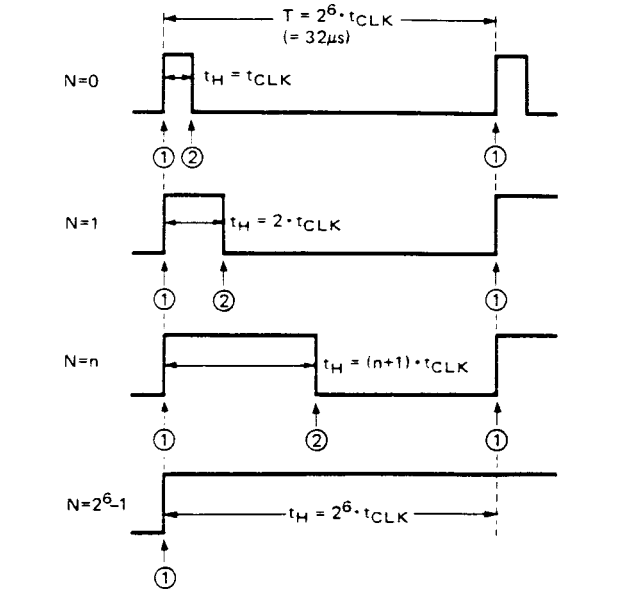


Fig. 10 — DAC2/DAC3/DAC4 OUTPUT WAVEFORM



NOTES:
- N : DATA REGISTER VALUE ($0 \leq N \leq 2^6-1$)
- T : PULSE CYCLE TIME ($T = 2^6 \cdot t_{CLK} = 32\mu s$)
- t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
- t_{CLK} : COUNTER CLOCK CYCLE TIME ($t_{CLK} = 1/2MHz = 0.5\mu s$)
- ① : COUNTER IS ZERO. (OVERFLOW)
- ② : COUNTER EXCEEDS DATA REGISTER.

FUNCTIONAL DESCRIPTION (Continued)

EXTERNAL FILTER CONFIGURATION

The on-chip pulse width modulator generates positive pulse waveforms similar to the one shown in Fig. 12 at the DAC outputs (DAC1 to DAC4). The pulse width (t_H) is proportional to the digital data programmed into the data register. The cycle time (T) is determined by the resolution value (6 or 13 bits).

User-designed low-pass filters are required at the DAC outputs to eliminate AC components from the output waveform and to convert the waveform to a DC voltage. Fig. 11 shows an example of a simple output configuration in which an RC integrator is used as the low-pass filter. With this circuit, the DAC waveform shown in Fig. 12 is converted to the V_{OUT} output waveform shown in Fig 13. Ripple and response time (t_R) depend on the time constant of the RC filter. A longer time constant reduces ripple but increases response time. A time constant that best meets the tradeoff between desired accuracy and response time should be chosen. Since the DAC outputs are high voltage open drain, they can be externally pulled up to a power supply higher than 5V. To prevent the output voltage from attenuating through the external low–pass filters.

Note: The low–pass filter shown in Fig. 11 is an example. In actual practice (depending on the user's system design), additional amplifiers, multi–stage filters, and other circuits will be needed for the external low–pass filter.

NOTICE

To change the DC output voltage of the external low-pass filter, the data register value must be updated to vary the positive pulse width (duty ratio) of the DAC output. All the bits on the data register cannot be changed at the same time. Bits must be updated a nibble at a time by the 4-bit parallel data loading. Because of the nibble-by-nibble updating and the DAC's single buffering, the data register value may become transient during update. During this pulse cycle, and depending on the transient value, an undesirable duty ratio disturbance may occur at the DAC output which affects the filter output. Therefore, it is necessary to design the output filter to eliminate disturbances in the DAC output waveform at the filter output.

This notice applies to both the 13–bit and 6–bit resolution converters. To avoid distrubances in the 13–bit resolution converter use its software, and to eliminate the disturbances, control the update timing of its data register value by monitoring the DAC1 output and the TMO3 output waveforms. When the DAC1 output is used in a steady state where the DAC1 data register bits are all set (i.e., data is "1FFF"), the DAC1 output remains high. Two cautions must be observed to avoid undefined DAC1 output during the output cycle time (less than one cycle time) when data is updated.

1. Do not use the data of "1FFF".
2. Do not change the DAC1 data register value (i.e., "1FFF") just before the counter becomes full (i.e., all bits are set) because an undesired pulse, due to the data change, may appear at the DAC1 output. This undesired pulse must be eliminated with the external filter.

Fig. 11 – OUTPUT CIRCUIT CONFIGURATION (EXAMPLE)

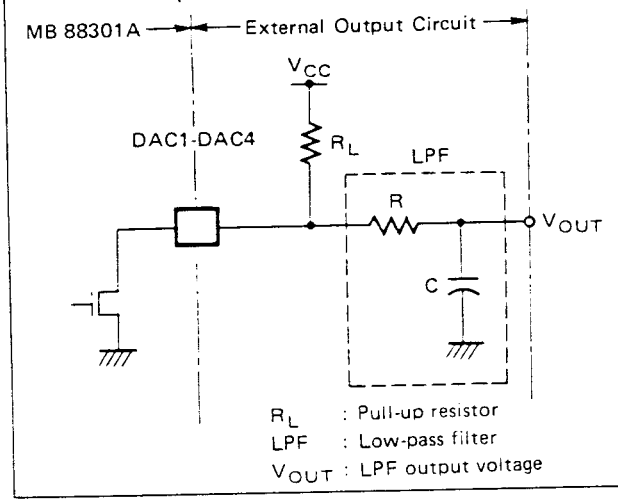


Fig. 12 – DAC OUTPUT WAVEFORM

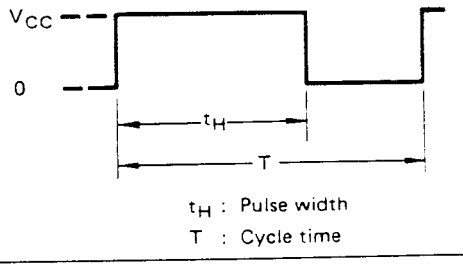
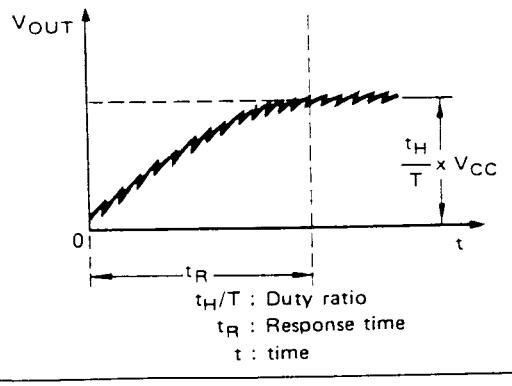


Fig. 13 – V_{OUT} OUTPUT WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Pins/Conditions	
Supply Voltage	V_{CC}	V_{SS} −0.3 to V_{SS} +8.0	V	V_{CC}	V_{SS} = 0 V
Input Voltage	V_{IN}	V_{SS} −0.3 to V_{SS} +8.0	V	DI0-DI3, LDI, EXTAL, XTAL	
Output Voltage	V_{OUT}	V_{SS} −0.3 to V_{SS} +15.0	V	DAC1-DAC4	
		V_{SS} −0.3 to V_{SS} +8.0		TMO1-TMO3	
Operating Temperature	T_A	−30 to +70	°C	Ambient temperature	
Storage Temperature	T_{stg}	−55 to +150	°C		

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Clock Frequency*	f_c	0.5		4.0	MHz
Operating Temperature	T_A	−30		70	°C

NOTE: * Crystal or ceramic resonator should be used. See Fig. 17.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Value			Unit
			Min.	Typ.	Max.	
Output High Voltage	V_{OH}	TMO1-TMO3 I_{OH} = −200μA	2.4			V
		DAC1-DAC4	Open Drain			
Output Low Voltage	V_{OL}	TMO1-TMO3 I_{OL} = 1.8mA			0.4	V
		DAC1-DAC4 I_{OL} = 2.0mA, 5kΩ External Pull Up Resistor			0.8	V
Output Leakage Current	I_{LOH}	DAC1-DAC4 V_{OH} = 13.2V, OFF State			50	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, All Outputs Open		15	25	mA

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Min.		Max.	Unit
LDI Pulse Width	P_{WLDI}	LDI Fig. 14, Fig. 16	5			μs
LDI Rise/Fall times	t_{rLDI} t_{fLDI}	LDI Fig. 14, Fig. 16			1.5	μs
Address/Data Setup Time	t_S	DI3 - DI0 Fig. 14, Fig. 16	0.5			μs
Address/Data Hold Time	t_H	DI3 - DI0 Fig. 14, Fig. 16	2			μs
TMO Rise/Fall times	t_{rTMO} t_{fTMO}	TM01-TM03 Fig. 15, Fig. 16			0.2	μs

Fig. 14 — ADDRESS/DATA INPUT TIMING

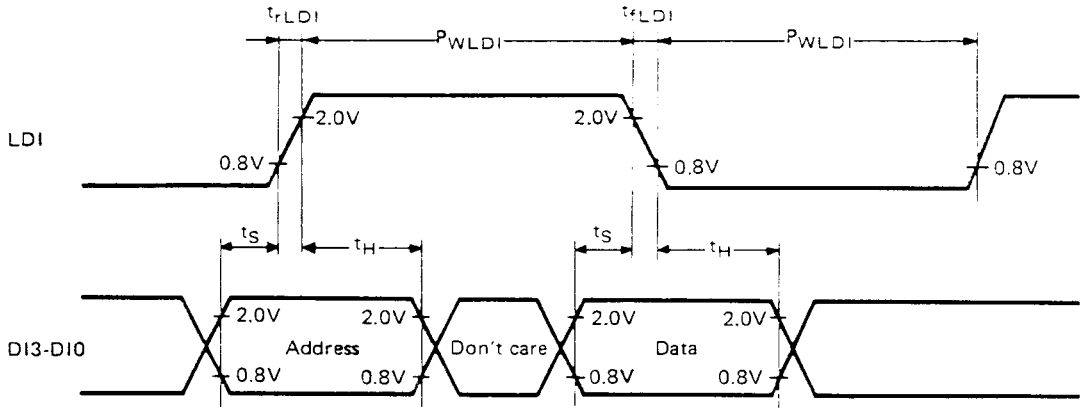
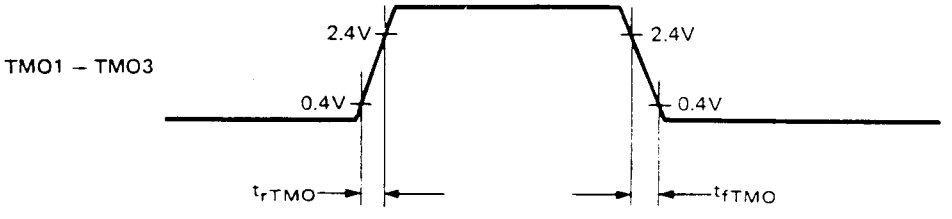


Fig. 15 — SYNCHRONIZATION CLOCK OUTPUT TIMING



AC CHARACTERISTICS (Continued)

Fig. 16 — AC TEST CONDITIONS

INPUT CONDITIONS

- Input Levels:
  2.0V for a logic "1"
  0.8V for a logic "0"

OUTPUT CONDITIONS

- Timing Reference Levels:
  2.4V for a logic "1"
  0.4V for a logic "0"
- Output Load Circuit:
  C_L = 100pF (including scope and jig capacitances)
  R_L = 4kΩ

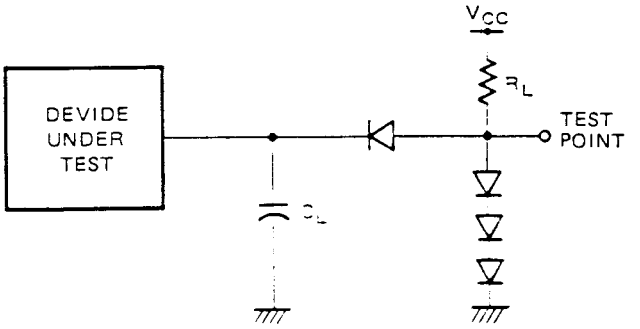
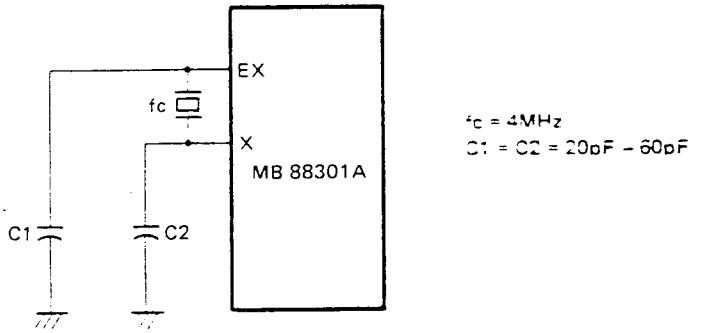


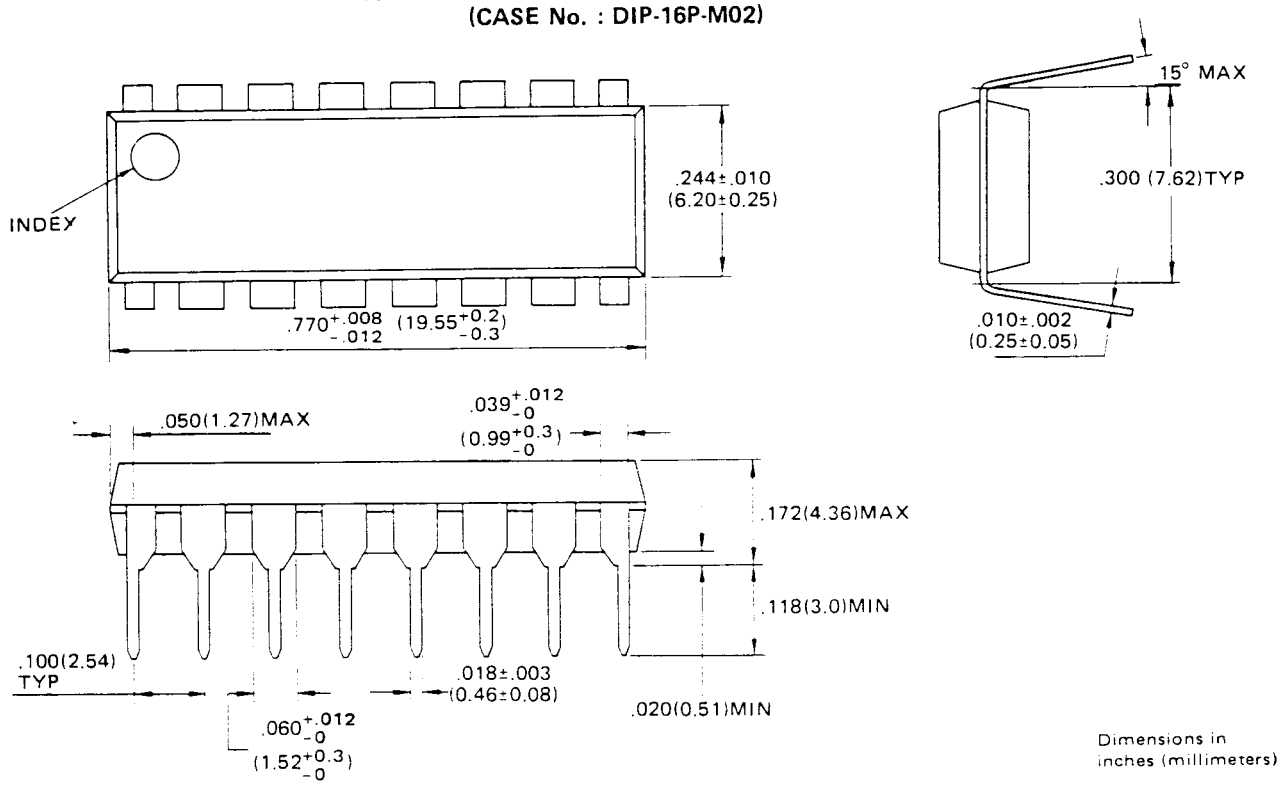
Fig. 17 — CRYSTAL/CERAMIC OSCILLATOR CIRCUIT



PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)

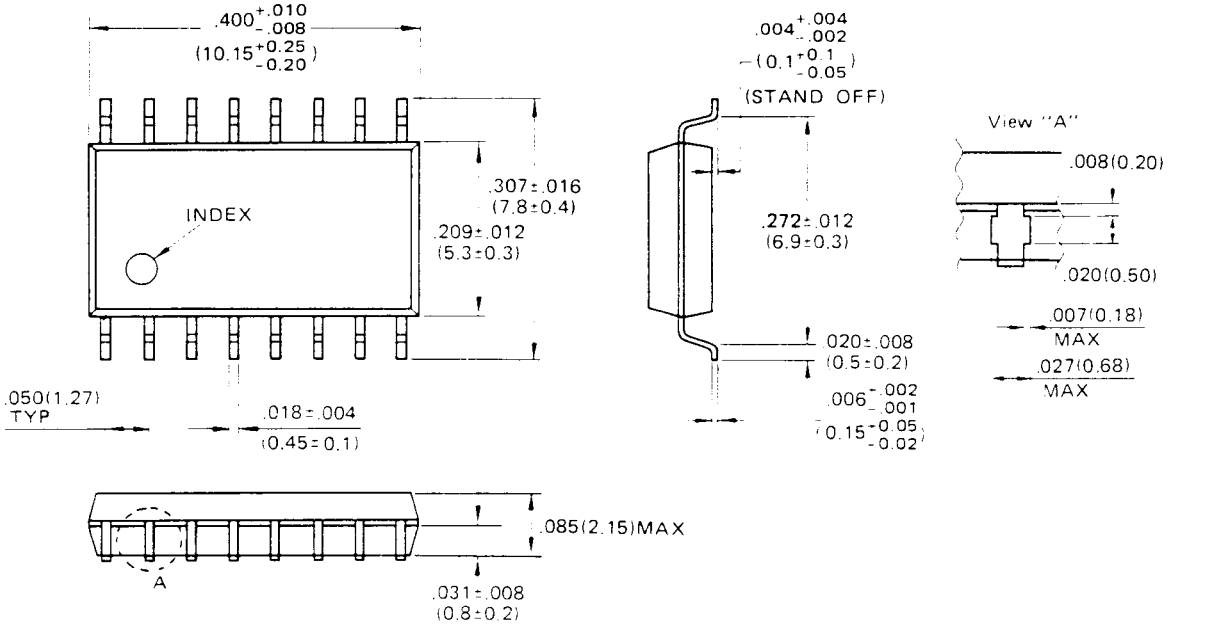


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

PLASTIC SOP(Suffix: -PF)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)