FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.
- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74LVC821 is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC827 is an 10-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.
A HIGH on $\overline{OE}n$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF V_{CC} = 3.3 V	10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC827D	24	SO	plastic	SO24/SOT137
74LVC827DB	24	SSOP	plastic	SSOP24/SOT340
74LVC827PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_9	data inputs
10	GND	ground (0 V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y_0 to Y_9	bus outputs
20	V_{CC}	positive supply voltage

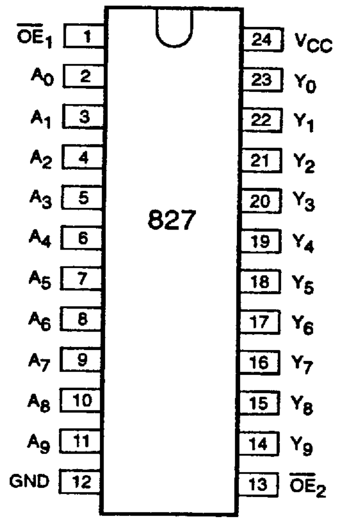

Fig.1 Pin configuration.

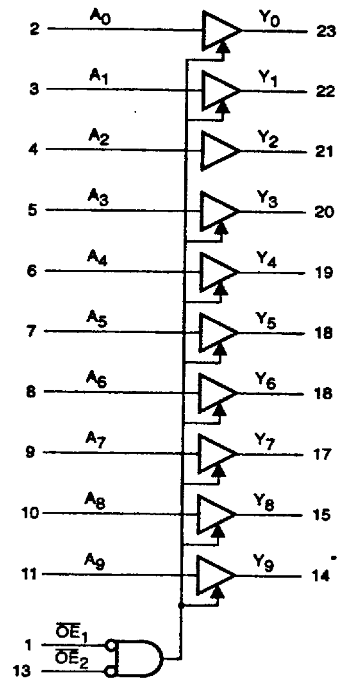

Fig.2 Logic symbol.

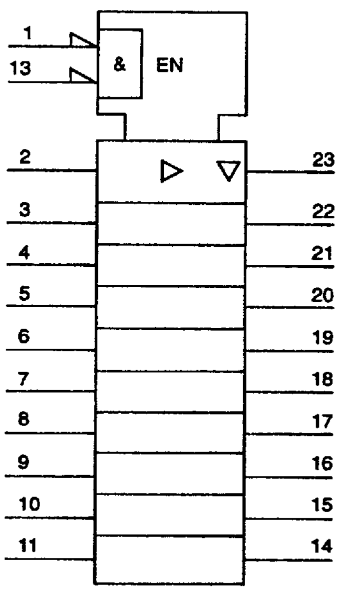

Fig.3 IEC logic symbol.

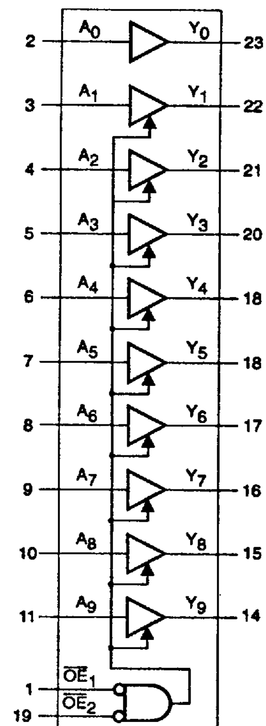

Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC827

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC827

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– – –	– – –	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time 1OE to $1Y_n$; 2OE to $2Y_n$	– – –	– – –	– 9.0 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 6
t_{PHZ}/t_{PLZ}	3-state output disable time 1OE to $1Y_n$; 2OE to $2Y_n$	– – –	– – –	– 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 6

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

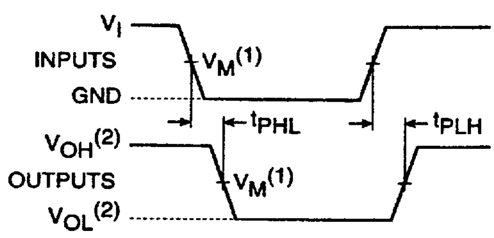

Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delays.

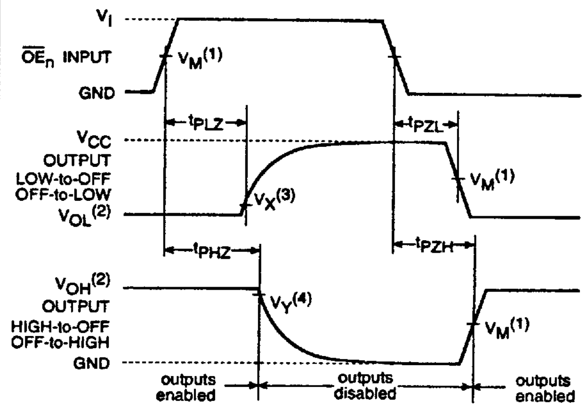

Fig.6 Waveforms showing the 3-state enable and disable times.

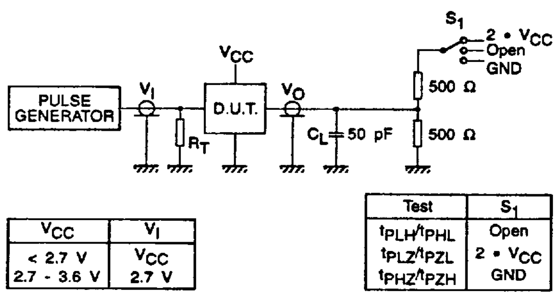

Fig.7 Load circuitry for switching times.

Notes:
(1) $V_M = 1.5\ V$ at $V_{CC} \geq 2.7\ V$
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7\ V$
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
(3) $V_X = V_{OL} + 0.3\ V$ at $V_{CC} \geq 2.7\ V$
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7\ V$
(4) $V_Y = V_{OH} - 0.3\ V$ at $V_{CC} \geq 2.7\ V$
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7\ V$

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