

[查询"MPC17510MTB"供应商](#)

1.2 A 15 V H-Bridge Motor Driver IC

The 17510 is a monolithic H-Bridge designed to be used in portable electronic applications such as digital and SLR cameras to control small DC motors.

The 17510 can operate efficiently with supply voltages as low as 2.0 V to as high as 15 V. Its low $R_{DS(ON)}$ H-Bridge output MOSFETs (0.45 Ω typical) can provide continuous motor drive currents of 1.2 A and handle peak currents up to 3.8 A. It is easily interfaced to low-cost MCUs via parallel 5.0 V compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

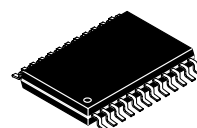
The 17510 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

Features

- 2.0 V to 15 V Continuous Operation
- Output Current 1.2 A (DC), 3.8 A (Peak)
- 450 m Ω $R_{DS(ON)}$ H-Bridge MOSFETs
- 5.0 V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown
- Cross-Conduction Suppression
- Pb-Free Packaging Designated by Suffix Code EJ

17510

H-BRIDGE MOTOR DRIVER



MTB SUFFIX
EJ SUFFIX (Pb-FREE)
98ASH70455A
24-LEAD TSSOP

ORDERING INFORMATION

| Device | Temperature Range (T _A) | Package |
|---------------|-------------------------------------|-----------|
| MPC17510EJ/R2 | -30°C to 65°C | 24 TSSOPW |
| MPC17510MTB | | |
| MPC17510MTBEL | | |

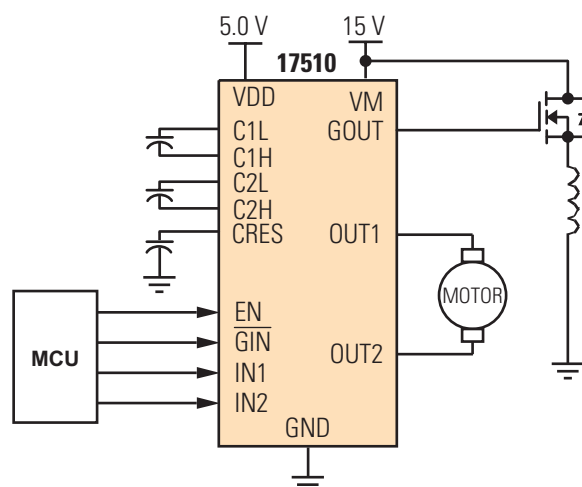


Figure 1. 17510 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

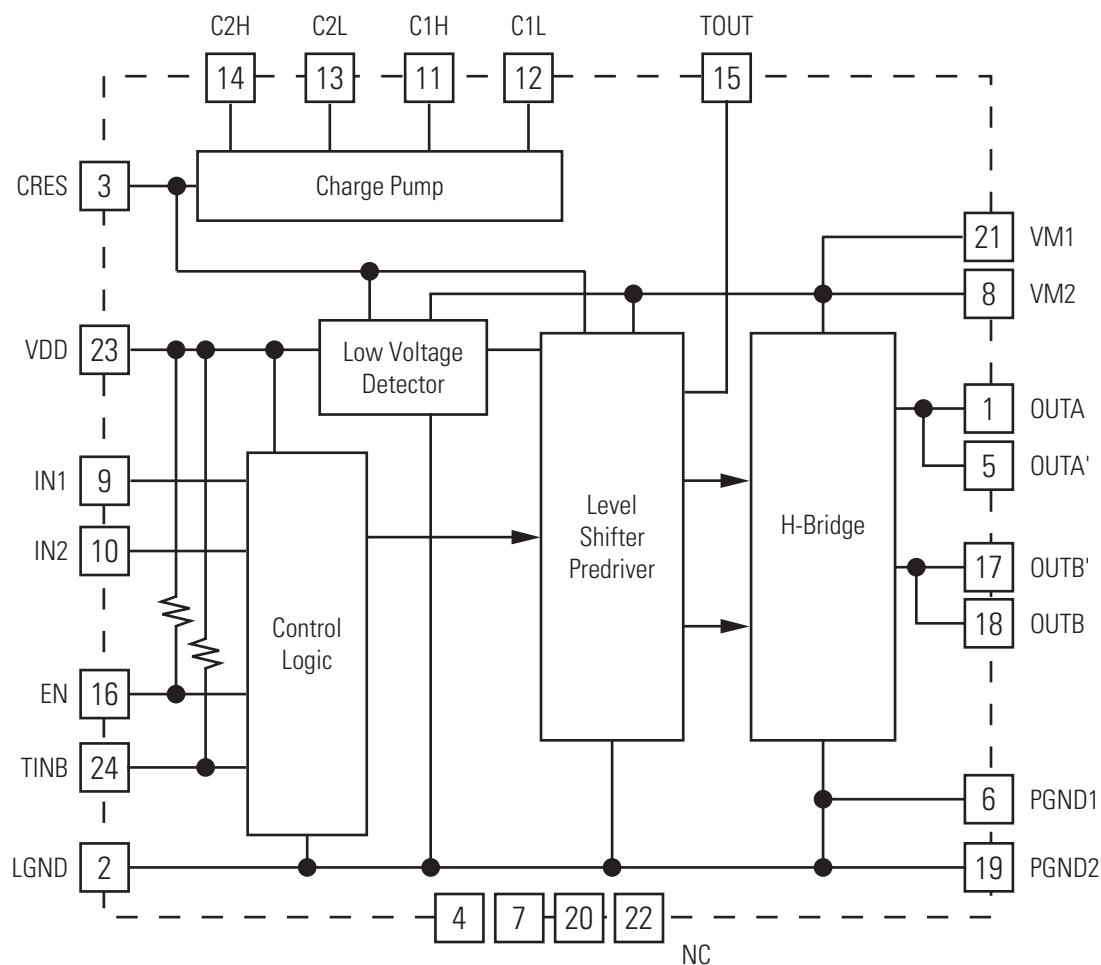


Figure 2. 17510 Simplified Internal Block Diagram

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PIN CONNECTIONS

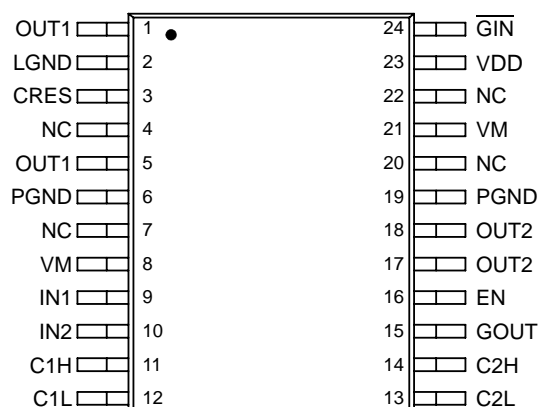


Figure 3. 17510 Pin Connections

Table 1. 17510 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 8](#).

| Pin Number | Pin Name | Formal Name | Definition |
|--------------|------------------------|---|--|
| 1, 5 | OUT1 | Output 1 | Driver output 1 pins. |
| 2 | LGND | Logic Ground | Logic ground. |
| 3 | CRES | Charge Pump Output Capacitor Connection | Charge pump reservoir capacitor pin. |
| 4, 7, 20, 22 | NC | No Connect | No connection to these pins. |
| 17, 18 | OUT2 | Output 2 | Driver output 2 pins. |
| 6, 19 | PGND | Power Ground | Power ground. |
| 8, 21 | VM | Motor Drive Power Supply | Motor power supply voltage input pins. |
| 9 | IN1 | Input Control 1 | Control signal input 1 pin. |
| 10 | IN2 | Input Control 2 | Control signal input 2 pin. |
| 11 | C1H | Charge Pump 1H | Charge pump bucket capacitor 1 (positive pole). |
| 12 | C1L | Charge Pump 1L | Charge pump bucket capacitor 1 (negative pole). |
| 13 | C2L | Charge Pump 2L | Charge pump bucket capacitor 2 (negative pole). |
| 14 | C2H | Charge Pump 2H | Charge pump bucket capacitor 2 (positive pole). |
| 15 | GOUT | Gate Driver Output | Output gate driver signal to external MOSFET switch. |
| 16 | $\overline{\text{EN}}$ | Enable Control | Enable control signal input pin. |
| 23 | VDD | Logic Supply | Control circuit power supply pin. |
| 24 | GIN | Gate Driver Input | LOW = True control signal for GOUT pin. |

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ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|--|-----------------|----------------------|------|
| Motor Supply Voltage | V_M | -0.5 – -16 | V |
| Charge Pump Output Voltage ⁽¹⁾ | V_{CRES} | -0.5 to 13 | V |
| Logic Supply Voltage | V_{DD} | -0.5 to 16 | V |
| Signal Input Voltage (EN, IN1, IN2, \overline{GIN}) | V_{IN} | -0.5 to $V_{DD}+0.5$ | V |
| Driver Output Current | | | A |
| Continuous | I_O | 1.2 | |
| Peak ⁽²⁾ | I_{OPK} | 3.8 | |
| ESD Voltage ⁽³⁾ | | | V |
| Human Body Model | V_{ESD1} | ±1900 | |
| Machine Model | V_{ESD2} | ±130 | |
| Storage Temperature | T_{STG} | -65 to 150 | °C |
| Operating Junction Temperature | T_J | -30 to 150 | °C |
| Operating Ambient Temperature | T_A | -30 to 65 | °C |
| Power Dissipation ⁽⁴⁾ | P_D | 1.0 | W |
| Thermal Resistance | $R_{\theta JA}$ | 120 | °C/W |
| Soldering Temperature ⁽⁵⁾ | T_{SOLDER} | 260 | °C |

Notes

- When supplied externally, connect via 3.0 kΩ resistor.
- $T_A = 25^\circ\text{C}$, 10 ms pulse at 200 ms interval.
- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100\text{ pF}$, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200\text{ pF}$, $R_{ZAP} = 0\ \Omega$).
- $T_A = 25^\circ\text{C}$, $R_{\theta JA} = 120^\circ\text{C/W}$, 37 mm x 50 mm Cu area (1.6 mm FR-4 PCB).
- Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

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STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_M = 15\text{ V}$, $V_{DD} = 5.0\text{ V}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------|-------|------|------|---------------|
| POWER | | | | | |
| Motor Supply Voltage | V_M | 2.0 | – | 15 | V |
| Logic Supply Voltage | V_{DD} | 4.0 | – | 5.5 | V |
| Capacitor for Charge Pump | C1, C2, C3 | 0.001 | – | 0.1 | μF |
| Standby Power Supply Current ⁽⁶⁾ | | | | | |
| Motor Supply Standby Current | I_{VMSTBY} | – | – | 1.0 | μA |
| Logic Supply Standby Current | $I_{VDDSTBY}$ | – | 0.3 | 1.0 | mA |
| Logic Supply Current ⁽⁷⁾ | I_{VDD} | – | 3.3 | 4.0 | mA |
| Low-Voltage Detection Circuit | | | | | V |
| Detection Voltage (V_{DD}) ⁽⁸⁾ | V_{DDDET} | 1.5 | 2.5 | 3.5 | |
| Detection Voltage (V_M) | V_{MDET} | 4.0 | 5.0 | 6.0 | |
| Driver Output ON Resistance ⁽⁹⁾ | $R_{DS(ON)}$ | – | 0.45 | 0.55 | Ω |
| $V_M = 2.0\text{ V}, 8.0\text{ V}, 15\text{ V}$ | | | | | |

GATE DRIVE

| | | | | | |
|--|----------------|------------------|------------------|------------|---|
| Gate Drive Voltage ⁽¹⁰⁾ | V_{CRES} | | | | V |
| No Current Load | | 12 | 13 | 13.5 | |
| Gate Drive Ability (Internally Supplied) | $V_{CRESLOAD}$ | | | | V |
| $I_{CRES} = -1.0\text{ mA}$ | | 10 | 11.2 | – | |
| Gate Drive Output | | | | | V |
| $I_{OUT} = -50\text{ }\mu\text{A}$ | $V_{GOUTHIGH}$ | $V_{CRES} - 0.5$ | $V_{CRES} - 0.1$ | V_{CRES} | |
| $I_{IN} = 50\text{ }\mu\text{A}$ | $V_{GOUTLOW}$ | LGND | LGND+0.1 | LGND+0.5 | |

CONTROL LOGIC

| | | | | | |
|---|----------|---------------------|-----|---------------------|---------------|
| Logic Input Voltage (EN, IN1, IN2, $\overline{\text{GIN}}$) | V_{IN} | 0 | – | V_{DD} | V |
| Logic Input Function ($4.0\text{ V} < V_{DD} < 5.5\text{ V}$) | | | | | |
| High-Level Input Voltage | V_{IH} | $V_{DD} \times 0.7$ | – | – | V |
| Low-Level Input Voltage | V_{IL} | – | – | $V_{DD} \times 0.3$ | V |
| High-Level Input Current | I_{IH} | – | – | 1.0 | μA |
| Low-Level Input Current | I_{IL} | -1.0 | – | – | μA |
| EN/ $\overline{\text{GIN}}$ Pin | I_{IL} | -200 | -50 | – | μA |

Notes

- Excluding pull-up resistor current, including current of gate-drive circuit.
- $f_{IN} = 100\text{ kHz}$.
- Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, $V_{CRES} = 7.5\text{ V}$.
- $I_O = 1.2\text{ A}$ source + sink.
- Input logic signal not present.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_M = 15\text{ V}$, $V_{DD} = 5.0\text{ V}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

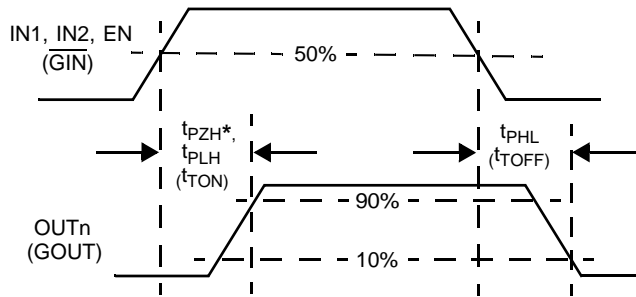
| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------------------|-----|-----|-------------|---------------|
| INPUT (EN, IN1, IN2, GIN) | | | | | |
| Pulse Input Frequency | f_{IN} | — | — | 200 | kHz |
| Input Pulse Rise Time ⁽¹¹⁾ | t_R | — | — | 1.0 (12) | μs |
| Input Pulse Fall Time ⁽¹³⁾ | t_F | — | — | 1.0 (12) | μs |
| OUTPUT | | | | | |
| Propagation Delay Time | | | | | μs |
| Turn-ON Time | t_{PZH} | — | 0.3 | 1.0 | μs |
| Turn-ON Time | t_{PLH} | — | 1.2 | 2.0 | |
| Turn-OFF Time | t_{PHL} | — | 0.5 | 1.0 | |
| GOUT Output Delay Time ⁽¹⁴⁾ | | | | | μs |
| Turn-ON Time | t_{TON} | — | — | 10 | μs |
| Turn-OFF Time | t_{TOFF} | — | — | 10 | |
| Charge Pump Circuit | | | | | |
| Oscillator Frequency | f_{OSC} | 100 | 200 | 400 | kHz |
| Rise Time ⁽¹⁵⁾ | $t_{\text{V}_{\text{CRES}}}$ | — | 0.1 | 1.0 | ms |
| Low-Voltage Detection Time | t_{VDDDET} | — | — | 10 | ms |

Notes

11. Time is defined between 10% and 90%.
12. That is, the input waveform slope must be steeper than this.
13. Time is defined between 90% and 10%.
14. Load is 500 pF.
15. Time to charge C_{RES} to 11 V after application of V_{DD} .

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TIMING DIAGRAMS



* The last state is "Z".

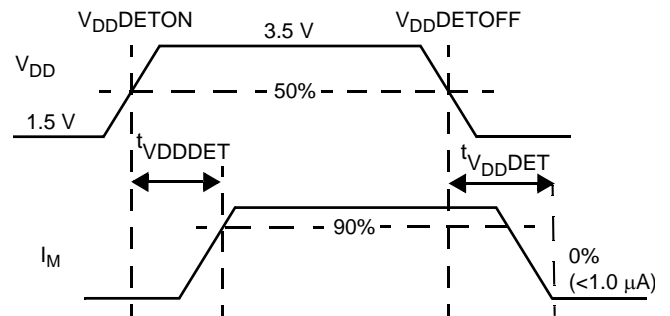
Figure 4. t_{PLH} , t_{PHL} , and t_{PZH} Timing

Figure 5. Low-Voltage Detection Timing

Table 5. Truth Table

| INPUT | | | | OUTPUT | | |
|-------|-----|-----|-----|--------|------|------|
| EN | IN1 | IN2 | GIN | OUT1 | OUT2 | GOUT |
| H | L | L | X | Z | Z | X |
| H | H | L | X | H | L | X |
| H | L | H | X | L | H | X |
| H | H | H | X | L | L | X |
| L | X | X | X | L | L | L |
| H | X | X | L | X | X | H |
| H | X | X | H | X | X | L |

H = High.

L = Low.

Z = High impedance.

X = Don't care.

The GIN pin and EN pin are pulled up to V_{DD} with internal resistance.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17510 is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17510 can operate efficiently with supply voltages as low as 2.0 V to as high as 15 V, and it can provide continuous motor drive currents of 1.2 A while handling peak currents up to 3.8 A. It is easily interfaced to low-cost MCUs via parallel 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17510 has four operating modes: Forward, Reverse, Brake, and Tri-States (High Impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0 A rms output current capability, make the 17510 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17510 devices can be used to control bipolar stepper motors. The 17510 can also be used to excite transformer primary

windings with a switched square wave to produce secondary winding AC currents.

As shown in [Figure 2, 17510 Simplified Internal Block Diagram](#), page 2, the 17510 is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: ENable input logic HIGH, one INput logic LOW, and the other INput logic HIGH (to define output polarity). The 17510 can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low-side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also be implemented by taking the ENable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to [Table 5, Truth Table](#), page 7).

The 17510 outputs are capable of providing a continuous DC load current of up to 1.2 A. An internal charge pump supports PWM frequencies to 200 kHz. The EN pin also controls the charge pump, turning it off when EN = LOW, thus allowing the 17510 to be placed in a power-conserving sleep mode.

FUNCTIONAL PIN DESCRIPTION

OUTPUT 1 AND OUTPUT2 (OUT1, OUT2)

The OUT1 and OUT2 pins provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these pins would be a small DC motor. These outputs will connect to either VM or PGND, depending on the states of the control inputs (refer to [Table 5, Truth Table](#), page 7).

POWER GROUND AND LOGIC GROUND (PGND, LGND)

The power and logic ground pins (PGND and LGND) should be connected together with a very low-impedance connection.

CHARGE PUMP RESERVOIR CAPACITOR (CRES)

The CRES pin provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this pin can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the CRES pin will be approximately three times the V_{DD} voltage, as the internal charge pump utilizes a voltage tripler circuit. The V_{CRES} voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

MOTOR SUPPLY VOLTAGE INPUT (VM)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUT1 and OUT2. All VM pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

CONTROL SIGNAL INPUT AND ENABLE CONTROL SIGNAL INPUT (IN1, IN2, EN)

The IN1, IN2, and EN pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to [Table 5, Truth Table](#)).

GATE DRIVER INPUT (GIN)

The \overline{GIN} input controls the GOUT pin. When \overline{GIN} is set logic LOW, GOUT supplies a level-shifted high-side gate drive signal to an external MOSFET. When \overline{GIN} is set logic HIGH, GOUT is set to GND potential.

[查询"MPC17510MTB"供应商](#)**CHARGE PUMP BUCKET CAPACITOR (C1L, C1H, C2L, C2H)**

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μ F.

GATE DRIVER OUTPUT (GOUT)

The GOUT output pin provides a level-shifted, high-side gate drive signal to an external MOSFET with C_{ISS} up to 500 pF.

CONTROL CIRCUIT POWER SUPPLY (VDD)

The VDD pin carries the 5.0 V supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

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TYPICAL APPLICATIONS

[Figure 6](#) shows a typical application for the 17510.

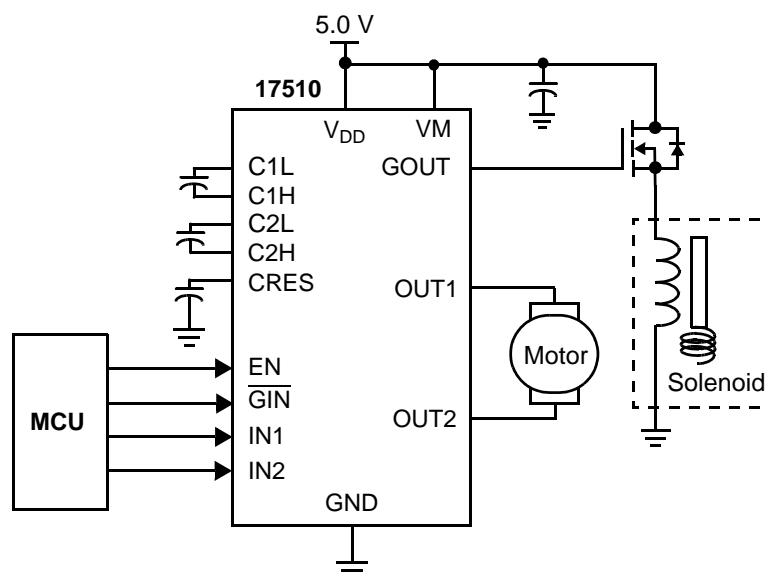


Figure 6. 17510 Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply pin (VM) (see [Figure 7](#)).

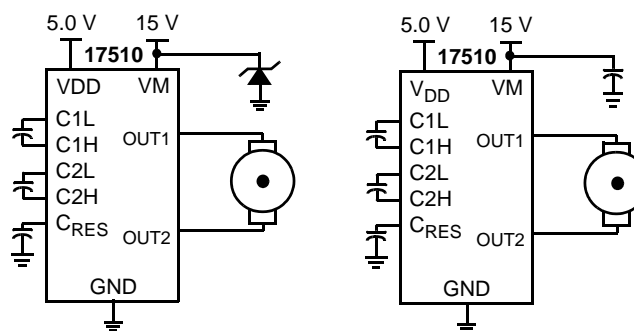


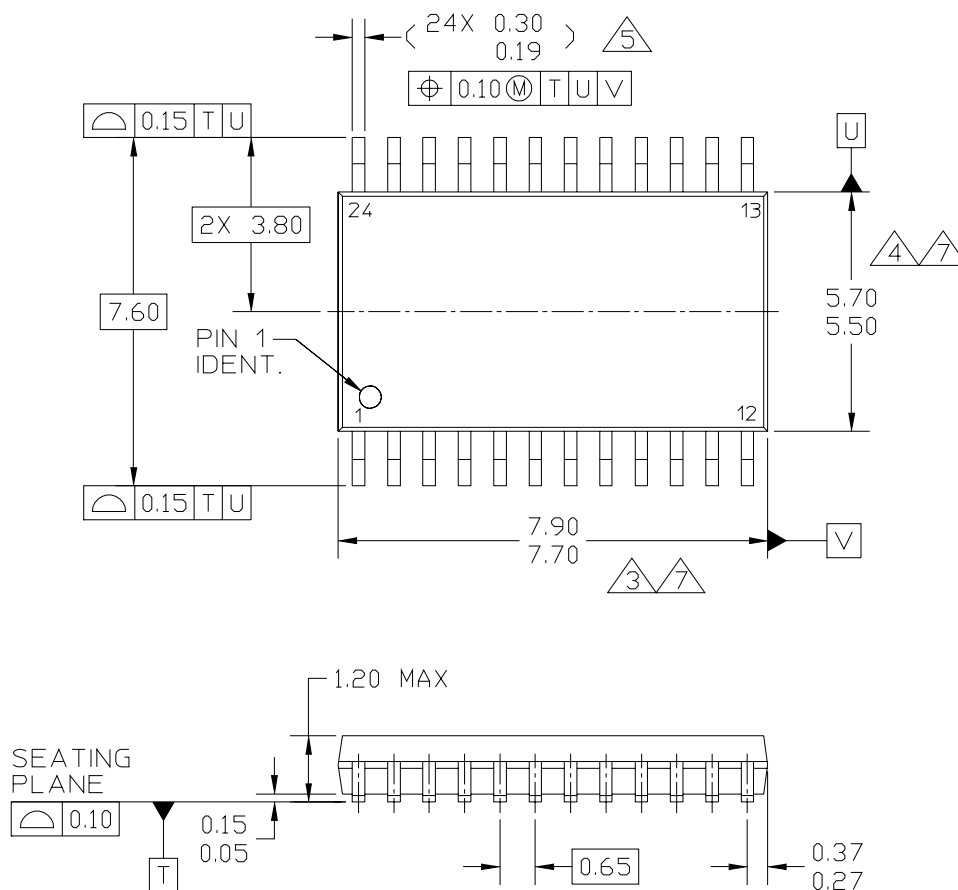
Figure 7. CEMF Snubbing Techniques

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PACKAGING

PACKAGE DIMENSIONS

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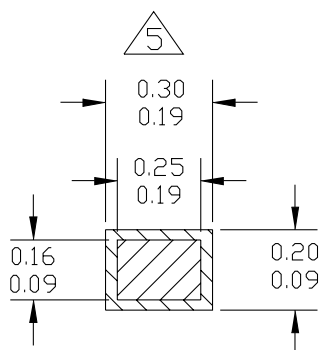
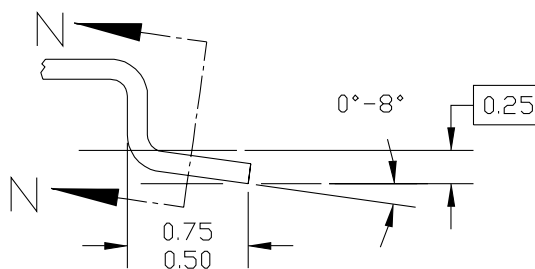
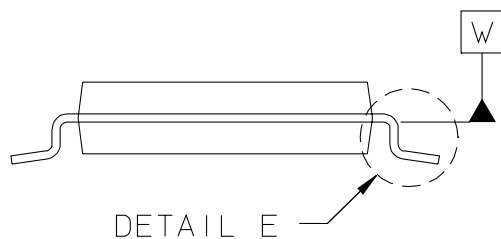


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24-PIN
PLASTIC PACKAGE
98ASH70455A
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PACKAGE DIMENSIONS (continued)



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REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|----------|--------|---|
| 2.0 | 7/2006 | <ul style="list-style-type: none">Implemented a Revision History page.Converted to Freescale format, and updated to the prevailing form and styleAdded EJ Pb-FREE package |
| 3.0 | 1/2007 | <ul style="list-style-type: none">Corrected symbol in Table 3, Driver Output ON Resistance from "W" to "Ω" |

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