PRELIMINARY **CY14B256L**

256-Kbit (32K x 8) nvSRAM

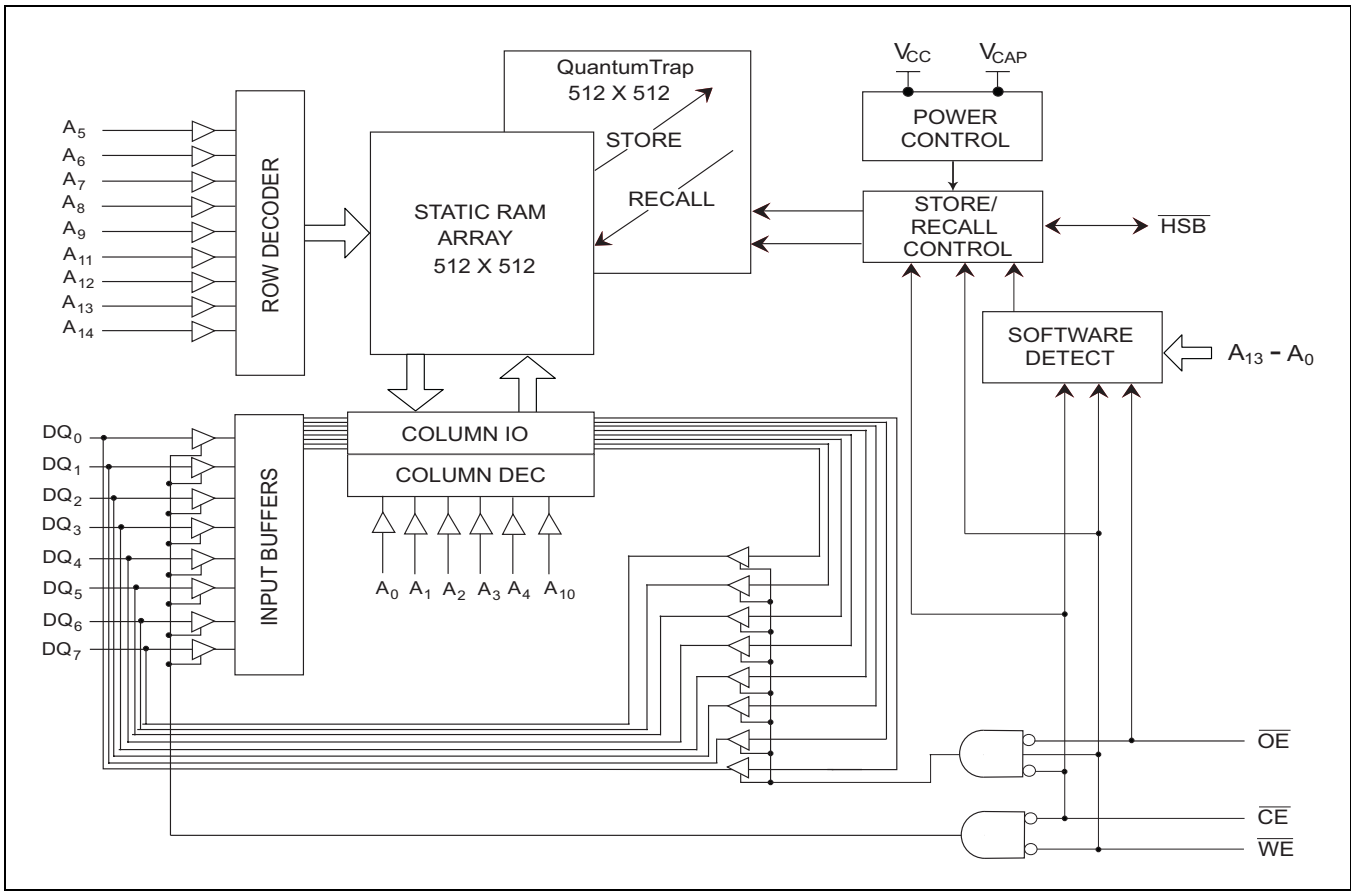
Features

- 25 ns, 35 ns, and 45 ns access times
- “Hands-off” automatic *STORE* on power down with only a small capacitor
- *STORE* to QuantumTrap™ nonvolatile elements is initiated by software, device pin, or AutoStore™ on power down
- *RECALL* to SRAM initiated by software or power up
- Infinite *READ, WRITE,* and *RECALL* cycles
- 10 mA typical I_{CC} at 200 ns cycle time
- 200,000 *STORE* cycles to QuantumTrap
- 20-year data retention @ 55°C
- Single 3V operation with tolerance of +15%, –10%
- Commercial and industrial temperature
- SOIC and SSOP packages
- RoHS compliance

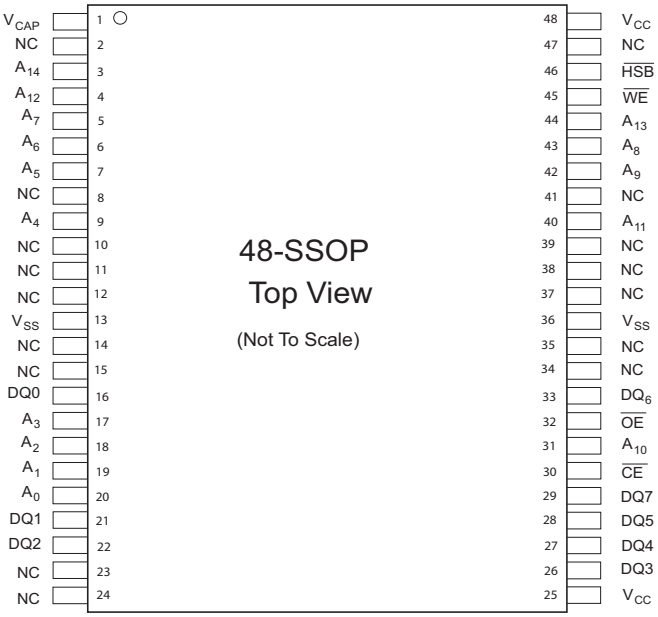
Functional Description

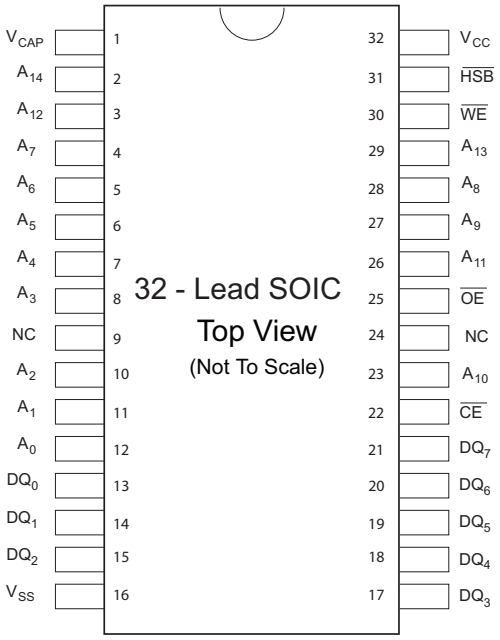
The Cypress CY14B256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world’s most reliable nonvolatile memory. The SRAM provides infinite read and write cycles while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. The STORE and RECALL operations are also available under software control.

Logic Block Diagram



Pin Configurations





Pin Definitions

Pin Name	IO Type	Description
$A_0 – A_{14}$	Input	**Address inputs used to select one of the 32,768 bytes of the nvSRAM**.
DQ0 – DQ7	Input Output	**Bidirectional data IO lines**. Used as input or output lines depending on operation.
NC	No Connect	**No Connects**. This pin is not connected to the die.
$\overline{WE}$	Input	**Write Enable Input, active LOW**. When selected LOW, enables data on the IO pins to be written to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V_{SS}	Ground	**Ground for the device**. Must be connected to ground of the system.
V_{CC}	Power Supply	**Power supply inputs to the device**.
$\overline{HSB}$	Input Output	**Hardware Store Busy**. When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected. (connection optional)
V_{CAP}	Power Supply	**AutoStore capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The CY14B256L nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14B256L supports infinite reads and writes just like a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200,000 STORE operations.

SRAM READ

The CY14B256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are low while $\overline{WE}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs will be valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought high, or $\overline{WE}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are low and $\overline{HSB}$ is high. The address inputs must be stable before entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes high at the end of the cycle. The data on the common IO pins IO_{0-7} will be written into the memory t_{SD} before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep the OE HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines.

If $\overline{OE}$ is left low, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes low.

AutoStore Operation

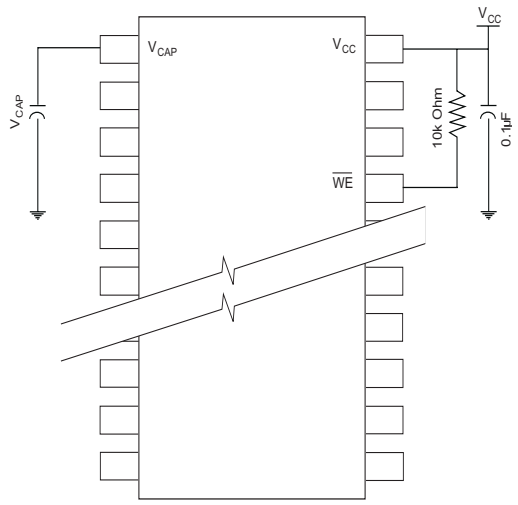
The CY14B256L stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by $\overline{HSB}$, Software Store, activated by an address sequence, and AutoStore, on device power down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B256L.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 1 on page 4 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC Electrical Characteristics on page 7 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up must be placed on $\overline{WE}$ to hold it inactive during power up.

To reduce unnecessary nonvolatile stores, AutoStore, and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an AutoStore cycle is in progress.

Figure 1. AutoStore Mode



Hardware STORE ($\overline{HSB}$) Operation

The CY14B256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. Use the $\overline{HSB}$ pin to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the CY14B256L conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the CY14B256L continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

During any STORE operation, regardless of how it was initiated, the CY14B256L continues to drive the $\overline{HSB}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14B256L remains disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it must be left unconnected.

Hardware RECALL (Power Up)

During power up, or after any low power condition

(V_{CC} < V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B256L software STORE cycle is initiated by executing sequential $\overline{CE}$-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0x0E38, valid READ
2. Read address 0x31C7, valid READ
3. Read address 0x03E0, valid READ
4. Read address 0x3C1F, valid READ
5. Read address 0x303F, valid READ
6. Read address 0x0FC0, initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$-controlled READs or $\overline{OE}$-controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle commences, and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence. It is not necessary that OE be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Software RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$-controlled READ operations must be performed:

1. Read address 0x0E38, valid READ
2. Read address 0x31C7, valid READ
3. Read address 0x03E0, valid READ
4. Read address 0x3C1F, valid READ
5. Read address 0x303F, valid READ
6. Read address 0x0C63, initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements.

Data Protection

The CY14B256L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} < V_{SWITCH}. If the CY14B256L is in a WRITE mode (both $\overline{CE}$ and $\overline{WE}$ low) at power up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on $\overline{CE}$ or $\overline{WE}$ is detected. This protects against inadvertent writes during power up or brownout conditions.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A13 – A0	Mode	IO	Power
H	X	X	X	Not Selected	Output High-Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x03F8	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x07F0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High-Z	Active I_{CC2}[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High-Z	Active[1, 2, 3]

Notes
1. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 15 address lines on the CY14B256L, only the lower 14 lines are used to control software modes.
3. IO state depends on the state of $\overline{OE}$. The IO table shown assumes $\overline{OE}$ low.

Preventing AutoStore

Disable the AutoStore function by initiating an AutoStore Disable Sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable Sequence, the following sequence of $\overline{CE}$-controlled READ operations must be performed:

1. Read address 0x0E38 valid READ
2. Read address 0x31C7 valid READ
3. Read address 0x03E0 valid READ
4. Read address 0x3C1F valid READ
5. Read address 0x303F valid READ
6. Read address 0x03F8 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, the following sequence of $\overline{CE}$-controlled READ operations must be performed:

1. Read address 0x0E38 valid READ
2. Read address 0x31C7 valid READ
3. Read address 0x03E0 valid READ
4. Read address 0x3C1F valid READ
5. Read address 0x303F valid READ
6. Read address 0x07F0 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Noise Considerations

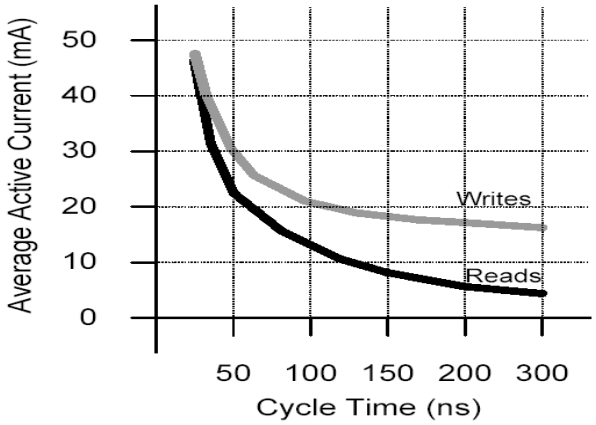
The CY14B256L is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduces circuit noise.

Low Average Active Power

CMOS technology provides the CY14B256L the benefit of drawing less current when it is cycled at times longer than 50 ns. *Figure 2* shows the relationship between I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC} = 3.45V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B256L depends on the following items:

- The duty cycle of chip enable.
- The overall cycle rate for accesses.
- The ratio of READs to WRITEs.
- The operating temperature.
- The V_{CC} level.
- IO loading.

Figure 2. Current vs. Cycle Time



Maximum Ratings

Exceeding maximum ratings may impair the useful life of device. For user guidelines, not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND..... –0.5V to 4.1V

Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage ..... –0.5V to Vcc + 0.5V

Transient Voltage (< 20 ns) on Any Pin to Ground Potential..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Pb Soldering Temperature (3 seconds) ..... +260°C

Output Short Circuit Current [4] ..... 15 mA

Static Discharge Voltage..... > 2001V (in accordance with MIL-STD-883, method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.45V
Industrial	–40°C to +85°C	2.7V to 3.45V

DC Electrical Characteristics

(over the operating range) VCC = 2.7V to 3.45V [5, 6]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA	Commercial		65 55 50	mA mA mA
			Industrial		55 (t_{RC} = 45 ns)	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All inputs do not care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns, 3V, 25°C typical	$\overline{WE}$ > (V_{CC} – 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All inputs do not care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE}$ > (V_{CC} – 0.2). All others V_{IN} < 0.2V or > (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			3	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$		– 1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > V_{IH}		– 1	+1	µA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = – 2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 5V rated		17	120	µF

Notes

4. Outputs shorted for no more than one second. No more than one output shorted at a time.
5. Typical conditions for the active current shown on the front page of the data sheet are average values at 25°C (room temperature), and V_{CC} = 3V. Not 100% tested.
6. The HSB pin has I_{OUT} = –10 µA for V_{OH} of 2.4 V, this parameter is characterized but not tested.

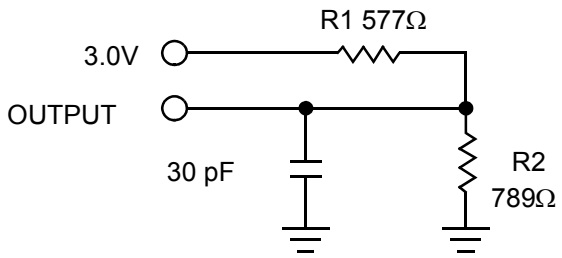
Capacitance[7]

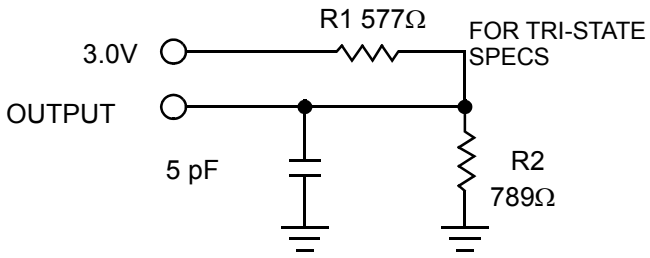
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0 V	7	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance [7]

Parameter	Description	Test Conditions	32-SOIC	48-SSOP	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		TBD	TBD	°C/W

AC Test Loads





AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%)..... ≤5 ns
Input and Output Timing Reference Levels..... 1.5 V

Note
7. These parameters are guaranteed but not tested.

AC Switching Characteristics

Parameter		Description	25 ns part		35 ns part		45 ns part		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	Min	Max	
SRAM READ Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
t_{RC} [8]	t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA} [9]	t_{AA}	Address Access Time		25		35		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
t_{OHA} [9]	t_{OH}	Output Hold After Address Change	3		3		3		ns
t_{LZCE} [10]	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE} [10]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE} [10]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [10]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU} [7]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [7]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns
SRAM WRITE Cycle									
t_{WC}	t_{WC}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [10, 11]	t_{WZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE} [10]	t_{OW}	Output Active after End of Write	3		3		3		ns

Notes
8. $\overline{WE}$ must be HIGH during SRAM READ Cycles.
9. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
10. Measured ± 200 mV from steady state output voltage.

AutoStore/Power Up RECALL

Parameter	Description	CY14B256L		Unit
		Min	Max	
$t_{HRECALL}$ [12]	Power Up RECALL Duration		20	ms
t_{STORE} [13, 14]	STORE Cycle Duration		12.5	ms
V_{SWITCH}	Low Voltage Trigger Level		2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		µs

Software Controlled STORE/RECALL Cycle [15, 16]

Parameter	Description	25 ns part		35 ns part		45 ns part		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{CW}	Clock Pulse Width	20		25		30		ns
t_{GHAX}	Address Hold Time	1		1		1		ns
t_{RECALL}	RECALL Duration		50		50		50	µs
t_{SS} [17, 18]	Soft Sequence Processing Time		70		70		70	µs

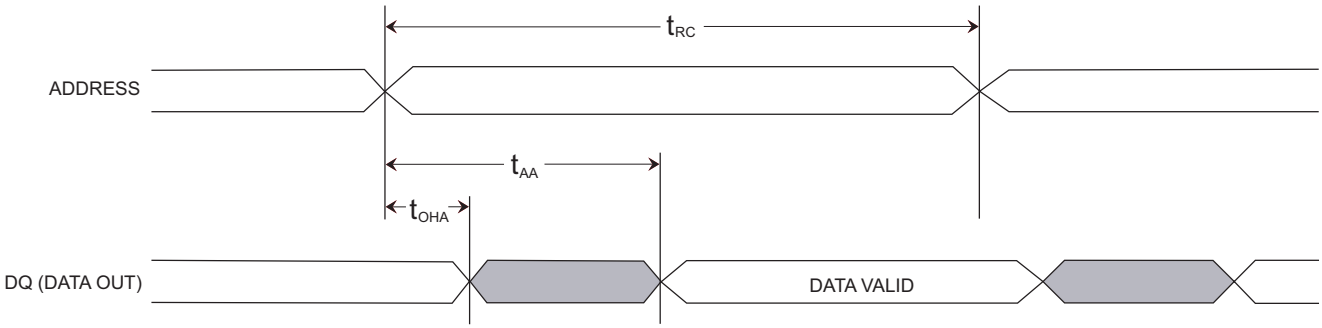
Hardware STORE Cycle

Parameter	Description	CY14B256L		Unit
		Min	Max	
t_{DELAY} [19]	Time allowed to complete SRAM Cycle	1	70	µs
t_{HLHX}	Hardware STORE Pulse Width	15		ns

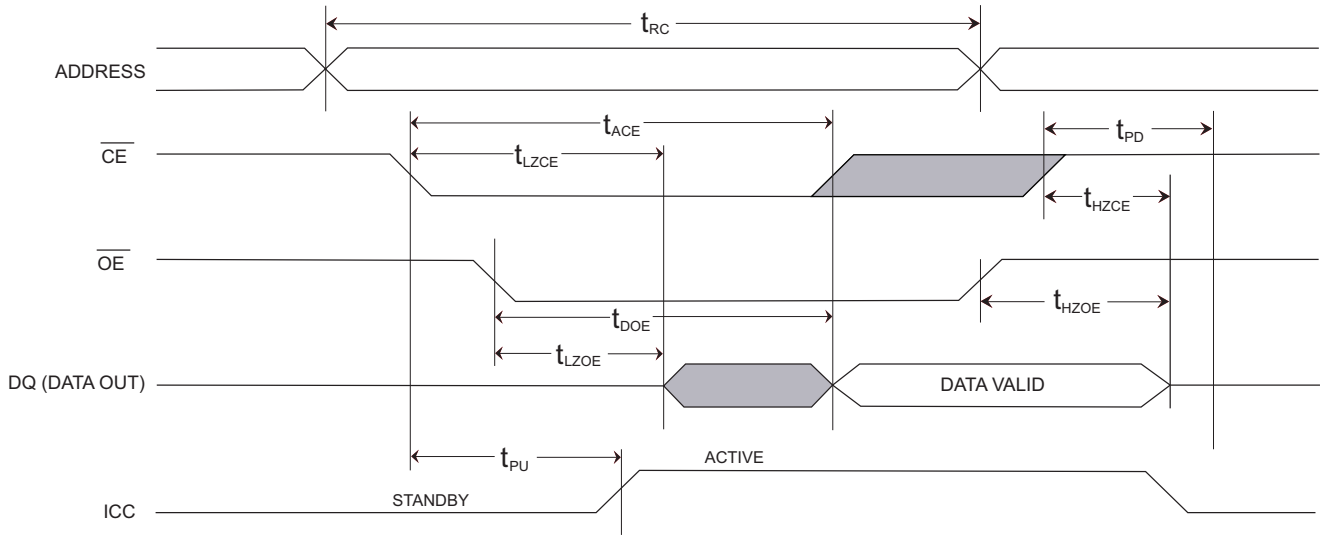
Notes
11. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
12. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
13. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE takes place.
14. Industrial grade devices require 15 ms max.
15. The software sequence is clocked with $\overline{CE}$-controlled or $\overline{OE}$-controlled READs.
16. The six consecutive addresses must be read in the order listed in the Table 1,Mode Selection, on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.
17. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register the command.
18. Commands like STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.
19. READ and WRITE cycles in progress before $\overline{HSB}$ are given this amount of time to complete.

Switching Waveforms

SRAM Read Cycle 1 (address controlled) [8, 9, 20]



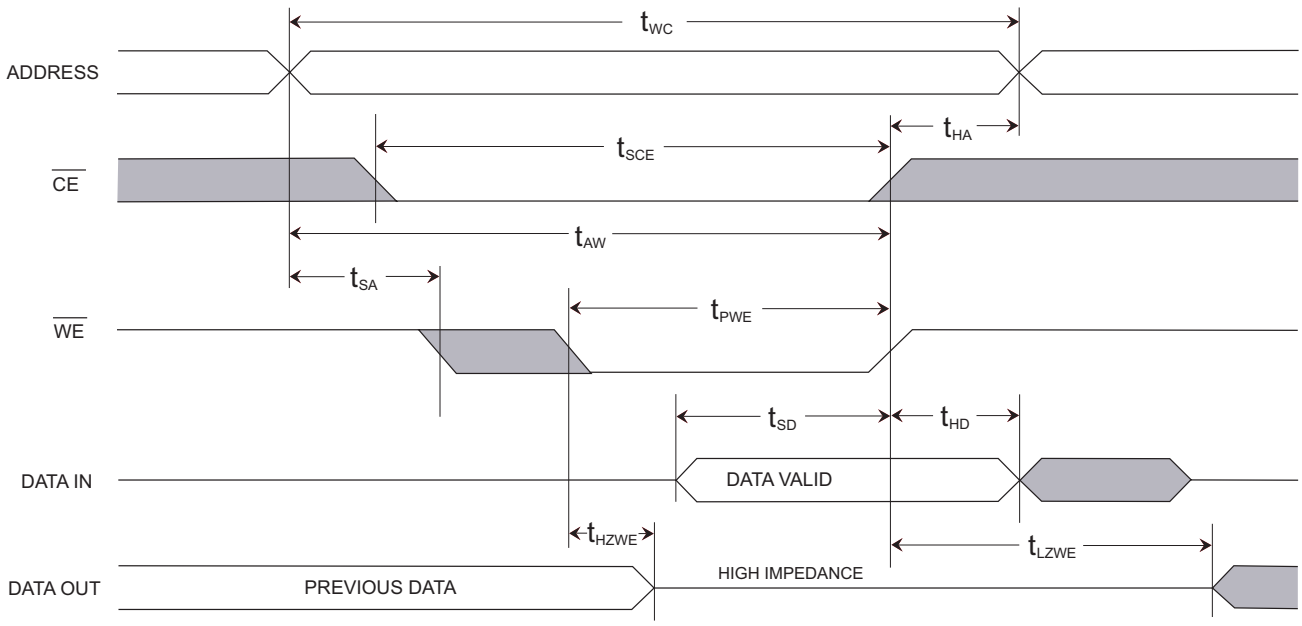
SRAM Read Cycle 2 ($\overline{CE}$ controlled) [8, 20]



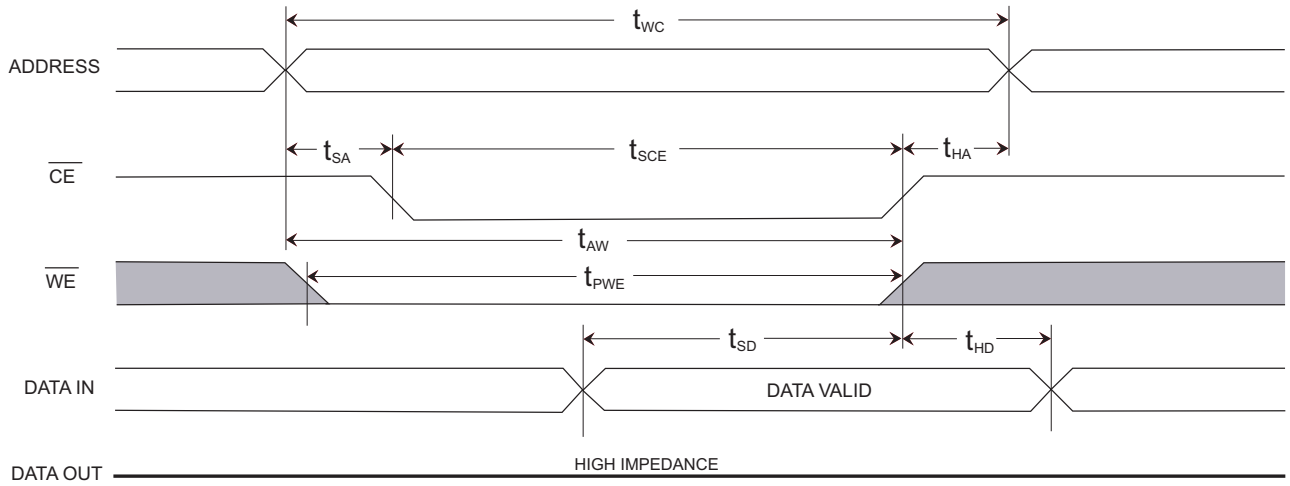
Note
20. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

SRAM Write Cycle 1 ($\overline{WE}$ controlled) [20, 21]



SRAM Write Cycle 2 ($\overline{CE}$ controlled)



Note
21. $\overline{CE}$ or $\overline{WE}$ must be > V_{IH} during address transitions.

Switching Waveforms (continued)

Figure 3. AutoStore/Power Up RECALL

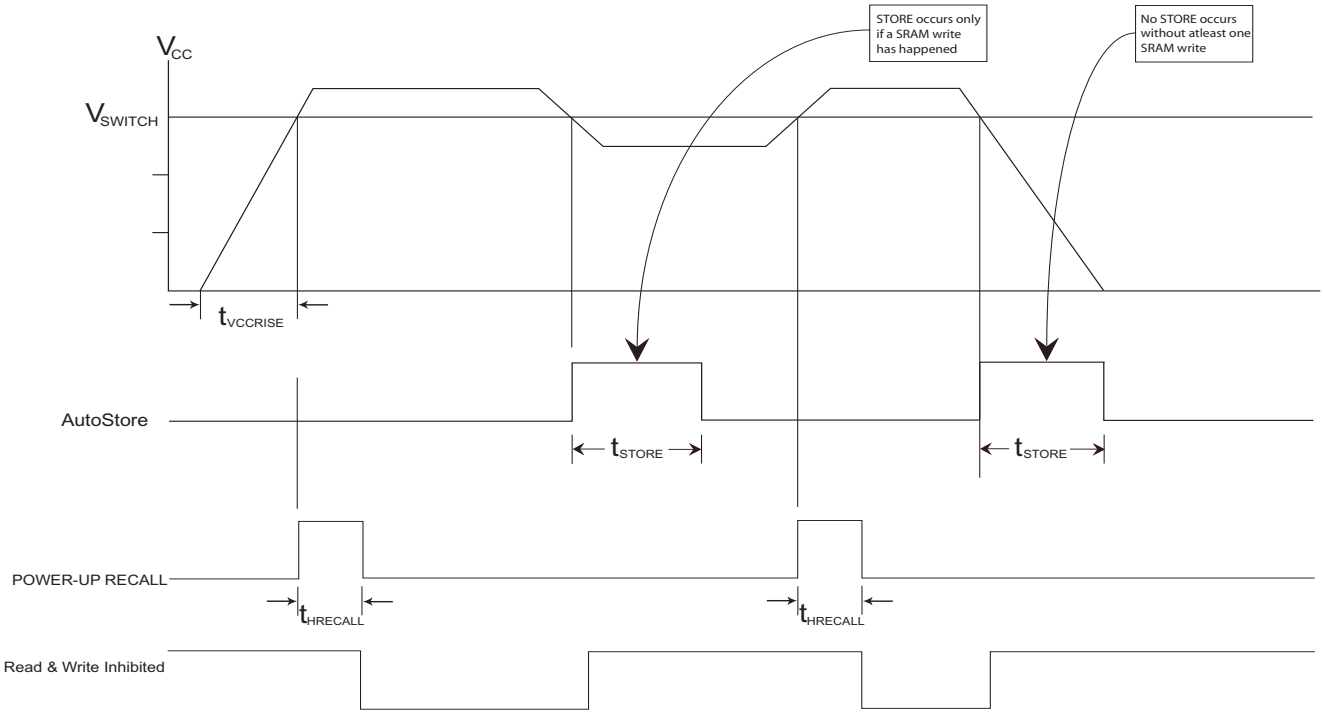
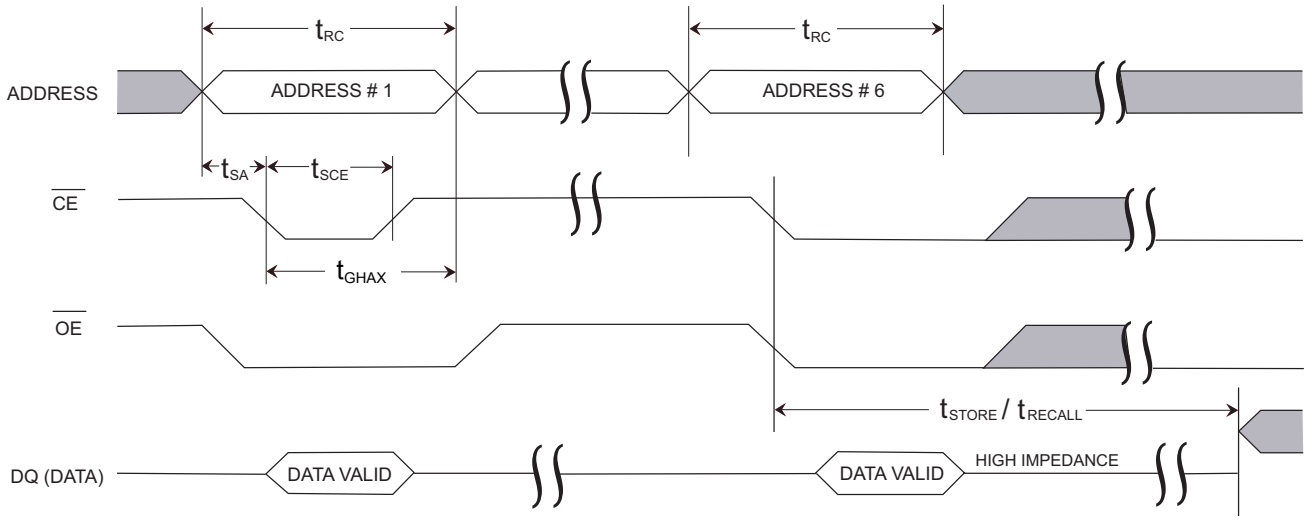


Figure 4. $\overline{CE}$-Controlled Software STORE/RECALL Cycle [16]



Switching Waveforms (continued)

Figure 5. $\overline{OE}$-Controlled Software STORE/RECALL Cycle [16]

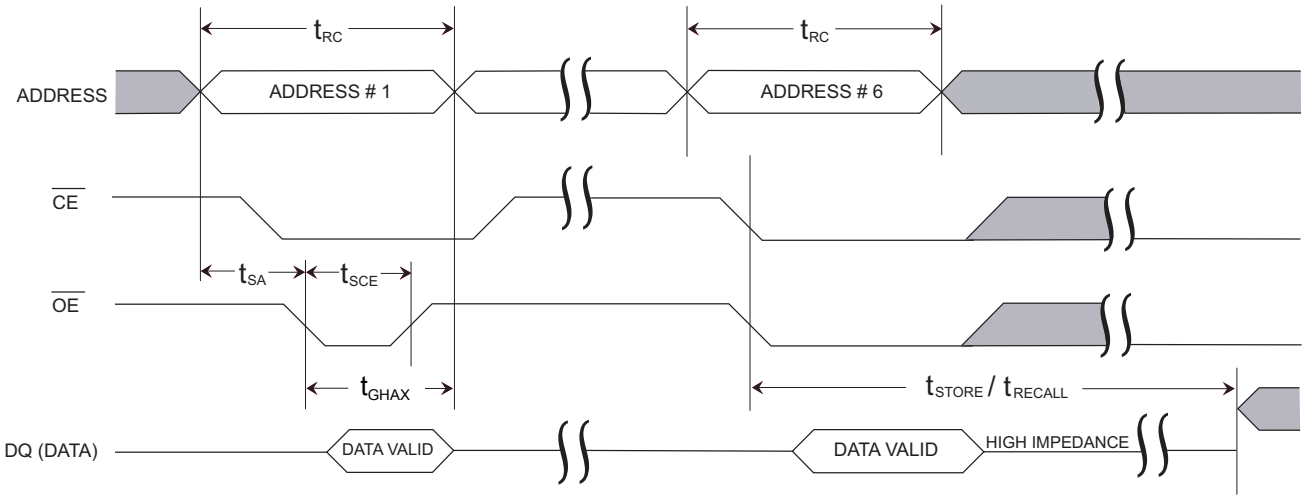


Figure 6. Hardware STORE Cycle

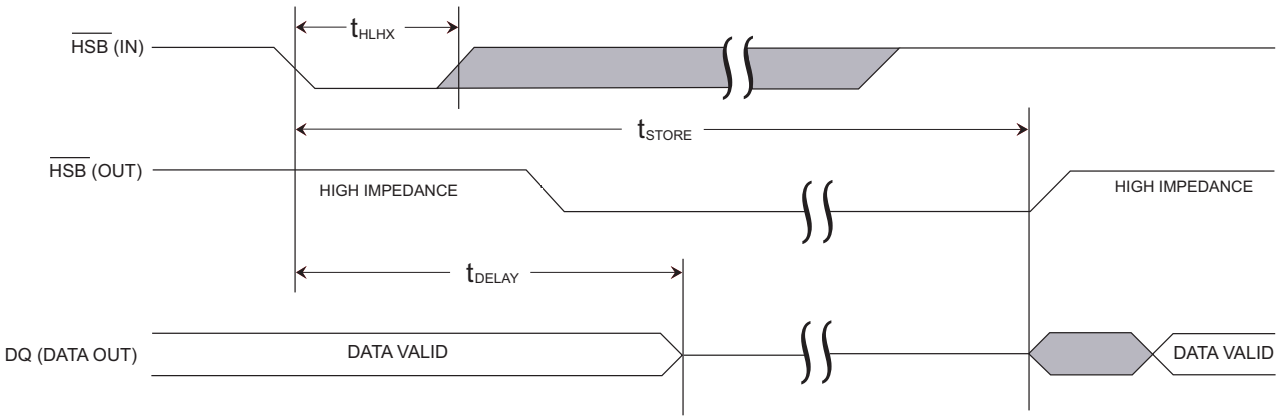
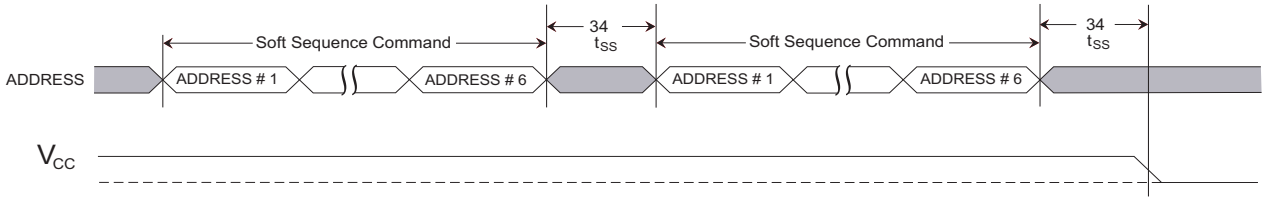
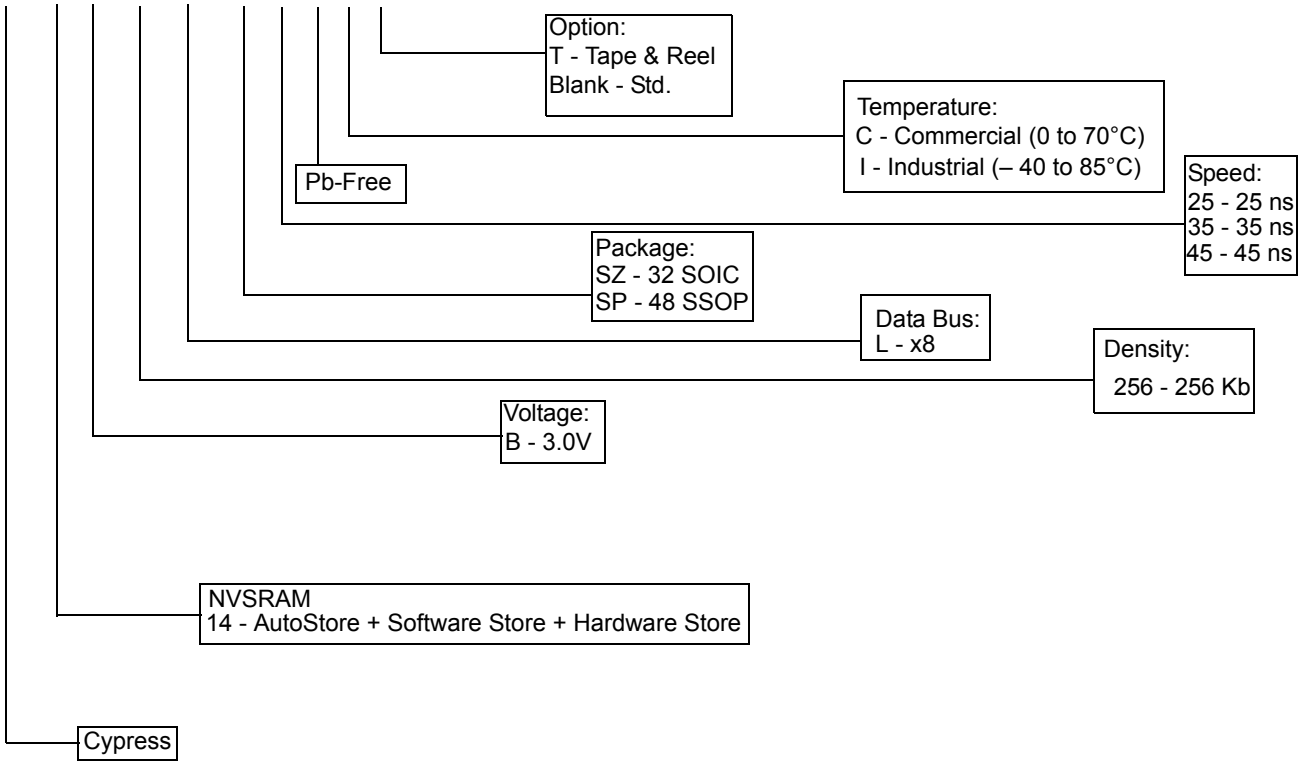


Figure 7. Soft Sequence Processing [17, 18]



Part Numbering Nomenclature

CY 14 B 256 L - SZ 25 X C T



Ordering Information

All of the above mentioned parts are of “Pb-free” type. Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B256L-SZ25XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SP25XCT	51-85061	48-pin SSOP	
35	CY14B256L-SZ35XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SP35XCT	51-85061	48-pin SSOP	
45	CY14B256L-SZ45XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SP45XCT	51-85061	48-pin SSOP	
45	CY14B256L-SZ45XIT	51-85127	32-pin SOIC	Industrial
	CY14B256L-SP45XIT	51-85061	48-pin SSOP	
	CY14B256L-SZ45XI	51-85127	32-pin SOIC	
	CY14B256L-SP45XI	51-85061	48-pin SSOP	

Package Diagrams

Figure 8. 32-pin (300-Mil) SOIC, 51-85127

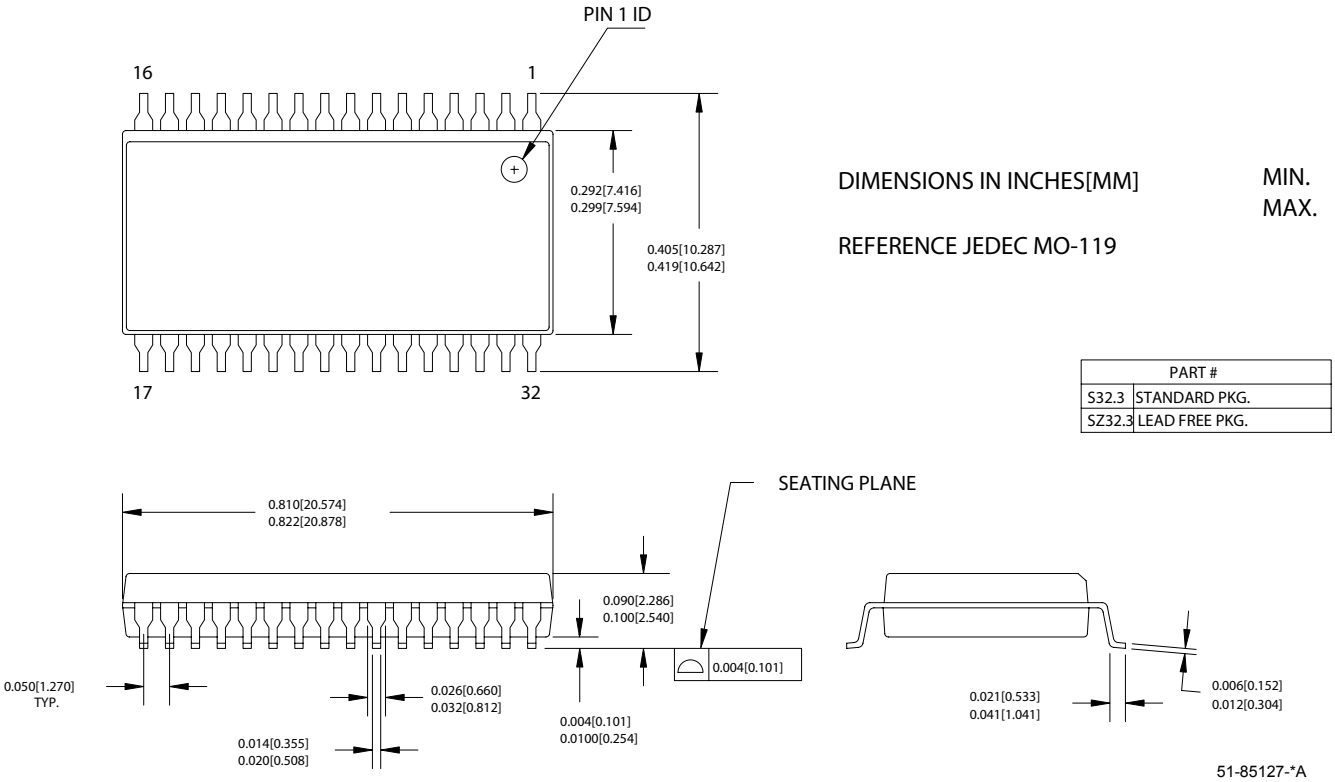
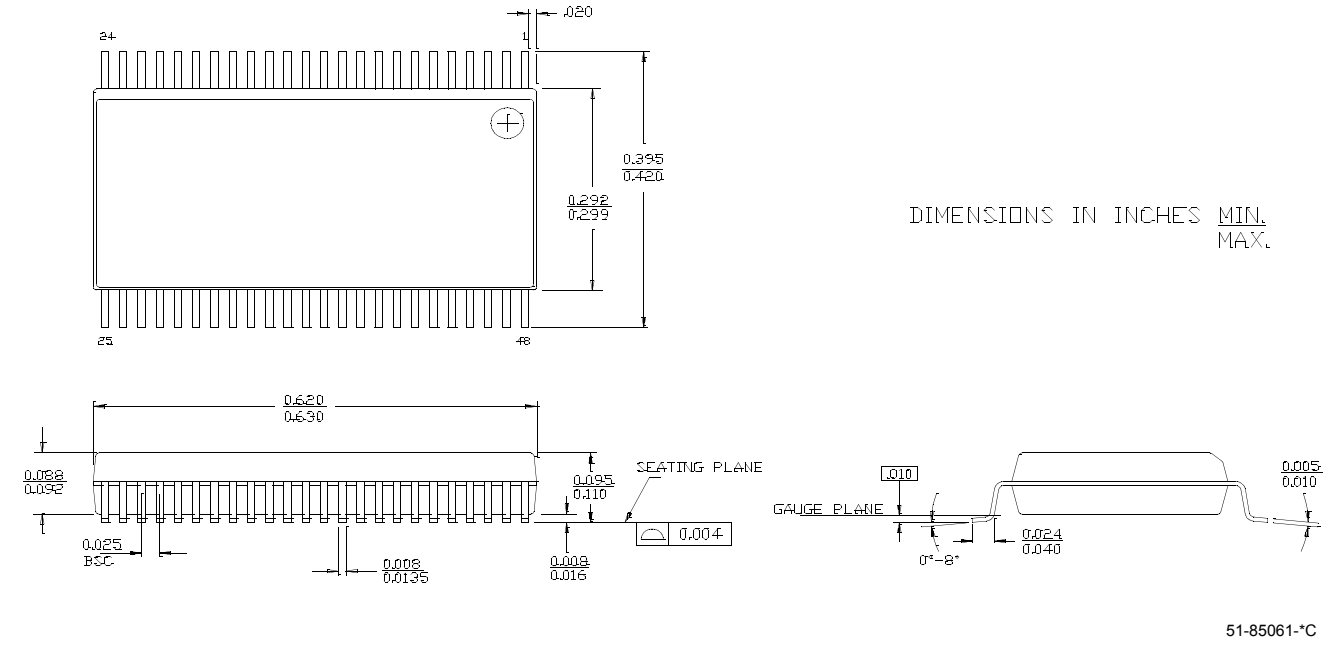


Figure 9. 48-pin Shrunk Small Outline Package, 51-85061



Document History Page

Document Title: CY14B256L, 256-Kbit (32K x 8) nvSRAM Document Number: 001-06422				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	425138	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on External Web
*B	471966	See ECN	TUP	Changed $V_{IH(min)}$ from 2.2V to 2.0V Changed t_{RECALL} from 60 µs to 50 µs Changed Endurance from 1Million Cycles to 500K Cycles Changed Data Retention from 100 Years to 20 Years Added Soft Sequence Processing Time Waveform Updated Part Numbering Nomenclature and Ordering Information
*C	503277	See ECN	PCI	Changed from “Advance” to “Preliminary” Changed the term “Unlimited” to “Infinite” Changed endurance from 500K cycles to 200K cycles Device operation: Tolerance limit changed from + 20% to + 15% in the “Features Section” and “Operating Range Table” Removed Icc_1 values from the DC table for 25 ns and 35 ns industrial grade Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V Added temperature spec. to data retention - 20 years at 55°C Changed the max value of Vcap storage capacitor from 120 µF to 57 µF Updated “Part Nomenclature Table” and “Ordering Information Table”
*D	597004	See ECN	TUP	Removed $V_{SWITCH(min)}$ spec from the AutoStore/Power Up RECALL table Changed t_{GLAX} spec from 20 ns to 1 ns Added $t_{DELAY(max)}$ spec of 70 µs in the Hardware STORE Cycle table Removed t_{HLBL} specification Changed t_{SS} specification form 70 µs (min) to 70 µs (max) Changed $V_{CAP(max)}$ from 57 µF to 120 µF
*E	696097	See ECN	VKN	Added footnote 6 related to $\overline{HSB}$ Changed t_{GLAX} to t_{GHAX}