

## **SWITCHING N-CHANNEL POWER MOS FET**

## DESCRIPTION

The 2SK3900 is N-channel MOS Field Effect Transistor designed for high current switching applications.

### **FEATURES**

- Super low on-state resistance
- $R_{DS(on)1} = 8.0 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 41 \text{ A})$
- $R_{DS(on)2} = 10 \text{ m}\Omega \text{ MAX.}$  (Vgs = 4.5 V, ID = 41 A)
- Low Ciss: Ciss = 3500 pF TYP.
- · Built-in gate protection diode

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	60	V
Gate to Source Voltage (VDs = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±82	А
Drain Current (pulse) Note1	D(pulse)	±246	Α
Total Power Dissipation (Tc = $25^{\circ}$ C)	P <sub>T1</sub>	104	W
Total Power Dissipation ( $T_A = 25^{\circ}C$ )	Рт2	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Energy Note2	Eas	141	mJ
Repetitive Avalanche Current Note3	lar	37.5	Α
Repetitive Avalanche Energy Note3	Ear	141	mJ

#### **Notes 1.** PW $\leq$ 10 $\mu$ s, Duty Cycle $\leq$ 1%

- 2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H
- **3.** RG = 25  $\Omega$ , Tch(peak)  $\leq$  150°C

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#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE		
2SK3900-ZP	TO-263 (MP-25ZP)		





ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 41 A	28.1	56		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 10 V, Id = 41 A		6.3	8.0	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 41 A		7.4	10	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		3500		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		660		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		240		pF
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 41 A		18		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		11		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 0 Ω		62		ns
Fall Time	tr			5.5		ns
Total Gate Charge	QG	V <sub>DD</sub> = 48 V		65.5		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		11.5		nC
Gate to Drain Charge	Qgd	I⊳ = 82 A		16.5		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 82 A, VGS = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	IF = 82 A, VGS = 0 V		41		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		61		nC

Note Pulsed

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

#### **TEST CIRCUIT 2 SWITCHING TIME**

D.U.T.

-///--0

RG

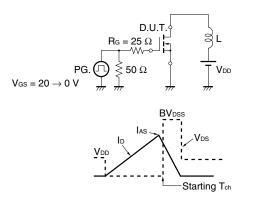
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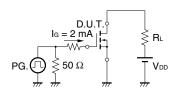
 $\tau = 1 \,\mu s$ Duty Cycle  $\leq 1\%$ 

 $V_{\text{GS}}$ 

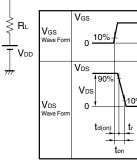
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## **TEST CIRCUIT 3 GATE CHARGE**

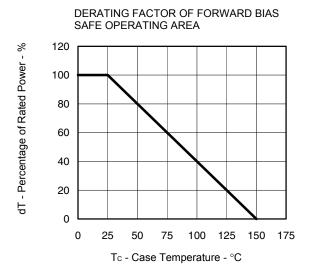


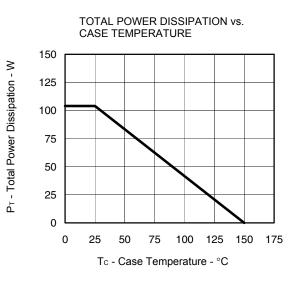




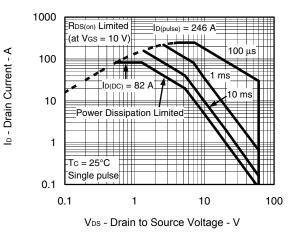
VGS	V <sub>GS</sub>
Wave Form	0 10% V <sub>GS</sub> 90%
VDS Wave Form	$V_{DS} = \frac{10\%}{10\%} \frac{10\%}{10\%} \frac{10\%}{10\%} \frac{10\%}{10\%}$

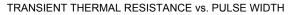
## TYPICAL CHARACTERISTICS ( $T_A = 25^{\circ}C$ )

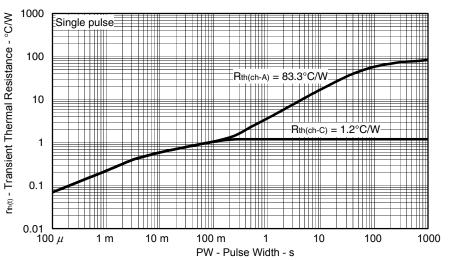


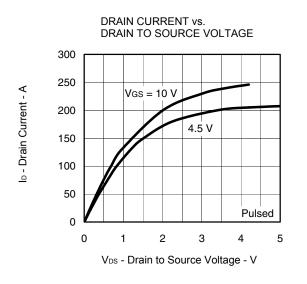


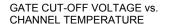
FORWARD BIAS SAFE OPERATING AREA

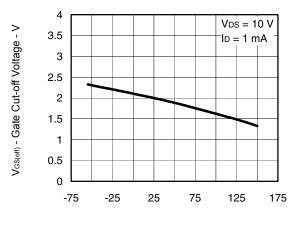




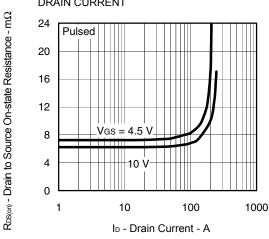


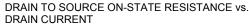




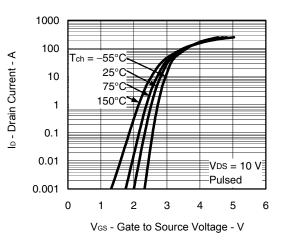


Tch - Channel Temperature - °C

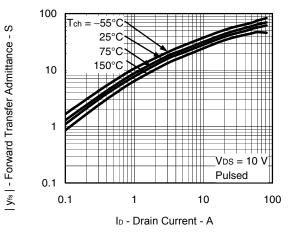




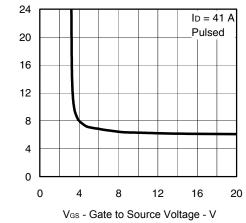
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT







GATE TO SOURCE VOLTAGE

 $R_{\text{DS}(\text{on})}$  - Drain to Source On-state Resistance -  $m\Omega$ 



1000

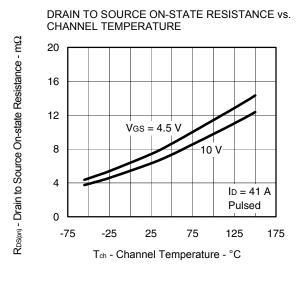
100

10

1

0.1

t<sub>id(on)</sub>, tr, t<sub>d(off)</sub>, tr - Switching Time - ns



SWITCHING CHARACTERISTICS

1

ID - Drain Current - A

VDD = 30 V

VGS = 10

 $R_G = 0 \Omega$ 

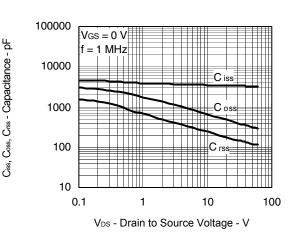
td(off)

tf

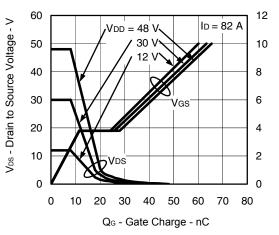
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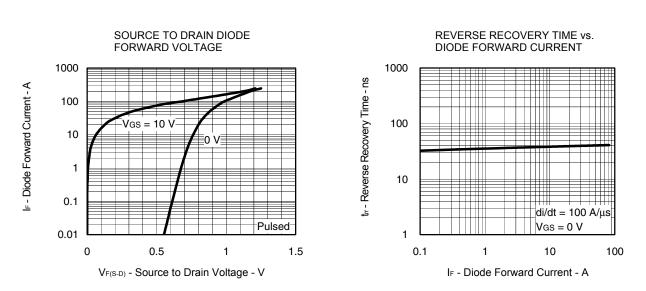
td(on)

100



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

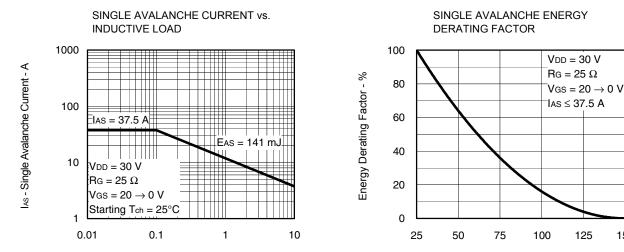




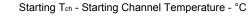
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

V<sub>GS</sub> - Gate to Source Voltage - V

150



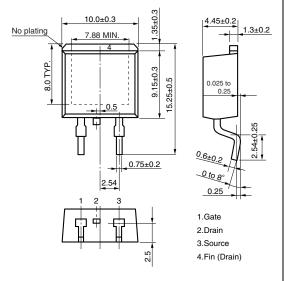
L - Inductive Load - mH



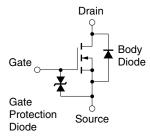
NEC

## PACKAGE DRAWING (Unit: mm)

# TO-263 (MP-25ZP)



## EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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