Philips Components

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ECL Products	

10132
Multiplexer/Latch

Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 44mA**

DESCRIPTION

The 10132 is a Dual 2-Input Multiplexer with Clocked D-type Latches and a Common Reset. The Latch can be clocked by the common Clock (CP) when the Clock Enable input ($\overline{CE}$) is Low or by the Clock Enable input when the common Clock is held in the Low-State. The outputs are latched by the positive transition of the Clock. Any change at the data input will be registered at the output only if the Clock is Low.

Data inputs are selected by a common data Select (S). All unused inputs must be tied Low to V_{IL} or V_{EE}.

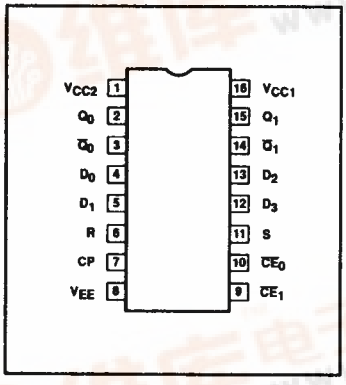
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10132N
16–Pin Ceramic DIP	10132F

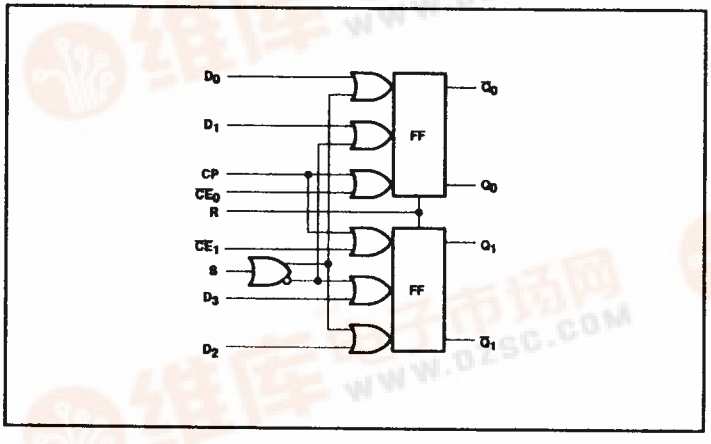
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S	Data Select Input
R	Reset Input
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



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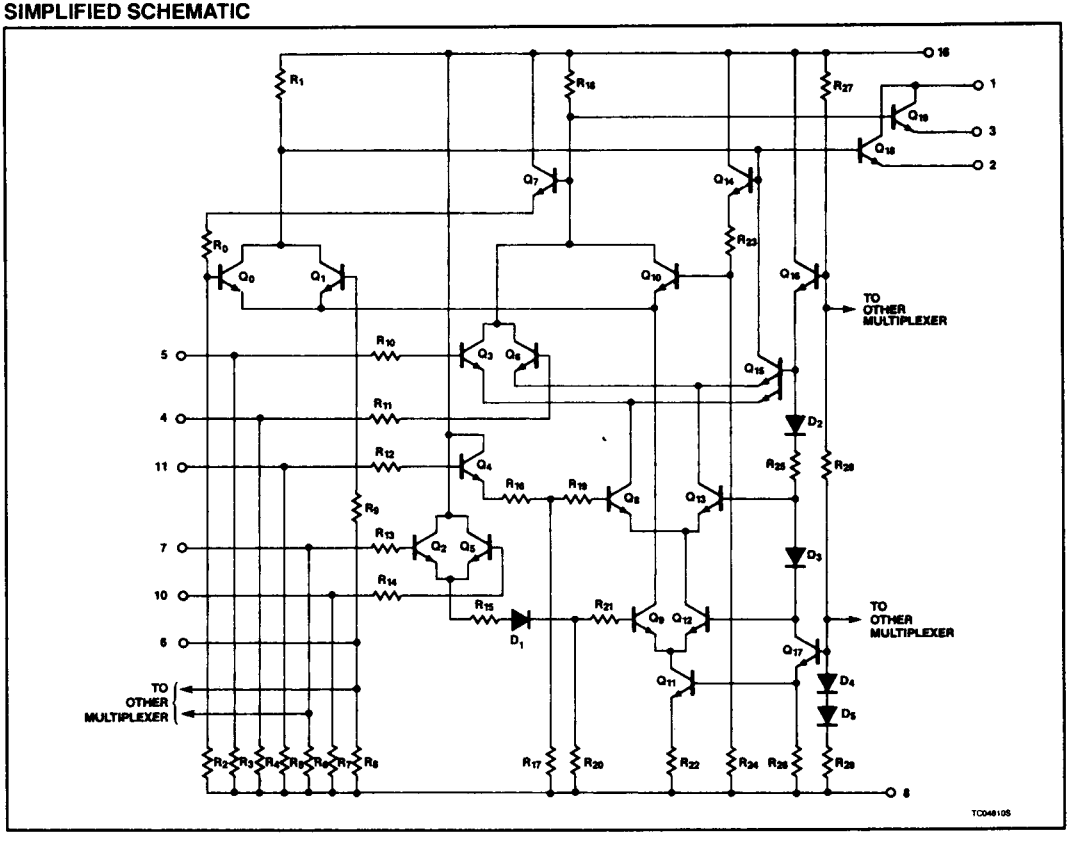
SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS				OUTPUT
R	S	CP*	$\overline{CE}$*	Q_{n+1}
L	L	L	L	D_0
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	D_1
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	X	X	H	L
H	X	H	X	L
H	X	L	L	Q_n

* Conditions for CP and $\overline{CE}$ may be interchanged as indicated in the function table.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to D_0 input with	−1060		−890	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$	−960		−810	mV
			$T_A = +85°C$	outputs, apply V_{ILMIN} to all inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to D_0 input with	−1080			mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to D_0 input with	−980			mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to D_0 input with			−1655	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to D_0 input with			−1630	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to all inputs. For	−1890		−1675	mV
			$T_A = +25°C$	$\overline{Q}_n$ outputs, apply V_{IHMAX} to D_0 input with	−1850		−1650	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to D_0 input with V_{ILMIN} applied to all			460	µA
			$T_A = +25°C$	other inputs. Apply V_{IHMAX} to D_1 input and S input			290	µA
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			290	µA
		R input	$T_A = -30°C$	Apply V_{IHMAX} to CP and R			620	µA
			$T_A = +25°C$	inputs with V_{ILMIN} applied			390	µA
			$T_A = +85°C$	to all other inputs.			390	µA
		CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied			290	µA
			$T_A = +85°C$	to all other inputs.			290	µA
		S, $\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to S or $\overline{CE}_n$ input			425	µA
			$T_A = +25°C$	under test, one at a time, with			265	µA
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.			265	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				60	mA
			$T_A = +25°C$			44	55	mA
			$T_A = +85°C$				60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1, 2	1.00 1.00	3.60 3.60	1.00 1.00	3.00 3.00	3.30 3.30	1.00 1.00	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay R to Q_n, $\overline{Q}_n$		1.00 1.00	4.00 4.00	1.00 1.00		3.80 3.80	1.00 1.00	4.20 4.20	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$		1.00 1.00	6.00 6.00	1.00 1.00		5.70 5.70	1.00 1.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n, $\overline{Q}_n$		1.00 1.00	4.80 4.80	1.00 1.00		4.60 4.60	1.00 1.00	5.00 5.00	ns ns
t_s	Setup time D_n to CP		2.50		2.50			2.50		ns
t_h	Hold time D_n to CP		1.50		1.50			1.50		ns
t_s	Setup time S to CP		3.50		3.50			3.50		ns
t_h	Hold time S to CP		1.00		1.00			1.00		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.50 1.50	3.70 3.70	1.50 1.50		3.50 3.50	1.50 1.50	3.80 3.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

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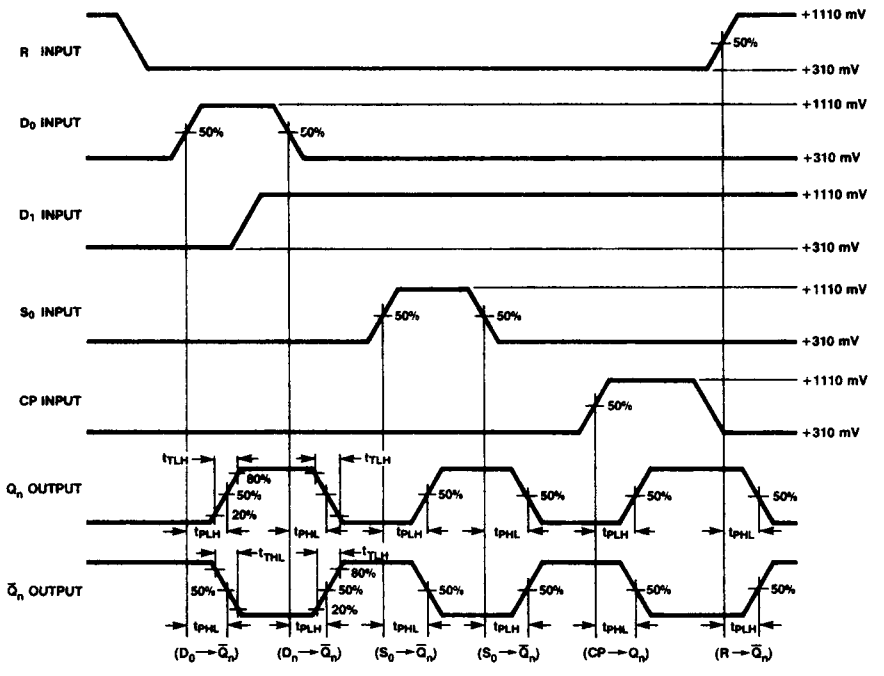
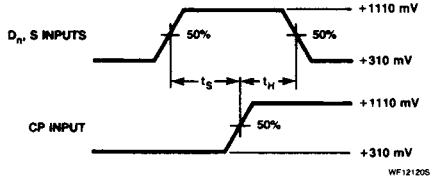
AC WAVEFORMS



NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

Waveform 1. Propagation Delay and Transition Times



NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

Waveform 2. Setup and Hold Times