NEC

MOS INTEGRATED CIRCUIT

μPD720130

USB2.0 to IDE Bridge

The μPD720130 is designed to perform a bridge between USB 2.0 and ATA/ATAPI. The μPD720130 complies with the Universal Serial Bus Specification Revision 2.0 full-/high-speed signaling and works up to 480 Mbps. The μPD720130 is integrated CISC processor, ATA/ATAPI controller, endpoint controller (EPC), serial interface engine (SIE), and USB2.0 transceiver into a single chip. The USB2.0 protocol and class specific protocol (bulk only protocol) are handled by USB2.0 transceiver, SIE, and EPC. And the transport layer is performed by V30MZ CISC processor which is in the μPD720130. The software to control the μPD720130 is located in an embedded ROM. In the future, the μPD720130 will be released to support external Flash Memory / EEPROM™ option to update function by firmware.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD720130 User's Manual: S16412E

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
- Compliant with ATA/ATAPI-6 (LBA48, PIO Mode 0-4, Multi Word DMA Mode 0-2, Ultra DMA Mode 0-4)
- USB2.0 high-speed bus powered device capability
- Certified by USB implementers forum and granted with USB 2.0 high-speed Logo (TID :40320125)
- One USB2.0 high-speed transceiver / receiver with full-speed transceiver / receiver
- USB2.0 High-speed or Full-speed packet protocol sequencer (Serial Interface Engine)
- Automatic chirp assertion and full-/high-speed mode change
- USB Reset, Suspend and Resume signaling detection
- Supports power control functionality for IDE device as CD-ROM and HDD
- Supports set feature (TEST_MODE) functionality
- System Clock is generated by 30 MHz X'tal
- 2.5 V and 3.3 V power supply

ORDERING INFORMATION

	Part Number	Package
	μPD720130GC-9EU	100-pin plastic TQFP (fine pitch) (14 × 14)
★	μPD720130GC-9EU-SIN	100-pin plastic TQFP (fine pitch) (14 × 14)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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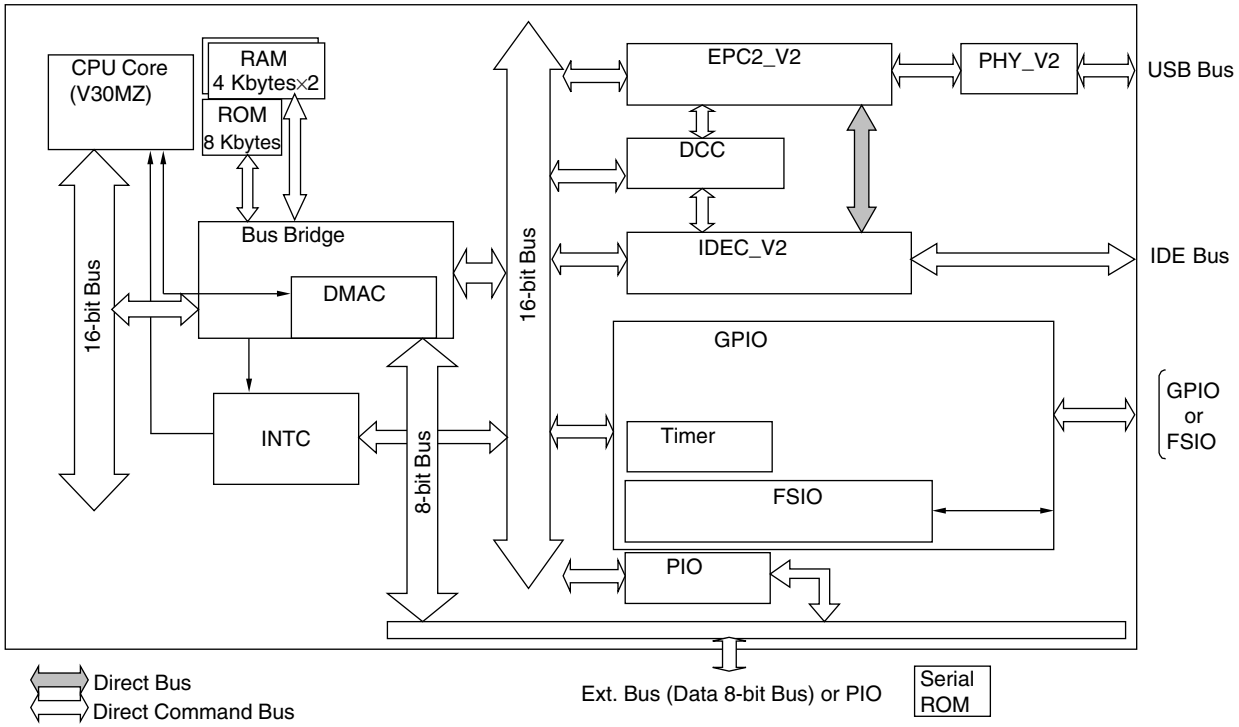
The mark ★ shows major revised points.

BLOCK DIAGRAM



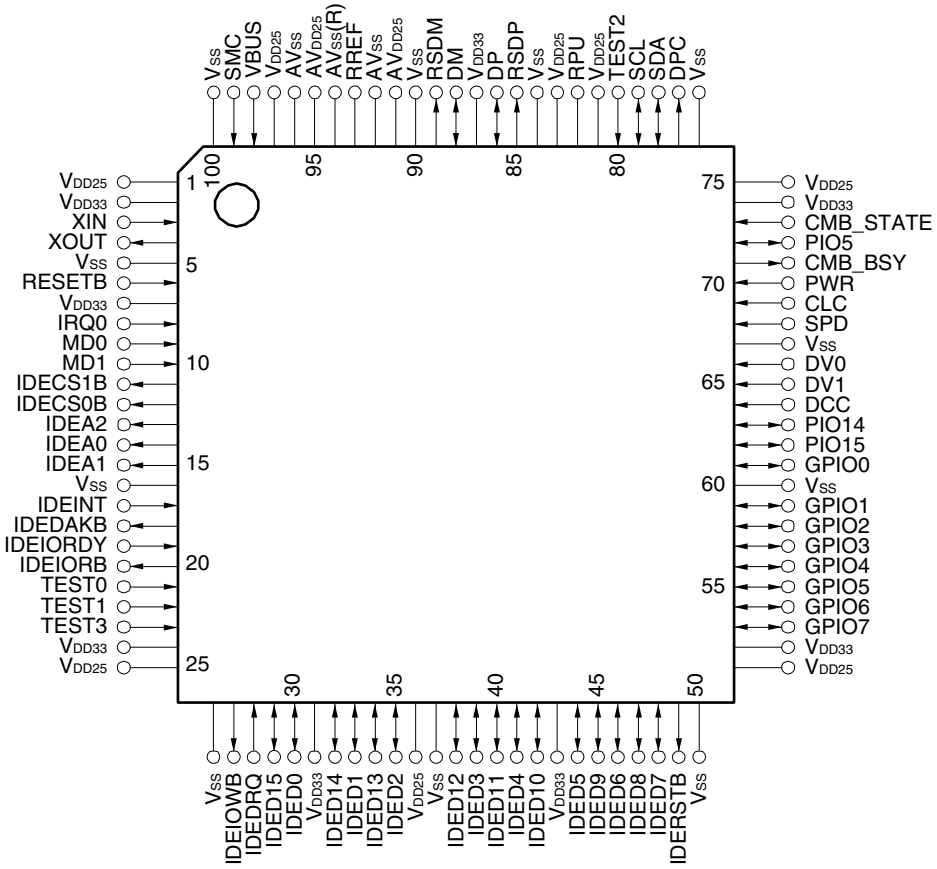
V30MZ	: CISC CPU core
RAM	: 8-Kbyte work RAM for firmware
ROM	: 8-Kbyte ROM for built-in firmware
PHY_V2	: USB2.0 transceiver with serial interface engine
EPC_V2	: Endpoint controller
IDEC_V2	: IDE controller
DCC	: ATA direct command controller
Bus Bridge	: Internal / external bus controller and DMA controller
INTC	: Interrupt controller (82C59 like)
GPIO	: General purpose 8-bit I/O controller
PIO	: Multipurpose 14-bit I/O controller
FSIO	: Flexible serial I/O

PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic TQFP (fine pitch) (14 × 14)**

μPD720130GC-9EU

★ μPD720130GC-9EU-SIN



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD25}	26	V_{SS}	51	V_{DD25}	76	V_{SS}
2	V_{DD33}	27	IDEIOWB	52	V_{DD33}	77	DPC
3	XIN	28	IDEDRQ	53	GPIO7	78	SDA
4	XOUT	29	IDED15	54	GPIO6	79	SCL
5	V_{SS}	30	IDED0	55	GPIO5	80	TEST2
6	RESETB	31	V_{DD33}	56	GPIO4	81	V_{DD25}
7	V_{DD33}	32	IDED14	57	GPIO3	82	RPU
8	IRQ0	33	IDED1	58	GPIO2	83	V_{DD25}
9	MD0	34	IDED13	59	GPIO1	84	V_{SS}
10	MD1	35	IDED2	60	V_{SS}	85	RSDP
11	IDECS1B	36	V_{DD25}	61	GPIO0	86	DP
12	IDECS0B	37	V_{SS}	62	PIO15	87	V_{DD33}
13	IDEA2	38	IDED12	63	PIO14	88	DM
14	IDEA0	39	IDED3	64	DCC	89	RSDM
15	IDEA1	40	IDED11	65	DV1	90	V_{SS}
16	V_{SS}	41	IDED4	66	DV0	91	AV_{DD25}
17	IDEINT	42	IDED10	67	V_{SS}	92	AV_{SS}
18	IDEDAKB	43	V_{DD33}	68	SPD	93	RREF
19	IDEIORDY	44	IDED5	69	CLC	94	AV_{SS}(R)
20	IDEIORB	45	IDED9	70	PWR	95	AV_{DD25}
21	TEST0	46	IDED6	71	CMB_BSY	96	AV_{SS}
22	TEST1	47	IDED8	72	PIO5	97	V_{DD25}
23	TEST3	48	IDED7	73	CMB_STATE	98	VBUS
24	V_{DD33}	49	IDERSTB	74	V_{DD33}	99	SMC
25	V_{DD25}	50	V_{SS}	75	V_{DD25}	100	V_{SS}

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

(1/2)

Pin Name	I/O	Buffer Type	Active Level	Function
XIN	I	2.5 V Input		System clock input or oscillator In
XOUT	O	2.5 V Output		Oscillator out
RESETB	I	3.3 V Schmitt Input	Low	Asynchronous reset signaling
MD(1:0)	I	3.3 V Input		Function mode setting
IDECS(1:0)B	O (I/O)	5 V tolerant Output	Low	IDE host chip select
IDEA(2:0)	O (I/O)	5 V tolerant Output		IDE address bus
IDEINT	I (I/O)	5 V tolerant Input	High	IDE interrupt request from device to host
IDEDAKB	O (I/O)	5 V tolerant Output	Low	IDE DMA acknowledge
IDEIORDY	I (I/O)	5 V tolerant Input	High	IDE IO channel ready
IDEIORB	O (I/O)	5 V tolerant Output	Low	IDE IO read strobe
IDEIOWB	O (I/O)	5 V tolerant Output	Low	IDE IO write strobe
IDEDRQ	I (I/O)	5 V tolerant Input	High	IDE DMA request from device to host
IDED(15:0)	I/O	5 V tolerant I/O		IDE data bus
IDERSTB	O (I/O)	5 V tolerant Output	Low	IDE reset from host to device
DCC	I (I/O)	3.3 V Input		IDE controller operational mode setting
DV(1:0)	I (I/O)	3.3 V Input		Device select
CLC	I (I/O)	3.3 V Input		System clock setting
PWR	I (I/O)	3.3 V Input		Bus powered /self-powered select
CMB_BSY	O (I/O)	3.3 V Output		Combo IDE bus busy
CMB_STATE	I (I/O)	3.3 V Input		Combo IDE bus state
DPC	O (I/O)	3.3 V Output		Power control signaling for IDE device
SDA	I/O	3.3 V I/O		Serial ROM data signaling
SCL	I/O	3.3 V I/O		Serial ROM clock signaling
VBUS	I	5 V Schmitt Input [Note]		VBUS monitoring
DP	I/O	USB high speed D+ I/O		USB's high speed D+ signal
DM	I/O	USB high speed D– I/O		USB's high speed D– signal
RSDP	O	USB full speed D+ Output		USB's full speed D+ signal
RSDM	O	USB full speed D– Output		USB's full speed D– signal
RPU	A	USB Pull-up control		USB's 1.5 kΩ pull-up resistor control
RREF	A	Analog		Reference resistor
SPD	I (I/O)	3.3 V Input		NEC private
SMC	I	3.3 V Input		Scan mode control
TEST(3:0)	I	3.3 V Input		Test mode setting

Note VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. System must ensure that the input voltage level for VBUS pin is less than 3.0 V due to the absolute maximum rating is not exceeded.

(2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
GPIO(7:0)	I/O	3.3 V Schmitt I/O		General purpose IO port (for future extension)
PIO(15:14)	I/O	3.3 V I/O		IO port (for future extension)
PIO(5)	I/O	3.3 V Schmitt I/O		IO port (for future extension)
IRQ0	I	3.3 V Schmitt Input	High	External interrupt input (for future extension)
AV_{DD25}				2.5 V V_{DD} for Analog circuit
V_{DD25}				2.5 V V_{DD}
V_{DD33}				3.3 V V_{DD}
AV_{SS}				V_{SS} for Analog circuit
V_{SS}				V_{SS}

Remarks 1. “5 V tolerant“ means that the buffer is 3.3 V buffer with 5 V tolerant circuit.

2. The signal marked as “(I/O)” in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

2. FUNCTION INFORMATION

USB to IDE system can be realized by the μPD720130, Serial ROM which has USB vender ID, product ID, etc, and power control circuit. The μPD720130 can be selected bus powered mode or self powered mode. If all power consumption for USB to IDE system is less than the specification of bus powered device, it will be possible to realize high-speed capable bus powered system. The μPD720130 has some features for bus powered system. Also, some system may control target IDE device by two IDE controllers. At the time, IDE bus arbitration should be required to each IDE controller. The μPD720130 has a feature of IDE bus arbitration, too.

The setting of IDE controller in the μPD720130 is controlled by data in serial ROM or external pin setting. If there is any inconsistency between data in serial ROM and external pin setting, the data in serial ROM is higher priority than external pin setting.

2.1 Data in Serial ROM

The μPD720130 loads some data such as Vendor ID, Product ID and some additional USB related information, etc from serial ROM when the μPD720130 is initialized. Example of data in serial ROM is as follows. ExPinReset and ExPinSet fields hold data which is related to the external pin setting.

Table 2-1. Data in Serial ROM

Data size	Symbol	Description
1 Word	Flags	Control for descriptor overwrite
1 Byte	ExPinReset	PWR, CLC, DCC, DV[1:0] Reset bit map field
1 Byte	ExPinSet	PWR, CLC, DCC, DV[1:0] Set bit map field
1 Word	idVendor	idVendor field in Device descriptor
1 Word	idProduct	idProduct field in Device descriptor
1 Word	bcdDevice	bcdDevice field in Device descriptor
1 Byte	MaxPower BUS	MaxPower field in Configuration descriptor for Bus powered mode
1 Byte	MaxPower Self	MaxPower field in Configuration descriptor for Self powered mode
1 Byte	bInterfaceClass	bInterfaceClass field in Interface descriptor
1 Byte	bInterfaceSubClass	bInterfaceSubClass field in Interface descriptor
1 Byte	bInterfaceProtocol	bInterfaceProtocol field in Interface descriptor
1 Word	TxMode Reset	IDE transmission type such as Ultra DMA 66 Reset bit map field
1 Word	TxMode Set	IDE transmission type such as Ultra DMA 66 Set bit map field
32 Bytes	ManufactureString	String descriptor for Manufacturer
32 Bytes	ProductString	String descriptor for Product
32 Bytes	SerialString	String descriptor for Device serial number

2.2 External Pin Setting

Usually, serial ROM should be used to keep Vendor ID, Product ID and some additional USB related information. And then, the external pin setting of the μPD720130 is not so important to realize USB to IDE bridge system. The recommended external pin setting is as follows.

Table 2-2. Recommended External Pin Setting

Pin Name	Setting
MD1	1
MD0	0
SCL	Pull Up Note 1
SDA	Pull Up
DV1	"L" clamp
DV0	"L" clamp
CLC	"L" clamp
PWR	"L" clamp
DCC	Pull Down Note 2
GPIO(7:0)	"L" clamp
PIO(14:15)	"L" clamp
PIO5	"L" clamp
SPD	"H" clamp
TEST(3:0)	"L" clamp
SMC	"L" clamp
IRQ0	"L" clamp

Notes 1. If serial ROM size is more than 2 Kbytes, SCL should be pull down.

2. If target IDE device is not fixed, it is preferable that DCC pin can switch pull-up or pull-down.

The setting for any other pins such as CMB_BSY, CMB_STATE depends on USB2.0 to IDE Bridge system. For example, if two IDE controllers control one target IDE device and one of two IDE controllers is the μPD720130, CMB_BSY and CMB_STATE are used to handshake between two IDE controller chips. On the other hand, when the μPD720130 is only controller of target IDE device, CMB_BSY should be opened and CMB_STATE should be clamped to "L".

2.3 Control Bit in Serial ROM or External Pin Setting

The following tables show IDE status and control bit in serial ROM or external pin setting.

Table 2-3. DV1/DV0, CLC, PWR Setting

No.	Device Power	Internal Clock	ATA/ATAPI	Setting in Serial ROM or External Pin			
				PWR	CLC	DV1	DV0
0	Bus Powered	7.5 MHz	No device connected	1	1	1	1
1			ATA	1	1	1	0
2			ATAPI	1	1	0	1
3			Reserved	1	1	0	0
4		60 MHz	No device connected	1	0	1	1
5			ATA	1	0	1	0
6			ATAPI	1	0	0	1
7			Reserved	1	0	0	0
8	Self Powered	60 MHz	No device connected	0	1	1	1
9			Combo (ATA)	0	1	1	0
10			Combo (ATAPI)	0	1	0	1
11			Reserved	0	1	0	0
12			No device connected	0	0	1	1
13			ATA	0	0	1	0
14			ATAPI	0	0	0	1
15			Auto device detect	0	0	0	0

Remark Setting No. 0, 3, 4, 7, 8, 11, and 12 are prohibited to use.

Table 2-4. DV1/DV0, DCC Setting

Condition				DCC Pin Setting	DCC Setting in Serial ROM	Description
DV1	DV0	Mode	Target Device			
1	0	ATA	ATA	0	No setting	Ultra, Multi Word DMA are disabled
				0	Reset	Ultra, Multi Word DMA are disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra, Multi Word DMA are disabled
				1	Set	Ultra, Multi Word DMA are enabled.
0	1	ATAPI	ATAPI	0	No setting	Ultra DMA is disabled
				0	Reset	Ultra DMA is disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra DMA is disabled
				1	Set	Ultra, Multi Word DMA are enabled.
0	0	Auto device detect	ATA	0	No setting	Ultra, Multi Word DMA are disabled
				0	Reset	Ultra, Multi Word DMA are disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra, Multi Word DMA are disabled
				1	Set	Ultra, Multi Word DMA are enabled.
			ATAPI	0	No setting	Ultra DMA is disabled
				0	Reset	Ultra DMA is disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra DMA is disabled
				1	Set	Ultra, Multi Word DMA are enabled.

Remark PIO mode 0-4 are always enabled.

2.4 Combo Mode Function

The μPD720130 can be used to realize that two IDE controller chips control one target IDE device in one system. To realize IDE bus arbitration between two IDE controller chips, the μPD720130 has CMB_BSY and CMB_STATE. Combo mode is enabled when PWR = 0 and CLC = 1.

CMB_BSY and CMB_STATE connect to other IDE controller chip as follows.

Figure 2-1. CMB_BSY and CMB_STATE Connection between Two IDE Controller Chips

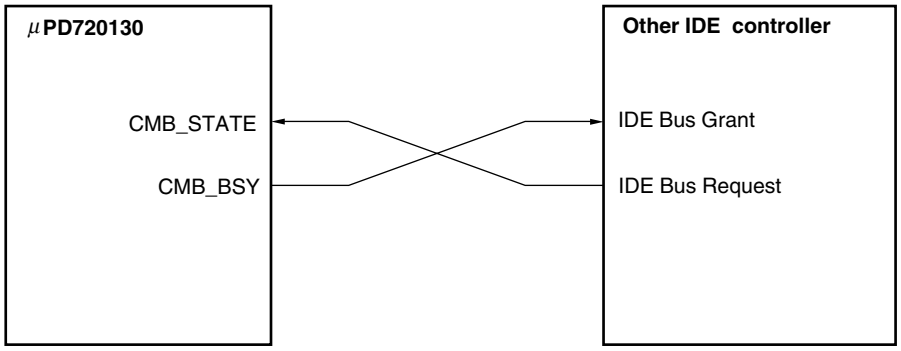
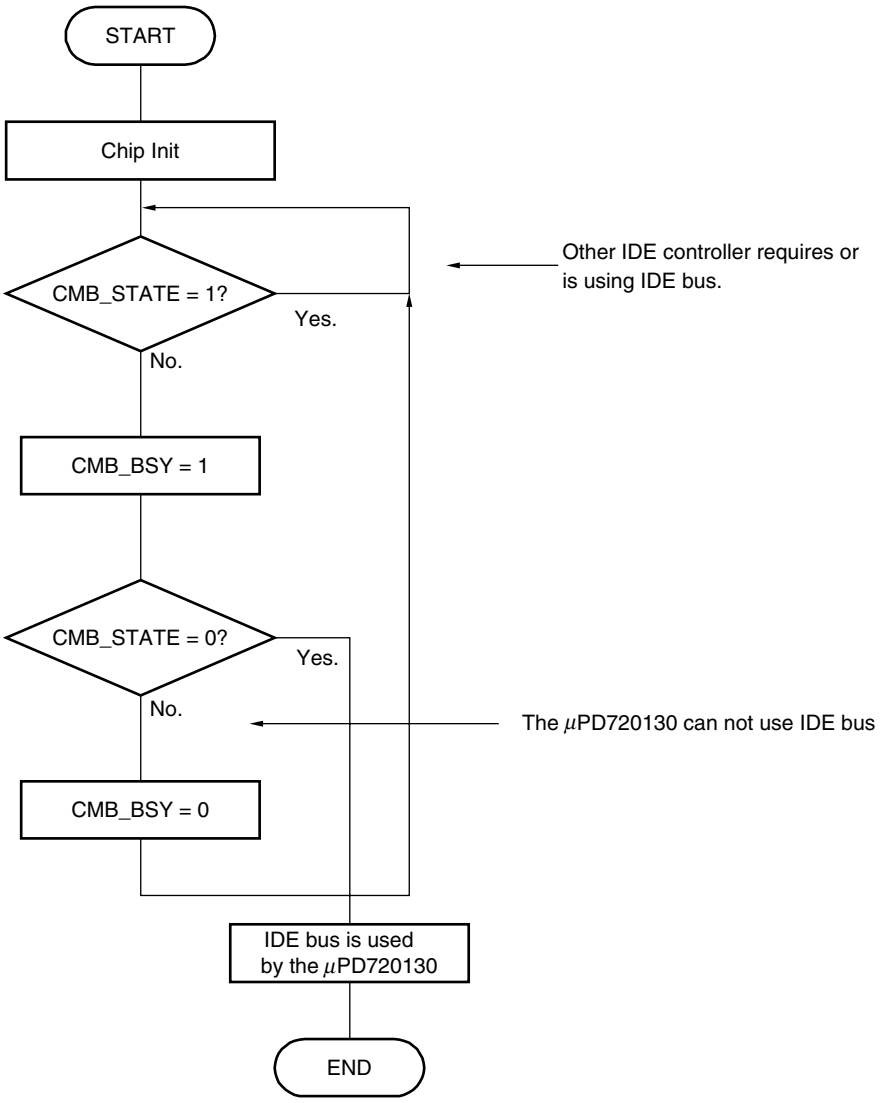


Table 2-5. Description of CMB_BSY and CMB_STATE

Pin Name	Direction	Value	Description
CMB_STATE	IN	0	Other IDE controller does not require or does not use IDE bus.
		1	Other IDE controller requires or is using IDE bus.
CMB_BSY	OUT	0	The μPD720130 does not require or does not use IDE bus.
		1	The μPD720130 requires or is using IDE bus.

The IDE bus arbitration will be done by following sequence. The μPD720130 will confirm whether other IDE controller requires or is using IDE bus or not. If other IDE controller does not require or does not use IDE bus, the μPD720130 will use IDE bus.

Figure 2-2. IDE Bus Arbitration Sequence

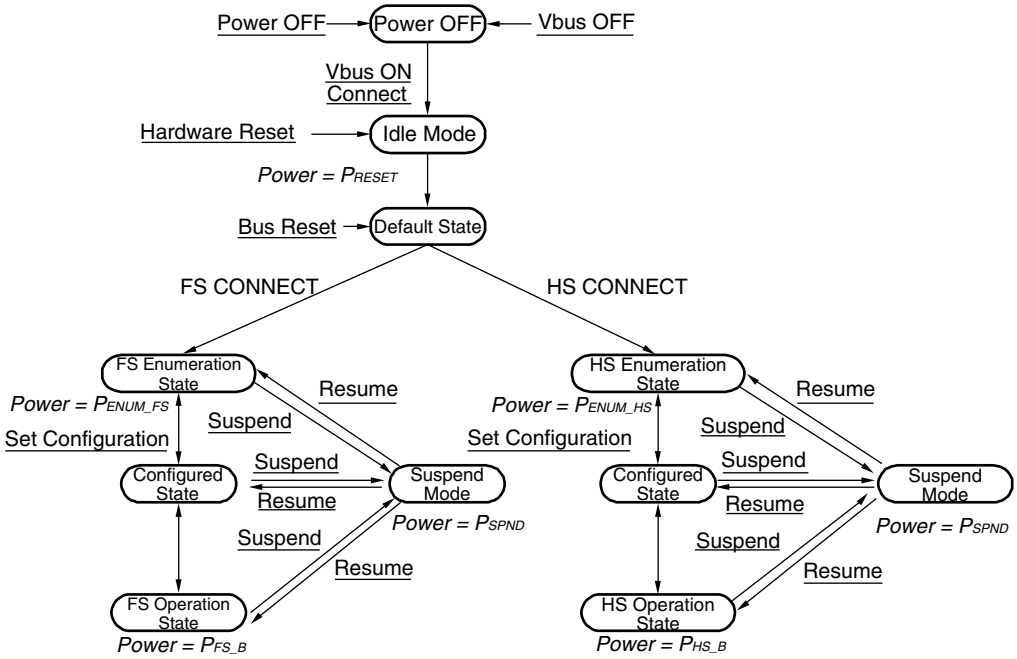


2.5 Power Control

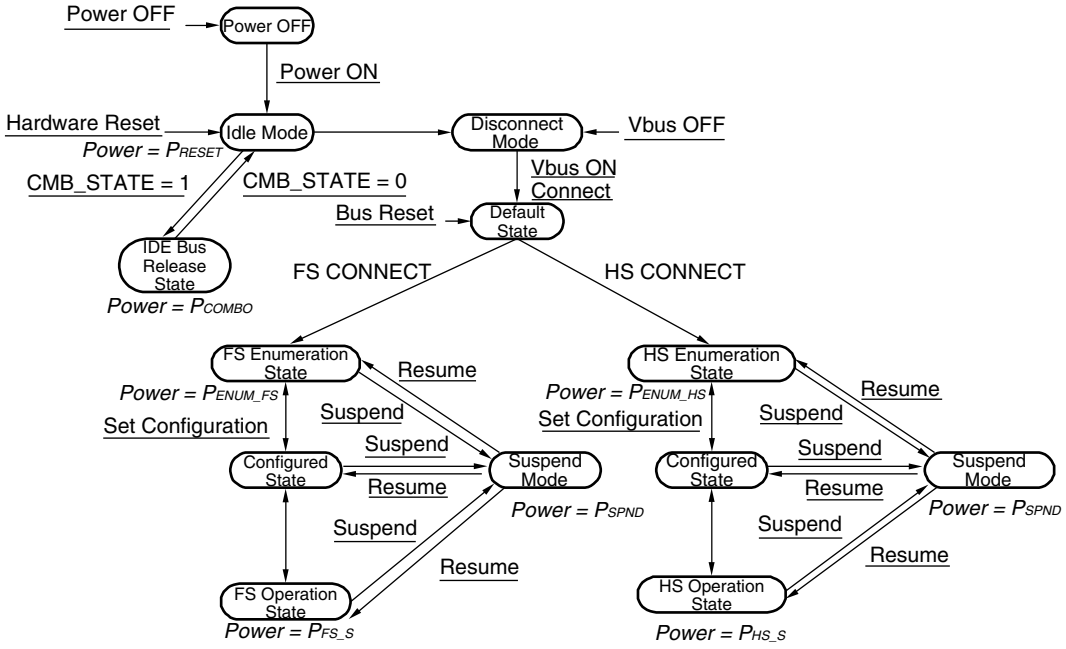
To realize bus-powered or high performance self-powered USB2.0 to IDE Bridge system, the μPD720130 has two internal system clock mode. One is 7.5 MHz for bus-powered mode and the other is 60 MHz for self-powered mode. The μPD720130 controls the power state by events as follows. The word with under line shows event. The Italic word shows the power state.

Figure 2-3. Power State Control

(a) Bus-powered Mode

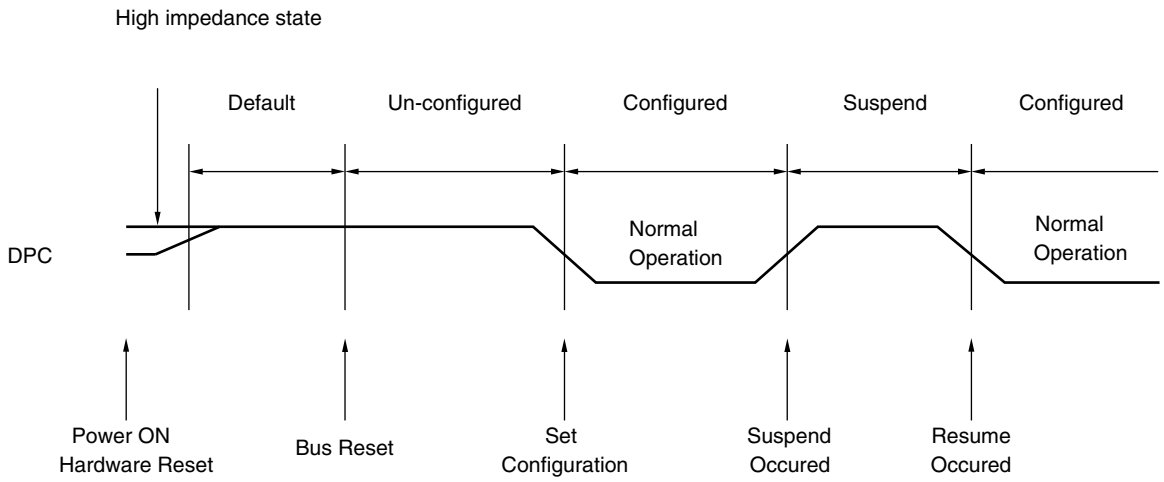


(b) Self-powered Mode



To realize bus-powered USB2.0 to IDE Bridge system, the power consumption for IDE device should be controlled by the power state of the μPD720130. The μPD720130 has DPC pin to control IDE device's power circuit. DPC pin's output level relates to USB device states. DPC should be pull up to 3.3 V because DPC output becomes high impedance state until the μPD720130 is initialized.

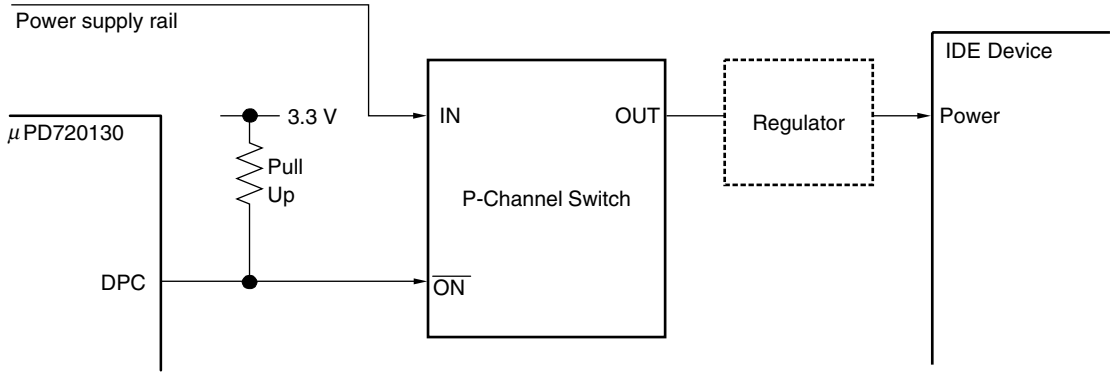
Figure 2-4. DPC Pin to Control IDE Device's Power Circuit



Following reference circuit can cut off power supply to IDE device during the μPD720130 is under default and un-configured state. Also, the power supply to IDE device is disabled during suspend state, too.

Power consumption of total system under default, un-configured, and suspend state can be reduced by DPC pin.

Figure 2-5. Power Control Circuit Example



3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 2.5 V oscillator interface
  XIN, XOUT
- 3.3 V input buffer
  MD(1:0), TEST(3:0), SMC
- 3.3 V schmitt input buffer
  RESETB, IRQ0
- 3.3 V input buffer with enable (OR type)
  DCC, DV(1:0), SPD, CLC, PWR, CMB_STATE
- 3.3 V I_{OL} = 6 mA 3-state output buffer
  CMB_BSY, DPC
- 3.3 V I_{OL} = 3 mA bi-directional schmitt buffer with input enable (OR-type)
  GPIO(7:0), PIO5, SDA, SCL
- 3.3 V I_{OL} = 6 mA bi-directional buffer with input enable (OR-type)
  PIO(15:14)
- 5 V schmitt input buffer
  VBUS
- 5 V I_{OL} = 6 mA 3-state output buffer
  IDECS(1:0)B, IDEA(2:0), IDEDAKB, IDEIORB, IDEIOWB, IDERSTB
- 5 V I_{OL} = 6 mA bi-directional buffer with input enable (OR-type)
  IDED(15:0), IDEINT, IDEIORDY, IDEDRQ
- USB interface
  DP, DM, RSDP, RSDM, RREF, RPU

Remark Above, “5 V” refers to a 3.3 V buffer with 5-V tolerant circuit. Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3.3 V, which is the V_{DD33} voltage.

3.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “Max.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresys voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input pins. Input rise time is transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input fall time to input pins. Input fall time is transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

3.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}	3.3 V power supply rail	–0.5 to +4.6	V
	V_{DD25}	2.5 V power supply rail	–0.5 to +3.6	V
Input voltage, 5 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Input voltage, 3.3 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Input voltage, 2.5 V buffer	V_I	2.3 V ≤ V_{DD25} ≤ 2.7 V V_I < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output voltage, 5 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Output voltage, 3.3 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Output voltage, 2.5 V buffer	V_O	2.3 V ≤ V_{DD25} ≤ 2.7 V V_O < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output current, 5 V buffer	I_O	I_{OL} = 6 mA	20	mA
Output current, 3.3 V buffer	I_O	I_{OL} = 6 mA	20	mA
		I_{OL} = 3 mA	10	mA
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Two Power Supply Rails Limitation

The μPD720130 has two power supply rails (2.5 V, 3.3 V). The system will require the time when power supply rail is stable at V_{DD} level. And, there will be difference between the time of V_{DD25} and V_{DD33}. The μPD720130 requires that V_{DD25} should be stable before V_{DD33} becomes stable. At this case, the system must ensure that the absolute maximum ratings for V_I / V_O are not exceeded. System reset signaling should be asserted more than specified time after both V_{DD25} and V_{DD33} are stable.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD33}	3.3 V for V_{DD33} pins	3.0	3.3	3.6	V
	V_{DD25}	2.5 V for V_{DD25} pins	2.3	2.5	2.7	V
	V_{DD25}	2.5 V for AV_{DD25} pins	2.3	2.5	2.7	V
High-level input voltage	V_{IH}					
5.0 V high-level input voltage			2.0		5.5	V
3.3 V high-level input voltage			2.0		V_{DD33}	V
2.5 V high-level input voltage			1.7		V_{DD25}	V
Low-level input voltage	V_{IL}					
5.0 V low-level input voltage			0		0.8	V
3.3 V low-level input voltage			0		0.8	V
2.5 V low-level input voltage			0		0.7	V
Hysteresis voltage	V_H					
5 V hysteresis voltage			0.3		1.5	V
3.3 V hysteresis voltage			0.2		1.0	V
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

DC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

Control Pin Block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD33}, V_{DD25}$ or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note			–250	mA
Low-level output current	I_{OL}				
5.0 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	3.0		mA
High-level output current	I_{OH}				
5.0 V high-level output current		V_{OH} = 2.4 V	–2.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	–6.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	–3.0		mA
Input leakage current	I_I				
3.3 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA
5.0 V buffer		$V_I = V_{DD}$ or V_{SS}		±10	μA

Note The output short circuit time is one second or less and is only for one pin on the LSI.

USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Serial Resistor between DP (DM) and RSDP (RSDM)	R_S		38.61	39.39	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}	1.5 kΩ ±5% consists of resistance of transistor and pull-up resistor	1.485	1.515	Ω
Termination voltage for upstream facing port pull-up	V_{TERM}		3.0	3.6	V
Input Levels for Full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	$\lvert(D+) - (D-)\rvert$	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to V_{SS}	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling level	See **Figure 3-4**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10.0	+10.0	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10.0	+10.0	mV
Chirp J level (differential signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (differential signal)	V_{CHIRPK}		−900	−500	mV

Figure 3-1. Differential Input Sensitivity Range for Low-/full-speed

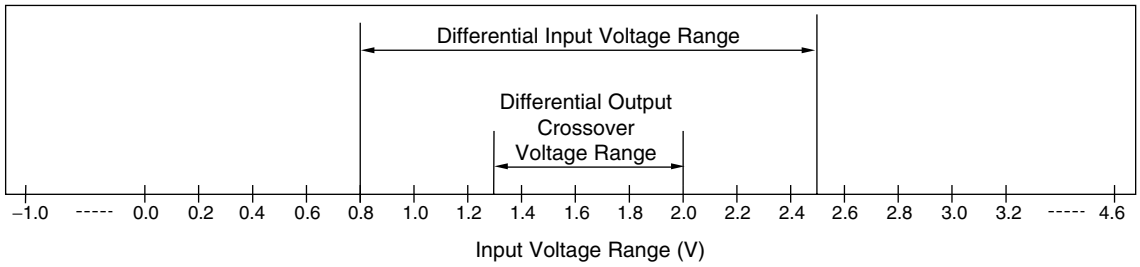


Figure 3-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

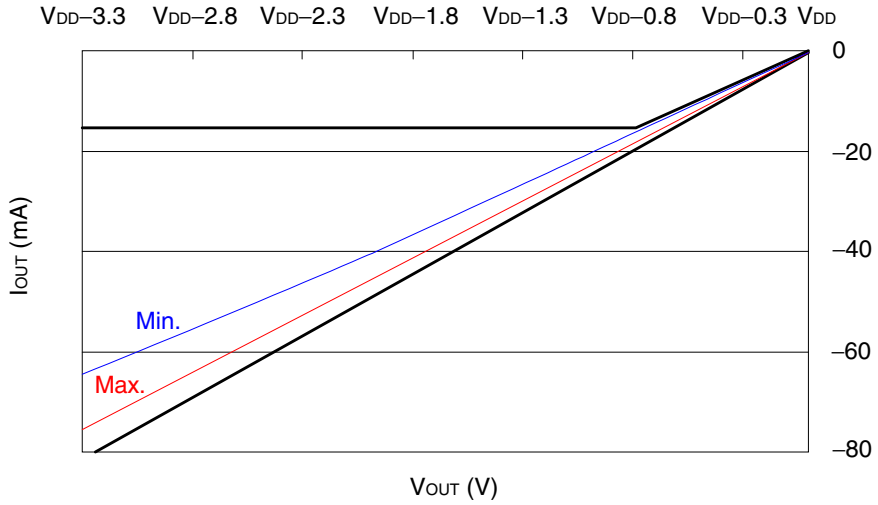


Figure 3-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

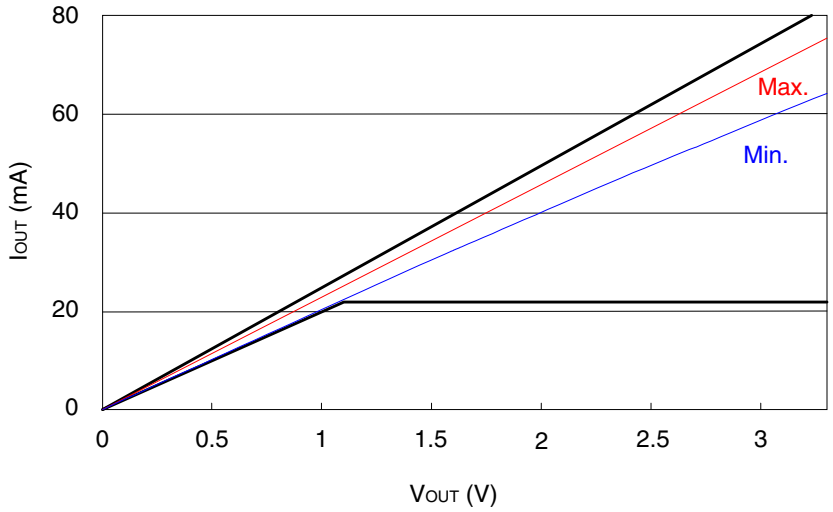


Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

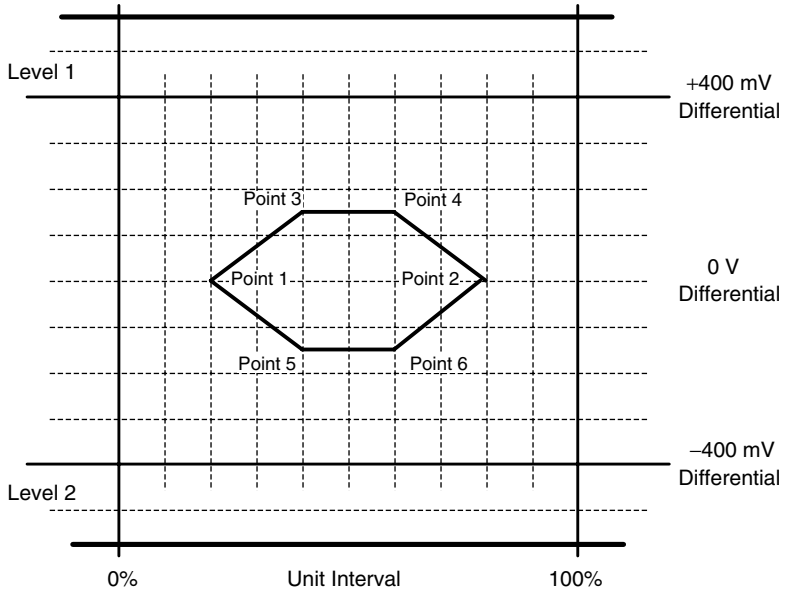
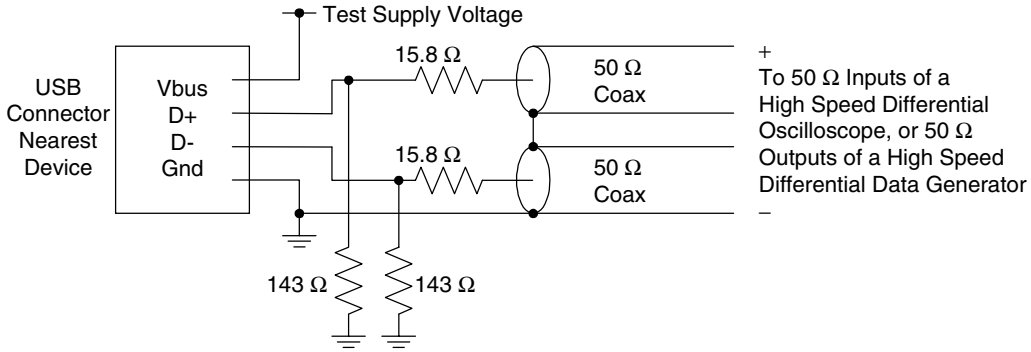


Figure 3-5. Receiver Measurement Fixtures



Pin Capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{DD} = 0 V, T_A = 25°C	4	6	pF
Output capacitance	C_{OUT}	f_C = 1 MHz	4	6	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	4	6	pF

Power Consumption

(1) The power consumption when device works as bus-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-BUS}$	The power consumption under unconfigured stage				
	High-speed operating	57	3	10	mA
	Full-speed operating	23	4	10	mA
P_{W-BUS}	The power consumption when device works				
	High-speed operating	110	22	10	mA
	Full-speed operating	113	13	10	mA
$P_{W\_SPD-BUS}$	The power consumption under suspend state	10	235	5	μA

(2) The power consumption when device works as self-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-SELF}$	The power consumption under unconfigured stage				
	High-speed operating	85	5	10	mA
	Full-speed operating	60	5	10	mA
P_{W-SELF}	The power consumption when device works				
	High-speed operating	120	25	10	mA
	Full-speed operating	113	13	10	mA
$P_{W\_SPD-SELF}$	The power consumption under suspend state	50	5	5	mA
P_{W_UNP}	The power consumption under unplug state	87	3	10	mA
P_{W_COM}	The power consumption under combo mode The device is releasing the IDE bus.	90	5	10	mA

AC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

System Clock Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	X'tal	−500 ppm	30	+500 ppm	MHz
		Oscillator block	−500 ppm	30	+500 ppm	MHz
Clock duty cycle	t_{DUTY}		45	50	55	%

Remarks 1. Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of X'tal or Oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

System Reset signaling

Parameter	Symbol	Conditions	Min.	Max.	Unit
Reset active time	t_{rst}		2		μs

USB Interface Block

(1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% - 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate for device which are high-speed capable	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance):					
To next transition	t_{DJ1}		−3.5	+3.5	ns
For paired transitions	t_{DJ2}		−4.0	+4.0	ns
Source jitter for differential transition to SE0 transition	t_{FDEOP}		−2	+5	ns
Receiver jitter:					
To next transition	t_{JR1}		−18.5	+18.5	ns
For paired transitions	t_{JR2}		−9	+9	ns
Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(2/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
High-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{HSR}		500		ps
Fall time (90% - 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 3-6**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 3-6**.				
Receiver jitter tolerance	See **Figure 3-4**.				
Device Event Timings					
Time from internal power good to device pulling D+ beyond V_{IHZ} (min.) (signaling attached)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	t_{ATTDB}			100	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	t_{SCA}		2.5		μs
Sample time for suspend vs reset	t_{CSR}		100	875	μs
Time to detect bus suspend state	t_{SPD}		3.000	3.125	ms
Power down under suspend	t_{SUS}			10	ms
Reversion time from suspend to high-speed	t_{RHS}			1.333	μs
Drive Chirp K width	t_{CKO}		1		ms
Finish Chirp K assertion	t_{FCA}			7	ms
Start sequencing Chirp K-J-K-J-K-J	t_{SSC}			100	μs
Finish sequencing Chirp K-J	t_{FSC}		–500	–100	μs
Detect sequencing Chirp K-J width	t_{CSI}		2.5		μs
Sample time for sequencing Chirp	t_{SCS}		1	2.5	ms
Reversion time to high-speed	t_{RHA}			500	μs
High-speed detection start time	t_{HDS}		2.5	3000	μs
Reset completed time	t_{DRS}		10		ms

IDE Interface Block

PIO mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min.)	t_0	600	383	240	180	120	ns
Address setup time (min.)	t_1	70	50	30	30	25	ns
16 bits DIOR/DIOW pulse width (min.)	t_2	165	125	100	80	70	ns
8 bits DIOR/DIOW pulse width (min.)		290	290	290	80	70	ns
DIOR/DIOW recovery time (min.)	t_{2i}	–	–	–	70	25	ns
DIOW data setup time (min.)	t_3	60	45	30	30	20	ns
DIOW data hold time (min.)	t_4	30	20	15	10	10	ns
DIOR data setup time (min.)	t_5	50	35	20	20	20	ns
DIOR data hold time (min.)	t_6	5	5	5	5	5	ns
DIOR 3-state delay time (max.)	t_{6Z}	30	30	30	30	30	ns
Address hold time (min.)	t_9	20	15	10	10	10	ns
IORDY read data valid time (min.) Note	t_{RD}	0	0	0	0	0	ns
IORDY setup time (min.) Note	t_A	35	35	35	35	35	ns
IORDY pulse width (max.) Note	t_B	1250	1250	1250	1250	1250	ns
IORDY Inactive to Hi-Z time (max.) Note	t_C	5	5	5	5	5	ns

Note IORDY is an option in mode 0 - 2. IORDY is essential in modes 3 and 4.

Multi Word DMA mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Unit
Cycle time (min.)	t_0	480	150	120	ns
DIOR/DIOW pulse width (min.)	t_D	215	80	70	ns
DIOR data access time (max.)	t_E	150	60	50	ns
DIOR data hold time (min.)	t_F	5	5	5	ns
DIOR data setup time (min.)	t_{Gr}	100	30	20	ns
DIOW data setup time (min.)	t_{Gw}	100	30	20	ns
DIOW data hold time (min.)	t_H	20	15	10	ns
DMACK setup time (min.)	t_I	0	0	0	ns
DMACK hold time (min.)	t_J	20	5	5	ns
DIOR negate pulse width (min.)	t_{Kr}	50	50	25	ns
DIOW negate pulse width (min.)	t_{Kw}	215	50	25	ns
DIOR-DMARQ delay time (max.)	t_{Lr}	120	40	35	ns
DIOW-DMARQ delay time (max.)	t_{Lw}	40	40	35	ns
DMACK 3-state delay time (max.)	t_Z	20	25	25	ns
CS setup time (min.)	t_M	50	30	25	ns
CS hold time (min.)	t_N	15	10	10	ns

Ultra DMA mode

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Average cycle time for 2 cycles	t_{2CYC}	240	-	160	-	120	-	90	-	60	-	ns
Minimum cycle time for 2 cycles	t_{2CYC}	235	-	156	-	117	-	86	-	57	-	ns
Cycle time for 1 cycle	t_{CYC}	114	-	75	-	55	-	39	-	25	-	ns
Data setup time on receive side	t_{DS}	15	-	10	-	7	-	7	-	5	-	ns
Data hold time on receive side	t_{DH}	5	-	5	-	5	-	5	-	5	-	ns
Data setup time on transmit side	t_{DVS}	70	-	48	-	34	-	20	-	6	-	ns
Data hold time on transmit side	t_{DVH}	6	-	6	-	6	-	6	-	6	-	ns
First STROBE time	t_{FS}	0	230	0	200	0	170	0	130	0	120	ns
Interlock time with limitation	t_{LI}	0	150	0	150	0	150	0	100	0	100	ns
Minimum interlock time	t_{MLI}	20	-	20	-	20	-	20	-	20	-	ns
Interlock time without limitation	t_{UI}	0	-	0	-	0	-	0	-	0	-	ns
Output release time	t_{AZ}	-	10	-	10	-	10	-	10	-	10	ns
Output delay time	t_{ZAH}	20	-	20	-	20	-	20	-	20	-	ns
Output stabilization time (from release)	t_{ZAD}	0	-	0	-	0	-	0	-	0	-	ns
Envelope time	t_{ENV}	20	70	20	70	20	70	20	55	20	55	ns
STROBE DMARDY delay time	t_{SR}	-	50	-	30	-	20	-	NA	-	NA	ns
Last STROBE time	t_{RFS}	-	75	-	60	-	50	-	60	-	60	ns
Pause time	t_{RP}	160	-	125	-	100	-	100	-	100	-	ns
IORDY pull-up time	t_{IORYZ}	-	20	-	20	-	20	-	20	-	20	ns
IORDY wait time	t_{ZIORY}	0	-	0	-	0	-	0	-	0	-	ns
DMACK setup/hold time	t_{ACK}	20	-	20	-	20	-	20	-	20	-	ns
STROBE STOP time	t_{SS}	50	-	50	-	50	-	50	-	50	-	ns

Serial ROM interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Clock frequency	t_{SCL}			100	KHz
Clock pulse width low	t_{LOW}		4.7		μs
Clock pulse width high	t_{HIGH}		4.0		μs
Clock Low to data valid	t_{AA}		100	4500	ns
Start hold time	$t_{HD.STA}$		4.0		μs
Start setup time	$t_{SU.STA}$		4.7		μs
Data in hold time	$t_{HD.DAT}$		0		ns
Data in setup time	$t_{SU.DAT}$		0.2		μs
Data out hold time	t_{DH}		50		ns
Stop setup time	$t_{SU.STO}$		4.7		μs
Time the bus must be free before a new transmission can start	t_{BUF}		10		μs
Write cycle time	t_{WR}		10		ms

Figure 3-6. Transmit Waveform for Transceiver at DP/DM

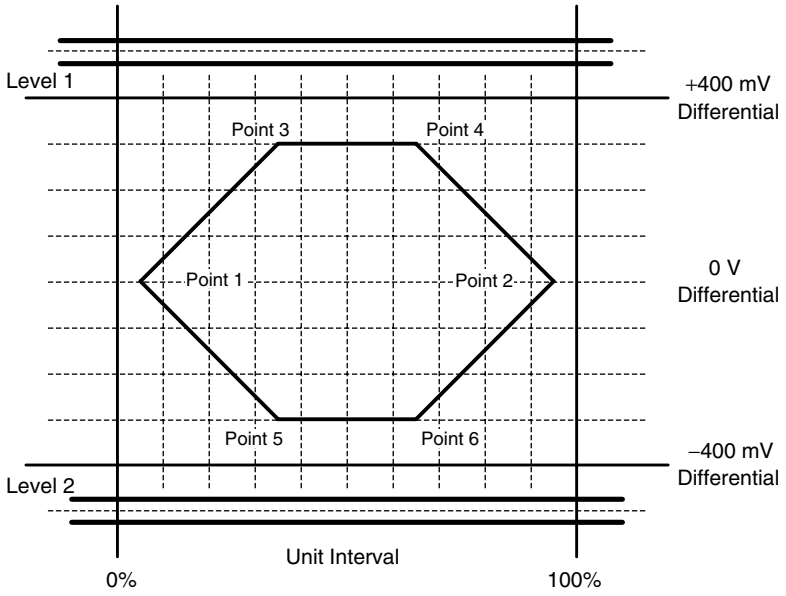
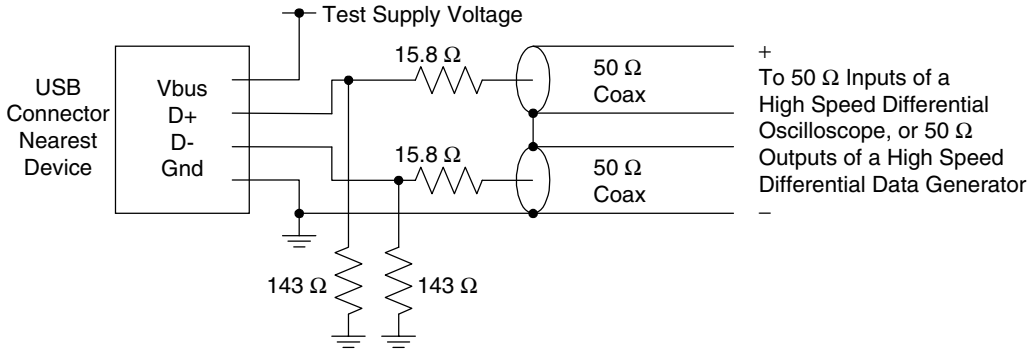


Figure 3-7. Transmitter Measurement Fixtures



Timing Diagram

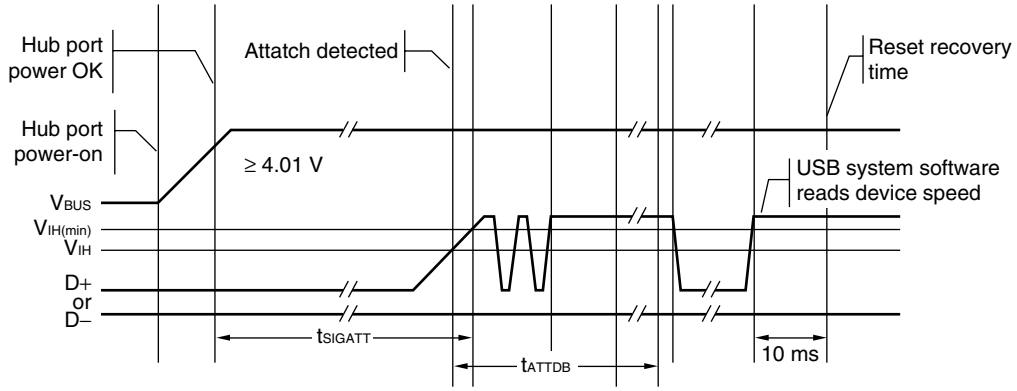
System reset timing

Remark After RESET is negated, this chip read the serial ROM first. Do not reset while the serial ROM is read. The serial ROM is completed to read below time, after RESET is negated.

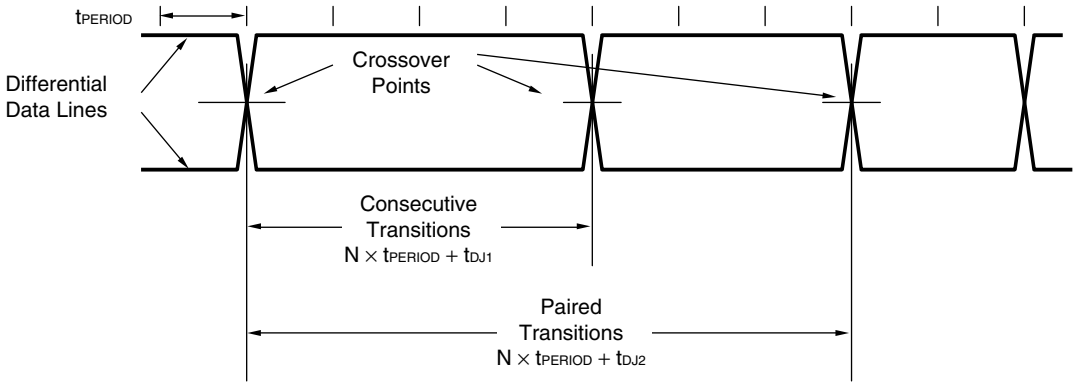
5 + 0.1197 × bytes (serial ROM size) + 0.5678 (ms)

Example In the case of 512 bytes: 66.855 ms, in the case of 8 Kbytes: 986.15 ms

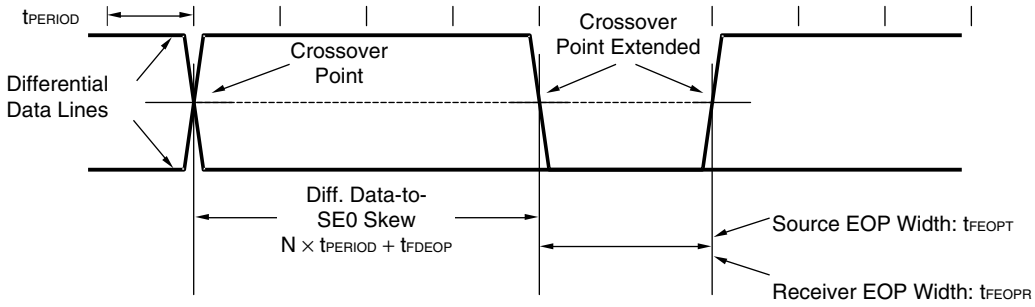
USB power-on and connection events



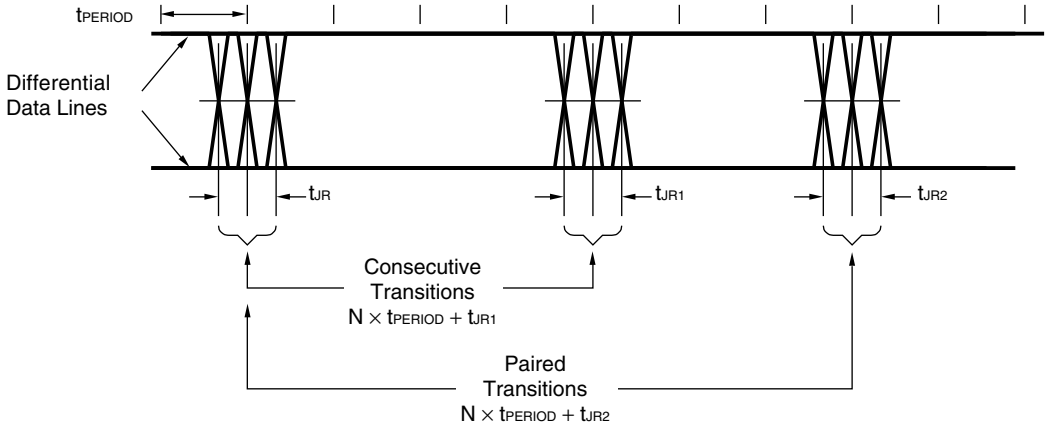
USB differential data jitter for full-speed



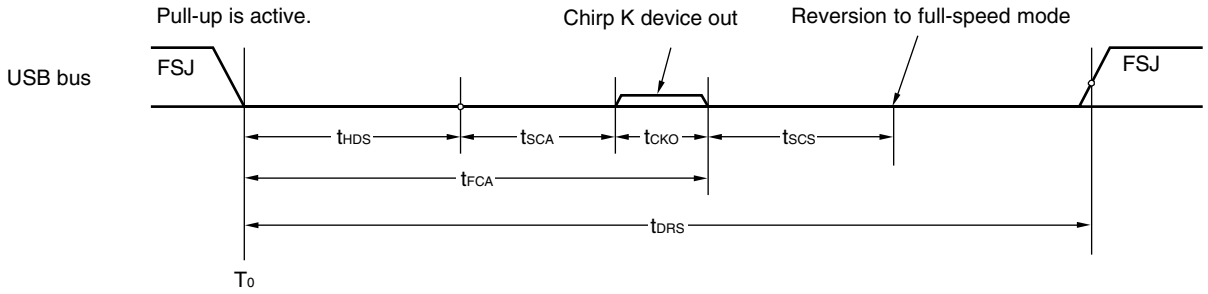
USB differential-to-EOP transition skew and EOP width for full-speed



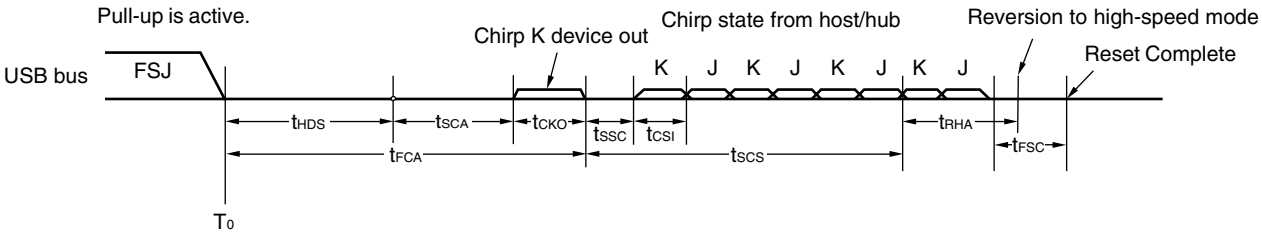
USB receiver jitter tolerance for full-speed



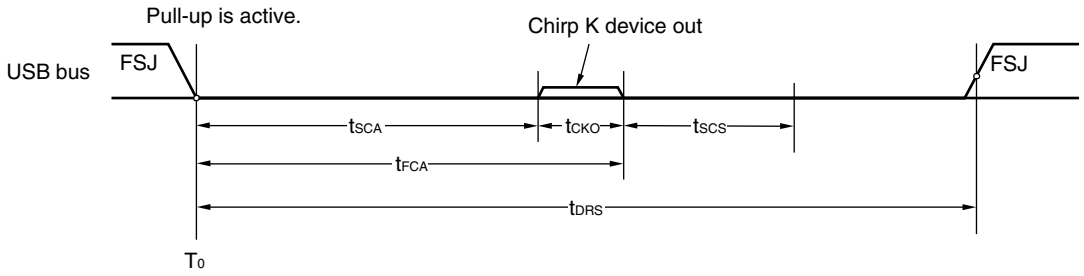
USB connection sequence on full-speed system bus



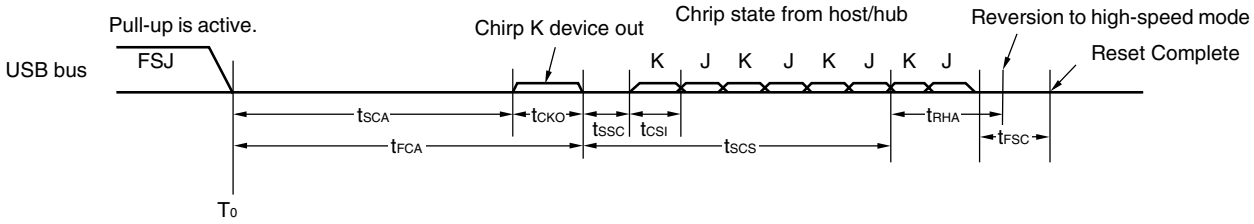
USB connection sequence on high-speed system bus



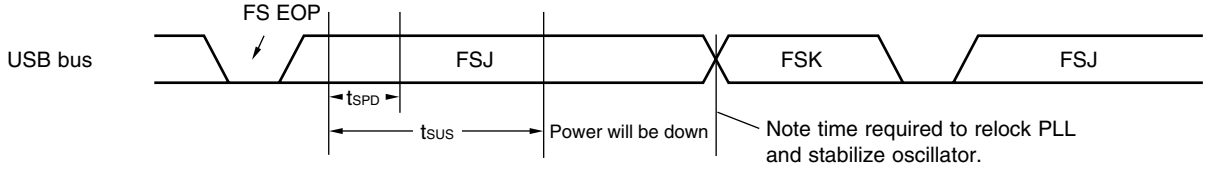
USB reset sequence from suspend state on full-speed system bus



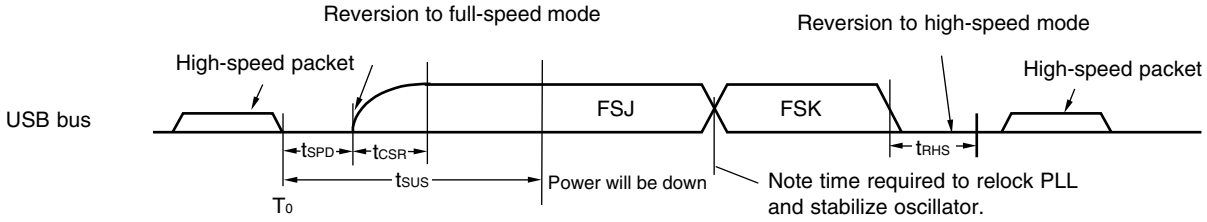
USB reset sequence from suspend state on high-speed system bus



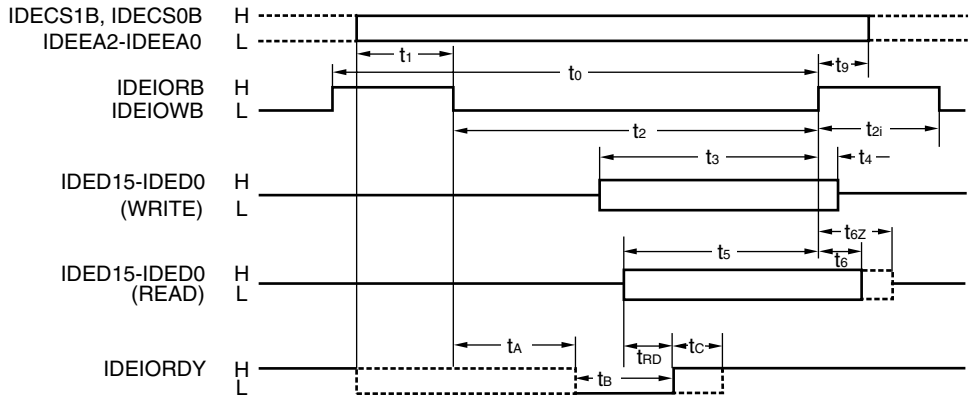
USB suspend and resume on full-speed system bus



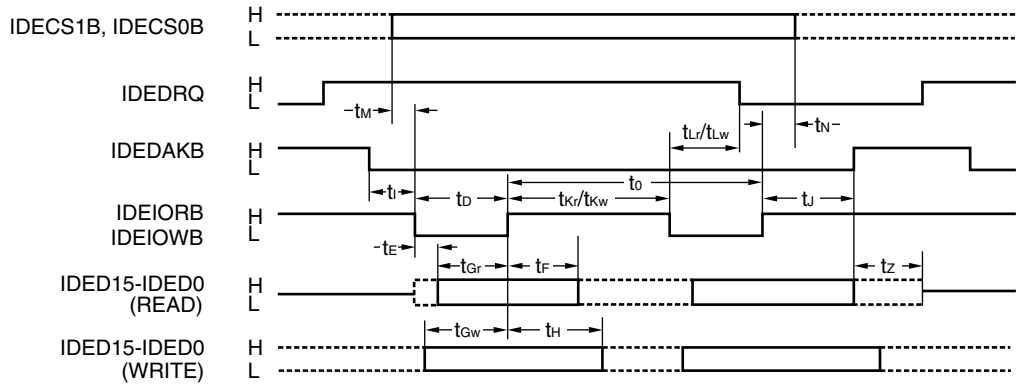
USB suspend and resume on high-speed system bus



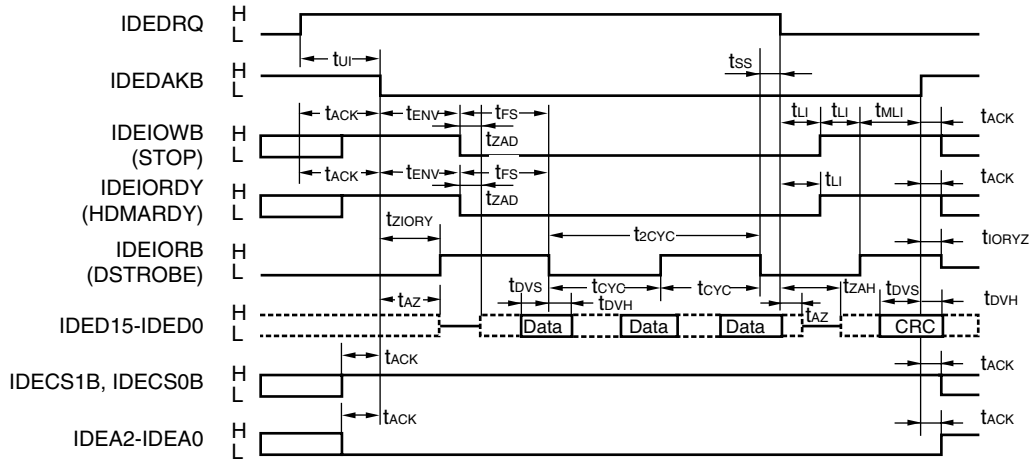
IDE PIO mode timing



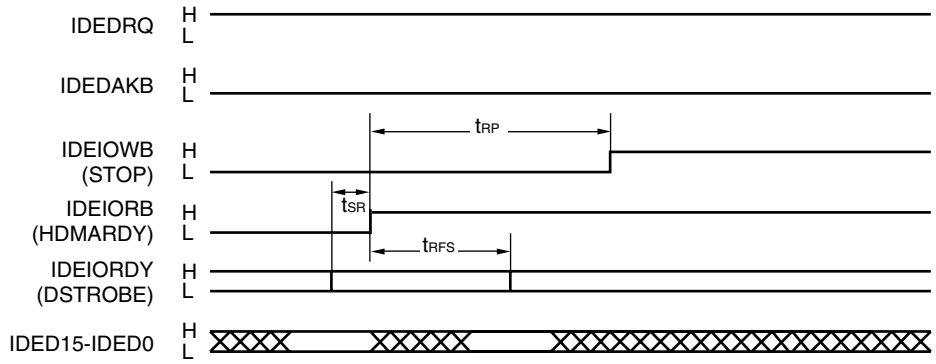
IDE multi word DMA mode timing



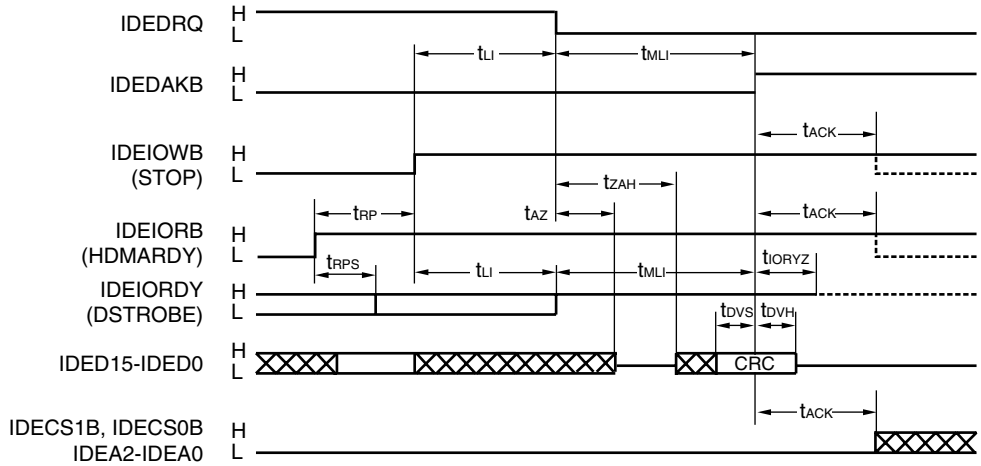
IDE ultra DMA mode data-in timing



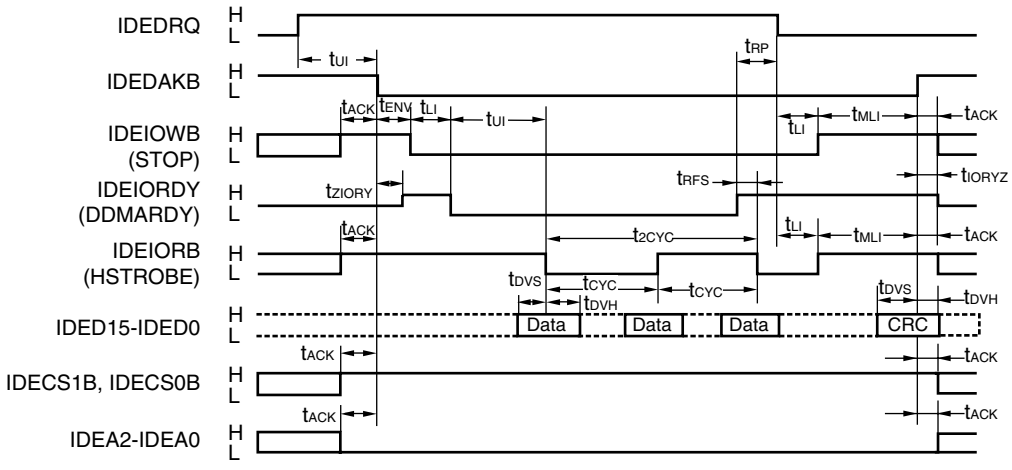
IDE ultra DMA mode data-in stop timing



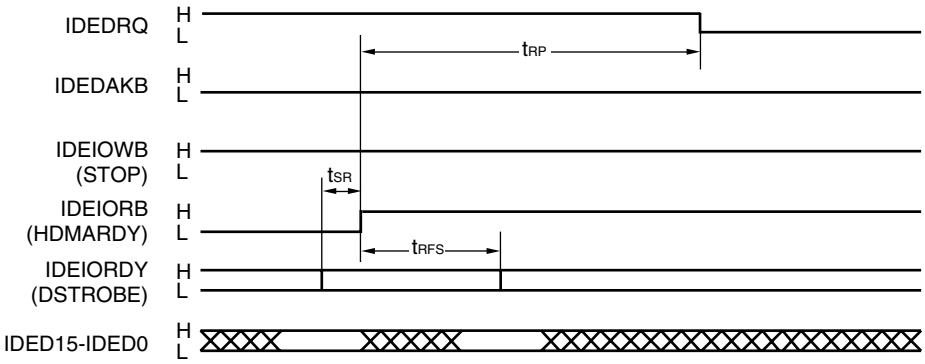
IDE ultra DMA mode data-in end timing



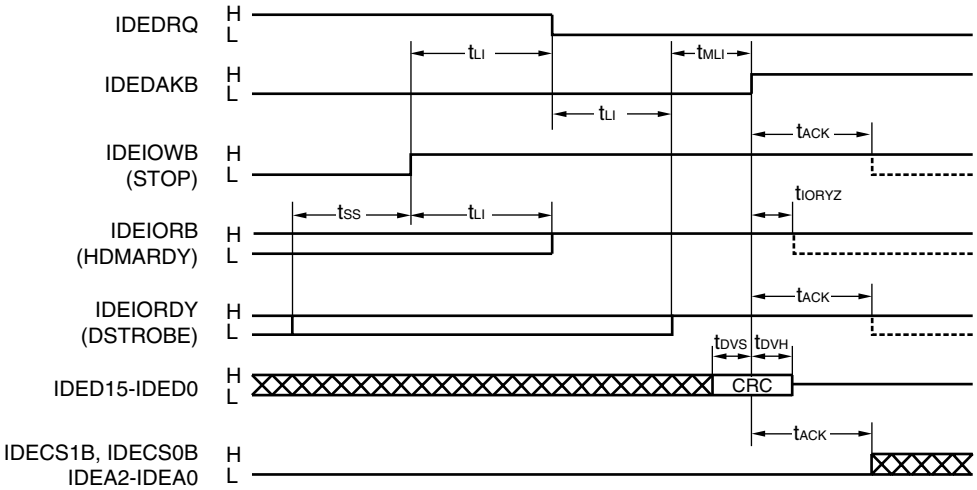
IDE ultra DMA mode data-out timing



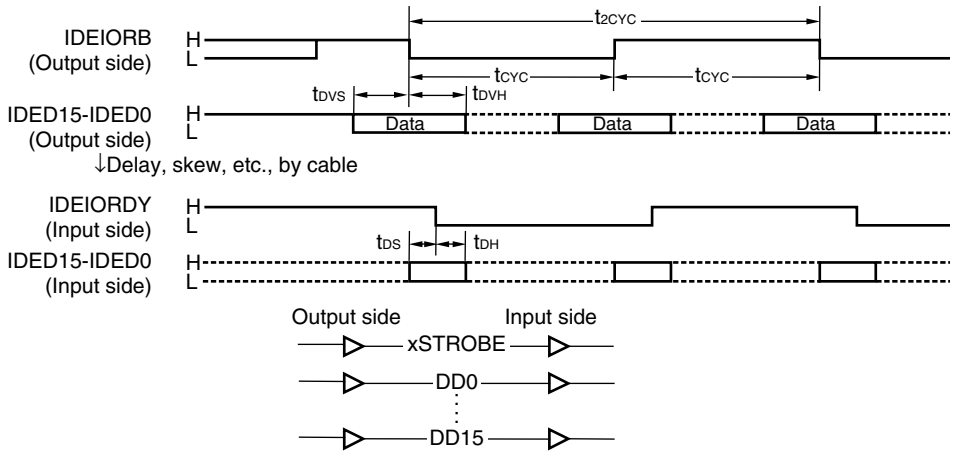
IDE ultra DMA mode data-out stop timing



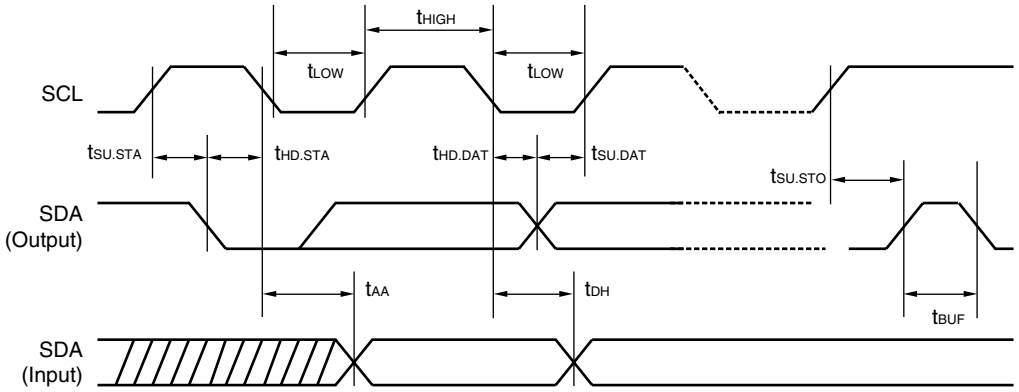
IDE ultra DMA mode data-out end timing



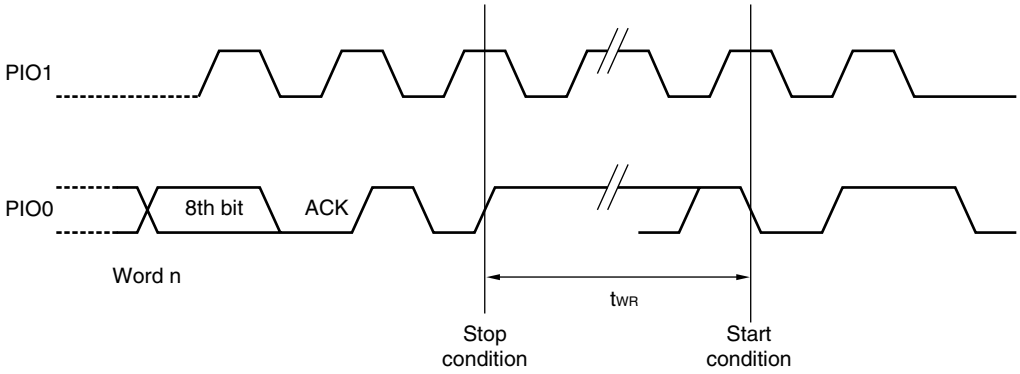
IDE ultra DMA mode data skew timing



Serial ROM access timing



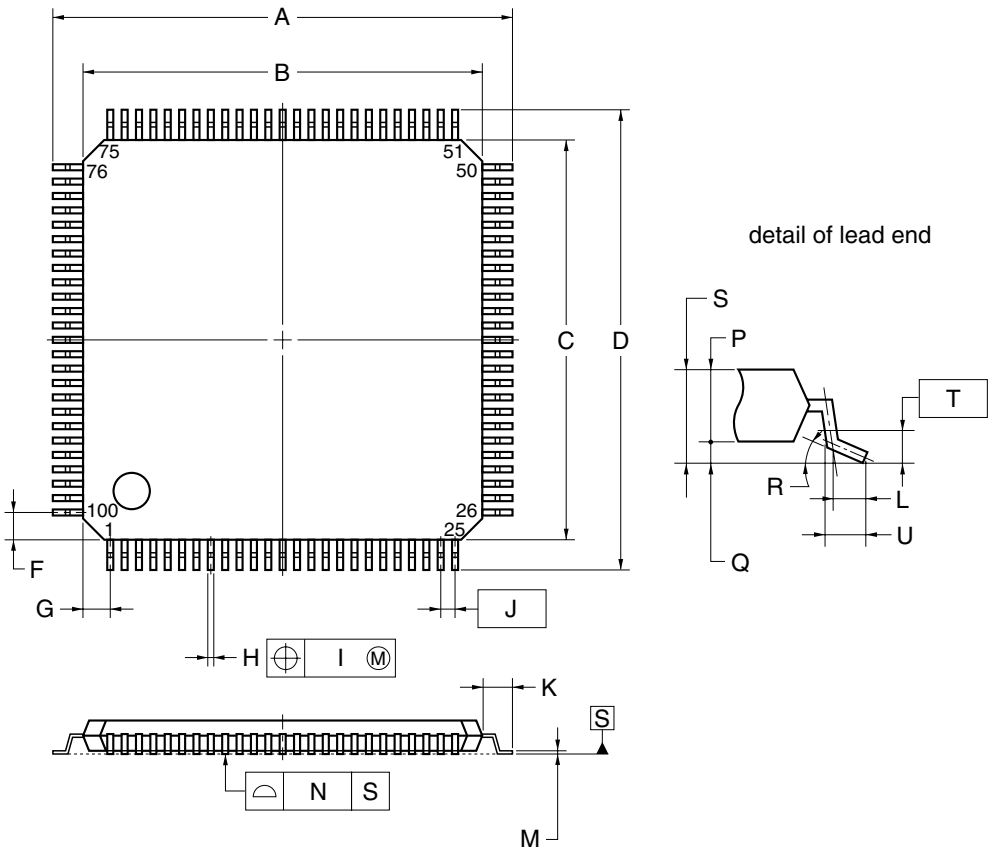
Serial ROM write cycle timing



4. PACKAGE DRAWING

- μPD720130GC-9EU

★ **100-PIN PLASTIC TQFP (FINE PITCH) (14x14)**



NOTE

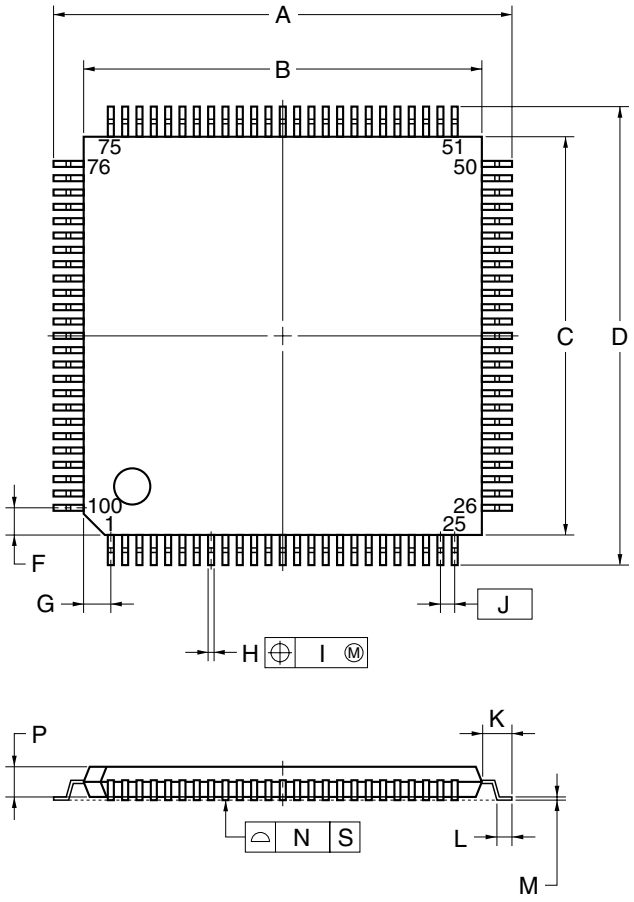
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

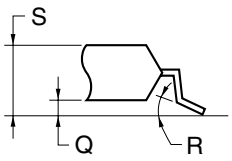
P100GC-50-9EU

★ • μPD720130GC-9EU-SIN

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S100GC-50-9EU-2

5. RECOMMENDED SOLDERING CONDITIONS

The μPD720130 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact your NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD720130GC-9EU: 100-pin plastic TQFP (Fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds or less (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

★ **μPD720130GC-9EU-SIN: 100-pin plastic TQFP (Fine pitch) (14 × 14)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds or less (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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USB logo is a trademark of USB Implementers Forum, Inc.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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