TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS102C – Revised October 2003

CD40147B Types

10-Line to 4-Line BCD Priority Encoder

High-Voltage Types (20-Volt Rating)

The CD40147B CMOS encoder features priority encoding of the inputs to ensure that only the highest-order data line is encoded. Ten data input lines (0-9) are encoded to four-line (8, 4, 2, 1) BCD. The highest priority line is line 9. All four output lines are logic 1 (V_{SS}) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low-power Schottky load. The CD40147B is functionally similar to the TTL54/74147 if pin 15 is tied low.

The CD40147B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Encodes 10-line to 4-line BCD
- Active low inputs and outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
    1 V at V_{DD} = 5 V
    2 V at V_{DD} = 10 V
    2.5 V at V_{DD} = 15 V

Applications:

- Keyboard encoding
- 10-line to BCD encoding
- Range selection

FUNCTIONAL DIAGRAM

92CS-30552
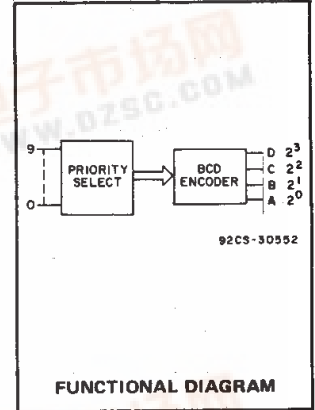
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

* INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 – CD40147B logic diagram.

92CM-30956

TRUTH TABLE (Negative Logic)

INPUTS										OUTPUTS			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	1	0	0	1

0 = High Level   1 = Low Level   X = Don't Care

Fig. 2 — Typical output low (sink) current characteristics.

92CS-24518R3
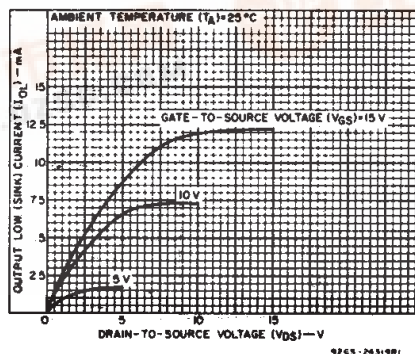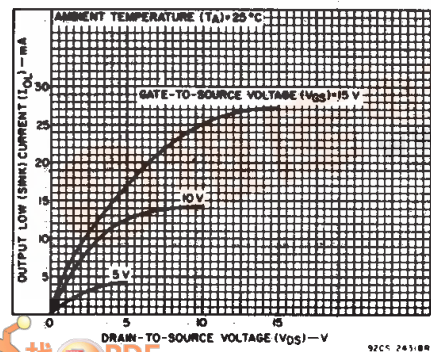
Fig. 3 — Minimum output low (sink) current characteristics.
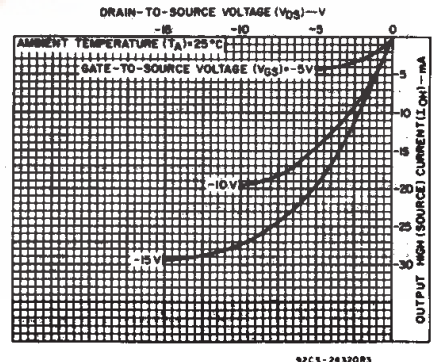
92CS-24519R1

Fig. 4 — Typical output high (source) current characteristics.

92CS-24320R3

CD40147B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)............. 100mW
OPERATING-TEMPERATURE RANGE (T_A) ....−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ....−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
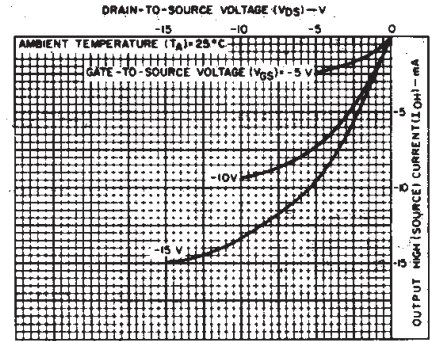At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

Fig. 5 — Minimum output high (source) current characteristics.
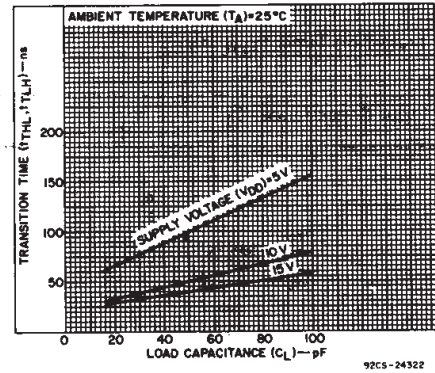
Fig. 6 — Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

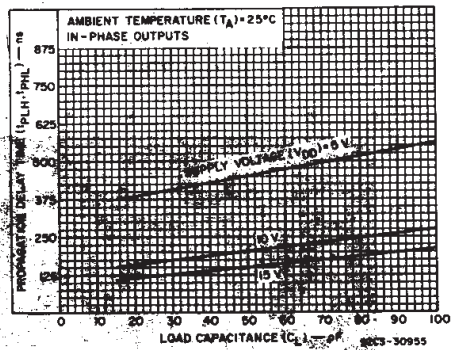| CHARAC-TERISTIC	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent	—	0,5	5	5	5	150	150	—	0.04	5	
Device	—	0,10	10	10	10	300	300	—	0.04	10	µA
Current, I_{DD}	—	0,15	15	20	20	600	600	—	0.04	20	
Max.	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	
Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	mA
I_{OL} Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
(Source)	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	mA
Current,	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
I_{OH} Min.	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage:	—	0,5	5	0.05				—	0	0.05	
Low-Level,	—	0,10	10	0.05				—	0	0.05	V
V_{OL} Max.	—	0,15	15	0.05				—	0	0.05	
Output Voltage:	—	0,5	5	4.95				4.95	5	—	
High-Level,	—	0,10	10	9.95				9.95	10	—	V
V_{OH} Min.	—	0,15	15	14.95				14.95	15	—	
Input Low	0.5,4.5	—	5	1.5				—	—	1.5	
Voltage,	1,9	—	10	3				—	—	3	V
V_{IL} Max.	1.5,13.5	—	15	4				—	—	4	
Input High	0.5,4.5	—	5	3.5				3.5	—	—	
Voltage,	1,9	—	10	7				7	—	—	V
V_{IH} Min.	1.5,13.5	—	15	11				11	—	—	
Input Current	—	0,18	18	±0.1	±0.1	±1	±1	—	±10⁻⁵	±0.1	µA
I_{IN} Max.											

Fig. 7 — Propagation delay time as a function of load capacitance.

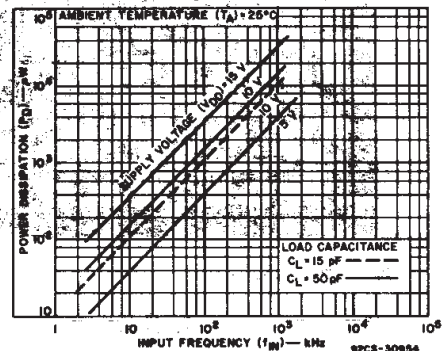Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns,
C_L = 50 pF, R_L = 200 kΩ

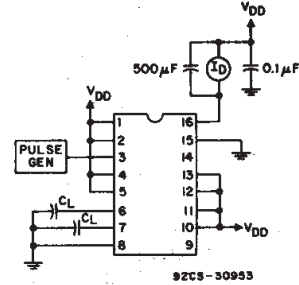| CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS ALL TYPES		UNITS
			Typ.	Max.	
Propagation Delay Time, t_{PLH}, t_{PHL} In-Phase Output	Any input to any output	5	450	900	ns
		10	200	400	
		15	150	300	
Out-of-Phase Output		5	425	850	ns
		10	175	350	
		15	125	250	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_1	Any Input		5	7.5	pF

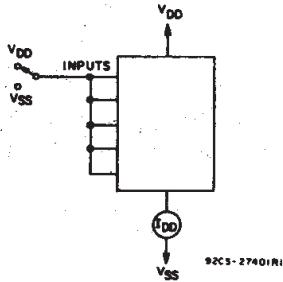Fig. 9 — Dynamic power dissipation test circuit.
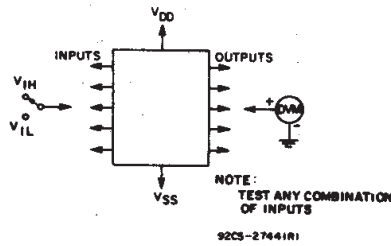

Fig. 10 — Quiescent device current test circuit.

Fig. 11 — Input voltage test circuit.
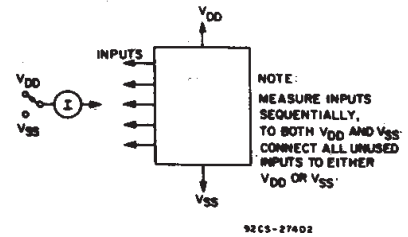
Fig. 12 — Input current test circuit.
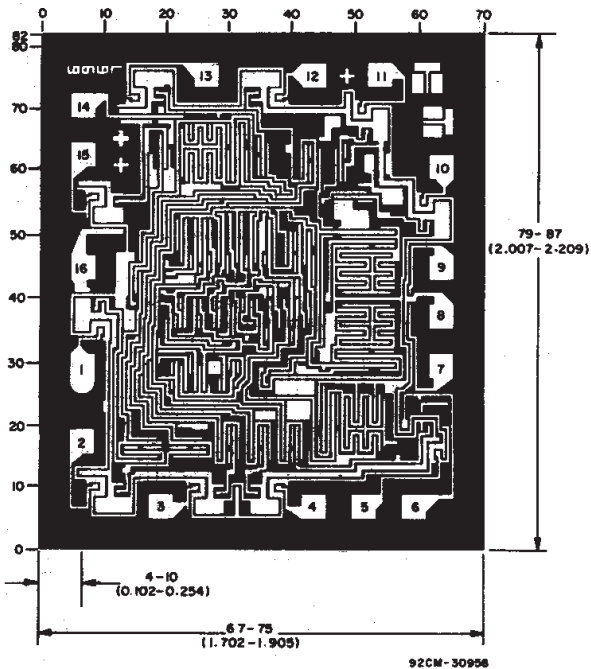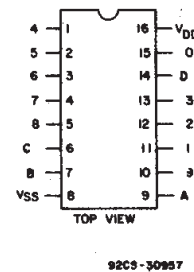

CD40147B
TERMINAL
ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD40147BH

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD40147BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD40147BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD40147BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40147BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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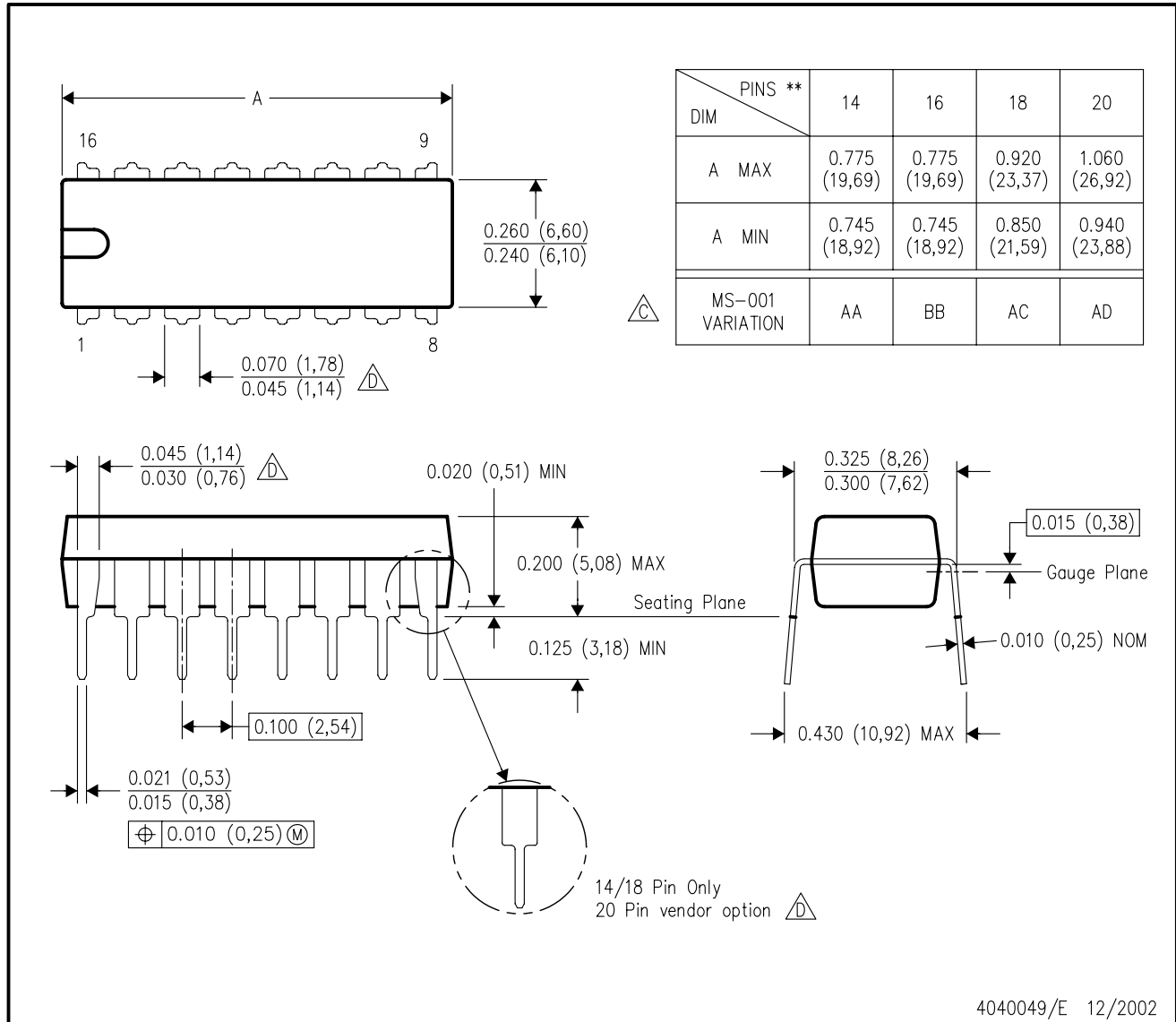
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N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
⚠C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) ⚠D

0.045 (1,14)
0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⚠D

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      ⚠C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      ⚠D   The 20 pin end lead shoulder width is a vendor option, either half or full width.
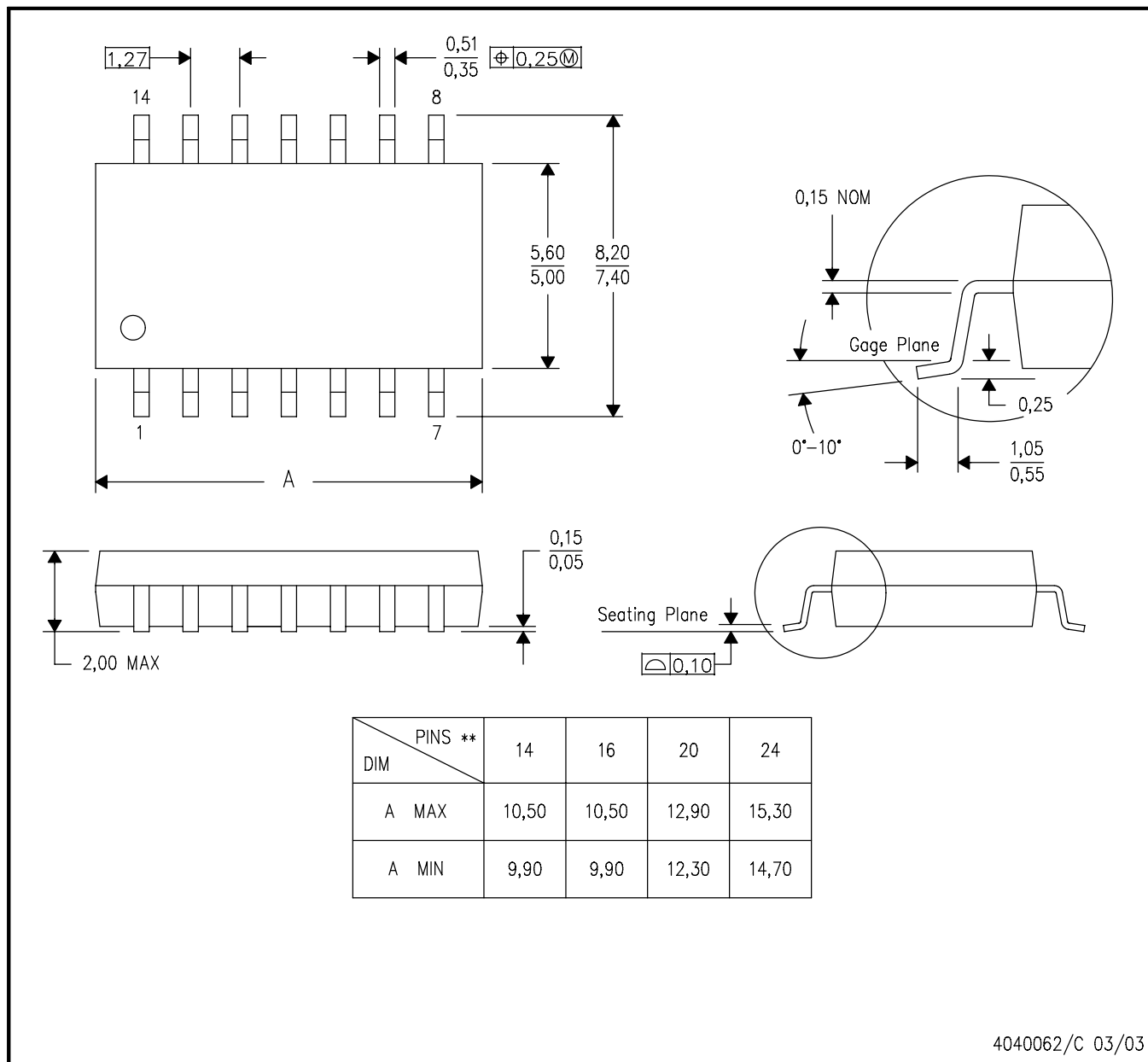
D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F   07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AC.

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MECHANICAL DATA

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
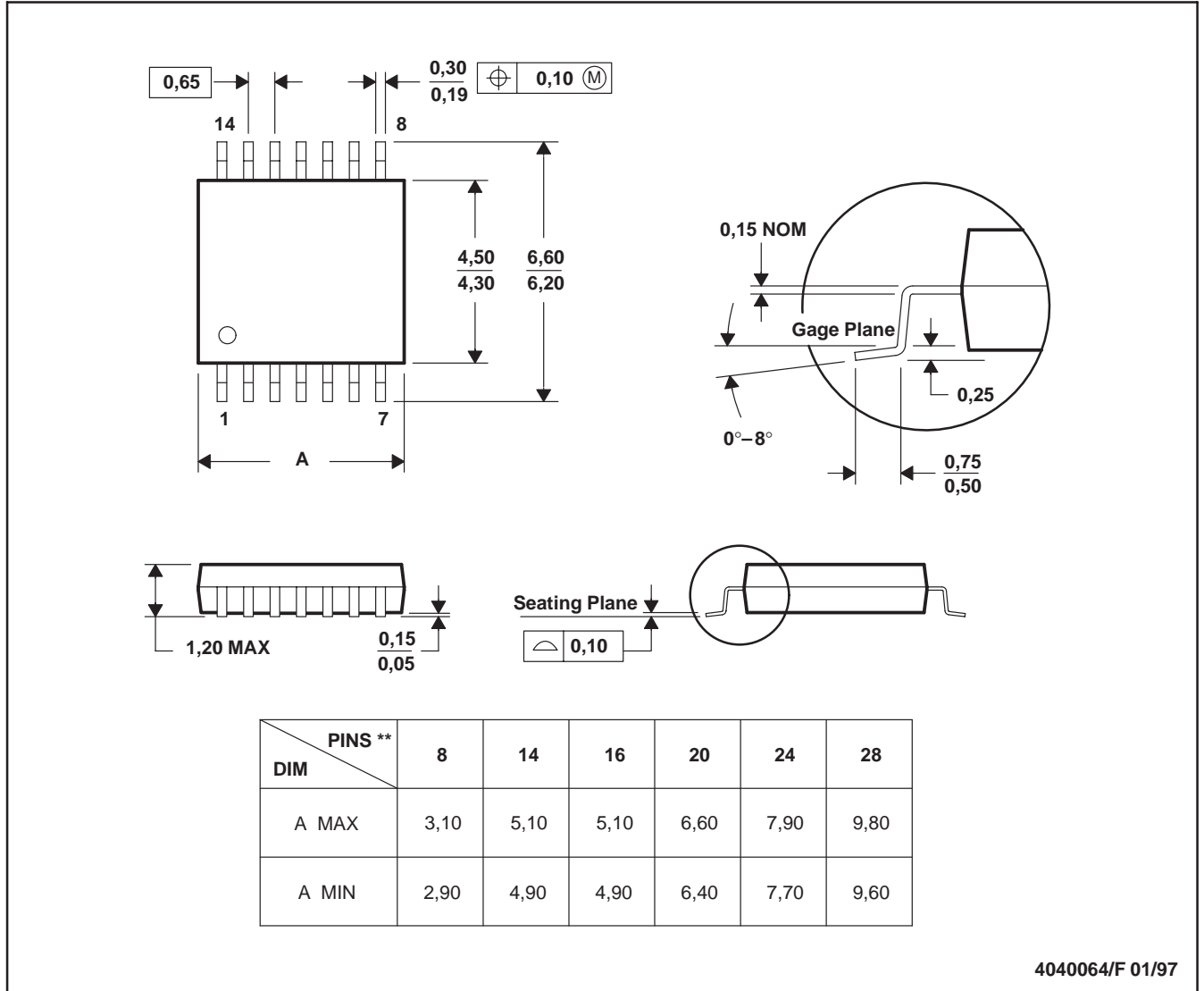
MECHANICAL DATA

PW (R-PDSO-G**)　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

	PINS **	8	14	16	20	24	28
DIM							
A	MAX	3,10	5,10	5,10	6,60	7,90	9,80
A	MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:　A. All linear dimensions are in millimeters.
　　　　　B. This drawing is subject to change without notice.
　　　　　C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　　D. Falls within JEDEC MO-153

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