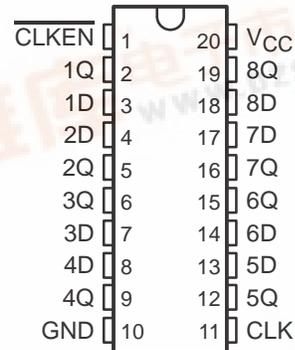PCB

SN54ABT377, SN74ABT377
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLOCK ENABLE
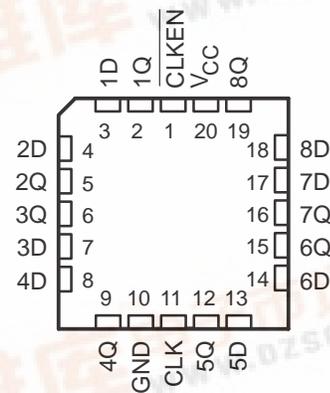
SCBS156B – FEBRUARY 1991 – REVISED JULY 1994

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs**

SN54ABT377 . . . J PACKAGE
SN74ABT377 . . . DB, DW, OR N PACKAGE
(TOP VIEW)

CLKEN	1		20	V_{CC}
1Q	2		19	8Q
1D	3		18	8D
2D	4		17	7D
2Q	5		16	7Q
3Q	6		15	6Q
3D	7		14	6D
4D	8		13	5D
4Q	9		12	5Q
GND	10		11	CLK

SN54ABT377 . . . FK PACKAGE
(TOP VIEW)

Pins (top, left to right): 1D, 1Q, CLKEN, V_{CC}, 8Q — numbered 3 2 1 20 19

2D	4	18	8D
2Q	5	17	7D
3Q	6	16	7Q
3D	7	15	6Q
4D	8	14	6D

Pins (bottom): 4Q, GND, CLK, 5Q, 5D — numbered 9 10 11 12 13

description

The 'ABT377 are 8-bit positive-edge-triggered D-type flip-flops with a clock (CLK) input. They are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable (CLKEN) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at CLKEN.

The SN74ABT377 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT377 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT377 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
CLKEN	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	H or L	X	Q_0

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TEXAS INSTRUMENTS
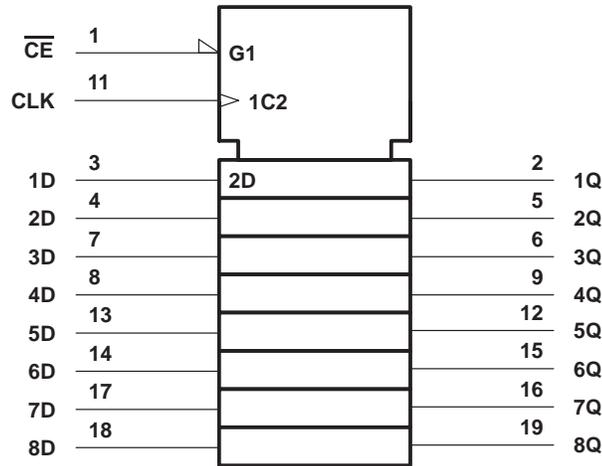
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
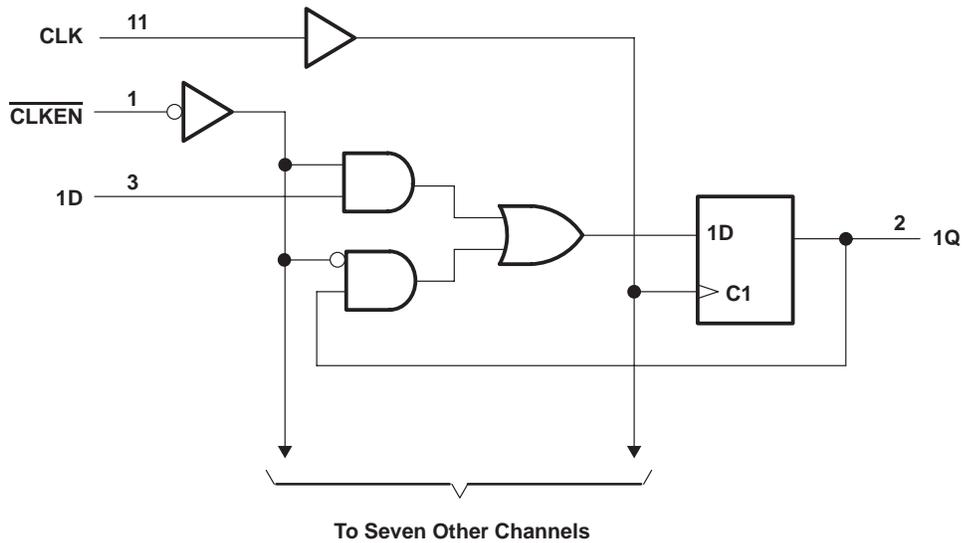
To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT377 .... 96 mA
　　　　　　　　　　　　　　　　　　　　　SN74ABT377 .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... −18 mA
Output clamp current, I_{OK} (V_O < 0) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package .... 0.6 W
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　DW package .... 1.6 W
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　N package .... 1.3 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
　functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
　implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
　　　　2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils,
　　　　　 except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations*
　　　　　 application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT377		SN74ABT377		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25°C$			SN54ABT377		SN74ABT377		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA				−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -3$ mA		2.5			2.5		2.5		V
	$V_{CC} = 5$ V, $I_{OH} = -3$ mA		3			3		3		
	$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
		$I_{OH} = -32$ mA	2*					2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
		$I_{OL} = 64$ mA			0.55*				0.55	
I_I	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡	$V_{CC} = 5.5$ V, $V_O = 2.5$ V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		1	250		250		250	µA
		Outputs low		24	30		30		30	mA
ΔI_{CC}§	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	$V_I = 2.5$ V or 0.5 V			3						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

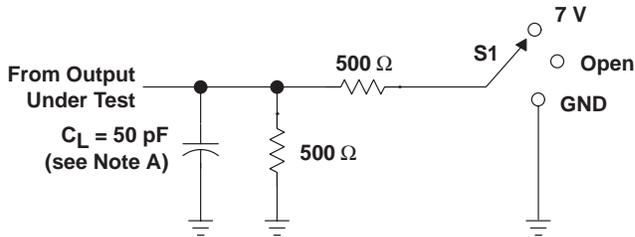|			$V_{CC} = 5$ V, $T_A = 25°C$		SN54ABT377		SN74ABT377		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high or low	2		2.5		2		ns
		$\overline{CLKEN}$ high or low	3		3		3		
t_h	Hold time after CLK↑	Data high or low	1.8¶		1.8¶		1.8¶		ns
		$\overline{CLKEN}$ high or low	1.8¶		1.8¶		1.8¶		

¶ This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25°C$			SN54ABT377		SN74ABT377		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	2.2	4.5	6	2.2	7	2.2	6.5	ns
t_{PHL}			3.1	5.3	6.8	2	7.6	3.1	7.3	

PARAMETER MEASUREMENT INFORMATION

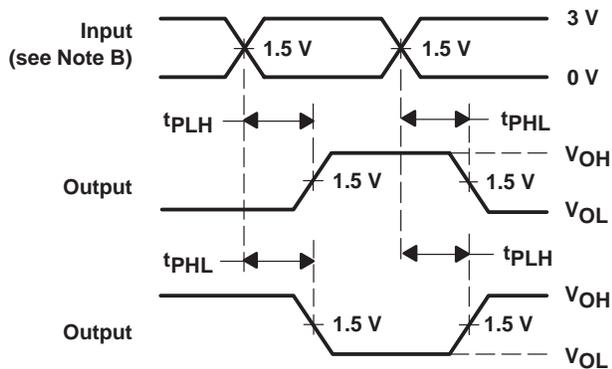**LOAD CIRCUIT FOR OUTPUTS**

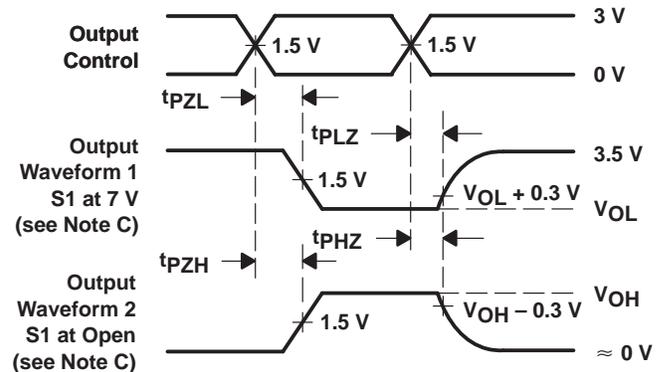| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
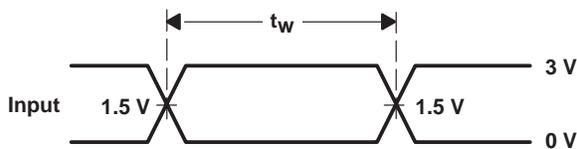
**VOLTAGE WAVEFORMS
PULSE DURATION**
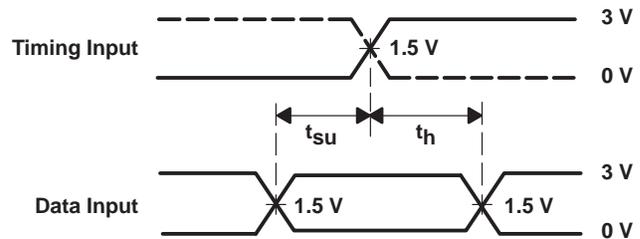
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
     B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
     C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
     D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9314801Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9314801QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9314801QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN74ABT377DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74ABT377DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ABT377DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ABT377N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SNJ54ABT377FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT377J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT377W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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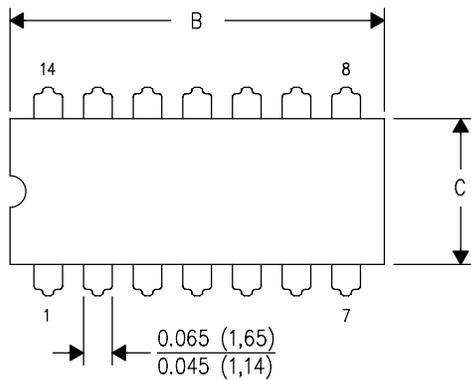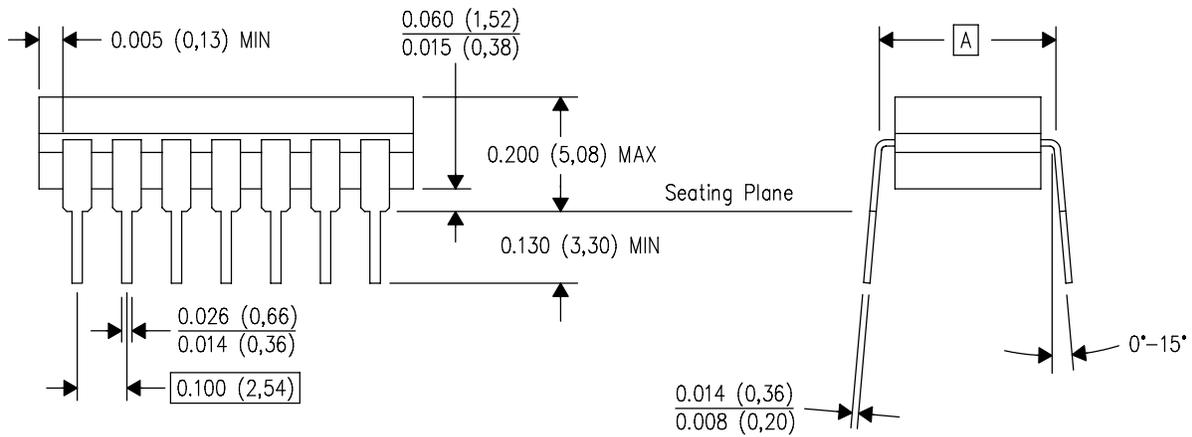
DIM PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

A

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

0°-15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
           B.   This drawing is subject to change without notice.
           C.   This package is hermetically sealed with a ceramic lid using glass frit.
           D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
           E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.300\ (7,62)}{0.245\ (6,22)}$

Base and Seating Plane

$\dfrac{0.100\ (2,45)}{0.045\ (1,14)}$

$\dfrac{0.009\ (0,23)}{0.004\ (0,10)}$

0.320 (8,13) MAX

1   20

0.540 (13,72) MAX

$\dfrac{0.022\ (0,56)}{0.015\ (0,38)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$

$\dfrac{0.370\ (9,40)}{0.250\ (6,35)}$
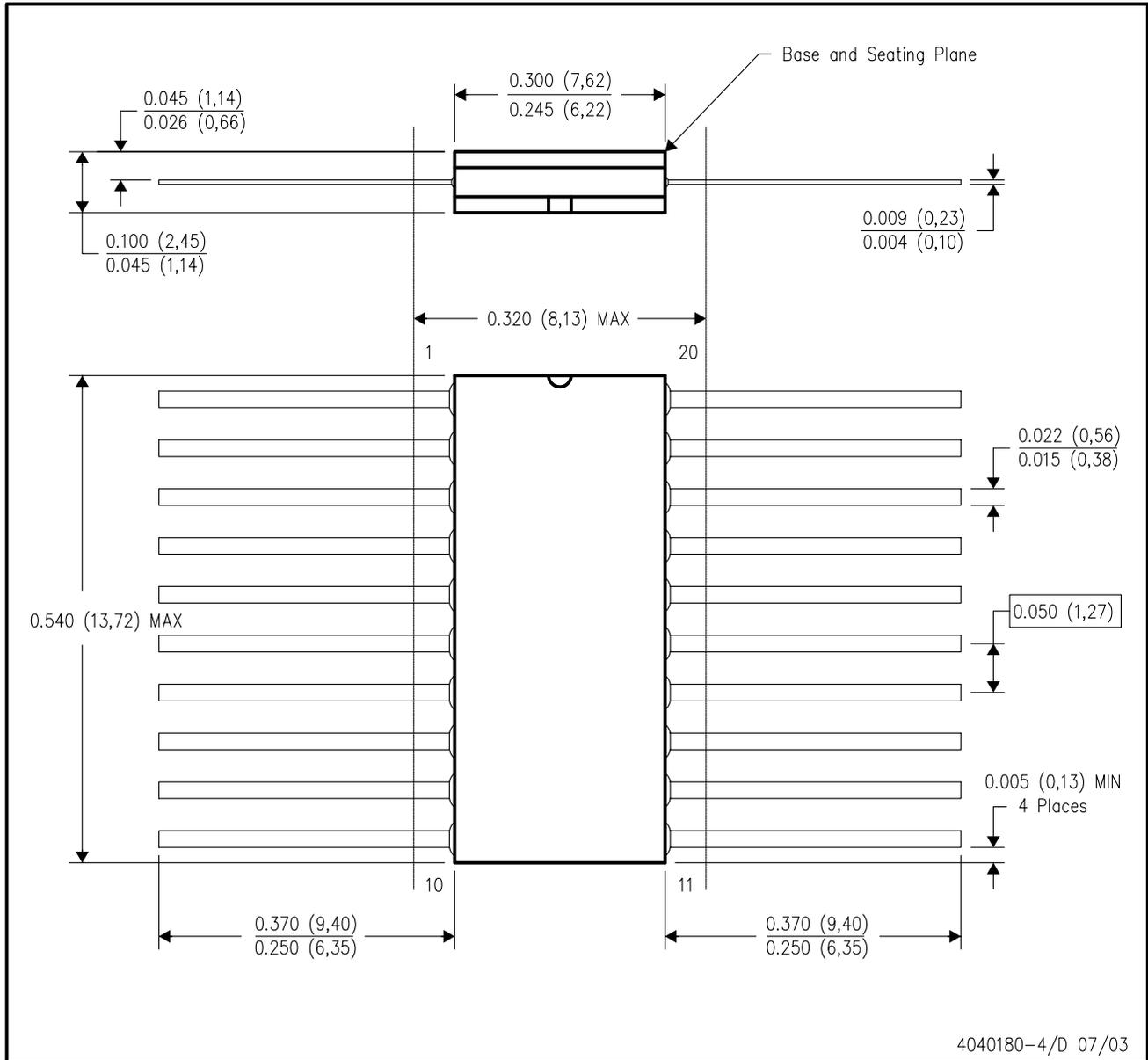
4040180−4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
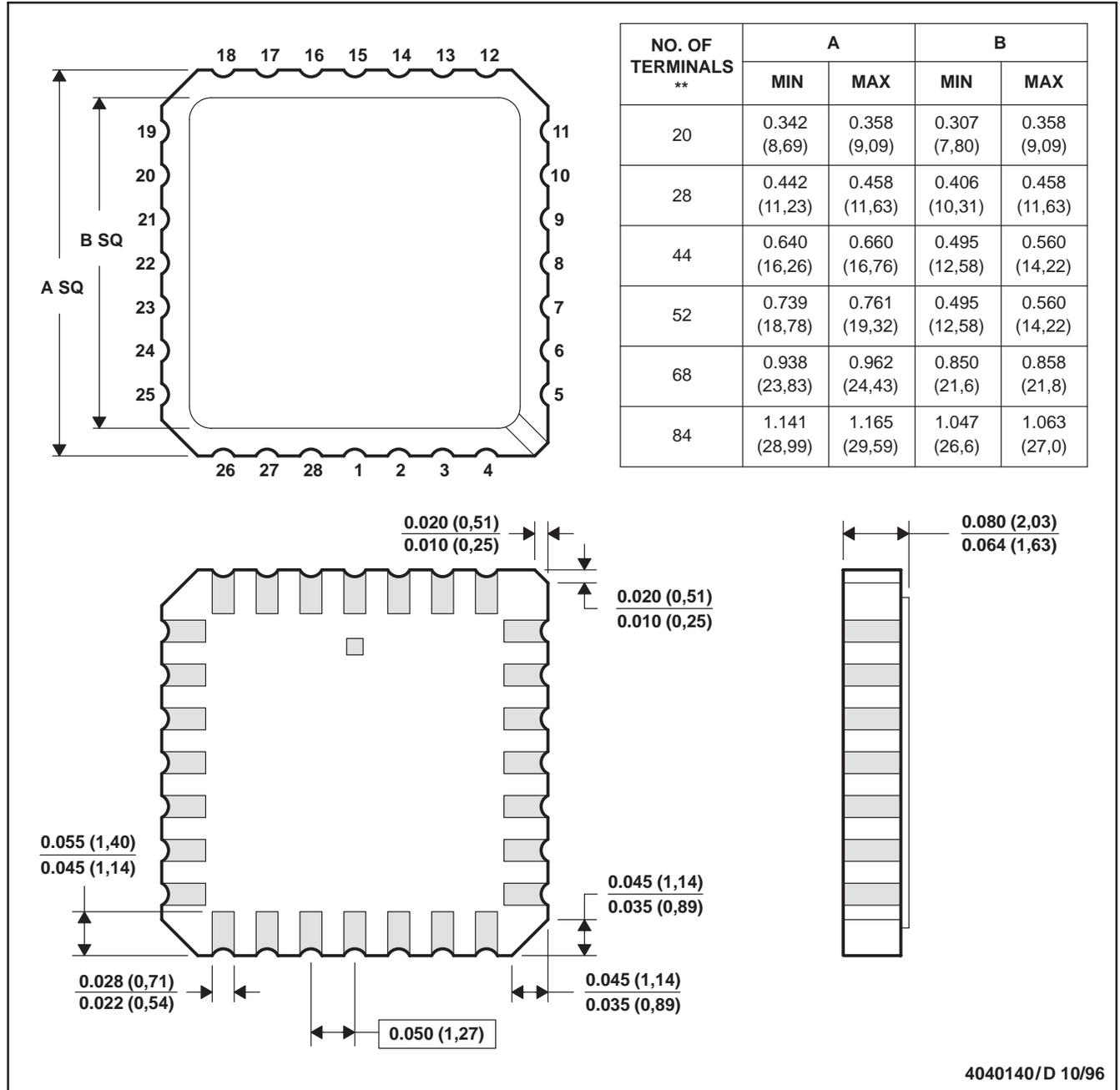   E. Falls within Mil−Std 1835 GDFP2−F20

MECHANICAL DATA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
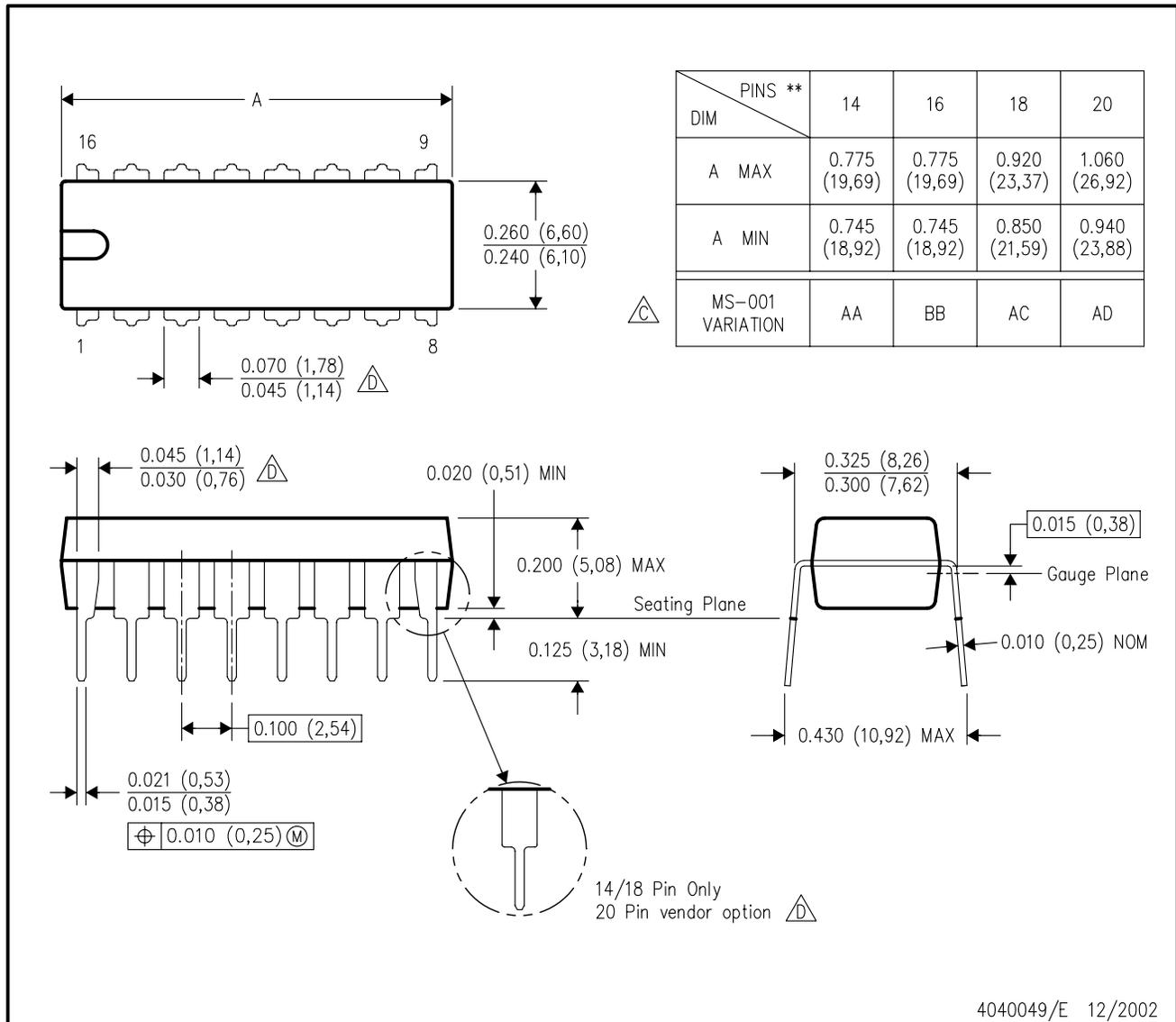D. The terminals are gold plated.
E. Falls within JEDEC MS-004

TEXAS
INSTRUMENTS

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002
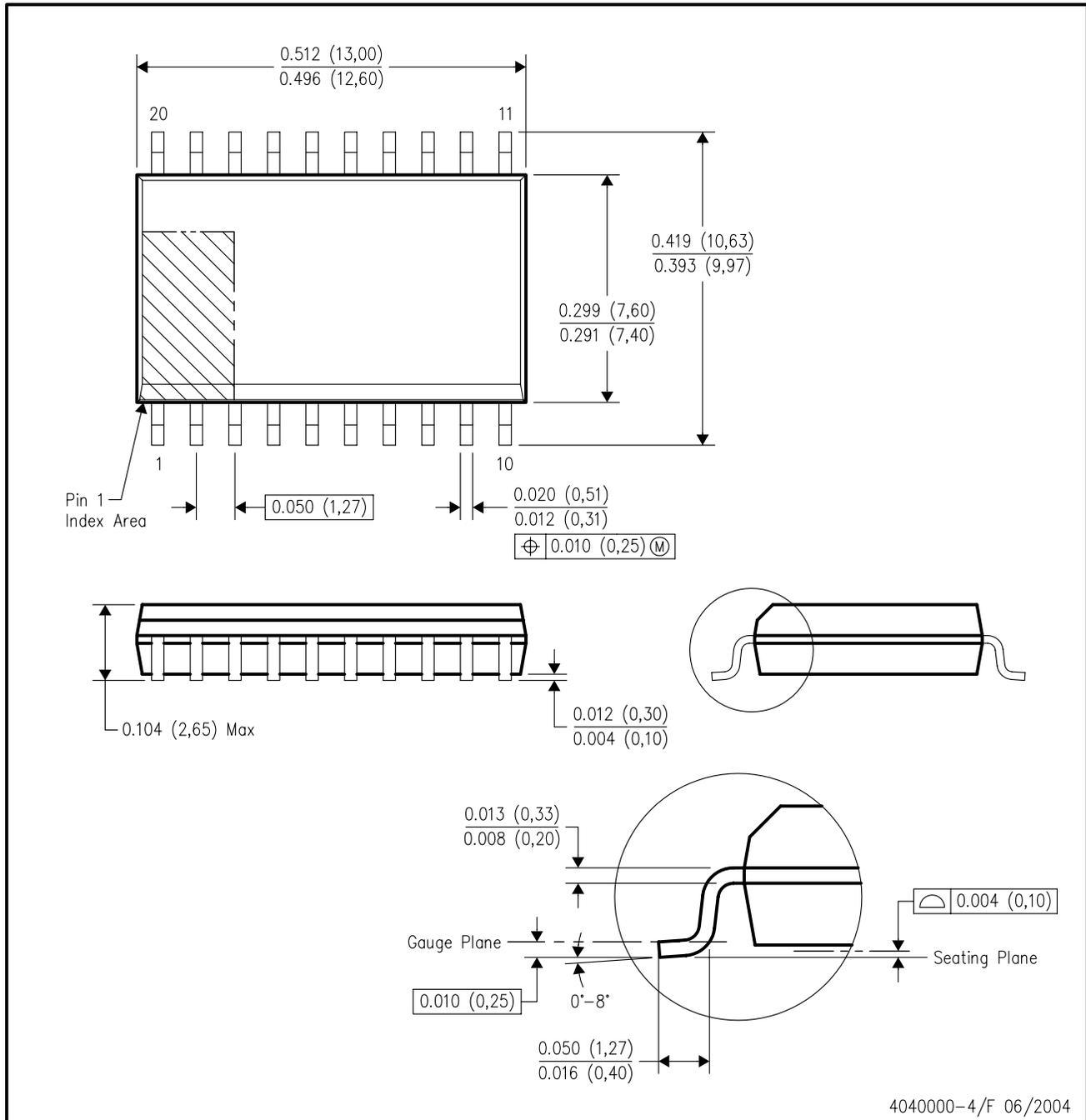
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

⌒ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
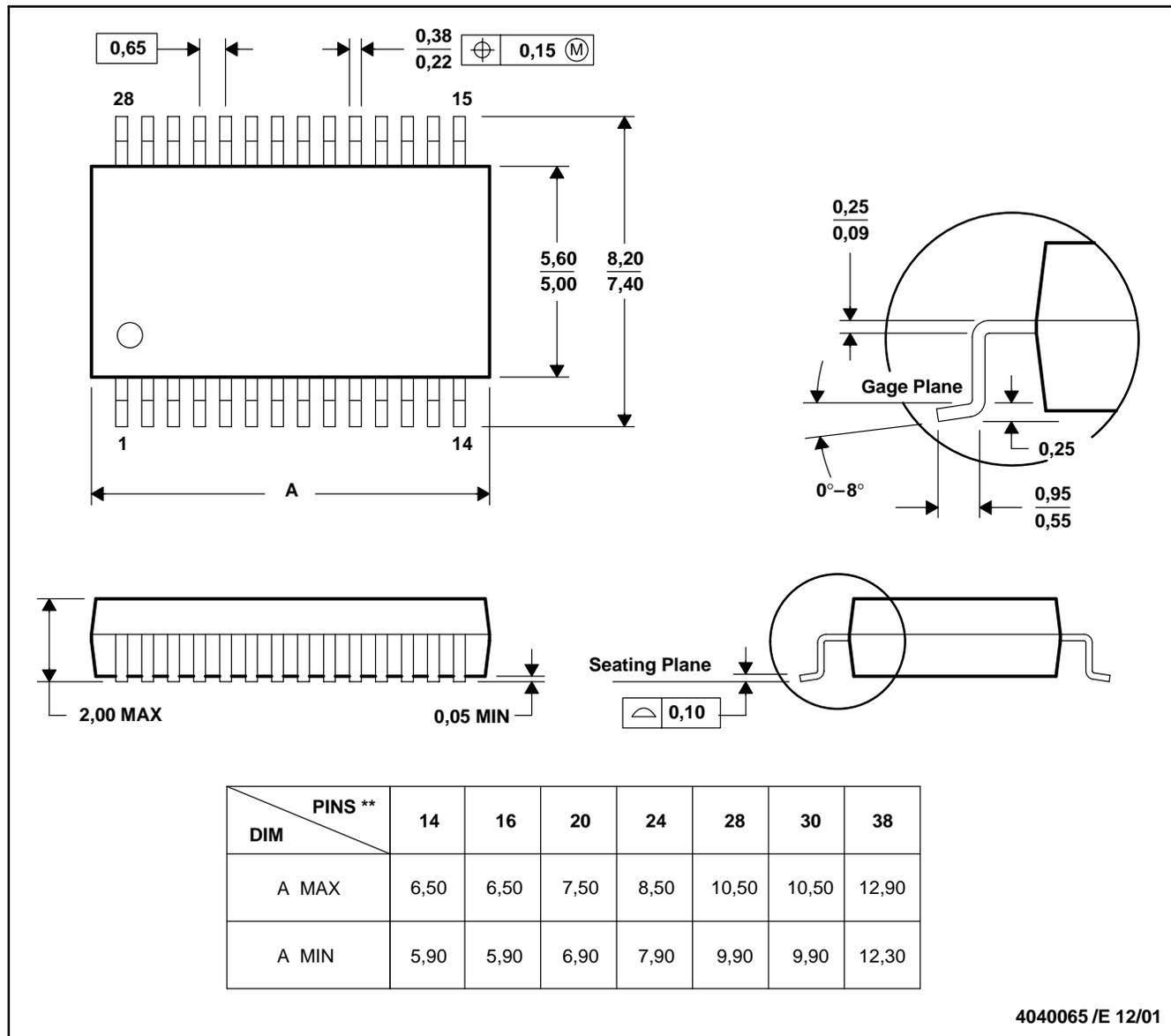   D. Falls within JEDEC MS−013 variation AC.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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