

# MC14001UB, MC14011UB

## UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

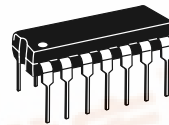
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



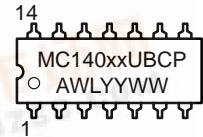
ON Semiconductor®

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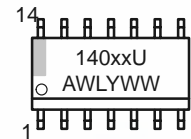
### MARKING DIAGRAMS



PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



xx = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

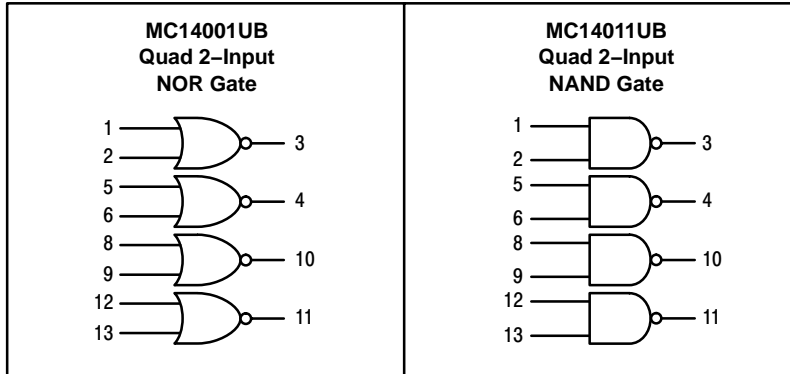
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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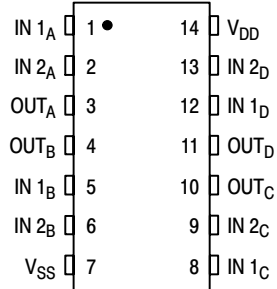
## LOGIC DIAGRAMS



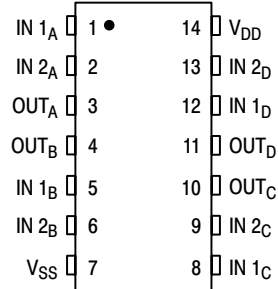
$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7  
 FOR ALL DEVICES

## PIN ASSIGNMENTS

**MC14001UB**  
Quad 2-Input NOR Gate



**MC14011UB**  
Quad 2-Input NAND Gate



# MC14001UB, MC14011UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	-	1.0	-	2.25	1.0	-	1.0	Vdc
		10	-	2.0	-	4.50	2.0	-	2.0	
		15	-	2.5	-	6.75	2.5	-	2.5	
	"1" Level I <sub>IH</sub>	5.0	4.0	-	4.0	2.75	-	4.0	-	Vdc
		10	8.0	-	8.0	5.50	-	8.0	-	
		15	12.5	-	12.5	8.25	-	12.5	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mAdc
		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
		10	-0.62	-	-0.5	-0.9	-	-0.35	-	
	Sink I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	
		15	4.2	-	3.4	8.8	-	2.4	-	
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	0.25	-	0.0005	0.25	-	7.5	µAdc
		10	-	0.5	-	0.0010	0.5	-	15	
		15	-	1.0	-	0.0015	1.0	-	30	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 µA/kHz) f + I <sub>DD</sub> /N							µAdc
10	I <sub>T</sub> = (0.6 µA/kHz) f + I <sub>DD</sub> /N									
15	I <sub>T</sub> = (0.8 µA/kHz) f + I <sub>DD</sub> /N									

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in µH (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

## SWITCHING CHARACTERISTICS (Note 5) (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time t <sub>TLH</sub> = (3.0 ns/pF) C <sub>L</sub> + 30 ns t <sub>TLH</sub> = (1.5 ns/pF) C <sub>L</sub> + 15 ns t <sub>TLH</sub> = (1.1 ns/pF) C <sub>L</sub> + 10 ns	t <sub>TLH</sub>	5.0	-	180	360	ns
		10	-	90	180	
		15	-	65	130	
Output Fall Time t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	t <sub>THL</sub>	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
Propagation Delay Time t <sub>PLH</sub> , t <sub>PHL</sub> = (1.7 ns/pF) C <sub>L</sub> + 30 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.66 ns/pF) C <sub>L</sub> + 22 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.50 ns/pF) C <sub>L</sub> + 15 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	-	90	180	ns
		10	-	50	100	
		15	-	40	80	

5. The formulas given are for the typical characteristics only at 25°C.

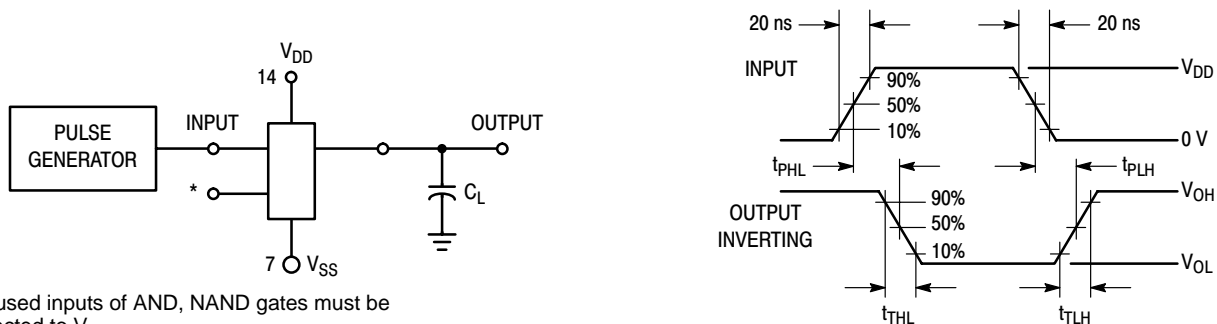
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## MC14001UB, MC14011UB

### ORDERING INFORMATION

Device	Package	Shipping†
MC14001UBCP	PDIP-14	500 Units / Rail
MC14001UBCPG	PDIP-14 (Pb-Free)	500 Units / Rail
MC14001UBD	SOIC-14	55 Units / Rail
MC14001UBDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14001UBDR2	SOIC-14	2500 / Tape & Reel
MC14001UBDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC14011UBCP	PDIP-14	500 Units / Rail
MC14011UBCPG	PDIP-14 (Pb-Free)	500 Units / Rail
MC14011UBD	SOIC-14	55 Units / Rail
MC14011UBDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14011UBDR2	SOIC-14	2500 / Tape & Reel
MC14011UBDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

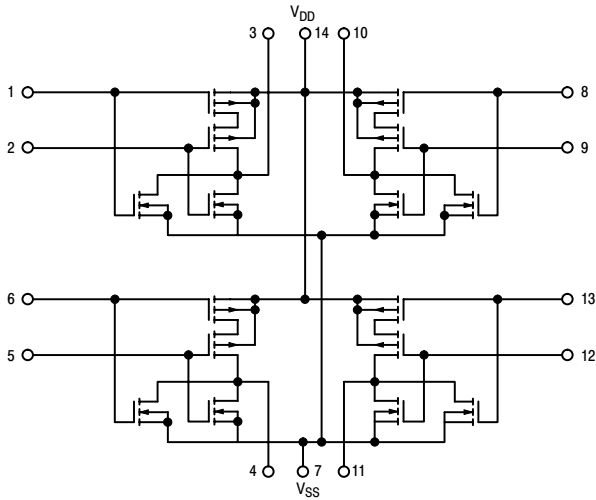


\*All unused inputs of AND, NAND gates must be connected to  $V_{DD}$ .  
All unused inputs of OR, NOR gates must be connected to  $V_{SS}$ .

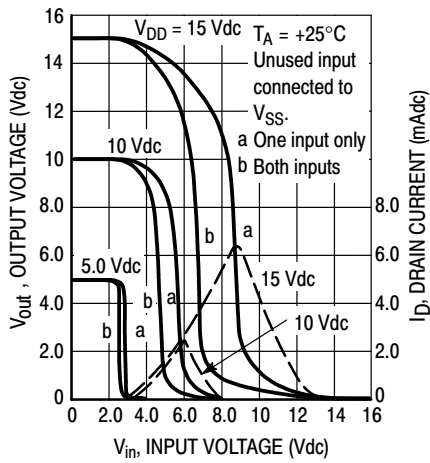
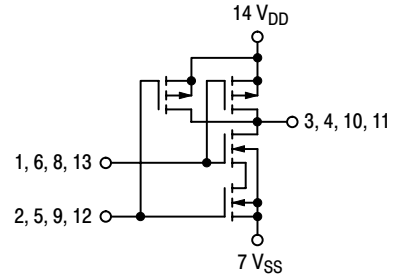
**Figure 1. Switching Time Test Circuit and Waveforms**

# MC14001UB, MC14011UB

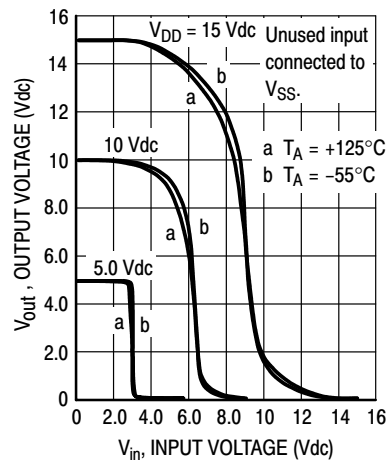
**MC14001UB CIRCUIT SCHEMATIC**



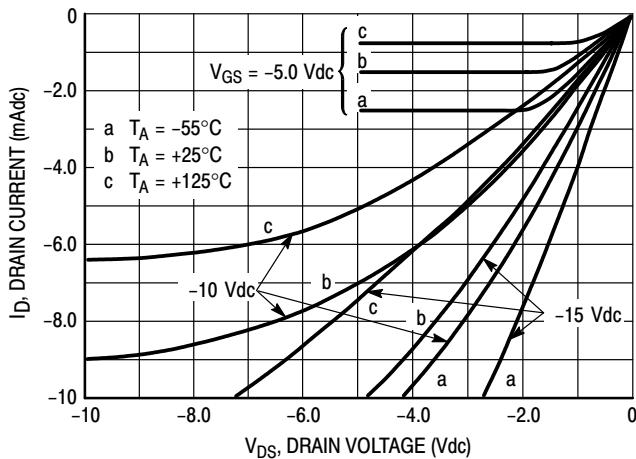
**MC14011UB CIRCUIT SCHEMATIC  
(1/4 of Device Shown)**



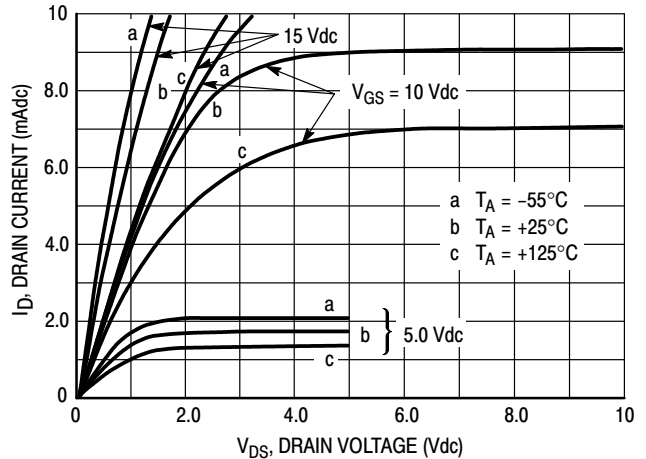
**Figure 2. Typical Voltage and Current Transfer Characteristics**



**Figure 3. Typical Voltage Transfer Characteristics versus Temperature**



**Figure 4. Typical Output Source Characteristics**

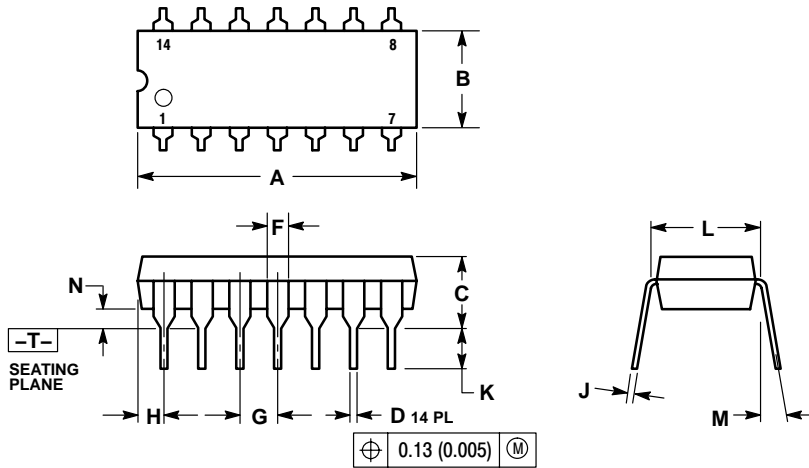


**Figure 5. Typical Output Sink Characteristics**

# MC14001UB, MC14011UB

## PACKAGE DIMENSIONS

**P SUFFIX**  
 PLASTIC DIP PACKAGE  
 CASE 646-06  
 ISSUE N



**NOTES:**

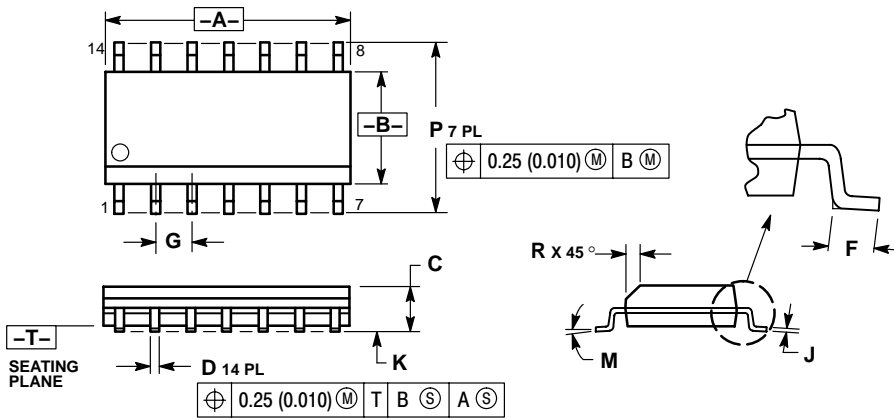
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---		10°	
N	0.015	0.039	0.38	1.01

# MC14001UB, MC14011UB

## PACKAGE DIMENSIONS


**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751A-03  
 ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

## MC14001UB, MC14011UB

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