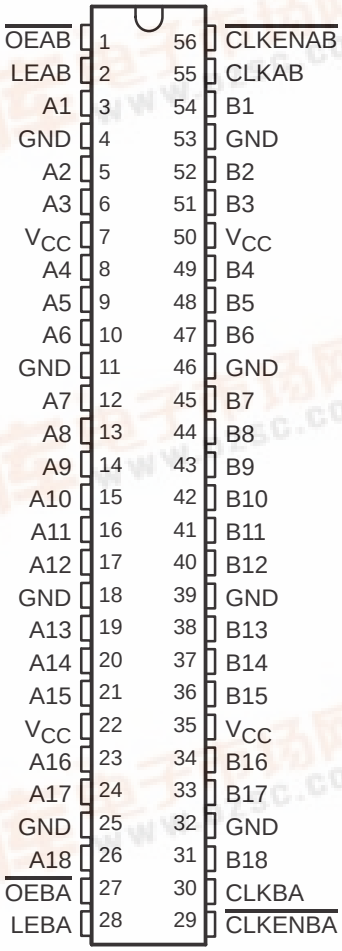
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16601 . . . WD PACKAGE
SN74ABT16601 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16601 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16601 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

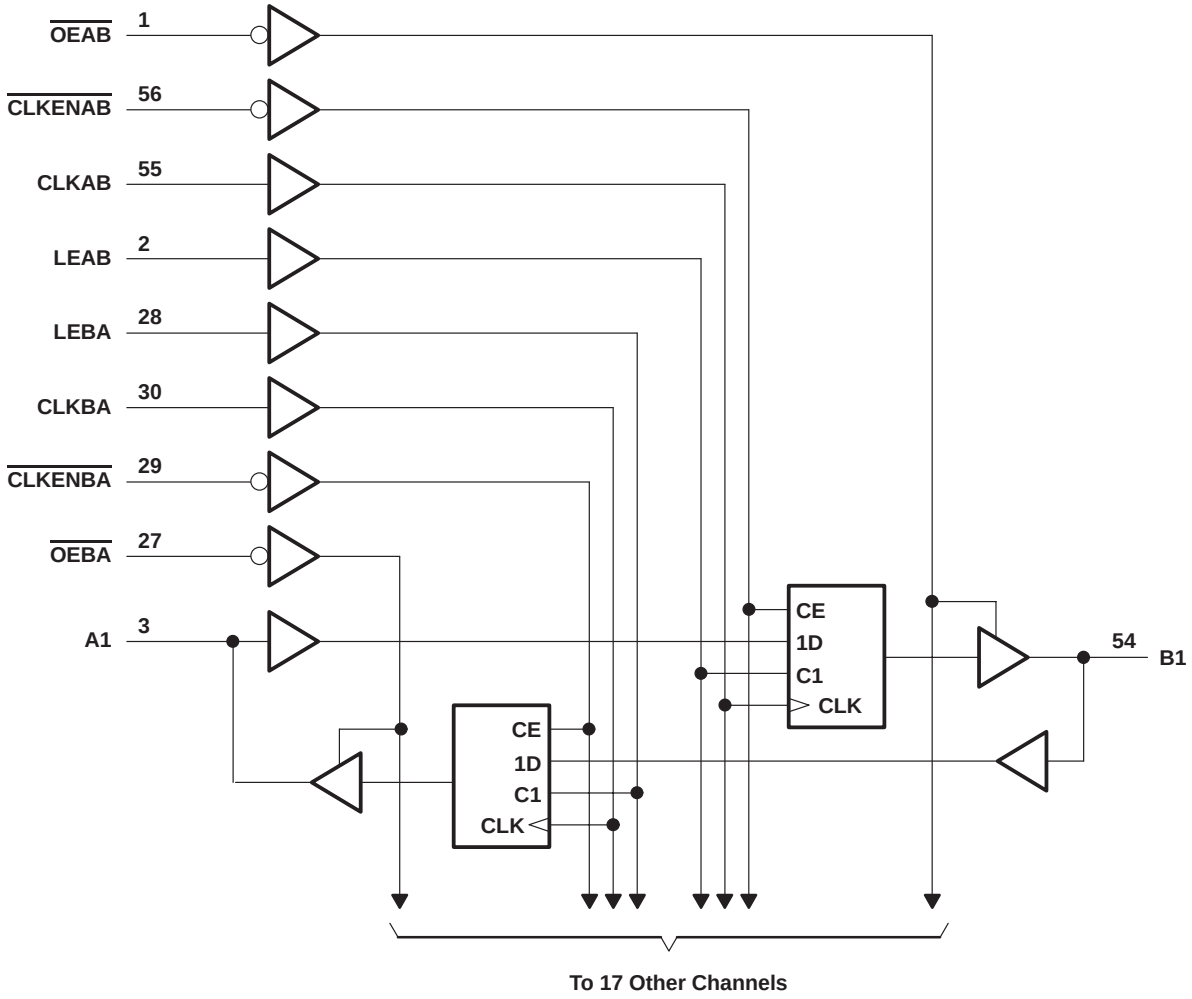
INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16601 . . . . . 96 mA
SN74ABT16601 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 81°C/W
DL package . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT16601		SN74ABT16601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT16601		SN74ABT16601		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
	A or B ports					±20**		±100		±20	
I_{off}		V_{CC} = 0,	V_I or $V_O \le$ 4.5 V			±100				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V			–10		–10		–10	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		1.9	3		2		3	mA
			Outputs low		28	36		35		36	
			Outputs disabled		1.6	3		2		3	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50				50	µA
								1.5			mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** This limit applies only to the SN74ABT16601.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16601		SN74ABT16601		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3		3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4.6		4		ns
		A before LEAB↓ or B before LEBA↓	CLK high	2.5		2.5		
			CLK low	1.3		1		
		$\overline{CLKEN}$ before CLK↑		2.9		2.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0.4		0		ns
		A after LEAB↓ or B after LEBA↓		2.8		2		
		$\overline{CLKEN}$ after CLK↑		0		0		

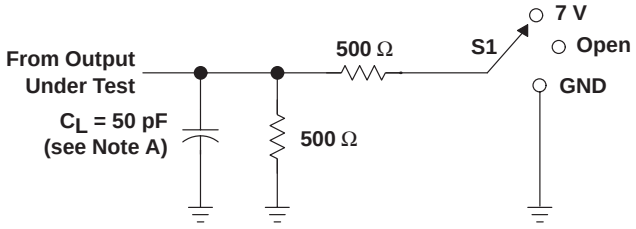
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16601					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150	200		150		MHz
t_{PLH}	A or B	B or A	1.5	2.5	4.1	1	4.6	ns
t_{PHL}			1.5	3.4	4.7	1	5.1	
t_{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	1	5.6	ns
t_{PHL}			2	3.7	5	1	5.5	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1	5.2	ns
t_{PHL}			1.5	3.2	4.4	1	5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4	5	1	5.7	ns
t_{PZL}			2	4.2	5.6	1	6	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.8	1	6.8	ns
t_{PLZ}			1.5	3.4	5.3	1	6.3	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

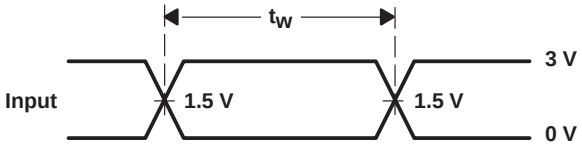
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16601					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150	200		150		MHz
t_{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4	ns
t_{PHL}			1.5	3.4	4.7	1.5	4.9	
t_{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	2	5	ns
t_{PHL}			2	3.7	5	2	5.2	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1.5	4.7	ns
t_{PHL}			1.5	3.2	4.4	1.5	4.6	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4	5	2	5.5	ns
t_{PZL}			2	4.2	5.6	2	5.8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.4	2	6.2	ns
t_{PLZ}			1.5	3.4	4.7	1.5	5.4	

PARAMETER MEASUREMENT INFORMATION

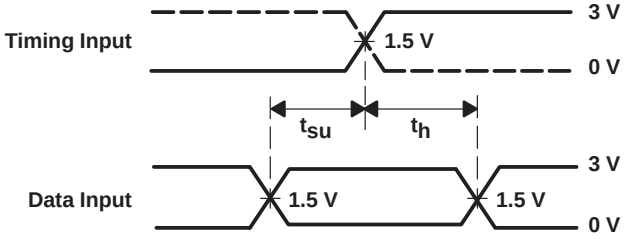


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

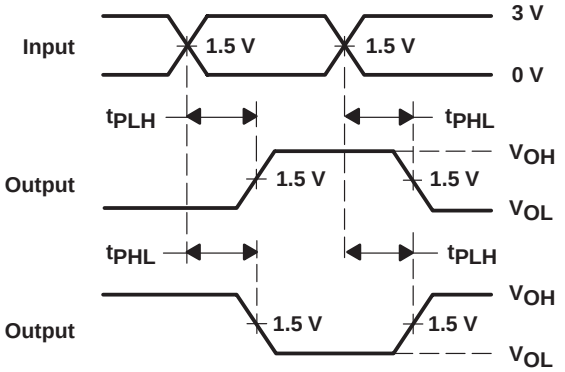
LOAD CIRCUIT



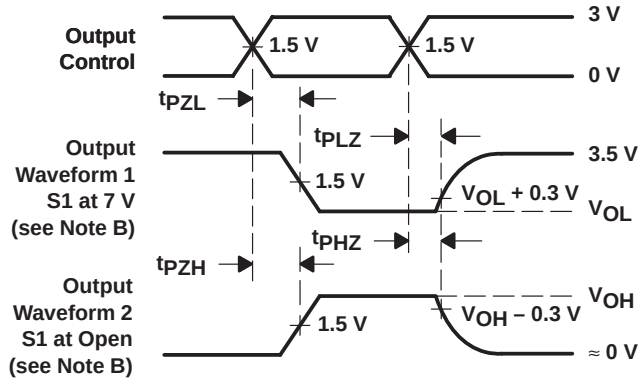
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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