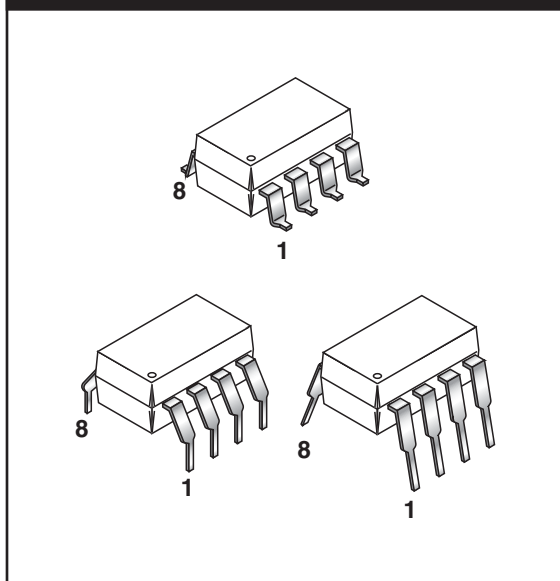
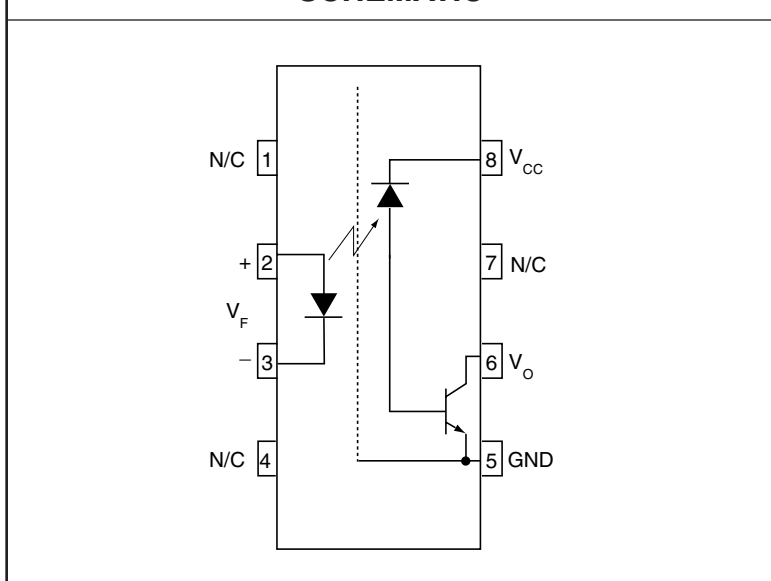


HCPL4503M

PACKAGE



SCHEMATIC



DESCRIPTION

The HCPL4503M optocoupler consists of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor. The base of the phototransistor is not bonded out to a pin for improved noise immunity.

An internal noise shield provides superior common mode rejection of 15kV/μs minimum.

FEATURES

- VISO = 5kV RMS is standard for all devices
- High speed-1 MBit/s
- Superior CMR, $CM_H = 50 \text{ kV/ms}$ (typical); $CM_L = 30 \text{ kV/ms}$ (typical)
- No base connection for improved noise immunity
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700, Vol 2)
- VDE approval pending

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

HCPL4503M

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T_{STG}	-40 to +125	$^\circ\text{C}$
Operating Temperature	T_{OPR}	-40 to +100	$^\circ\text{C}$
Lead Solder Temperature	T_{SOL}	260 for 10 sec	$^\circ\text{C}$
EMITTER			
DC/Average Forward Input Current	I_F (avg)	25	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	I_F (pk)	50	mA
Peak Transient Input Current - ($\leq 1 \mu\text{s}$ P.W., 300 pps)	I_F (trans)	1.0	A
Reverse Input Voltage	V_R	5	V
Input Power Dissipation	P_D	100	mW
DETECTOR			
Average Output Current	I_O (avg)	8	mA
Peak Output Current	I_O (pk)	16	mA
Supply Voltage	V_{CC}	-0.5 to 30	V
Output Voltage	V_O	-0.5 to 20	V
Output power dissipation	P_D	100	mW

HCPL4503M

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
EMITTER						
Input Forward Voltage	($I_F = 16 \text{ mA}$, $T_A = 25^\circ\text{C}$)	V_F		1.45	1.7	V
	($I_F = 16 \text{ mA}$)				1.8	
Input Reverse Breakdown Voltage	($I_R = 10 \mu\text{A}$)	B_{VR}	5.0			V
Temperature coefficient of forward voltage	($I_F = 16 \text{ mA}$)	$(\Delta V_F / \Delta T_A)$		-1.6		mV/ $^\circ\text{C}$
DETECTOR						
Logic high output current	($I_F = 0 \text{ mA}$, $V_O = V_{CC} = 5.5 \text{ V}$) ($T_A = 25^\circ\text{C}$)	I_{OH}		0.001	0.5	μA
	($I_F = 0 \text{ mA}$, $V_O = V_{CC} = 15 \text{ V}$) ($T_A = 25^\circ\text{C}$)			0.005	1	
	($I_F = 0 \text{ mA}$, $V_O = V_{CC} = 15 \text{ V}$)				50	
Logic low supply current	($I_F = 16 \text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15 \text{ V}$)	I_{CCL}		120	200	μA
Logic high supply current	($I_F = 0 \text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15 \text{ V}$) ($T_A = 25^\circ\text{C}$)	I_{CCH}			1	μA
	($I_F = 0 \text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15 \text{ V}$)				2	

** All Typicals at $T_A = 25^\circ\text{C}$

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TRANSFER CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)						
Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
COUPLED Current transfer ratio (Note 5)	($I_F = 16\text{ mA}$, $V_O = 0.4\text{ V}$) (Note 1) ($V_{CC} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$)	CTR	19	27	50	%
	($I_F = 16\text{ mA}$, $V_{CC} = 4.5\text{ V}$, $V_{OL} = 0.5\text{ V}$)		15	30		
Logic low output voltage output voltage	($I_F = 16\text{ mA}$, $I_O = 3\text{ mA}$) ($V_{CC} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$)	V_{OL}			0.5	V
	($I_F = 16\text{ mA}$, $I_O = 2.4\text{ mA}$) ($V_{CC} = 4.5\text{ V}$)				0.5	

** All Typical at $T_A = 25^\circ\text{C}$

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C unless otherwise specified., $V_{CC} = 5\text{ V}$)						
Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
Propagation delay time to logic low	($R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 2) (Fig. 7) $T_A = 25^\circ\text{C}$	T_{PHL}		0.45	0.8	μs
	($R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 2) (Fig. 7)				1.0	μs
Propagation delay time to logic high	($R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 2) (Fig. 7) $T_A = 25^\circ\text{C}$	T_{PLH}		0.3	0.8	μs
	($R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 2) (Fig. 7)				1.0	μs
Common mode transient immunity at logic high	($I_F = 0\text{ mA}$, $V_{CM} = 1,500\text{ V}_{P-P}$) $T_A = 25^\circ\text{C}$, ($R_L = 1.9\text{ k}\Omega$) (Note 3) (Fig. 8)	ICM_{HI}	15,000	50,000		$\text{V}/\mu\text{s}$
Common mode transient immunity at logic low	($I_F = 16\text{ mA}$, $V_{CM} = 1,500\text{ V}_{P-P}$) ($R_L = 1.9\text{ k}\Omega$) (Note 3) (Fig. 8)	ICM_{LI}	15,000	30,000		$\text{V}/\mu\text{s}$

** All Typical at $T_A = 25^\circ\text{C}$

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ISOLATION CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)						
Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) ($T_A = 25^\circ\text{C}$, $t = 5$ s) ($V_{I-O} = 3000$ VDC) (Note 4)	I_{I-O}			1.0	μA
Withstand insulation test voltage	($RH \leq 50\%$, $T_A = 25^\circ\text{C}$) (Note 4) ($t = 1$ min.)	V_{ISO}	5,000			V_{RMS}
Resistance (input to output)	(Note 9) ($V_{I-O} = 500$ VDC)	R_{I-O}		10^{12}		Ω
Capacitance (input to output)	(Note 4) ($f = 1$ MHz)	C_{I-O}		0.6		pF

Notes

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
2. The $1.9\text{ k}\Omega$ load represents 1 TTL unit load of 1.6 mA and $5.6\text{ k}\Omega$ pull-up resistor.
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{ V}$).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.

HCPL4503M

Fig. 1 Normalized CTR vs. Forward Current

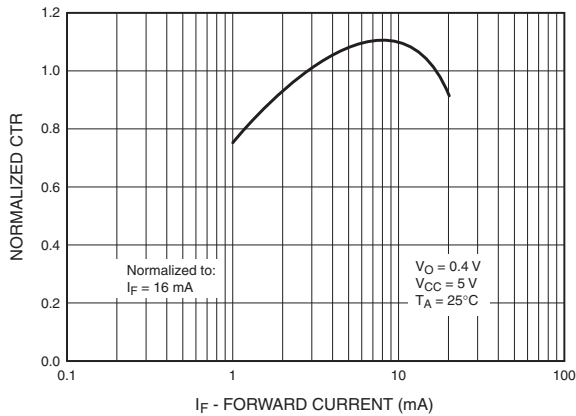


Fig. 2 Normalized CTR vs. Temperature

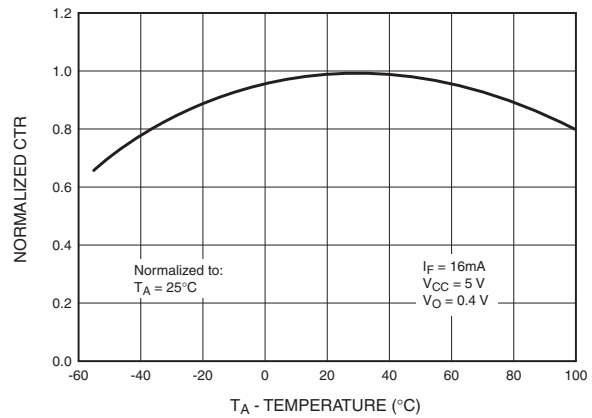


Fig. 3 Output Current vs. Output Voltage

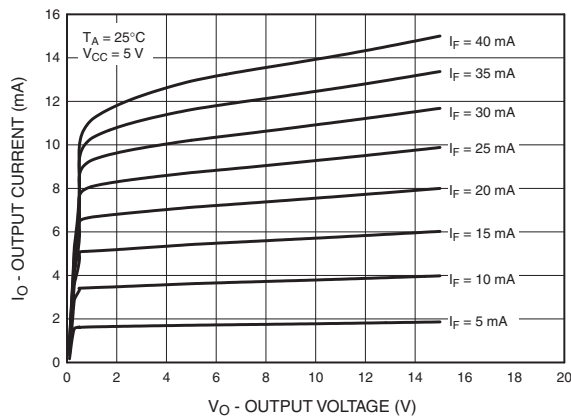


Fig. 4 Logic High Output Current vs. Temperature

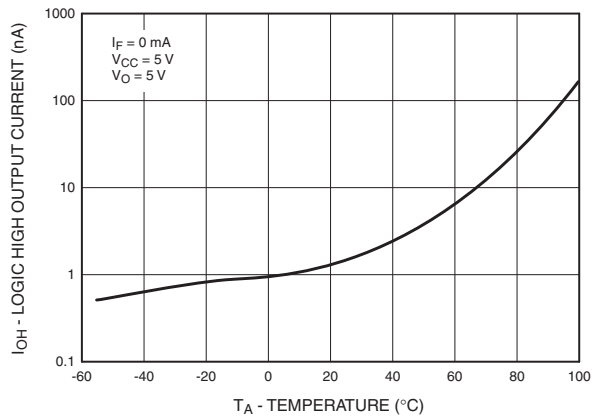


Fig. 5 Propagation Delay vs. Temperature

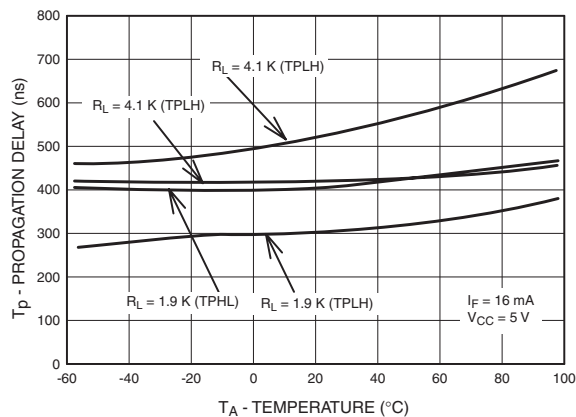
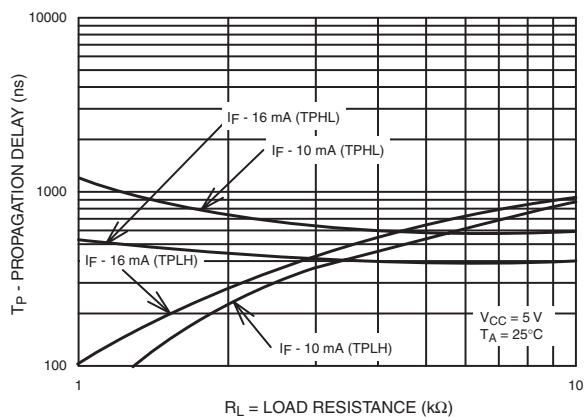


Fig. 6 Propagation Delay vs. Load Resistance



HCPL4503M

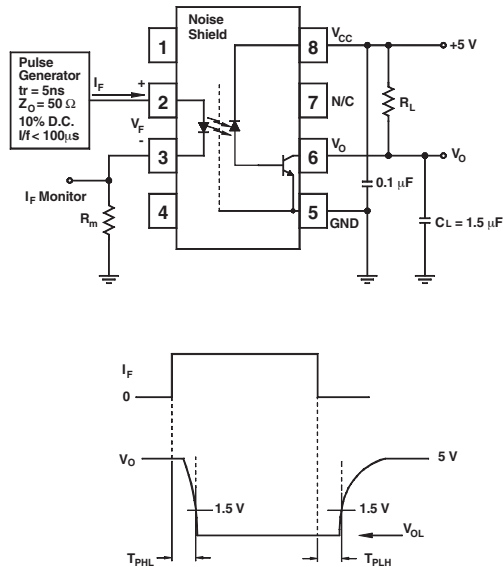


Fig. 7 Switching Time Test Circuit

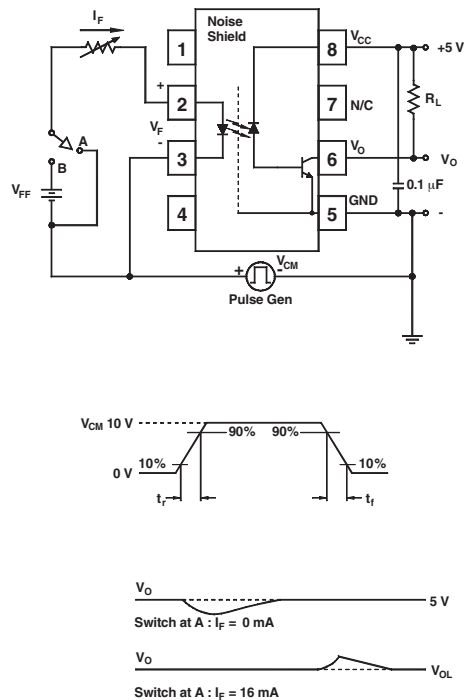
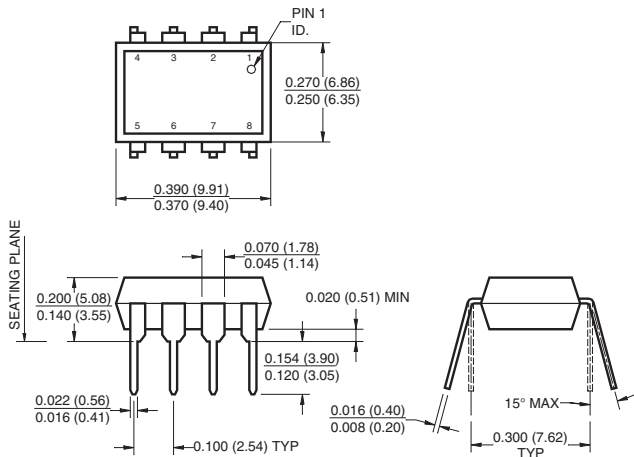


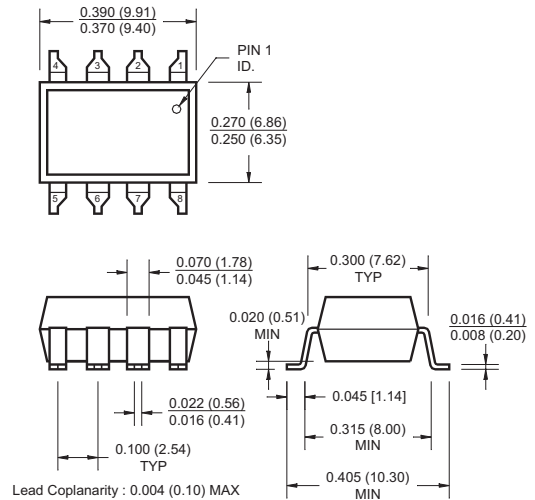
Fig. 8 Common Mode Immunity Test Circuit

HCPL4503M

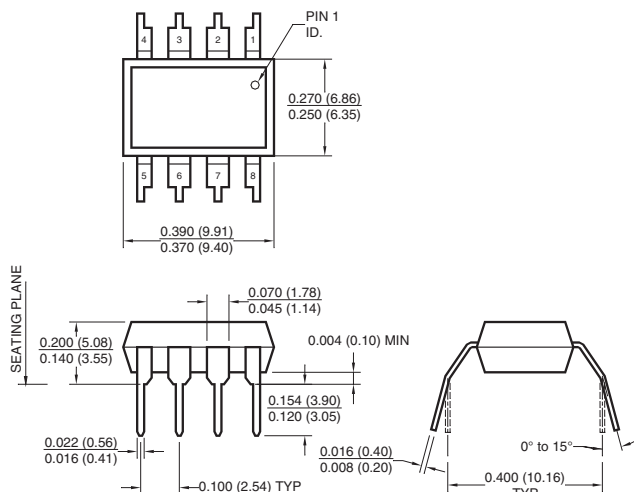
Package Dimensions (Through Hole)



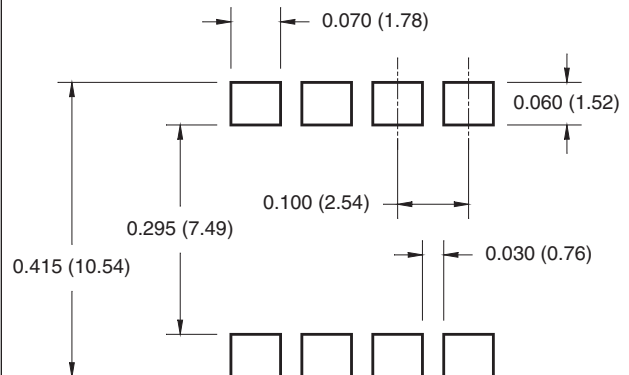
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



8 - Pin Dip



NOTE

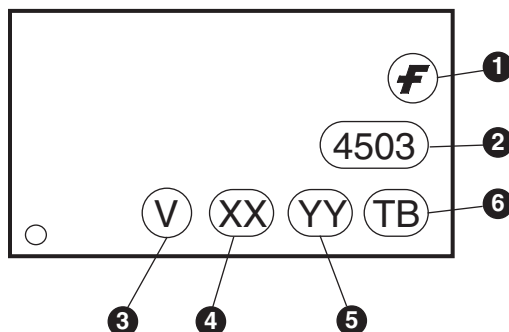
All dimensions are in inches (millimeters)

HCPL4503M

ORDERING INFORMATION

Option	Example Part Number	Description
S	HCPL4503SM	Surface Mount Lead Bend
SD	HCPL4503SDM	Surface Mount; Tape and reel (1,000 units per reel)
T	HCPL4503TM	0.4" Lead Spacing
V	HCPL4503VM	VDE0884 (approval pending)
TV	HCPL4503TVM	VDE0884 (approval pending); 0.4" lead spacing
SV	HCPL4503SVM	VDE0884 (approval pending); surface mount
SDV	HCPL4503SDVM	VDE0884 (approval pending); surface mount; tape and reel (1,000 units per reel)

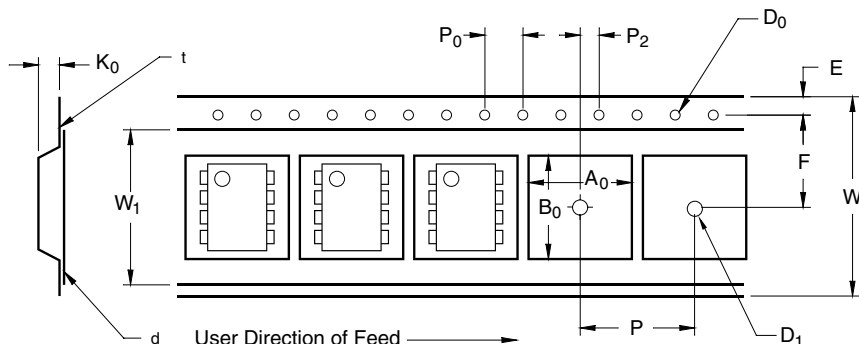
MARKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

HCPL4503M

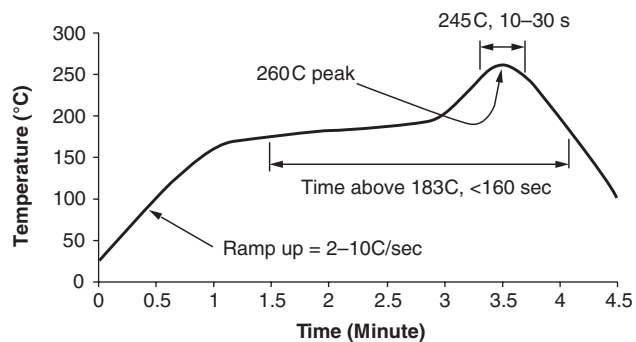
Carrier Tape Specifications



Description	Symbol	Dimension in mm
Tape Width	W	16.0 ± 0.3
Tape Thickness	t	0.30 ± 0.05
Sprocket Hole Pitch	P ₀	4.0 ± 0.1
Sprocket Hole Diameter	D ₀	1.55 ± 0.05
Sprocket Hole Location	E	1.75 ± 0.10
Pocket Location	F	7.5 ± 0.1
	P ₂	4.0 ± 0.1
Pocket Pitch	P	12.0 ± 0.1
Pocket Dimensions	A ₀	10.30 ± 0.20
	B ₀	10.30 ± 0.20
	K ₀	4.90 ± 0.20
Cover Tape Width	W ₁	1.6 ± 0.1
Cover Tape Thickness	d	0.1 max
Max. Component Rotation or Tilt		10°
Min. Bending Radius	R	30

HCPL4503M

Reflow Profile



- Peak reflow temperature: 260°C (package surface temperature)
- Time of temperature higher than 183°C for 160 seconds or less
- One time soldering reflow is recommended

HCPL4503M

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