NEC

MOS INTEGRATED CIRCUIT

# μPD753104, 753106, 753108

## 4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD753108 is one of the 75XL Series 4-bit single-chip microcontroller chips and has a data processing capability comparable to that of an 8-bit microcontroller.

The existing 75X Series containing an LCD controller/driver supplies an 80-pin package.

The μPD753108 supplies a 64-pin package (12 x 12 mm), which is suitable for small-scale systems.

It features expanded CPU functions and can provide high-speed operation at a low supply voltage of 1.8 V compared with the existing μPD75308B.

**For detailed function descriptions, refer to the following user's manual. Be sure to read the document before designing.**

**μPD753108 User's Manual: U10890E**

### Features

- ○ Low voltage operation: $V_{DD}$ = 1.8 to 5.5 V
  - • Can be driven by two 1.5-V batteries
- ○ On-chip memory
  - • Program memory (ROM):
    - 4096 x 8 bits (μPD753104)
    - 6144 x 8 bits (μPD753106)
    - 8192 x 8 bits (μPD753108)
  - • Data memory (RAM):
    - 512 x 4 bits
- ○ Capable of high-speed operation and variable instruction execution time for power saving
  - • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz with main system clock)
  - • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz with main system clock)
  - • 122 μs (@ 32.768 kHz with subsystem clock)
- ○ Internal programmable LCD controller/driver
- ○ Small package:
  - 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)
- ○ One-time PROM version: μPD75P3116

### Application

Remote controllers, cameras, hemadynamometers, electronic scale, gas meters, etc.

**Unless otherwise indicated, references in this data sheet to the μPD753108 mean the μPD753104 and μPD753106.**



**The mark ★ shows major revised points.**

Document No. U10086EJ3V0DS00 (3rd edition)
Date Published April 1997 N
Printed in Japan

## Ordering Information

| Part number | Package | ROM (x 8 bits) |
|---|---|---|
| μPD753104GC-xxx-AB8 | 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) | 4096 |
| μPD753104GK-xxx-8A8 | 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) | 4096 |
| μPD753106GC-xxx-AB8 | 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) | 6144 |
| μPD753106GK-xxx-8A8 | 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) | 6144 |
| μPD753108GC-xxx-AB8 | 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) | 8192 |
| μPD753108GK-xxx-8A8 | 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) | 8192 |

**Remark** xxx indicates the ROM code suffix.

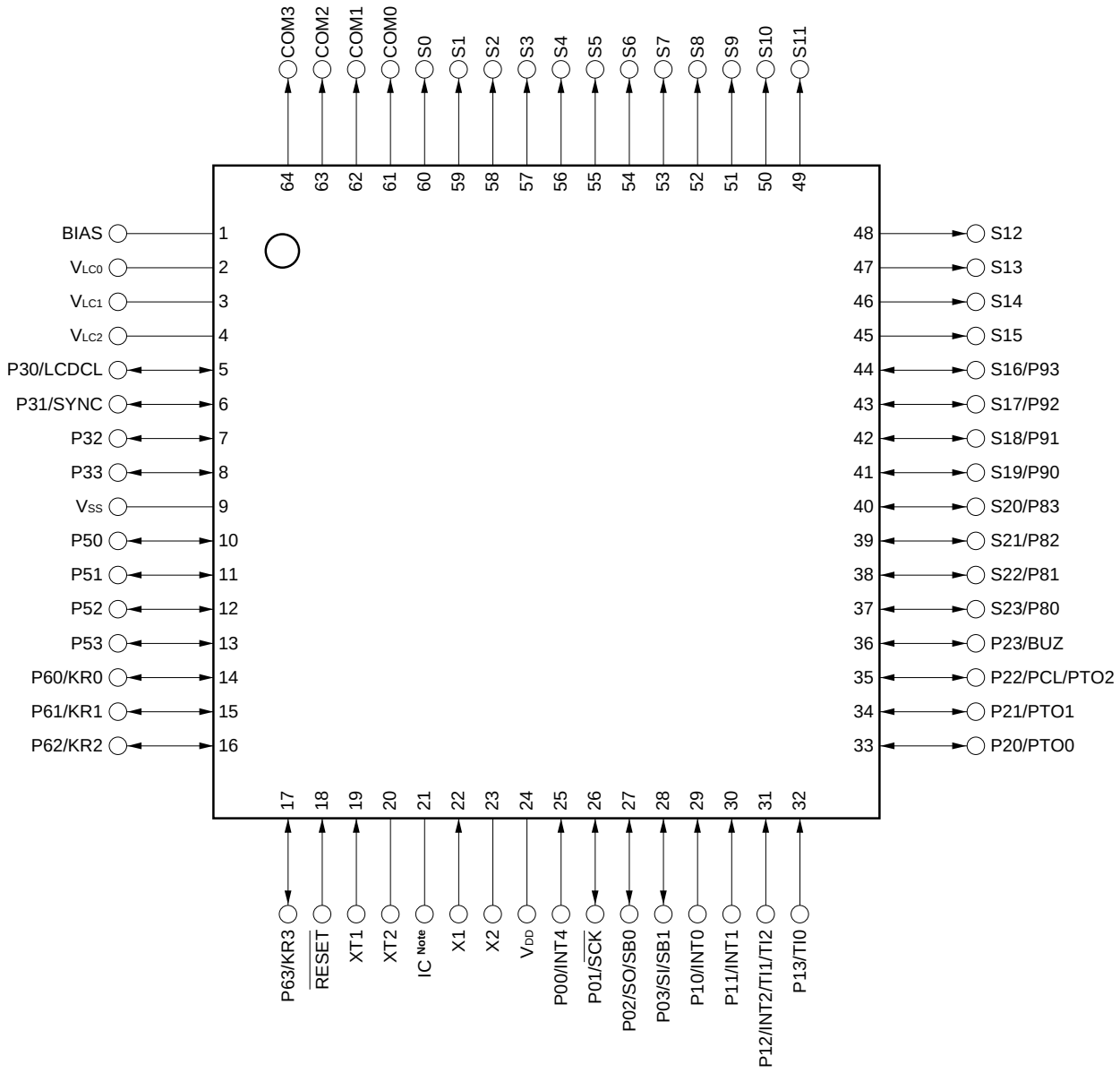
## Functional Outline

| Parameter | | | Function |
|---|---|---|---|
| Instruction execution time | | | • 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz with main system clock)<br>• 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz with main system clock)<br>• 122 μs (@ 32.768 kHz with subsystem clock) |
| On-chip memory | ROM | | 4096 x 8 bits (μPD753104) |
| | | | 6144 x 8 bits (μPD753106) |
| | | | 8192 x 8 bits (μPD753108) |
| | RAM | | 512 x 4 bits |
| General-purpose register | | | • 4-bit operation: 8 x 4 banks<br>• 8-bit operation: 4 x 4 banks |
| Input/ output port | CMOS input | 8 | On-chip pull-up resistors which can be specified by software: 7 |
| | CMOS input/output | 20 | On-chip pull-up resistors which can be specified by software: 12<br>Also used for segment pins: 8 |
| | N-ch open-drain input/output pins | 4 | On-chip pull-up resistors which can be specified by mask option, 13-V withstand voltage |
| | Total | 32 | |
| LCD controller/driver | | | • Segment selection: 16/20/24 segments (can be changed to CMOS input/ output port in 4 time-unit; max. 8)<br>• Display mode selection: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) |
| | | | • On-chip split resistor for LCD drive can be specified by mask option |
| Timer | | | 5 channels<br>• 8-bit timer/event counter: 3 channels (16-bit timer/event counter, carrier generator, timer with gate)<br>• Basic interval timer/watchdog timer: 1 channel<br>• Watch timer: 1 channel |
| Serial interface | | | • 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit<br>• 2-wire serial I/O mode<br>• SBI mode |
| Bit sequential buffer (BSB) | | | 16 bits |
| Clock output (PCL) | | | • Φ, 524, 262, 65.5 kHz (@ 4.19 MHz with main system clock)<br>• Φ, 750, 375, 93.8 kHz (@ 6.0 MHz with main system clock) |
| Buzzer output (BUZ) | | | • 2, 4, 32 kHz (@ 4.19 MHz with main system clock or @ 32.768 kHz with subsystem clock)<br>• 2.93, 5.86, 46.9 kHz (@ 6.0 MHz with main system clock) |
| Vectored interrupt | | | External: 3, Internal: 5 |
| Test input | | | External: 1, Internal: 1 |
| System clock oscillator | | | • Ceramic or crystal oscillator for main system clock oscillation<br>• Crystal oscillator for subsystem clock oscillation |
| Standby function | | | STOP/HALT mode |
| Supply voltage | | | $V_{DD}$ = 1.8 to 5.5 V |
| Package | | | • 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)<br>• 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) |

CONTENTS

## 1. PIN CONFIGURATION (Top View)

- **64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)**
  **μPD753104GC-xxx-AB8, μPD753106GC-xxx-AB8,**
  **μPD753108GC-xxx-AB8**
- **64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)**
  **μPD753104GK-xxx-8A8, μPD753106GK-xxx-8A8,**
  **μPD753108GK-xxx-8A8**



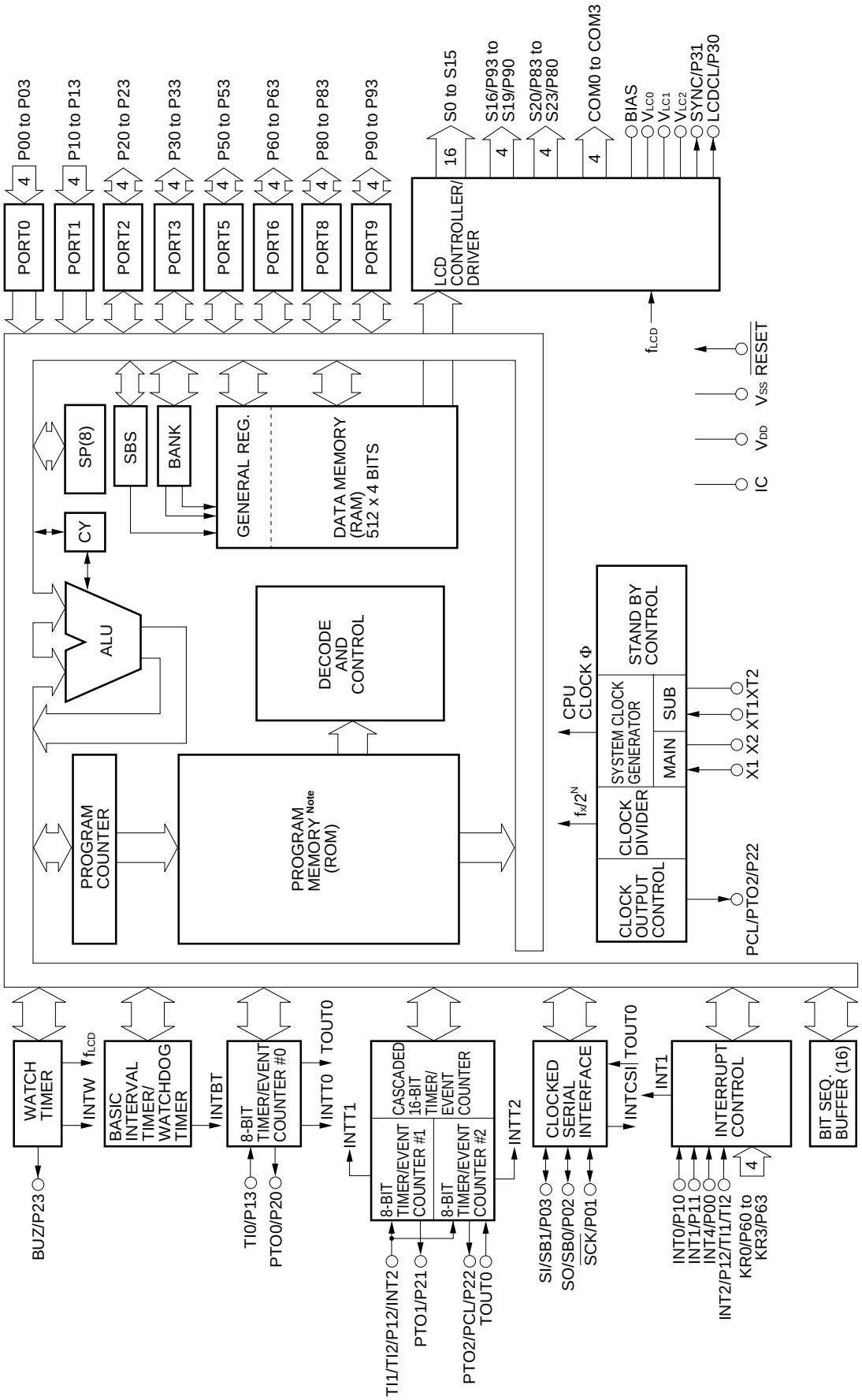

**Note** Connect the IC (Internally Connected) pin directly to $V_{DD}$.

**Pin Identification**

P00 to P03 : Port 0
P10 to P13 : Port 1
P20 to P23 : Port 2
P30 to P33 : Port 3
P50 to P53 : Port 5
P60 to P63 : Port 6
P80 to P83 : Port 8
P90 to P93 : Port 9
KR0 to KR3 : Key Return 0 to 3
$\overline{SCK}$ : Serial Clock
SI : Serial Input
SO : Serial Output
SB0, SB1 : Serial Data Bus 0, 1
$\overline{RESET}$ : Reset
S0 to S23 : Segment Output 0 to 23
COM0 to COM3 : Common Output 0 to 3

$V_{LC0}$ to $V_{LC2}$ : LCD Power Supply 0 to 2
BIAS : LCD Power Supply Bias Control
LCDCL : LCD Clock
SYNC : LCD Synchronization
TI0 to TI2 : Timer Input 0 to 2
PTO0 to PTO2 : Programmable Timer Output 0 to 2
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0, INT1, INT4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
X1, X2 : Main System Clock Oscillation 1, 2
XT1, XT2 : Subsystem Clock Oscillation 1, 2
$V_{DD}$ : Positive Power Supply
$V_{SS}$ : Ground
IC : Internally Connected

## 2. BLOCK DIAGRAM




**Note** The ROM capacity depends on the product.

## 3. PIN FUNCTIONS

### 3.1 Port Pins (1/2)

| Pin Name | Input/Output | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|---|
| P00 | Input | INT4 | 4-bit input port (PORT0).<br>For P01 to P03, connection of on-chip pull-up resistors can be specified by software in 3-bit units. | No | Input | (B) |
| P01 | Input/Output | $\overline{SCK}$ | | | | (F)-A |
| P02 | Input/Output | SO/SB0 | | | | (F)-B |
| P03 | Input/Output | SI/SB1 | | | | (M)-C |
| P10 | Input | INT0 | 4-bit input port (PORT1).<br>Connection of on-chip pull-up resistors can be specified by software in 4-bit units.<br>P10/INT0 can select noise elimination circuit. | No | Input | (B)-C |
| P11 | | INT1 | | | | |
| P12 | | TI1/TI2/INT2 | | | | |
| P13 | | TI0 | | | | |
| P20 | Input/Output | PTO0 | 4-bit input/output port (PORT2).<br>Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | E-B |
| P21 | | PTO1 | | | | |
| P22 | | PCL/PTO2 | | | | |
| P23 | | BUZ | | | | |
| P30 | Input/Output | LCDCL | Programmable 4-bit input/output port (PORT3).<br>This port can be specified for input/output bit-wise.<br>Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | E-B |
| P31 | | SYNC | | | | |
| P32 | | – | | | | |
| P33 | | – | | | | |
| P50-P53 Note 2 | Input/Output | – | N-ch open-drain 4-bit input/output port (PORT5).<br>A pull-up resistor can be contained bit-wise (mask option).<br>Withstand voltage is 13 V in open-drain mode. | No | High level (when pull-up resistors are provided) or high-impedance | M-D |

**Notes 1.** Characters in parentheses indicate the Schmitt trigger input.

**2.** If on-chip pull-up resistors are not specified by mask option (when used as N-ch open-drain input port), low-level input leakage current increases when input or bit manipulation instruction is executed.

### 3.1 Port Pins (2/2)

| Pin Name | Input/Output | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|---|
| P60 | Input/Output | KR0 | Programmable 4-bit input/output port (PORT6). This port can be specified for input/output bit-wise. Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | (F)-A |
| P61 | | KR1 | | | | |
| P62 | | KR2 | | | | |
| P63 | | KR3 | | | | |
| P80 | Input/Output | S23 | 4-bit input/output port (PORT8). Connection of on-chip pull-up resistors can be specified by software in 4-bit units Note 2. | Yes | Input | H |
| P81 | | S22 | | | | |
| P82 | | S21 | | | | |
| P83 | | S20 | | | | |
| P90 | Input/Output | S19 | 4-bit input/output port (PORT9). Connection of on-chip pull-up resistors can be specified by software in 4-bit units Note 2. | | Input | H |
| P91 | | S18 | | | | |
| P92 | | S17 | | | | |
| P93 | | S16 | | | | |

**Notes 1.** Characters in parentheses indicate the Schmitt trigger input.

★ **2.** When these pins are used as segment signal output pins, do not connect the on-chip pull-up resistor by software.

### 3.2 Non-port Pins (1/2)

| Pin Name | Input/Output | Alternate Function | Function | | After Reset | I/O Circuit TYPE Note 1 |
|---|---|---|---|---|---|---|
| TI0 | Input | P13 | Inputs external event pulses to the timer/event counter. | | Input | (B)-C |
| TI1 | | P12/INT2/TI2 | | | | |
| TI2 | | P12/INT2/TI1 | | | | |
| PTO0 | Output | P20 | Timer/event counter output | | Input | E-B |
| PTO1 | | P21 | | | | |
| PTO2 | | P22/PCL | | | | |
| PCL | | P22/PTO2 | Clock output | | | |
| BUZ | | P23 | Optional frequency output (for buzzer output or system clock trimming) | | | |
| $\overline{SCK}$ | Input/Output | P01 | Serial clock input/output | | Input | (F)-A |
| SO/SB0 | | P02 | Serial data output<br>Serial data bus input/output | | | (F)-B |
| SI/SB1 | | P03 | Serial data input<br>Serial data bus input/output | | | (M)-C |
| INT4 | Input | P00 | Edge detection vectored interrupt input (both rising edge and falling edge detection) | | Input | (B) |
| INT0 | Input | P10 | Edge detection vectored interrupt input (detection edge can be selected). INT0/P10 can select noise elimination circuit. | Noise elimination circuit/ asynchronous selection | Input | (B)-C |
| INT1 | | P11 | | Asynchronous | | |
| INT2 | | P12/TI1/TI2 | Rising edge detection testable input | Asynchronous | | |
| KR0-KR3 | Input | P60-P63 | Falling edge detection testable input | | Input | (F)-A |
| S0-S15 | Output | – | Segment signal output | | **Note 2** | G-A |
| S16-S19 | Output | P93-P90 | Segment signal output | | Input | H |
| S20-S23 | Output | P83-P80 | Segment signal output | | Input | H |
| COM0-COM3 | Output | – | Common signal output | | **Note 2** | G-B |
| $V_{LC0}$-$V_{LC2}$ | – | – | LCD drive power<br>On-chip split resistor is enabled (mask option). | | – | – |
| BIAS | Output | – | Output for external split resistor disconnect | | **Note 3** | – |
| LCDCL Note 4 | Output | P30 | Clock output for externally expanded driver | | Input | E-B |
| SYNC Note 4 | Output | P31 | Clock output for externally expanded driver synchronization | | Input | E-B |

**Notes 1.** Characters in parentheses indicate the Schmitt trigger input.

**2.** Each display output selects the following $V_{LCX}$ as input source.
S0-S15: $V_{LC1}$, COM0-COM2: $V_{LC2}$, COM3: $V_{LC0}$

**3.** When a split resistor is contained .....Low level
When no split resistor is contained .....High-impedance

**4.** These pins are provided for future system expansion.
At present, these pins are used only as pins P30 and P31.

### 3.2 Non-port Pins (2/2)

| Pin Name | Input/Output | Alternate Function | Function | After Reset | I/O Circuit TYPE Note |
|---|---|---|---|---|---|
| X1 | Input | – | Crystal/ceramic connection pin for the main system clock oscillation. When the external clock is used, input the external clock to pin X1, and the inverted phase of the external clock to pin X2. | – | – |
| X2 | – | | | | |
| XT1 | Input | – | Crystal connection pin for the subsystem clock oscillation. When the external clock is used, input the external clock to pin XT1, and the inverted phase of the external clock to pin XT2. Pin XT1 can be used as a 1-bit input (test) pin. | – | – |
| ★ XT2 | – | | | | |
| $\overline{\text{RESET}}$ | Input | – | System reset input (low-level active) | – | (B) |
| IC | – | – | Internally connected. Connect directly to $V_{DD}$. | – | – |
| $V_{DD}$ | – | – | Positive power supply | – | – |
| $V_{SS}$ | – | – | Ground potential | – | – |

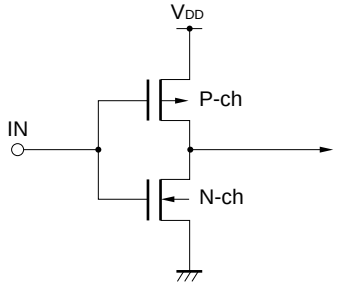
**Note** Characters in parentheses indicate the Schmitt trigger input.

### 3.3 Pin Input/Output Circuits

The μPD753108 pin input/output circuits are shown schematically.

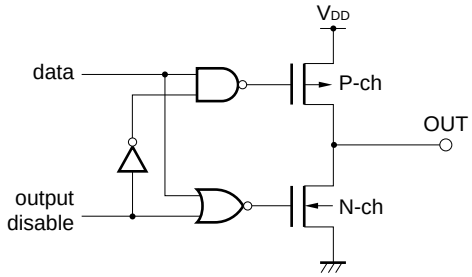
(1/2)

TYPE A



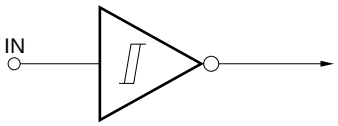

CMOS standard input buffer

TYPE D



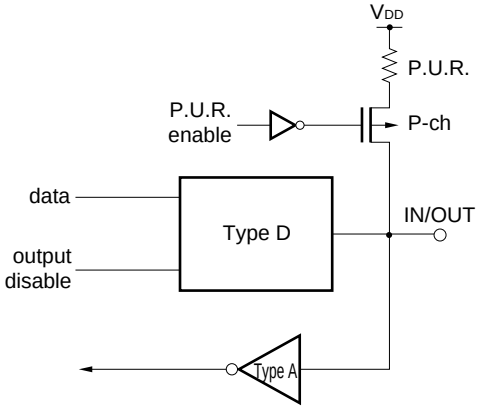

Push-pull output that can be placed in output high-impedance (both P-ch and N-ch off).

TYPE B



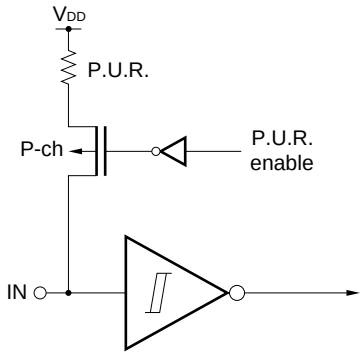

Schmitt trigger input with hysteresis characteristics

TYPE E-B



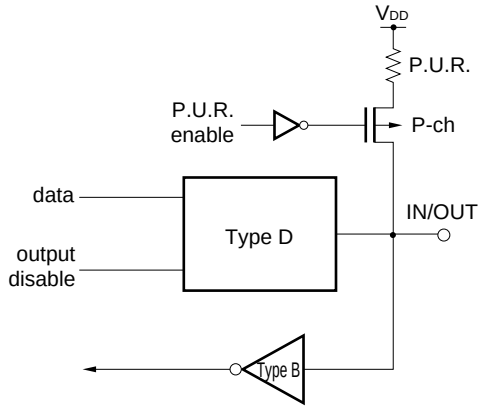

P.U.R. : Pull-Up Resistor

TYPE B-C




P.U.R. : Pull-Up Resistor

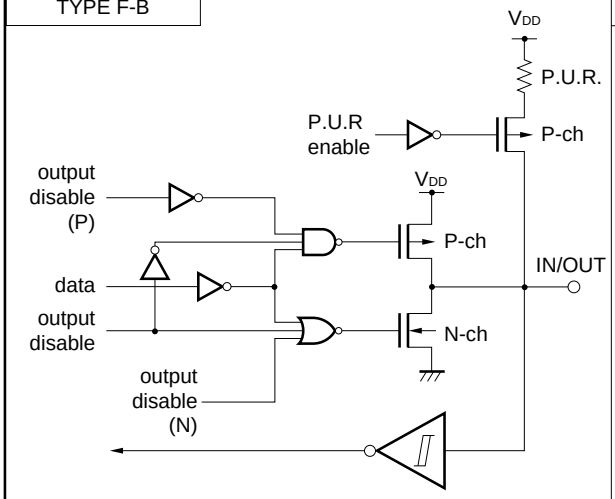
TYPE F-A




P.U.R. : Pull-Up Resistor

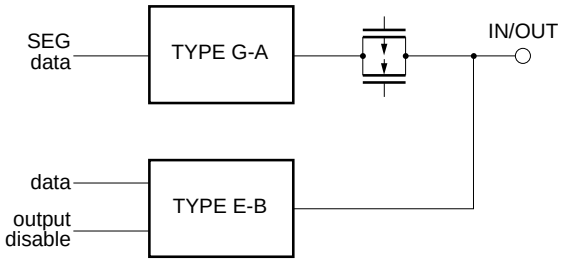
(2/2)

TYPE F-B

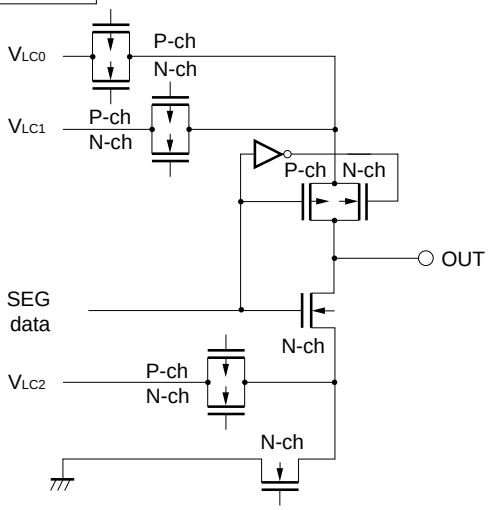



P.U.R. : Pull-Up Resistor

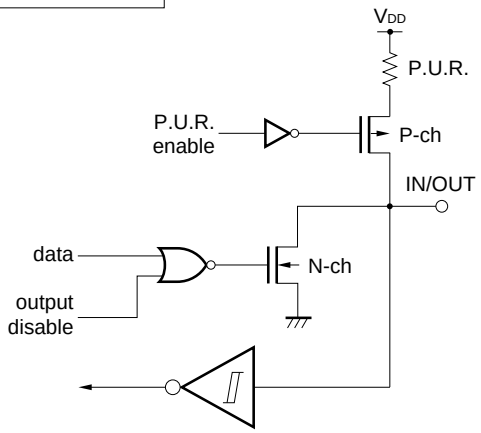
TYPE H




★ TYPE G-A

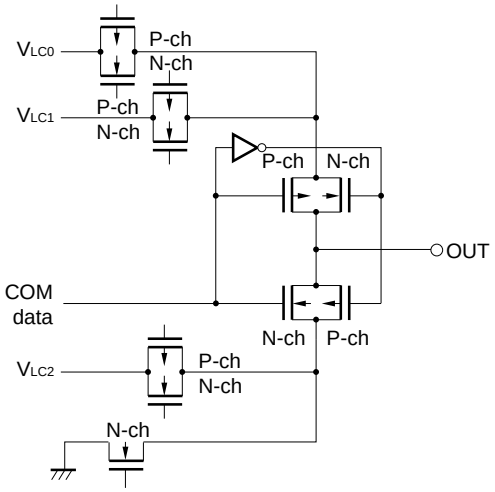



TYPE M-C

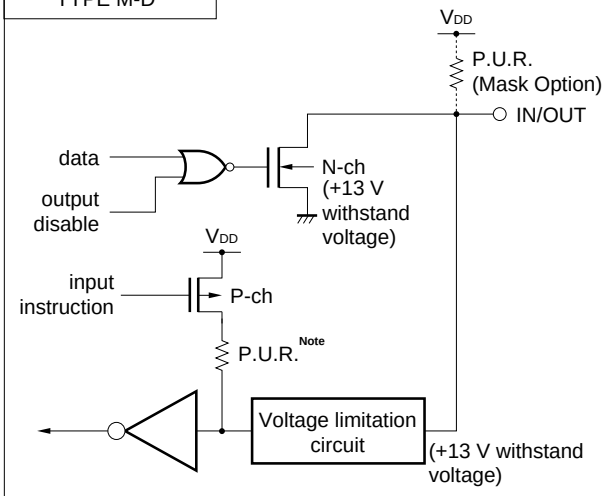



P.U.R. : Pull-Up Resistor

★ TYPE G-B




★ TYPE M-D




**Note** The pull-up resistor operates only when an input instruction is executed (current flows from $V_{DD}$ to the pin when the pin is low).

### 3.4 Recommended Connections for Unused Pins

★ **Table 3-1. List of Recommended Connections for Unused Pins**

| Pin | Recommended Connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ or $V_{DD}$ |
| P01/$\overline{SCK}$ | Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually |
| P02/SO/SB0 | |
| P03/SI/SB1 | Connect to $V_{SS}$ |
| P10/INT0, P11/INT1 | Connect to $V_{SS}$ or $V_{DD}$ |
| P12/TI1/TI2/INT2 | |
| P13/TI0 | |
| P20/PTO0 | Input state: Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually<br>Output state: Leave open |
| P21/PTO1 | |
| P22/PCL/PTO2 | |
| P23/BUZ | |
| P30/LCDCL | |
| P31/SYNC | |
| P32 | |
| P33 | |
| P50-P53 | Input state: Connect to $V_{SS}$<br>Output state: Connect to $V_{SS}$ (do not connect a pull-up resistor of mask option) |
| P60/KR0-P63/KR3 | Input state: Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually<br>Output state: Leave open |
| S0-S15 | Leave open |
| COM0-COM3 | |
| S16/P93-S19/P90 | Input state: Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually<br>Output state: Leave open |
| S20/P83-S23/P80 | |
| $V_{LC0}$-$V_{LC2}$ | Connect to $V_{SS}$ |
| BIAS | Only if all of $V_{LC0}$ to $V_{LC2}$ are unused, connect to $V_{SS}$.<br>In other cases, leave open. |
| XT1 Note | Connect to $V_{SS}$ or $V_{DD}$ |
| XT2 Note | Leave open |
| IC | Connect directly to $V_{DD}$ |

**Note** When the subsystem clock is not used, specify SOS.0 = 1 (so as not to use the on-chip feedback resistor).

## 4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

### 4.1 Difference between Mk I Mode and Mk II Mode

The CPU of the μPD753108 has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by bit 3 of the stack bank select register (SBS).

- Mk I mode: Upward compatible with the μPD75308B. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with the μPD75308B. Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16 Kbytes.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

| | Mk I mode | Mk II mode |
|---|---|---|
| Number of stack bytes for subroutine instructions | 2 bytes | 3 bytes |
| BRA !addr1 instruction<br>CALLA !addr1 instruction | Not available | Available |
| CALL !addr instruction | 3 machine cycles | 4 machine cycles |
| CALLF !faddr instruction | 2 machine cycles | 3 machine cycles |

★ **Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products exceeding 16 Kbytes.**

**When the Mk II mode is selected, the number of stack bytes used during execution of subroutine call instructions increases by one byte per stack compared to the Mk I mode. When the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by one machine cycle. Therefore, use the Mk I mode if the RAM efficiency and processing performance are more important than software compatibility.**

### 4.2 Setting Method of Stack Bank Select Register (SBS)

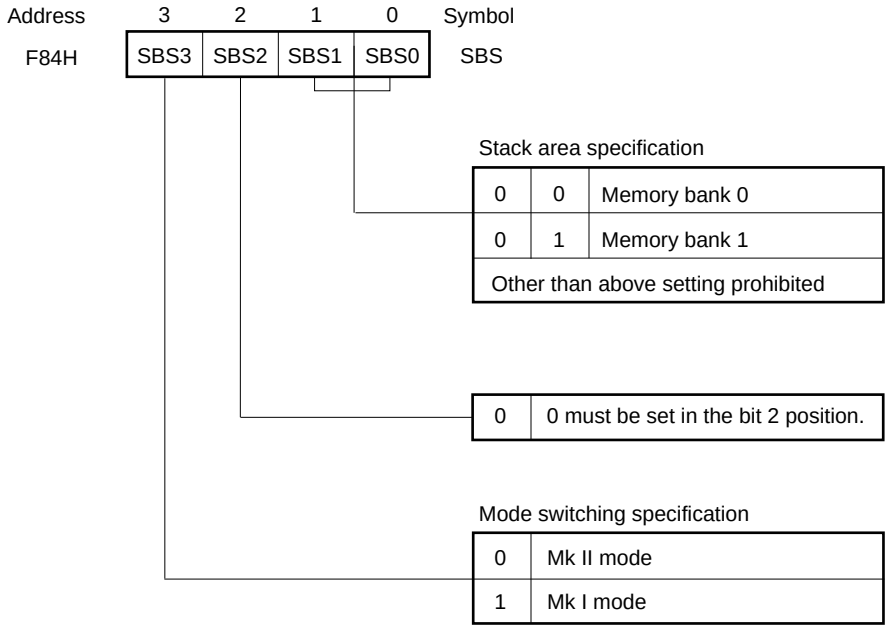
Switching between the Mk I mode and Mk II mode can be done by the stack bank select register (SBS). Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 100xB [Note] at the beginning of a program. When using the Mk II mode, it must be initialized to 000xB [Note].

**Note** Set the desired value in the x position.

**Figure 4-1. Stack Bank Select Register Format**




**Caution Since SBS. 3 is set to "1" after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to "0" to select the Mk II mode.**

## 5. MEMORY CONFIGURATION

- Program Memory (ROM) .... 4096 x 8 bits (μPD753104)
  .... 6144 x 8 bits (μPD753106)
  .... 8192 x 8 bits (μPD753108)

  - Addresses 0000H and 0001H
    Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset start is possible from any address.

  - Addresses 0002H to 000DH
    Vector table wherein the program start address and the values set for the RBE and MBE by each vectored interrupt are written. Interrupt processing can start from any address.

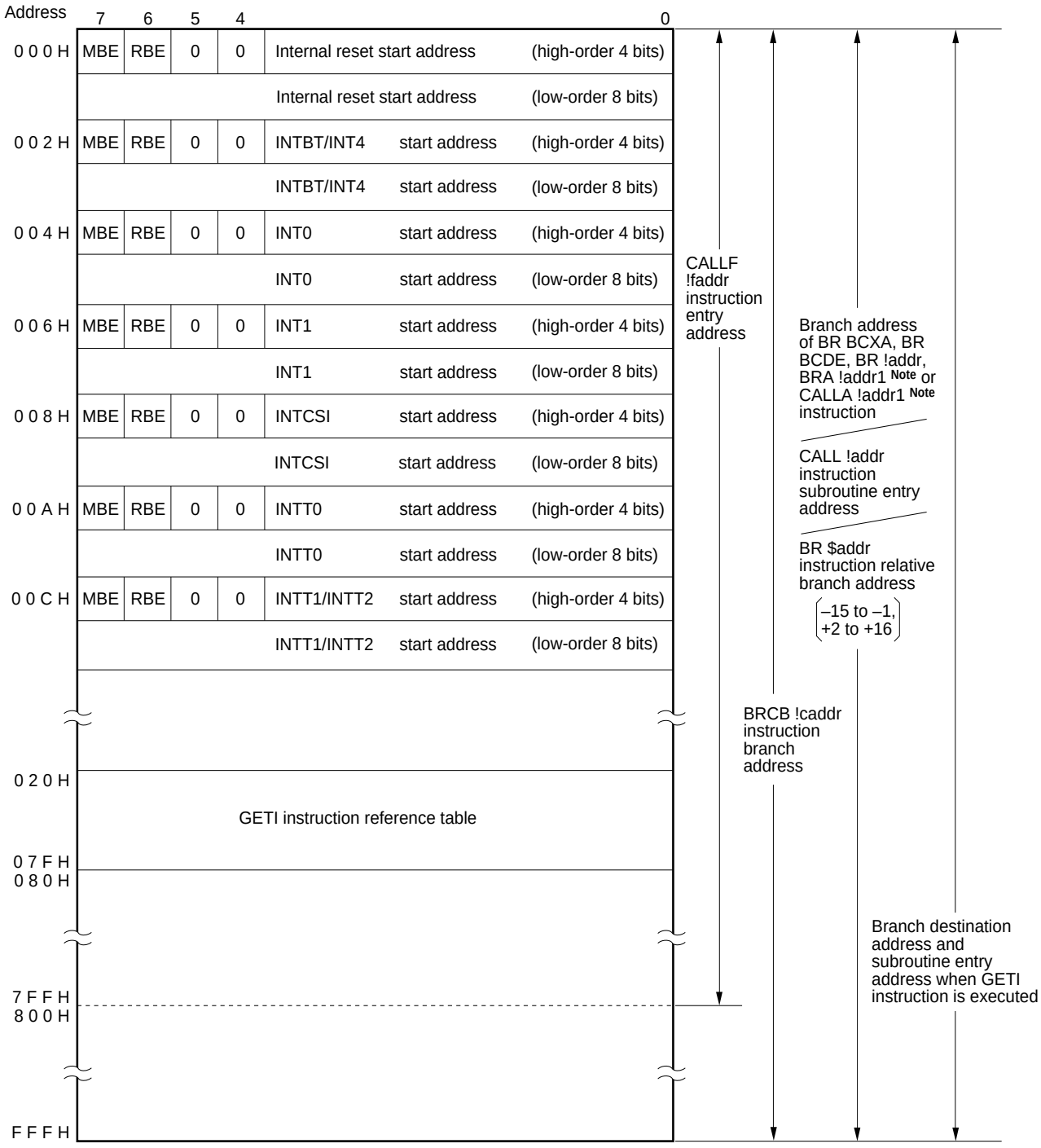
  - Addresses 0020H to 007FH
    Table area referenced by the GETI instruction [Note].

    **Note** The GETI instruction realizes a 1-byte instruction on behalf of any 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the number of program steps.

- Data Memory (RAM)
  - Data area ... 512 words x 4 bits (000H to 1FFH)
  - Peripheral hardware area ... 128 words x 4 bits (F80H to FFFH)

**Figure 5-1. Program Memory Map (1/3)**

**(a) μPD753104**

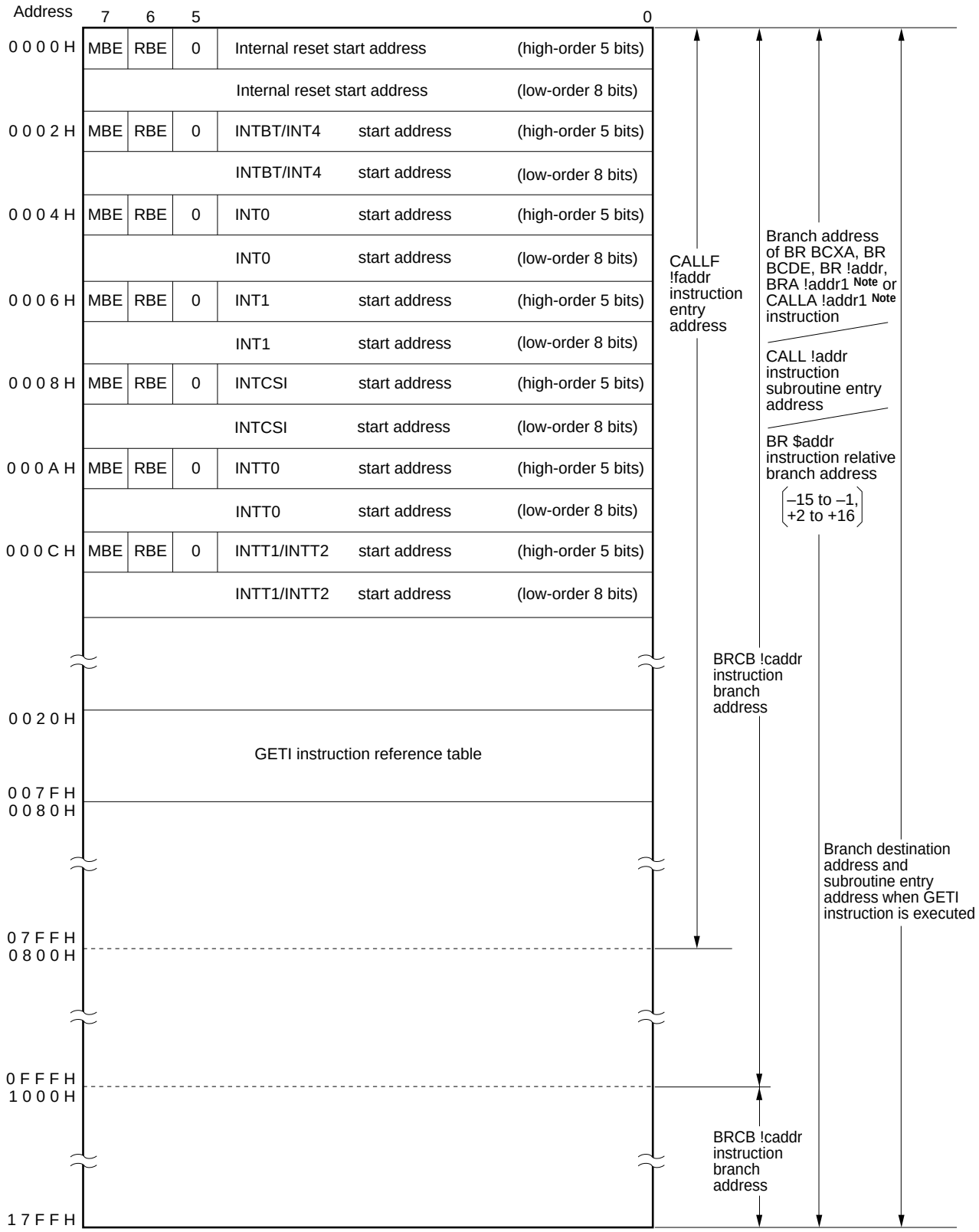



**Note** Can be used in Mk II mode only.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-1. Program Memory Map (2/3)**

**(b) μPD753106**

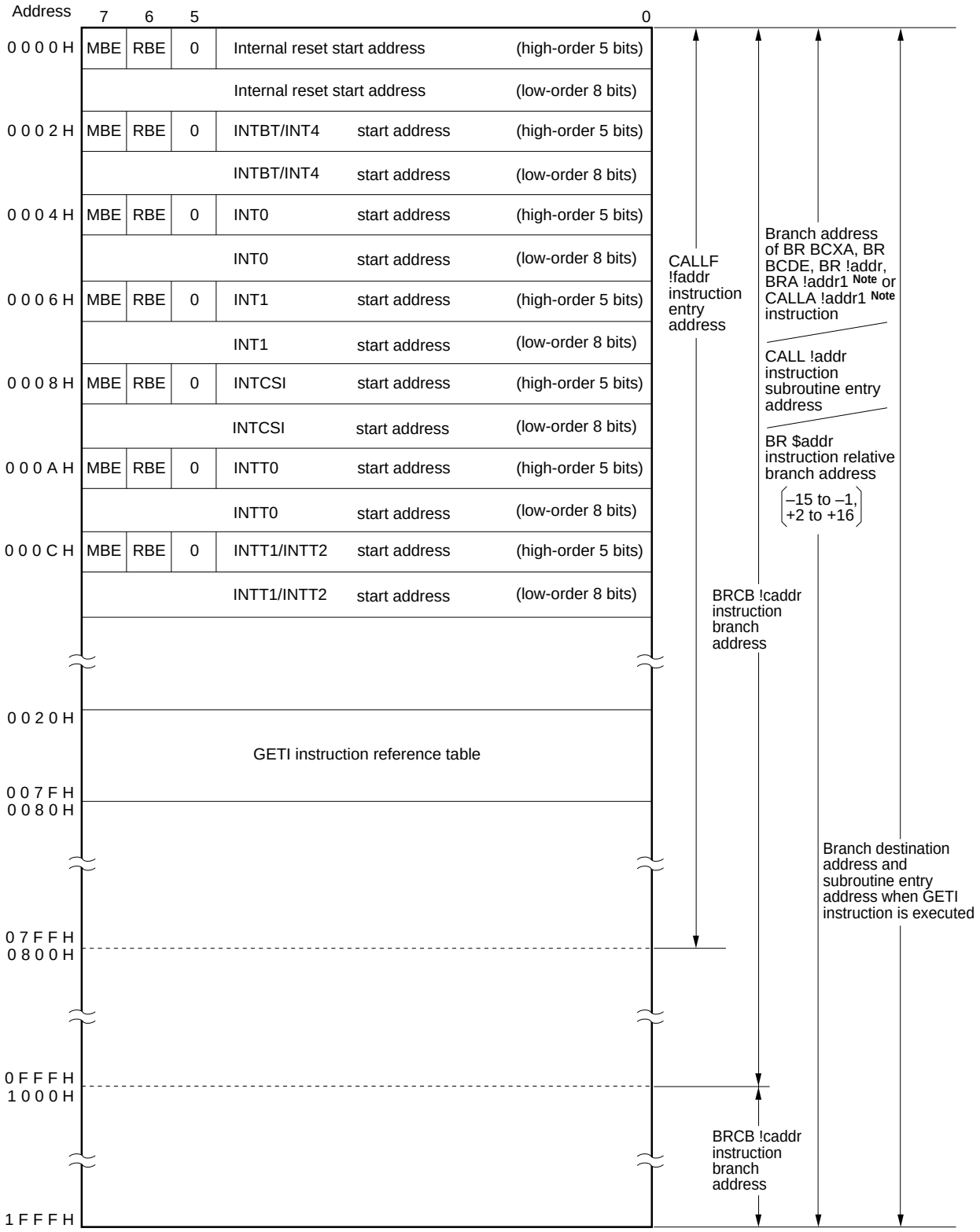



**Note** Can be used in Mk II mode only.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-1. Program Memory Map (3/3)**

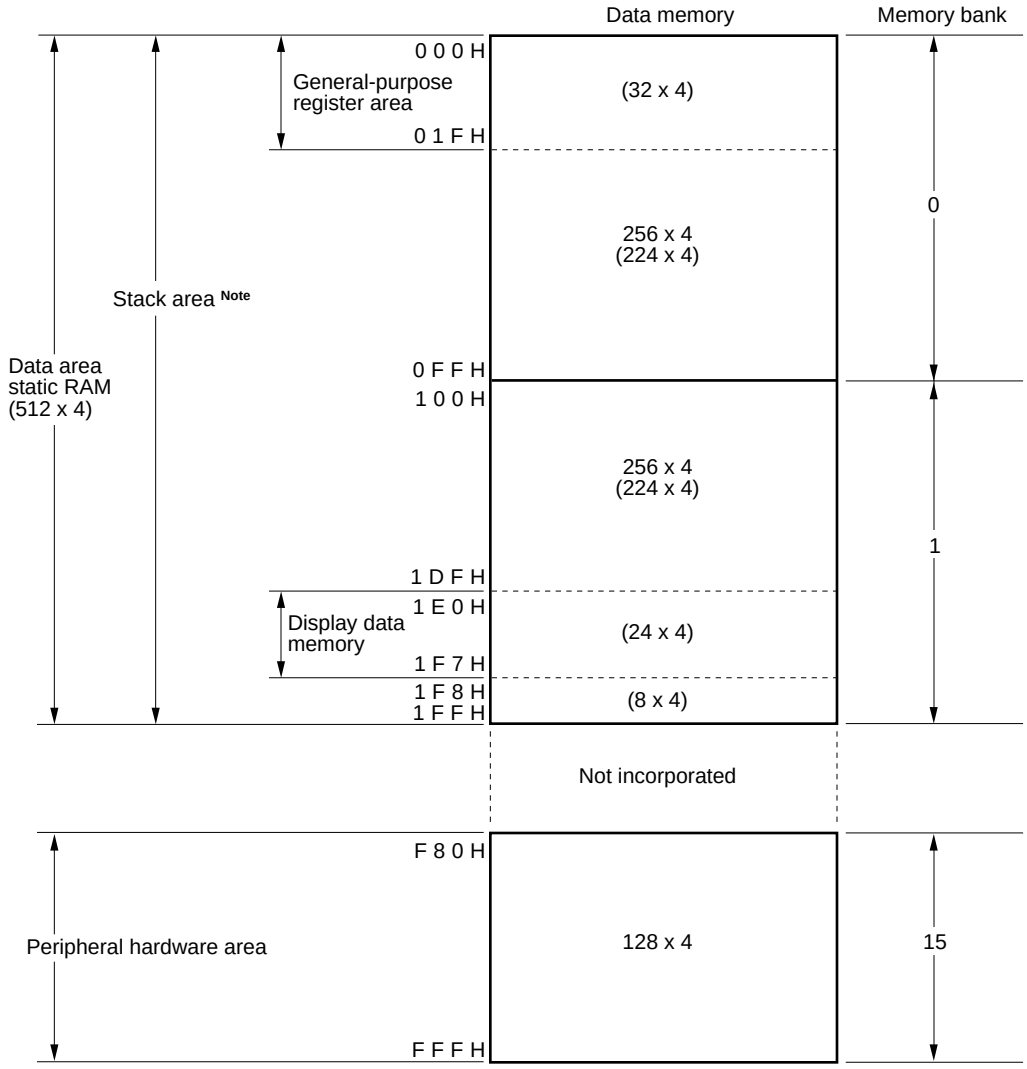
**(c) μPD753108**




**Note** Can be used in Mk II mode only.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

**Figure 5-2. Data Memory Map**




**Note** Either memory bank 0 or 1 can be selected for the stack area.

# 6. PERIPHERAL HARDWARE FUNCTION

## 6.1 Digital I/O Port

There are three kinds of I/O port.

- CMOS input ports (PORT 0, 1) : 8
- CMOS input/output ports (PORT 2, 3, 6, 8, 9) : 20
- N-ch open-drain input/output ports (PORT 5) : 4

Total 32

**Table 6-1. Types and Features of Digital Ports**

| Port name | Function | Operation and features | | Remarks |
|---|---|---|---|---|
| PORT0 | 4-bit input | When the serial interface function is used, the dual function pins function as output ports depending on the operation mode. | | Also used for the INT4, $\overline{SCK}$, SO/SB0, SI/SB1 pins. |
| PORT1 | | 4-bit input only port. | | Also used for the INT0-INT2/ TI1/TI2, TI0 pins. |
| PORT2 | 4-bit input/ output | Can be set to input mode or output mode in 4-bit units. | | Also used for the PTO0-PTO2/PCL, BUZ pins. |
| PORT3 | | Can be set to input mode or output mode bit-wise. | | Also used for the LCDCL, SYNC pins. |
| PORT5 | 4-bit input/ output (N-ch open-drain, 13 V withstand voltage) | Can be set to input mode or output mode in 4-bit units. On-chip pull-up resistor can be specified bit-wise by mask option. | | — |
| PORT6 | 4-bit input/ output | Can be set to input mode or output mode bit-wise. | | Also used for the KR0-KR3 pins. |
| PORT8 | | Can be set to input mode or output mode in 4-bit units. | Ports 8 and 9 are paired and data can be input/ output in 8-bit units. | Also used for the S20-S23 pins. |
| PORT9 | | | | Also used for the S16-S19 pins. |

## 6.2 Clock Generator

The clock generator is a device that generates the clock which is supplied to peripheral hardware on the CPU and is configured as shown in Figure 6-1.

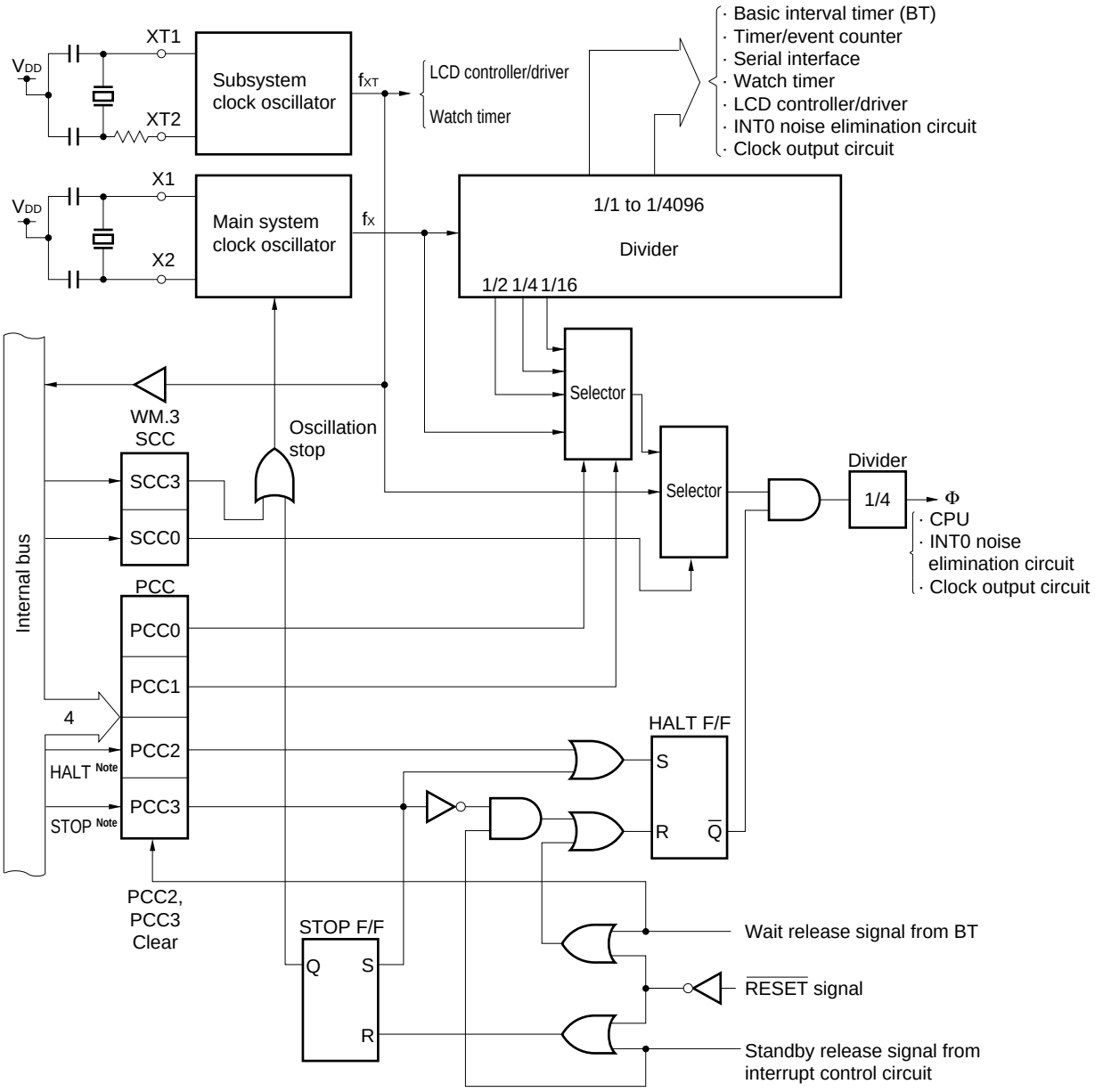
The clock generator operates according to how the processor clock control register (PCC) and system clock control register (SCC) are set.

There are two kinds of clocks, main system clock and subsystem clock.

The instruction execution time can also be changed.

- 0.95, 1.91, 3.81, 15.3 μs (main system clock: in 4.19-MHz operation)
- 0.67, 1.33, 2.67, 10.7 μs (main system clock: in 6.0-MHz operation)
- 122 μs (subsystem clock: in 32.768-kHz operation)

**Figure 6-1. Clock Generator Block Diagram**




**Note** Instruction execution

**Remarks 1.** $f_X$ = Main system clock frequency

**2.** $f_{XT}$ = Subsystem clock frequency

**3.** Φ = CPU clock

**4.** PCC: Processor Clock Control Register

**5.** SCC: System Clock Control Register

**6.** One clock cycle ($t_{CY}$) of the CPU clock is equal to one machine cycle of the instruction.

### 6.3 Subsystem Clock Oscillator Control Functions

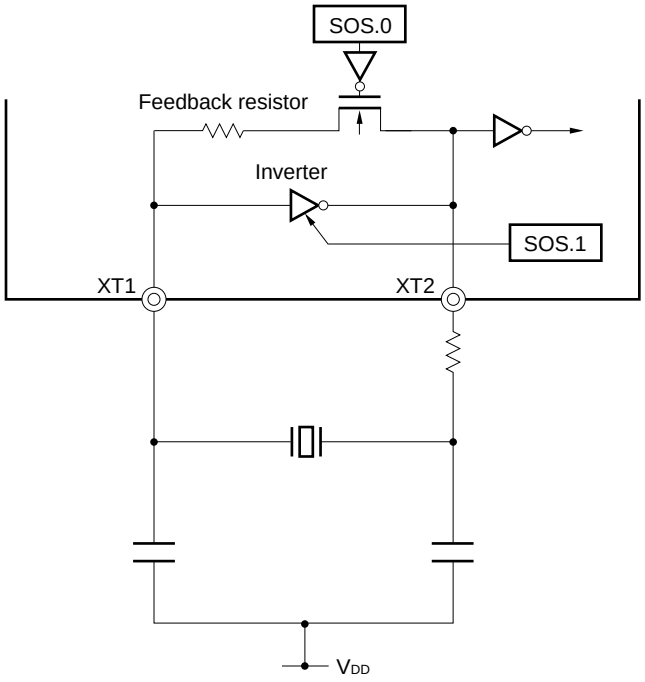
The μPD753108 subsystem clock oscillator has the following two control functions.

- Selects by software whether an on-chip feedback resistor is to be used or not [Note].
- Reduces current consumption by decreasing the drive current of the on-chip inverter when the supply voltage is high ($V_{DD} \geq 2.7$ V).

★ **Note** When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the on-chip feedback resistor) by software, connect XT1 to $V_{SS}$ or $V_{DD}$, and open XT2. This makes it possible to reduce the current consumption in the subsystem clock oscillator.

The above functions can be used by switching the bits 0 and 1 of the sub-oscillator control register (SOS). (See Figure 6-2.)

★ **Figure 6-2. Subsystem Clock Oscillator**

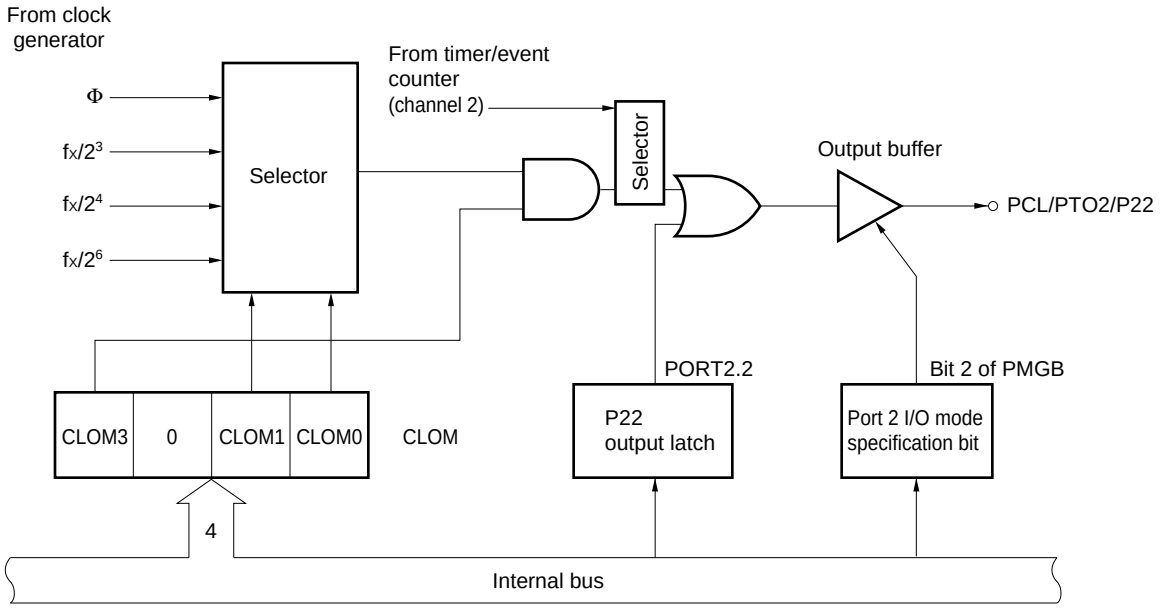


## 6.4 Clock Output Circuit

The clock output circuit is provided to output the clock pulses from the P22/PTO2/PCL pin to the remote control wave outputs and peripheral LSI's.

- Clock output (PCL): Φ, 524, 262, 65.5 kHz (main system clock: in 4.19-MHz operation)
  Φ, 750, 375, 93.8 kHz (main system clock: in 6.0-MHz operation)

**Figure 6-3. Clock Output Circuit Block Diagram**



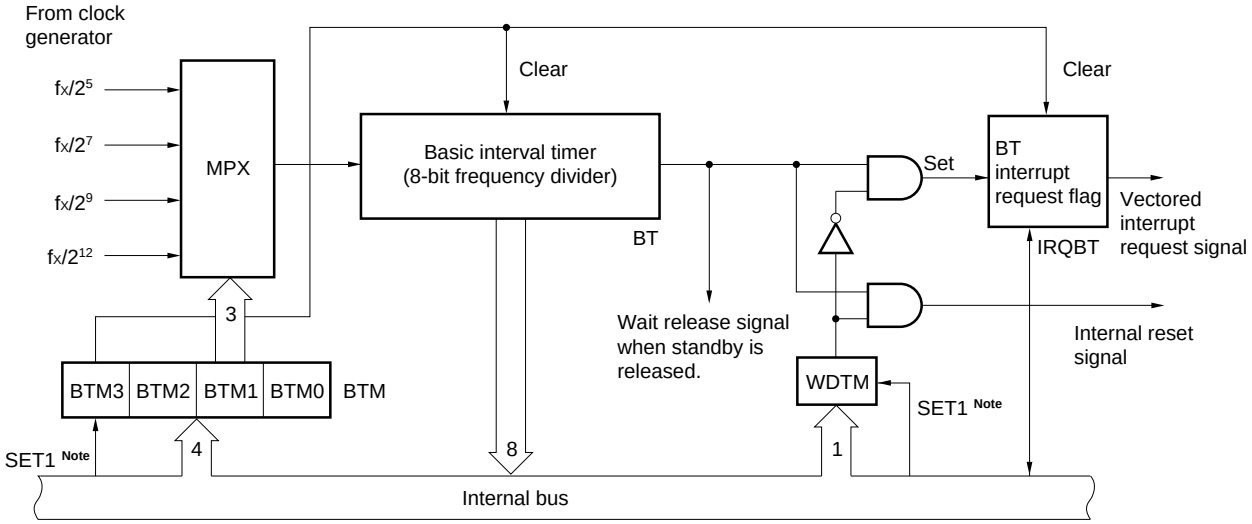

**Remark** Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

## 6.5 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- Interval timer operation to generate a reference time interrupt
- Watchdog timer operation to detect a runaway of program and reset the CPU
- Selects and counts the wait time when the standby mode is released
- Reads the contents of counting

**Figure 6-4. Basic Interval Timer/Watchdog Timer Block Diagram**



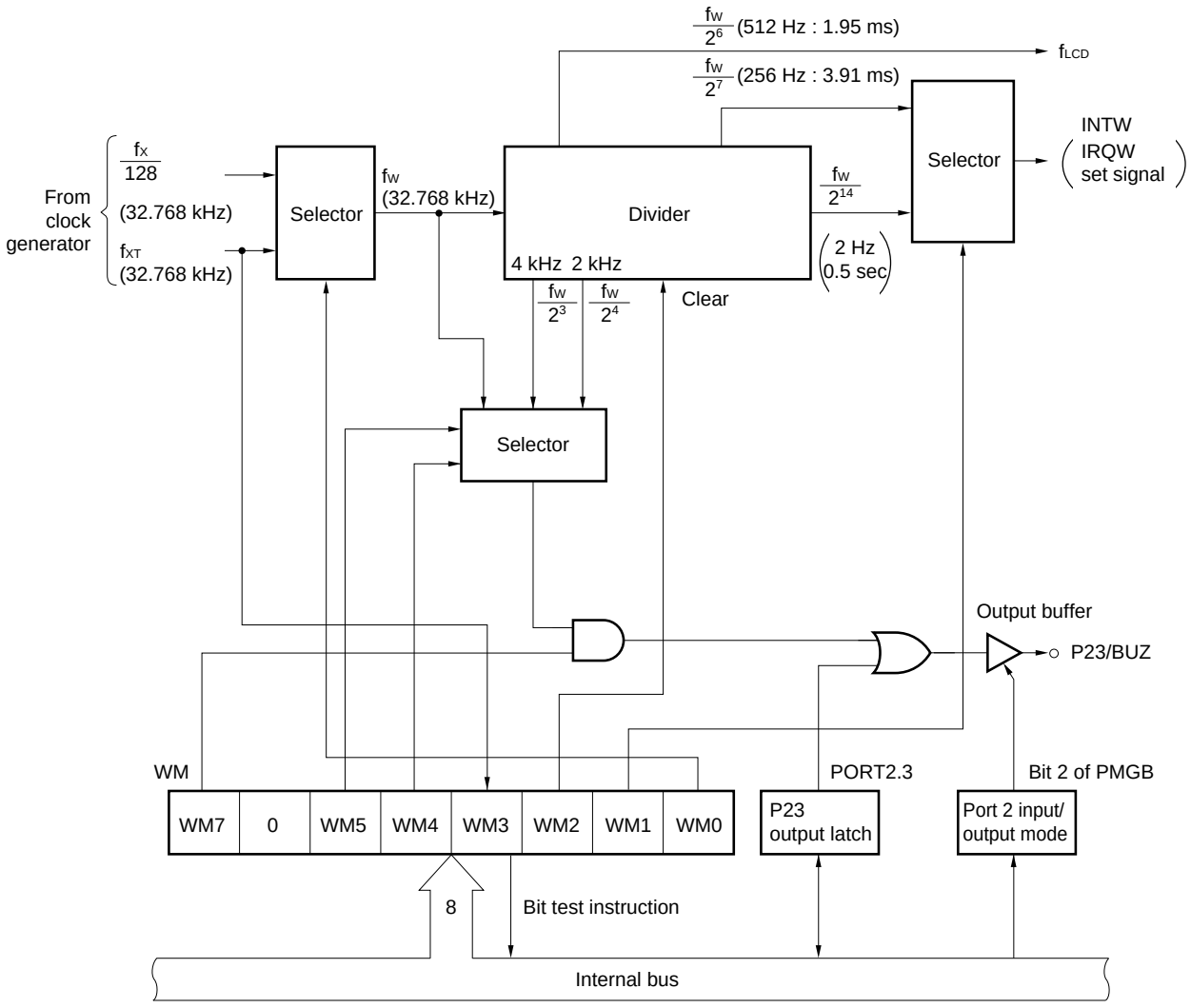

**Note** Instruction execution

## 6.6 Watch Timer

The μPD753108 has one watch timer channel which has the following functions.

- Sets the test flag (IRQW) at 0.5-second intervals. The standby mode can be released by the IRQW.
- 0.5-second interval can be created by both the main system clock (4.194304 MHz) and subsystem clock (32.768 kHz).
- Convenient for program debugging and checking as interval becomes 128 times longer (3.91 ms) with the fast feed mode.
- Outputs the frequencies (2.048, 4.096, 32.768 kHz) to the P23/BUZ pin, usable for buzzer and trimming of system clock oscillation frequencies.
- Clears the frequency divider to make the watch start with zero seconds.

**Figure 6-5. Watch Timer Block Diagram**




**Remark** The values enclosed in parentheses are applied when $f_X$ = 4.194304 MHz and $f_{XT}$ = 32.768 kHz.

## 6.7 Timer/Event Counter

The μPD753108 has three channels of timer/event counters. Its configuration is shown in Figures 6-6 to 6-8. The timer/event counter has the following functions.

- Programmable interval timer operation
- Square wave output of any frequency to the PTOn pin (n = 0 to 2)
- Event counter operation
- Divides the frequency of signal input via the TIn pin to 1-Nth of the original signal and outputs the divided frequency to the PTOn pin (frequency divider operation).
- Supplies the serial shift clock to the serial interface circuit.
- Reads the count value.

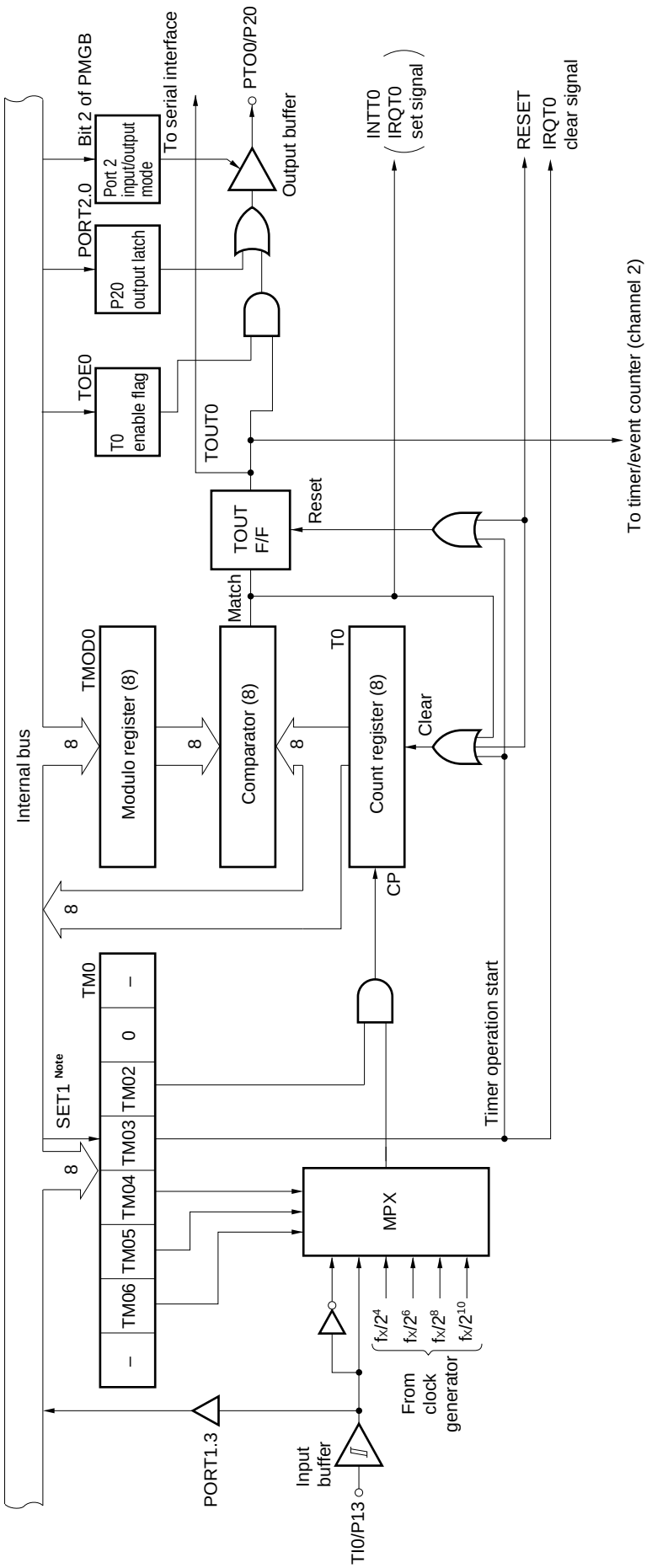
The timer/event counter operates in the following four modes as set by the mode register.

**Table 6-2. Operation Modes of Timer/Event Counter**

| Mode \ Channel | | Channel 0 | Channel 1 | Channel 2 |
|---|---|---|---|---|
| 8-bit timer/event counter mode | | Yes | Yes | Yes |
| | Gate control function | No [Note] | No | Yes |
| PWM pulse generator mode | | No | No | Yes |
| 16-bit timer/event counter mode | | No | Yes | |
| | Gate control function | No [Note] | Yes | |
| Carrier generator mode | | No | Yes | |

**Note** Used for gate control signal generation

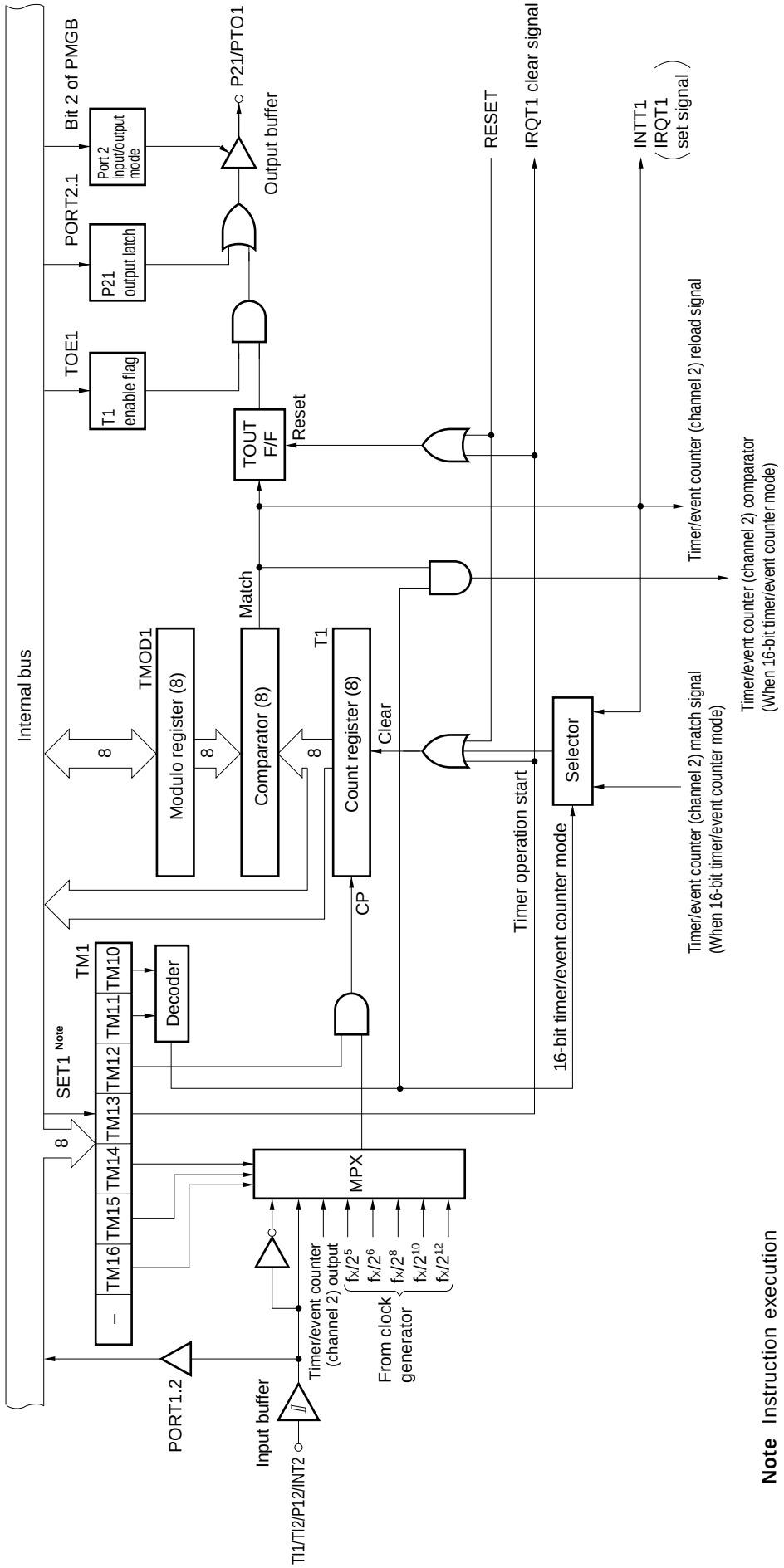
★ **Figure 6-6. Timer/Event Counter (Channel 0) Block Diagram**




**Note** Instruction execution

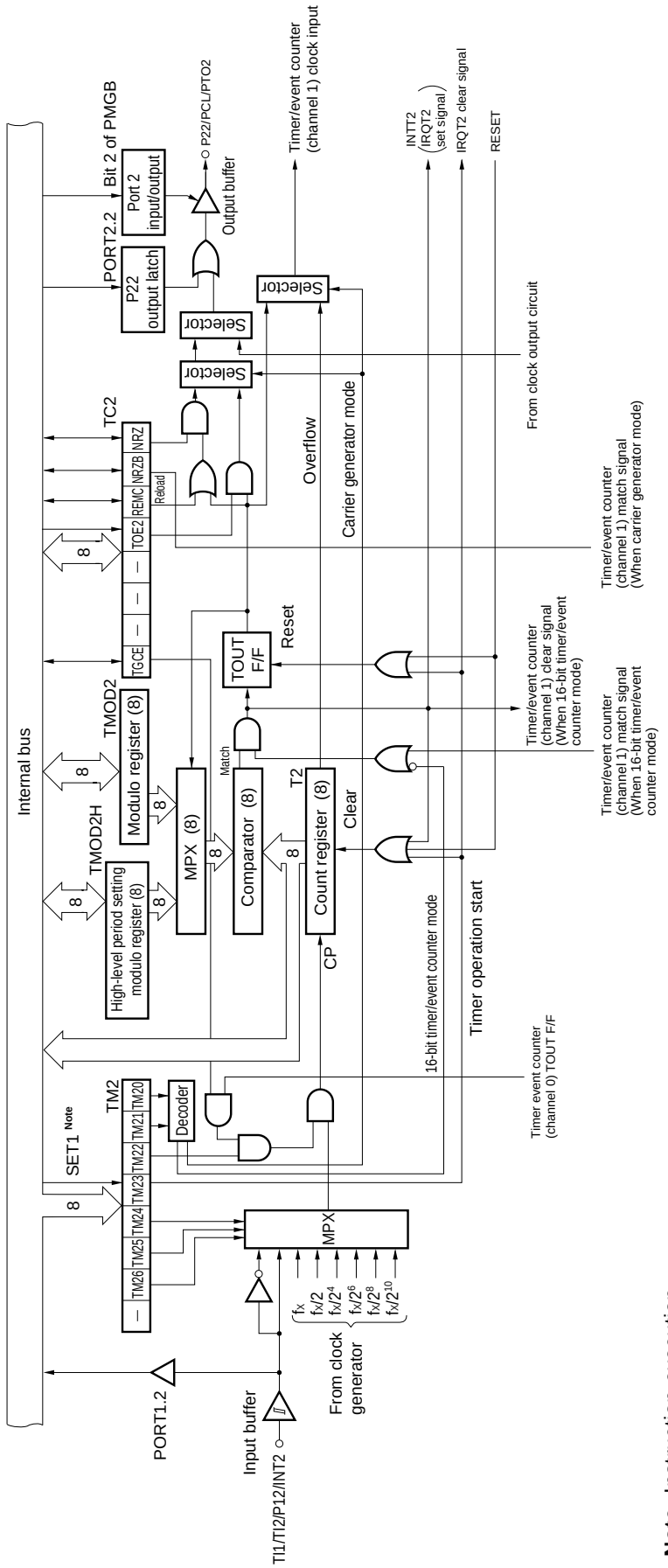
**Caution When setting data to TM0, be sure to set bit 1 to 0.**

**Figure 6-7. Timer/Event Counter (Channel 1) Block Diagram**




**Note** Instruction execution

**Figure 6-8. Timer/Event Counter (Channel 2) Block Diagram**



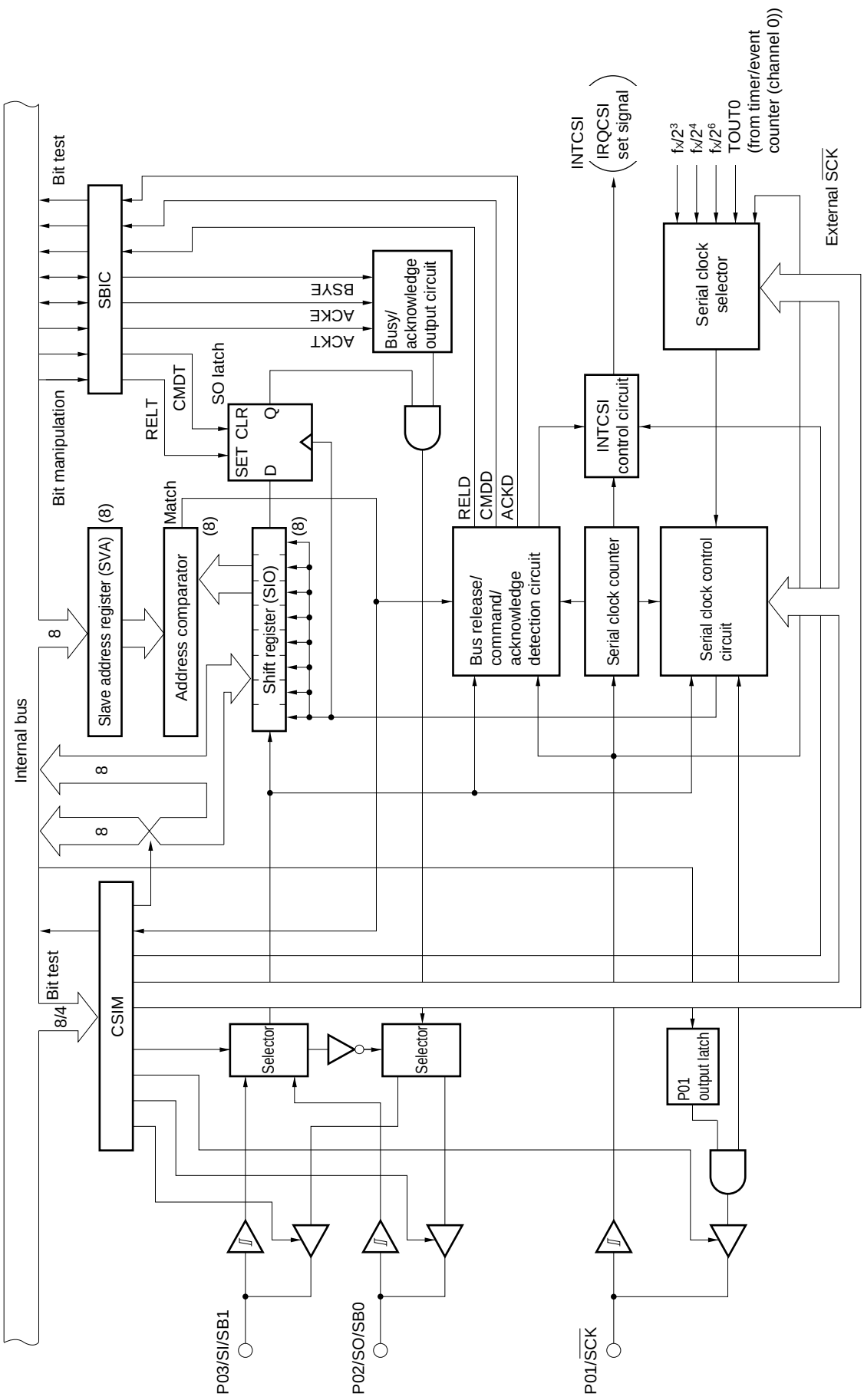

**Note** Instruction execution

### 6.8 Serial Interface

The μPD753108 incorporates a clock-synchronous 8-bit serial interface. The serial interface can be used in the following four modes.

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode

**Figure 6-9. Serial Interface Block Diagram**



### 6.9 LCD Controller/Driver

The μPD753108 incorporates a display controller which generates segment and common signals according to the display data memory contents and incorporates segment and common drivers which can drive the LCD panel directly.

The μPD753108 LCD controller/driver has the following functions:

- Display data memory is read automatically by DMA operation and segment and common signals are generated.
- Display mode can be selected from among the following five:
  <1> Static
  <2> 1/2 duty (time multiplexing by 2), 1/2 bias
  <3> 1/3 duty (time multiplexing by 3), 1/2 bias
  <4> 1/3 duty (time multiplexing by 3), 1/3 bias
  <5> 1/4 duty (time multiplexing by 4), 1/3 bias
- A frame frequency can be selected from among four in each display mode.
- A maximum of 24 segment signal output pins (S0 to S23) and four common signal output pins (COM0 to COM3).
- The segment signal output pins (S0 to S23) can be changed to the I/O ports (PORT8 and PORT9).
- Split resistor can be incorporated to supply LCD drive power (mask option).
  - Various bias methods and LCD drive voltages are applicable.
  - When display is off, current flowing through the split resistor is cut.
- Display data memory not used for display can be used for normal data memory.
- It can also operate by using the subsystem clock.

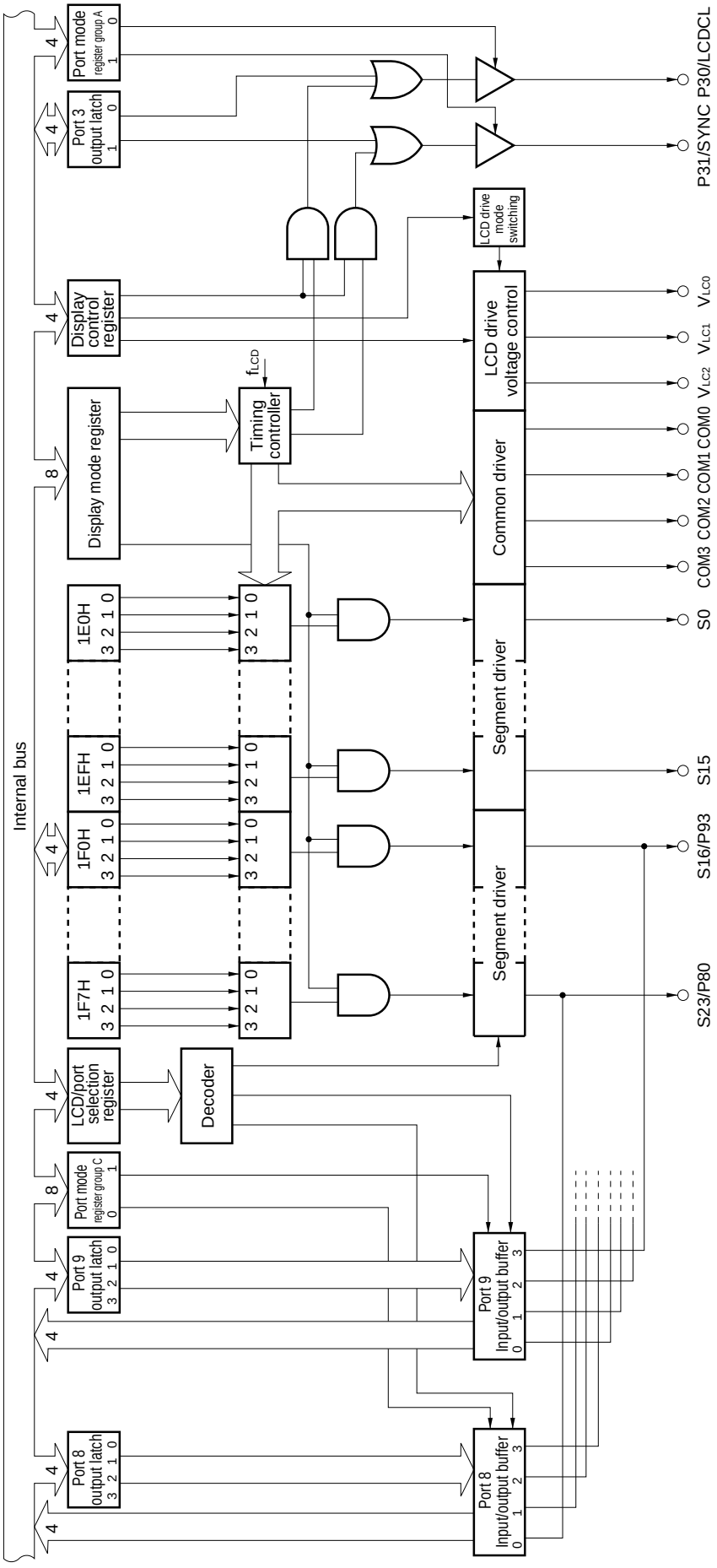
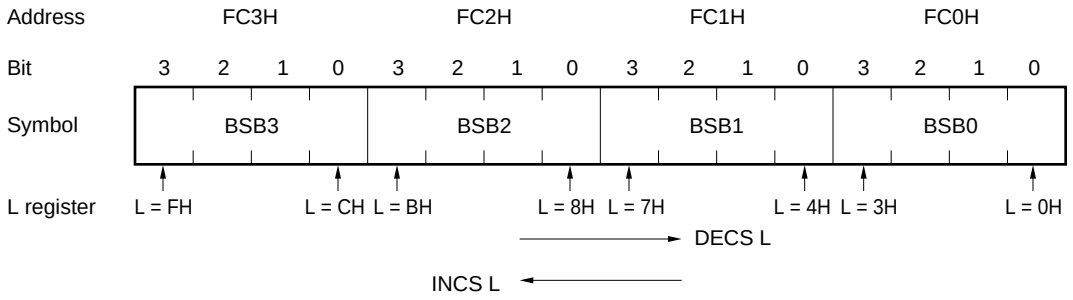



**Figure 6-10. LCD Controller/Driver Block Diagram**

### 6.10 Bit Sequential Buffer ..... 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing a long data bit-wise.

**Figure 6-11. Bit Sequential Buffer Format**




**Remarks 1.** In the pmem.@L addressing, the specified bit moves corresponding to the L register.

**2.** In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MBS specification.

## 7. INTERRUPT FUNCTION AND TEST FUNCTION

The μPD753108 has eight types of interrupt sources and two types of test sources. Of these test sources, INT2 has two types of edge detection testable inputs.

The interrupt control circuit of the μPD753108 has the following functions.

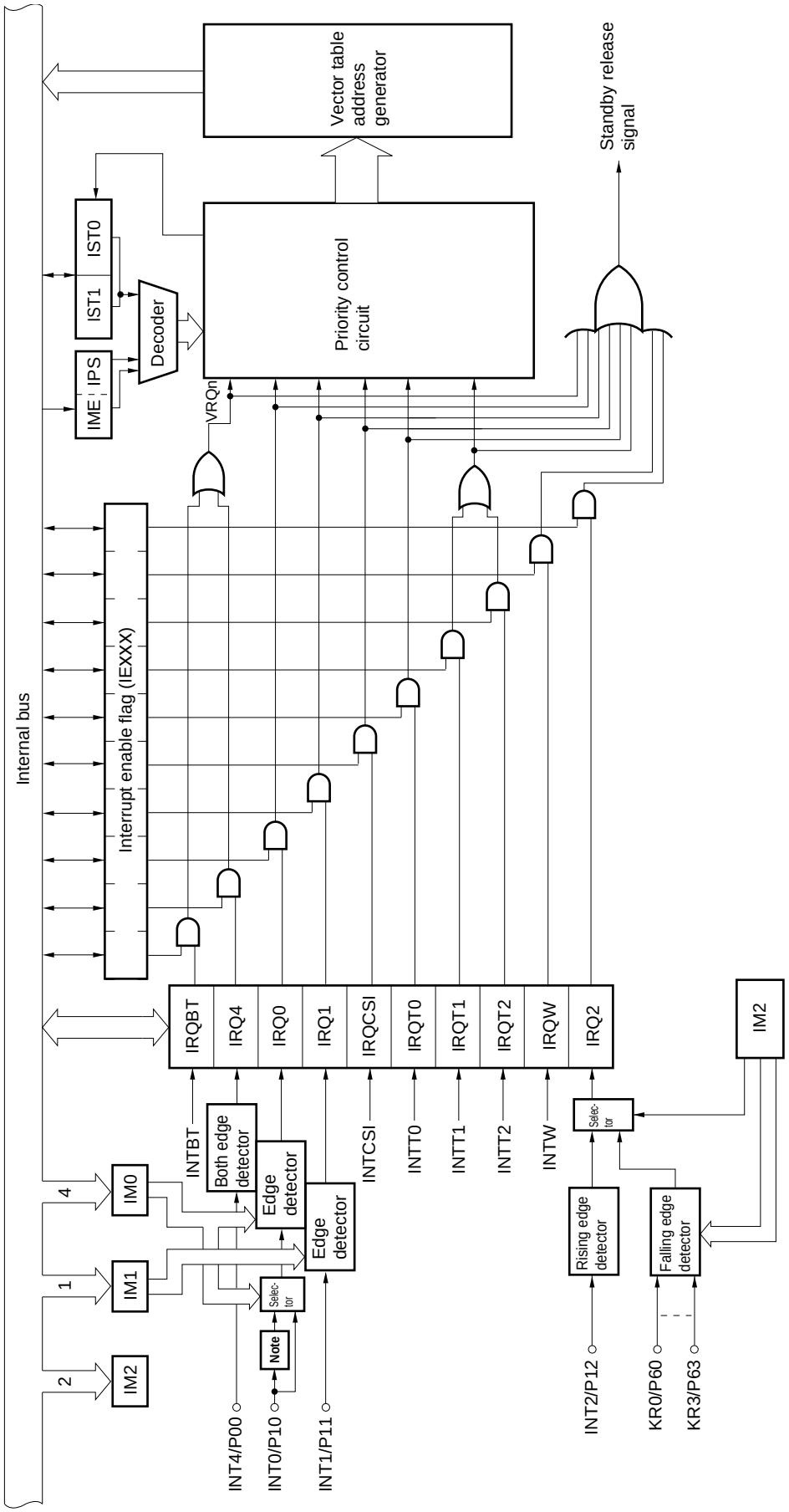
### (1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQxxx). An interrupt generation can be checked by software.
- Release the standby mode. An interrupt to be released can be selected by the interrupt enable flag.

### (2) Test function

- Test request flag (IRQxxx) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

**Figure 7-1. Interrupt Control Circuit Block Diagram**




**Note** Noise elimination circuit (Standby release is disabled when noise elimination circuit is selected.)

## 8. STANDBY FUNCTION

In order to reduce power dissipation while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD753108.

**Table 8-1. Operation Status in Standby Mode**

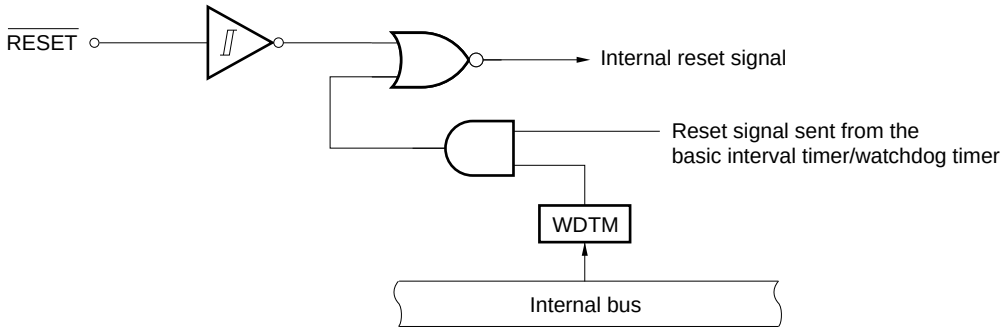
| Item \ Mode | | STOP mode | HALT mode |
|---|---|---|---|
| Set instruction | | STOP instruction | HALT instruction |
| System clock when set | | Settable only when the main system clock is used. | Settable both by the main system clock and subsystem clock. |
| Operation status | Clock generator | Main system clock stops oscillation. | Only the CPU clock Φ halts (oscillation continues). |
| | Basic interval timer/ watchdog timer | Operation stops. | Operable only when the main system clock is oscillated.<br>BT mode : IRQBT is set in the reference time interval<br>WT mode : Reset signal is generated by BT overflow |
| | Serial interface | Operable only when an external $\overline{SCK}$ input is selected as the serial clock. | Operable only when an external $\overline{SCK}$ input is selected as the serial clock or when the main system clock is oscillated. |
| | Timer/event counter | Operable only when a signal input to the TI0 to TI2 pins is specified as the count clock. | Operable only when a signal input to the TI0 to TI2 pins is specified as the count clock or when the main system clock is oscillated. |
| | Watch timer | Operable when $f_{XT}$ is selected as the count clock. | Operable. |
| | LCD controller/driver | Operable only when $f_{XT}$ is selected as the LCDCL. | Operable. |
| | External interrupt | The INT1, 2, and 4 are operable.<br>Only the INT0 is not operated [Note]. | |
| | CPU | The operation stops. | |
| Release signal | | Interrupt request signal sent from the operable hardware enabled by the interrupt enable flag or $\overline{RESET}$ signal input. | |

**Note** Can operate only when the noise elimination circuit is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

## 9. RESET FUNCTION

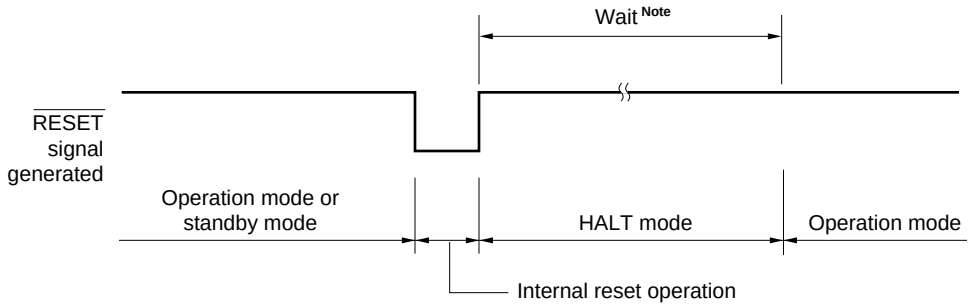
There are two reset inputs: external reset signal ($\overline{\text{RESET}}$) and reset signal sent from the basic interval timer/watchdog timer. When either one of the reset signals are input, an internal reset signal is generated. Figure 9-1 shows the configuration of the above two inputs.

**Figure 9-1. Configuration of Reset Function**




Generation of the $\overline{\text{RESET}}$ signal initializes each hardware as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

**Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation**




**Note** The following two times can be selected by the mask option.

$2^{17}/f_X$ (21.8 ms: @ 6.00-MHz operation, 31.3 ms: @ 4.19-MHz operation)

$2^{15}/f_X$ (5.46 ms: @ 6.00-MHz operation, 7.81 ms: @ 4.19-MHz operation)

**Table 9-1. Status of Each Hardware After Reset (1/2)**

| Hardware | | | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation in operation |
|---|---|---|---|---|
| Program counter (PC) | | μPD753104 | Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0. | Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0. |
| | | μPD753106, μPD753108 | Sets the low-order 5 bits of program memory's address 0000H to the PC12-PC8 and the contents of address 0001H to the PC7-PC0. | Sets the low-order 5 bits of program memory's address 0000H to the PC12-PC8 and the contents of address 0001H to the PC7-PC0. |
| PSW | Carry flag (CY) | | Held | Undefined |
| | Skip flag (SK0 to SK2) | | 0 | 0 |
| | Interrupt status flag (IST0, IST1) | | 0 | 0 |
| | Bank enable flag (MBE, RBE) | | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. |
| Stack pointer (SP) | | | Undefined | Undefined |
| Stack bank select register (SBS) | | | 1000B | 1000B |
| ★ Data memory (RAM) | | | Held | Undefined |
| General-purpose register (X, A, H, L, D, E, B, C) | | | Held | Undefined |
| Bank select register (MBS, RBS) | | | 0, 0 | 0, 0 |
| Basic interval timer/watchdog timer | Counter (BT) | | Undefined | Undefined |
| | Mode register (BTM) | | 0 | 0 |
| | Watchdog timer enable flag (WDTM) | | 0 | 0 |
| Timer/event counter (T0) | Counter (T0) | | 0 | 0 |
| | Modulo register (TMOD0) | | FFH | FFH |
| | Mode register (TM0) | | 0 | 0 |
| | TOE0, TOUT F/F | | 0, 0 | 0, 0 |
| Timer/event counter (T1) | Counter (T1) | | 0 | 0 |
| | Modulo register (TMOD1) | | FFH | FFH |
| | Mode register (TM1) | | 0 | 0 |
| | TOE1, TOUT F/F | | 0, 0 | 0, 0 |
| Timer/event counter (T2) | Counter (T2) | | 0 | 0 |
| | Modulo register (TMOD2) | | FFH | FFH |
| | High-level period setting modulo register (TMOD2H) | | FFH | FFH |
| | Mode register (TM2) | | 0 | 0 |
| | TOE2, TOUT F/F | | 0, 0 | 0, 0 |
| | REMC, NRZ, NRZB | | 0, 0, 0 | 0, 0, 0 |
| | TGCE | | 0 | 0 |
| Watch timer | Mode register (WM) | | 0 | 0 |

**Table 9-1. Status of Each Hardware After Reset (2/2)**

| Hardware | | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation in operation |
|---|---|---|---|
| Serial interface | Shift register (SIO) | Held | Undefined |
| | Operation mode register (CSIM) | 0 | 0 |
| | SBI control register (SBIC) | 0 | 0 |
| | Slave address register (SVA) | Held | Undefined |
| Clock generator, clock output circuit | Processor clock control register (PCC) | 0 | 0 |
| | System clock control register (SCC) | 0 | 0 |
| | Clock output mode register (CLOM) | 0 | 0 |
| Sub-oscillator control register (SOS) | | 0 | 0 |
| LCD controller/ driver | Display mode register (LCDM) | 0 | 0 |
| | Display control register (LCDC) | 0 | 0 |
| | LCD/port selection register (LPS) | 0 | 0 |
| Interrupt function | Interrupt request flag (IRQxxx) | Reset (0) | Reset (0) |
| | Interrupt enable flag (IExxx) | 0 | 0 |
| | Interrupt priority selection register (IPS) | 0 | 0 |
| | INT0, 1, 2 mode registers (IM0, IM1, IM2) | 0, 0, 0 | 0, 0, 0 |
| Digital port | Output buffer | Off | Off |
| | Output latch | Cleared (0) | Cleared (0) |
| | I/O mode registers (PMGA, B, C) | 0 | 0 |
| | Pull-up resistor setting register (POGA, B) | 0 | 0 |
| Bit sequential buffer (BSB0 to BSB3) | | Held | Undefined |

## 10. MASK OPTION

The μPD753108 has the following mask options.

- P50-P53 mask options
  Selects whether or not to internally connect a pull-up resistor.
  <1> Connect pull-up resistor internally bit-wise.
  <2> Do not connect pull-up resistor internally.
- $V_{LC0}$-$V_{LC2}$ pins, BIAS pin mask option
  Selects whether or not to internally connect LCD-driving split resistors.
  <1> Do not connect split resistor internally.
  <2> Connect four 10-kΩ (typ.) split resistors simultaneously internally.
  <3> Connect four 100-kΩ (typ.) split resistors simultaneously internally.
- Standby function mask option
  Selects the wait time with the $\overline{\text{RESET}}$ signal.
  <1> $2^{17}$/fx (21.8 ms: When fx = 6.0 MHz, 31.3 ms: When fx = 4.19 MHz)
  <2> $2^{15}$/fx (5.46 ms: When fx = 6.0 MHz, 7.81 ms: When fx = 4.19 MHz)
- Subsystem clock mask option
  Selects whether or not to use an internal feedback resistor.
  <1> Use internal feedback resistor.
  (Switch internal feedback resistor ON/OFF by software)
  <2> Do not use internal feedback resistor.
  (Disconnect internal feedback resistor by hardware)

## 11. INSTRUCTION SET

### (1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to "**RA75X ASSEMBLER PACKAGE USERS' MANUAL——LANGUAGE (EEU-1363)**". If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the register flags can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, see **User's Manual**.

| Expression format | Description method |
|---|---|
| reg<br>reg1 | X, A, B, C, D, E, H, L<br>X, B, C, D, E, H, L |
| rp<br>rp1<br>rp2<br>rp'<br>rp'1 | XA, BC, DE, HL<br>BC, DE, HL<br>BC, DE<br>XA, BC, DE, HL, XA', BC', DE', HL'<br>BC, DE, HL, XA', BC', DE', HL' |
| rpa<br>rpa1 | HL, HL+, HL–, DE, DL<br>DE, DL |
| n4<br>n8 | 4-bit immediate data or label<br>8-bit immediate data or label |
| mem<br>bit | 8-bit immediate data or label [Note]<br>2-bit immediate data or label |
| fmem<br>pmem | FB0H-FBFH, FF0H-FFFH immediate data or label<br>FC0H-FFFH immediate data or label |
| addr<br><br><br>addr1<br>(Mk II mode only)<br><br>caddr<br>faddr | 0000H-0FFFH immediate data or label (μPD753104)<br>0000H-17FFH immediate data or label (μPD753106)<br>0000H-1FFFH immediate data or label (μPD753108)<br>0000H-0FFFH immediate data or label (μPD753104)<br>0000H-17FFH immediate data or label (μPD753106)<br>0000H-1FFFH immediate data or label (μPD753108)<br>12-bit immediate data or label<br>11-bit immediate data or label |
| taddr | 20H-7FH immediate data (where bit0 = 0) or label |
| PORTn<br>IExxx<br>RBn<br>MBn | PORT0-PORT3, PORT5, PORT6, PORT8, PORT9<br>IEBT, IET0-IET2, IE0-IE2, IE4, IECSI, IEW<br>RB0-RB3<br>MB0, MB1, MB15 |

**Note** mem can be only used for even address in 8-bit data processing.

**(2) Legend in explanation of operation**

| | |
|---|---|
| A | : A register, 4-bit accumulator |
| B | : B register |
| C | : C register |
| D | : D register |
| E | : E register |
| H | : H register |
| L | : L register |
| X | : X register |
| XA | : XA register pair; 8-bit accumulator |
| BC | : BC register pair |
| DE | : DE register pair |
| HL | : HL register pair |
| XA' | : XA' expanded register pair |
| BC' | : BC' expanded register pair |
| DE' | : DE' expanded register pair |
| HL' | : HL' expanded register pair |
| PC | : Program counter |
| SP | : Stack pointer |
| CY | : Carry flag, bit accumulator |
| PSW | : Program status word |
| MBE | : Memory bank enable flag |
| RBE | : Register bank enable flag |
| PORTn | : Port n (n = 0 to 3, 5, 6, 8, 9) |
| IME | : Interrupt master enable flag |
| IPS | : Interrupt priority selection register |
| IExxx | : Interrupt enable flag |
| RBS | : Register bank selection register |
| MBS | : Memory bank selection register |
| PCC | : Processor clock control register |
| . | : Separation between address and bit |
| (xx) | : The contents addressed by xx |
| xxH | : Hexadecimal data |

### (3) Explanation of symbols under addressing area column

| | | | |
|---|---|---|---|
| *1 | MB = MBE·MBS<br>(MBS = 0, 1, 15) | | Data memory addressing |
| *2 | MB = 0 | | |
| *3 | MBE = 0 : MB = 0 (000H to 07FH)<br>MB = 15 (F80H to FFFH)<br>MBE = 1 : MB = MBS (MBS = 0, 1, 15) | | |
| *4 | MB = 15, fmem = FB0H to FBFH, FF0H to FFFH | | |
| *5 | MB = 15, pmem = FC0H to FFFH | | |
| *6 | μPD753104 | addr = 000H to FFFH | Program memory addressing |
| | μPD753106 | addr = 0000H to 17FFH | |
| | μPD753108 | addr = 0000H to 1FFFH | |
| *7 | addr = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | | |
| | addr1 = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | | |
| *8 | μPD753104 | caddr = 000H to FFFH | |
| | μPD753106 | caddr = 0000H to 0FFFH ($PC_{12}$ = 0) or<br>1000H to 17FFH ($PC_{12}$ = 1) | |
| | μPD753108 | caddr = 0000H to 0FFFH ($PC_{12}$ = 0) or<br>1000H to 1FFFH ($PC_{12}$ = 1) | |
| *9 | faddr = 0000H to 07FFH | | |
| *10 | taddr = 0020H to 007FH | | |
| *11 | μPD753104 | addr1 = 000H to FFFH | |
| | μPD753106 | addr1 = 0000H to 17FFH | |
| | μPD753108 | addr1 = 0000H to 1FFFH | |

**Remarks 1.** MB indicates memory bank that can be accessed.

**2.** In *2, MB = 0 independently of how MBE and MBS are set.

**3.** In *4 and *5, MB = 15 independently of how MBE and MBS are set.

**4.** *6 to *11 indicate the areas that can be addressed.

**(4) Explanation of number of machine cycles column**

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction Note: S = 2

**Note** 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

**Caution The GETI instruction is skipped in one machine cycle.**

One machine cycle is equal to one cycle of CPU clock (= $t_{CY}$); time can be selected from among four types by setting PCC.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Transfer | MOV | A, #n4 | 1 | 1 | A <- n4 | | String effect A |
| | | reg1, #n4 | 2 | 2 | reg1 <- n4 | | |
| | | XA, #n8 | 2 | 2 | XA <- n8 | | String effect A |
| | | HL, #n8 | 2 | 2 | HL <- n8 | | String effect B |
| | | rp2, #n8 | 2 | 2 | rp2 <- n8 | | |
| | | A, @HL | 1 | 1 | A <- (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A <- (HL), then L <- L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A <- (HL), then L <- L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A <- (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA <- (HL) | *1 | |
| | | @HL, A | 1 | 1 | (HL) <- A | *1 | |
| | | @HL, XA | 2 | 2 | (HL) <- XA | *1 | |
| | | A, mem | 2 | 2 | A <- (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA <- (mem) | *3 | |
| | | mem, A | 2 | 2 | (mem) <- A | *3 | |
| | | mem, XA | 2 | 2 | (mem) <- XA | *3 | |
| | | A, reg | 2 | 2 | A <- reg | | |
| | | XA, rp' | 2 | 2 | XA <- rp' | | |
| | | reg1, A | 2 | 2 | reg1 <- A | | |
| | | rp'1, XA | 2 | 2 | rp'1 <- XA | | |
| | XCH | A, @HL | 1 | 1 | A <-> (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A <-> (HL), then L <- L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A <-> (HL), then L <- L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A <-> (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA <-> (HL) | *1 | |
| | | A, mem | 2 | 2 | A <-> (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA <-> (mem) | *3 | |
| | | A, reg1 | 1 | 1 | A <-> reg1 | | |
| | | XA, rp' | 2 | 2 | XA <-> rp' | | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Table reference | MOVT | XA, @PCDE | 1 | 3 | ●μPD753104<br>XA <- $(PC_{11-8}+DE)_{ROM}$ | | |
| | | | | | ●μPD753106, 753108<br>XA <- $(PC_{12-8}+DE)_{ROM}$ | | |
| | | XA, @PCXA | 1 | 3 | ●μPD753104<br>XA <- $(PC_{11-8}+XA)_{ROM}$ | | |
| | | | | | ●μPD753106, 753108<br>XA <- $(PC_{12-8}+XA)_{ROM}$ | | |
| | | XA, @BCDE | 1 | 3 | XA <- $(BCDE)_{ROM}$ Note | *6 | |
| | | XA, @BCXA | 1 | 3 | XA <- $(BCXA)_{ROM}$ Note | *6 | |
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | CY <- (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY <- $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY <- $(H+mem_{3-0}.bit)$ | *1 | |
| | | fmem.bit, CY | 2 | 2 | (fmem.bit) <- CY | *4 | |
| | | pmem.@L, CY | 2 | 2 | $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ <- CY | *5 | |
| | | @H+mem.bit, CY | 2 | 2 | $(H+mem_{3-0}.bit)$ <- CY | *1 | |
| Operation | ADDS | A, #n4 | 1 | 1+S | A <- A+n4 | | carry |
| | | XA, #n8 | 2 | 2+S | XA <- XA+n8 | | carry |
| | | A, @HL | 1 | 1+S | A <- A+(HL) | *1 | carry |
| | | XA, rp' | 2 | 2+S | XA <- XA+rp' | | carry |
| | | rp'1, XA | 2 | 2+S | rp'1 <- rp'1+XA | | carry |
| | ADDC | A, @HL | 1 | 1 | A, CY <- A+(HL)+CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY <- XA+rp'+CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY <- rp'1+XA+CY | | |
| | SUBS | A, @HL | 1 | 1+S | A <- A–(HL) | *1 | borrow |
| | | XA, rp' | 2 | 2+S | XA <- XA–rp' | | borrow |
| | | rp'1, XA | 2 | 2+S | rp'1 <- rp'1–XA | | borrow |
| | SUBC | A, @HL | 1 | 1 | A, CY <- A–(HL)–CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY <- XA–rp'–CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY <- rp'1–XA–CY | | |

**Note** Set “0” in B register if the μPD753104 is used. Only low-order one bit of B register will be valid if the μPD753106 or 753108 is used.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Operation | AND | A, #n4 | 2 | 2 | A <- A ∧ n4 | | |
| | | A, @HL | 1 | 1 | A <- A ∧ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA <- XA ∧ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 <- rp'1 ∧ XA | | |
| | OR | A, #n4 | 2 | 2 | A <- A ∨ n4 | | |
| | | A, @HL | 1 | 1 | A <- A ∨ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA <- XA ∨ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 <- rp'1 ∨ XA | | |
| | XOR | A, #n4 | 2 | 2 | A <- A ∀ n4 | | |
| | | A, @HL | 1 | 1 | A <- A ∀ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA <- XA ∀ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 <- rp'1 ∀ XA | | |
| Accumulator manipulation | RORC | A | 1 | 1 | CY <- $A_0$, $A_3$ <- CY, $A_{n-1}$ <- $A_n$ | | |
| | NOT | A | 2 | 2 | A <- $\overline{A}$ | | |
| Increment and decrement | INCS | reg | 1 | 1+S | reg <- reg+1 | | reg = 0 |
| | | rp1 | 1 | 1+S | rp1 <- rp1+1 | | rp1 = 00H |
| | | @HL | 2 | 2+S | (HL) <- (HL)+1 | *1 | (HL) = 0 |
| | | mem | 2 | 2+S | (mem) <- (mem)+1 | *3 | (mem) = 0 |
| | DECS | reg | 1 | 1+S | reg <- reg–1 | | reg = FH |
| | | rp' | 2 | 2+S | rp' <- rp'–1 | | rp' = FFH |
| Comparison | SKE | reg, #n4 | 2 | 2+S | Skip if reg = n4 | | reg = n4 |
| | | @HL, #n4 | 2 | 2+S | Skip if (HL) = n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1+S | Skip if A = (HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2+S | Skip if XA = (HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2+S | Skip if A = reg | | A = reg |
| | | XA, rp' | 2 | 2+S | Skip if XA = rp' | | XA = rp' |
| Carry flag manipulation | SET1 | CY | 1 | 1 | CY <- 1 | | |
| | CLR1 | CY | 1 | 1 | CY <- 0 | | |
| | SKT | CY | 1 | 1+S | Skip if CY = 1 | | CY = 1 |
| | NOT1 | CY | 1 | 1 | CY <- $\overline{CY}$ | | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Memory bit manipulation | SET1 | mem.bit | 2 | 2 | (mem.bit) <- 1 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) <- 1 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) <- 1 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) <- 1 | *1 | |
| | CLR1 | mem.bit | 2 | 2 | (mem.bit) <- 0 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) <- 0 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) <- 0 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) <- 0 | *1 | |
| | SKT | mem.bit | 2 | 2+S | Skip if (mem.bit) = 1 | *3 | (mem.bit) = 1 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit) = 1 | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1 | *5 | (pmem.@L) = 1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit) = 1 | *1 | (@H+mem.bit) = 1 |
| | SKF | mem.bit | 2 | 2+S | Skip if (mem.bit) = 0 | *3 | (mem.bit) = 0 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit) = 0 | *4 | (fmem.bit) = 0 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 0 | *5 | (pmem.@L) = 0 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit) = 0 | *1 | (@H+mem.bit) = 0 |
| | SKTCLR | fmem.bit | 2 | 2+S | Skip if (fmem.bit) = 1 and clear | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear | *5 | (pmem.@L) = 1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit) = 1 and clear | *1 | (@H+mem.bit) = 1 |
| | AND1 | CY, fmem.bit | 2 | 2 | CY <- CY ∧ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY <- CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY <- CY ∧ (H+mem$_{3-0}$.bit) | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | CY <- CY ∨ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY <- CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY <- CY ∨ (H+mem$_{3-0}$.bit) | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | CY <- CY ∀ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY <- CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY <- CY ∀ (H+mem$_{3-0}$.bit) | *1 | |

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Branch | BR Note | addr | – | – | ● μPD753104<br>$PC_{11-0}$ <- addr<br>(Select appropriate instruction from among BR !addr, BRCB !caddr and BR $addr according to the assembler being used.) | *6 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr<br>(Select appropriate instruction from among BR !addr, BRCB !caddr and BR $addr according to the assembler being used.) | | |
| | | addr1 | – | – | ● μPD753104<br>$PC_{11-0}$ <- addr1<br>(Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.) | *11 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr1<br>(Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.) | | |
| | | !addr | 3 | 3 | ● μPD753104<br>$PC_{11-0}$ <- addr | *6 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr | | |
| | | $addr | 1 | 2 | ● μPD753104<br>$PC_{11-0}$ <- addr | *7 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr | | |
| | | $addr1 | 1 | 2 | ● μPD753104<br>$PC_{11-0}$ <- addr1 | | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr1 | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Branch | BR | PCDE | 2 | 3 | ● μPD753104<br>$PC_{11-0}$ <- $PC_{11-8}$+DE | | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- $PC_{12-8}$+DE | | |
| | | PCXA | 2 | 3 | ● μPD753104<br>$PC_{11-0}$ <- $PC_{11-8}$+XA | | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- $PC_{12-8}$+XA | | |
| | | BCDE | 2 | 3 | ● μPD753104<br>$PC_{11-0}$ <- BCDE Note 1 | *6 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- BCDE Note 2 | | |
| | | BCXA | 2 | 3 | ● μPD753104<br>$PC_{11-0}$ <- BCXA Note 1 | *6 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- BCXA Note 2 | | |
| | BRA Note 3 | !addr1 | 3 | 3 | ● μPD753104<br>$PC_{11-0}$ <- addr1 | *11 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- addr1 | | |
| | BRCB | !caddr | 2 | 2 | ● μPD753104<br>$PC_{11-0}$ <- $caddr_{11-0}$ | *8 | |
| | | | | | ● μPD753106, 753108<br>$PC_{12-0}$ <- $PC_{12}$+$caddr_{11-0}$ | | |
| Subroutine stack control | CALLA Note 3 | !addr1 | 3 | 3 | ● μPD753104<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, 0<br>$PC_{11-0}$ <- addr1, SP <- SP–6 | *11 | |
| | | | | | ● μPD753106, 753108<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ <- addr1, SP <- SP–6 | | |

**Notes 1.** "0" must be set to B register.

**2.** Only low-order one bit is valid in B register.

**3.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | CALL Note | !addr | 3 | 3 | ● μPD753104<br>(SP–3) <- MBE, RBE, 0, 0<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>$PC_{11-0}$ <- addr, SP <- SP–4 | *6 | |
| | | | | | ● μPD753106, 753108<br>(SP–3) <- MBE, RBE, 0, $PC_{12}$<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>$PC_{12-0}$ <- addr, SP <- SP–4 | | |
| | | | | 4 | ● μPD753104<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, 0<br>$PC_{11-0}$ <- addr, SP <- SP–6 | | |
| | | | | | ● μPD753106, 753108<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ <- addr, SP <- SP–6 | | |
| | CALLF Note | !faddr | 2 | 2 | ● μPD753104<br>(SP–3) <- MBE, RBE, 0, 0<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>$PC_{11-0}$ <- 0+faddr, SP <- SP–4 | *9 | |
| | | | | | ● μPD753106, 753108<br>(SP–3) <- MBE, RBE, 0, $PC_{12}$<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>$PC_{12-0}$ <- 00+faddr, SP <- SP–4 | | |
| | | | | 3 | ● μPD753104<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, 0<br>$PC_{11-0}$ <- 0+faddr, SP <- SP–6 | | |
| | | | | | ● μPD753106, 753108<br>(SP–2) <- x, x, MBE, RBE<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, $PC_{12}$<br>$PC_{12-0}$ <- 00+faddr, SP <- SP–6 | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | RET Note | | 1 | 3 | ● μPD753104<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>MBE, RBE, 0, 0 <- (SP+1), SP <- SP+4 | | |
| | | | | | ● μPD753106, 753108<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>MBE, RBE, 0, $PC_{12}$ <- (SP+1), SP <- SP+4 | | |
| | | | | | ● μPD753104<br>x, x, MBE, RBE <- (SP+4)<br>0, 0, 0, 0, <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2), SP <- SP+6 | | |
| | | | | | ● μPD753106, 753108<br>x, x, MBE, RBE <- (SP+4)<br>MBE, 0, 0, $PC_{12}$ <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2), SP <- SP+6 | | |
| | RETS Note | | 1 | 3+S | ● μPD753104<br>MBE, RBE, 0, 0 <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>SP <- SP+4<br>then skip unconditionally | | Unconditional |
| | | | | | ● μPD753106, 753108<br>MBE, RBE, 0, $PC_{12}$ <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>SP <- SP+4<br>then skip unconditionally | | |
| | | | | | ● μPD753104<br>0, 0, 0, 0 <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>x, x, MBE, RBE <- (SP+4)<br>SP <- SP+6<br>then skip unconditionally | | |
| | | | | | ● μPD753106, 753108<br>0, 0, 0, $PC_{12}$ <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>x, x, MBE, RBE <- (SP+4)<br>SP <- SP+4<br>then skip unconditionally | | |

**Note** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | RETI Note 1 | | 1 | 3 | ● μPD753104<br>MBE, RBE, 0, 0 <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>PSW <- (SP+4) (SP+5), SP <- SP+6 | | |
| | | | | | ● μPD753106, 753108<br>MBE, RBE, 0, $PC_{12}$ <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>PSW <- (SP+4) (SP+5), SP <- SP+6 | | |
| | | | | | ● μPD753104<br>0, 0, 0, 0 <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>PSW <- (SP+4) (SP+5), SP <- SP+6 | | |
| | | | | | ● μPD753106, 753108<br>0, 0, 0, $PC_{12}$ <- (SP+1)<br>$PC_{11-0}$ <- (SP) (SP+3) (SP+2)<br>PSW <- (SP+4) (SP+5), SP <- SP+6 | | |
| | PUSH | rp | 1 | 1 | (SP–1) (SP–2) <- rp, SP <- SP–2 | | |
| | | BS | 2 | 2 | (SP–1) <- MBS, (SP–2) <- RBS, SP <- SP–2 | | |
| | POP | rp | 1 | 1 | rp <- (SP+1) (SP), SP <- SP+2 | | |
| | | BS | 2 | 2 | MBS <- (SP+1), RBS <- (SP), SP <- SP+2 | | |
| Interrupt control | EI | | 2 | 2 | IME (IPS.3) <- 1 | | |
| | | IExxx | 2 | 2 | IExxx <- 1 | | |
| | DI | | 2 | 2 | IME (IPS.3) <- 0 | | |
| | | IExxx | 2 | 2 | IExxx <- 0 | | |
| Input/output | IN Note 2 | A, PORTn | 2 | 2 | A <- PORTn (n = 0-3, 5, 6, 8, 9) | | |
| | | XA, PORTn | 2 | 2 | XA <- PORTn+1, PORTn (n = 8) | | |
| | OUT Note 2 | PORTn, A | 2 | 2 | PORTn <- A (n = 3, 5, 6, 8, 9) | | |
| | | PORTn, XA | 2 | 2 | PORTn+1, PORTn <- XA (n = 8) | | |
| CPU control | HALT | | 2 | 2 | Set HALT Mode (PCC.2 <- 1) | | |
| | STOP | | 2 | 2 | Set STOP Mode (PCC.3 <- 1) | | |
| | NOP | | 1 | 1 | No Operation | | |
| Special | SEL | RBn | 2 | 2 | RBS <- n (n = 0-3) | | |
| | | MBn | 2 | 2 | MBS <- n (n = 0, 1, 15) | | |

**Notes 1.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**2.** While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1, and MBS must be set to 15.

| Instruction group | Mnemonic | Operand | Number of bytes | Number of machine cycles | Operation | Addressing area | Skip condition |
|---|---|---|---|---|---|---|---|
| Special | GETI Note 1, 2 | taddr | 1 | 3 | ● μPD753104<br>• When TBR instruction<br>$PC_{11-0}$ <- (taddr)$_{3-0}$ + (taddr+1) | *10 | |
| | | | | | • When TCALL instruction<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>(SP–3) <- MBE, RBE, 0, 0<br>$PC_{11-0}$ <- (taddr)$_{3-0}$ + (taddr+1)<br>SP <- SP–4 | | |
| | | | | | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | | ● μPD753106, 753108<br>• When TBR instruction<br>$PC_{12-0}$ <- (taddr)$_{4-0}$ + (taddr+1) | | |
| | | | | | • When TCALL instruction<br>(SP–4) (SP–1) (SP–2) <- $PC_{11-0}$<br>(SP–3) <- MBE, RBE, 0, $PC_{12}$<br>$PC_{12-0}$ <- (taddr)$_{4-0}$ + (taddr+1)<br>SP <- SP–4 | | |
| | | | | | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | 3 | ● μPD753104<br>• When TBR instruction<br>$PC_{11-0}$ <- (taddr)$_{3-0}$ + (taddr+1) | *10 | |
| | | | | 4 | • When TCALL instruction<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, 0<br>(SP–2) <- x, x, MBE, RBE<br>$PC_{11-0}$ <- (taddr)$_{3-0}$ + (taddr+1)<br>SP <- SP–6 | | |
| | | | | 3 | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |
| | | | | 3 | ● μPD753106, 753108<br>• When TBR instruction<br>$PC_{12-0}$ <- (taddr)$_{4-0}$ + (taddr+1) | | |
| | | | | 4 | • When TCALL instruction<br>(SP–6) (SP–3) (SP–4) <- $PC_{11-0}$<br>(SP–5) <- 0, 0, 0, $PC_{12}$<br>(SP–2) <- x, x, MBE, RBE<br>$PC_{12-0}$ <- (taddr)$_{4-0}$ + (taddr+1)<br>SP <- SP–6 | | |
| | | | | 3 | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed. | | Depending on the reference instruction |

**Notes 1.** The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.

**2.** The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

## 12. ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C)

| Parameter | Symbol | Test Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| Input voltage | $V_{I1}$ | Except port 5 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | Port 5 | On-chip pull-up resistor | –0.3 to $V_{DD}$ + 0.3 | V |
| | | | When N-ch open-drain | –0.3 to +14 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current high | $I_{OH}$ | Per pin | | –10 | mA |
| | | Total of all pins | | –30 | mA |
| Output current low | $I_{OL}$ | Per pin | | 30 | mA |
| | | Total of all pins | | 220 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 Note | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

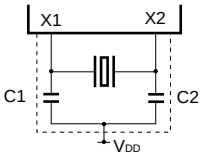
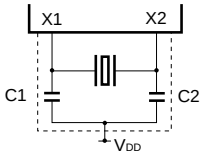
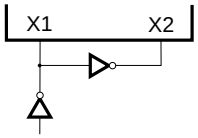
**Note** When LCD is driven in normal mode: $T_A$ = –10 to +85 °C

**Caution Exposure to Absolute Maximum Ratings even for instant may affect device reliability; exceeding the ratings could cause parmanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.**

### CAPACITANCE ($T_A$ = 25 °C, $V_{DD}$ = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz<br>Unmeasured pins returned to 0 V. | | | 15 | pF |
| Output capacitance | $C_{OUT}$ | | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | | | | 15 | pF |

**MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended constant | Parameter | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillation frequency (fx) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| | | Oscillation stabilization time Note 3 | After $V_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency (fx) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| | | Oscillation stabilization time Note 3 | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock |  | X1 input frequency (fx) Note 1 | | 1.0 | | 6.0 Note 2 | MHz |
| ★ | | X1 input high/low-level width ($t_{XH}$, $t_{XL}$) | | 83.3 | | 500 | ns |

**Notes 1.** The oscillation frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to the AC characteristics.

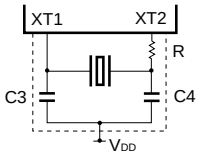
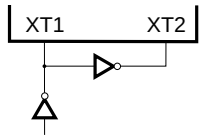
**2.** When the oscillation frequency is 4.19 MHz < fx ≤ 6.0 MHz at 1.8 V ≤ $V_{DD}$ < 2.7 V, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle time being less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

**3.** The oscillation stabilization time is necessary for oscillation to stabilize after applying $V_{DD}$ or releasing the STOP mode.

**Caution When using the main system clock oscillator, wiring in the area enclosed with the dotted line in the above figure should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as $V_{DD}$.**
- **Do not ground to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

**SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended constant | Parameter | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator |  | Oscillation frequency ($f_{XT}$) Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time Note 2 | $V_{DD}$ = 4.5 to 5.5 V | | 1.0 | 2 | s |
| | | | | | | 10 | |
| External clock |  | XT1 input frequency ($f_{XT}$) Note 1 | | 32 | | 100 | kHz |
| | | X1 input high/low-level width ($t_{XTH}$, $t_{XTL}$) | | 5 | | 15 | μs |

**Notes 1.** Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

**2.** The oscillation stabilization time is necessary for oscillation to stabilize after applying $V_{DD}$.

**Caution When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line in the above figure should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as $V_{DD}$.**
- **Do not ground to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

**The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, causing misoperation by noise more frequently than the main system clock oscillator. Special care should therefore be taken for wiring method when the subsystem clock is used.**

**RECOMMENDED OSCILLATOR CONSTANT**

**Ceramic Resonator ($T_A$ = –20 to +85 °C)**

| Manufacturer | Product name | Frequency (MHz) | Oscillator constant (pF) | | Oscillation voltage range ($V_{DD}$) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| Kyocera Corporation | KBR-1000F/Y | 1.0 | 100 | 100 | 1.8 | 5.5 | — |
| | KBR-2.0MS | 2.0 | 82 | 82 | 2.2 | | |
| | KBR-4.19MSA | 4.19 | 33 | 33 | 1.8 | | |
| | KBR-4.19MKS | | — | — | | | On-chip capacitor product |
| | PBRC 4.19A | | 33 | 33 | | | — |
| | PBRC 4.19B | | — | — | | | On-chip capacitor product |
| | KBR-6.0MSA | 6.0 | 33 | 33 | | | — |
| | KBR-6.0MKS | | — | — | | | On-chip capacitor product |
| | PBRC 6.00A | | 33 | 33 | | | — |
| | PBRC 6.00B | | — | — | | | On-chip capacitor product |

**Ceramic Resonator ($T_A$ = –40 to +85 °C)**

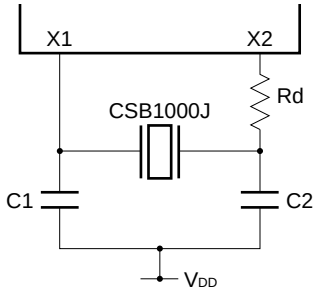
| Manufacturer | Product name | Frequency (MHz) | Oscillator constant (pF) | | Oscillation voltage range ($V_{DD}$) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| TDK | CCR1000K2 | 1.0 | 150 | 150 | 2.3 | 5.5 | — |
| | CCR2.0MC33 | 2.0 | — | — | 2.0 | | On-chip capacitor product |
| | FCR4.19MC5 | 4.19 | | | | | |
| | CCR4.19MC3 | | | | | | |
| | FCR6.0MC5 | 6.0 | | | 2.2 | | |
| | CCR6.0MC3 | | | | | | |

**Ceramic Resonator ($T_A$ = –20 to +80 °C)**

| Manufacturer | Product name | Frequency (MHz) | Oscillator constant (pF) | | Oscillation voltage range ($V_{DD}$) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| Murata Mfg. | CSB1000J | 1.0 | 100 | 100 | 2.4 | 5.5 | Rd = 5.6 kΩ Note |
| Co., Ltd. | CSA2.00MG | 2.0 | 30 | 30 | 1.8 | | — |
| | CST2.00MGW | | — | — | | | On-chip capacitor product |
| | CSA3.00MG | 3.0 | 30 | 30 | | | — |
| | CST3.00MGW | | — | — | | | On-chip capacitor product |
| | CSA4.19MG | 4.19 | 30 | 30 | | | — |
| | CST4.19MGW | | — | — | | | On-chip capacitor product |
| | CSA5.00MG | 5.0 | 30 | 30 | 2.2 | | — |
| | CSA5.00MGU | | | | 1.8 | | |
| | CST5.00MGW | | — | — | 2.2 | | On-chip capacitor product |
| | CST5.00MGWU | | | | 1.8 | | |
| | CSA6.00MG | 6.0 | 30 | 30 | 2.5 | | — |
| | CSA6.00MGU | | | | 1.8 | | |
| | CST6.00MGW | | — | — | 2.5 | | On-chip capacitor product |
| | CST6.00MGWU | | | | 1.8 | | |

**Note** If using the CSB1000J (1.0-MHz) ceramic resonator manufactured by Murata Mfg. Co., Ltd., a limiting resistor (Rd = 5.6 kΩ) is required (see figure below). A limiting resistor is not required if using the other recommended resonators.

**Recommended Main System Clock Circuit Example (using Murata Mfg. Co., Ltd. CSB1000J)**



**Crystal Resonator**

| Manufacturer | Product name | Frequency (MHz) | Oscillator constant (pF) | | Oscillation voltage range ($V_{DD}$) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| Kinseki | HC-49/U | 2.0 | 15 | 15 | 1.8 | 5.5 | $T_A$ = –20 to +70 °C |
| | | 4.19 | | | | | |
| | | 6.0 | | | 2.5 | 5.5 | |
| | HC-49/U-S | 4.19 | | | 1.8 | 5.5 | $T_A$ = –10 to +70 °C |
| | | 6.0 | | | 2.5 | 5.5 | |

**Caution The oscillator constant and the oscillation voltage range represent conditions for stable oscillation, but do not guarantee an accurate oscillation frequency. For an application circuit requiring an accurate oscillation frequency, it may be necessary to adjust the oscillation frequency of the resonator in the application circuit, in which case inquiries should be directed to the manufacturer of the resonator.**

**DC CHARACTERISTICS ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| | Parameter | Symbol | Test conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| ★ | Output current low | $I_{OL}$ | Per pin | | | | | 15 | mA |
| | | | Total of all pins | | | | | 150 | mA |
| | Input voltage high | $V_{IH1}$ | Ports 2, 3, 8, 9 | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | $V_{IH2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | $V_{IH3}$ | Port 5 | On-chip pull-up resistor | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | | | When N-ch open-drain | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0.7$V_{DD}$ | | 13 | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0.9$V_{DD}$ | | 13 | V |
| | | $V_{IH4}$ | X1, XT1 | | | $V_{DD}$–0.1 | | $V_{DD}$ | V |
| | Input voltage low | $V_{IL1}$ | Ports 2, 3, 5, 8, 9 | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.3$V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | 0.1$V_{DD}$ | V |
| | | $V_{IL2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.2$V_{DD}$ | V |
| | | | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | 0.1$V_{DD}$ | V |
| | | $V_{IL3}$ | X1, XT1 | | | 0 | | 0.1 | V |
| | Output voltage high | $V_{OH}$ | $\overline{\text{SCK}}$, SO, ports 2, 3, 6, 8, 9 $I_{OH}$ = –1.0 mA | | | $V_{DD}$–0.5 | | | V |
| | Output voltage low | $V_{OL1}$ | $\overline{\text{SCK}}$, SO, ports 2, 3, 5, 6, 8, 9 | | $I_{OL}$ = 15 mA, $V_{DD}$ = 4.5 to 5.5 V | | 0.2 | 2.0 | V |
| | | | | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | | $V_{OL2}$ | SB0, SB1 | N-ch open-drain pull-up resistor ≥ 1 kΩ | | | | 0.2$V_{DD}$ | V |
| | Input leakage current high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Pins other than X1, XT1 | | | | 3 | μA |
| | | $I_{LIH2}$ | | X1, XT1 | | | | 20 | μA |
| | | $I_{LIH3}$ | $V_{IN}$ = 13 V | Port 5 (When N-ch open-drain) | | | | 20 | μA |
| | Input leakage current low | $I_{LIL1}$ | $V_{IN}$ = 0 V | Pins other than X1, XT1, port 5 | | | | –3 | μA |
| | | $I_{LIL2}$ | | X1, XT1 | | | | –20 | μA |
| ★ | | $I_{LIL3}$ | | Port 5 (When N-ch open-drain) When input instruction is not executed | | | | –3 | μA |
| | | | | Port 5 (When N-ch open-drain) When input instruction is executed | | | | –30 | μA |
| | | | | | $V_{DD}$ = 5.0 V | | –10 | –27 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | –3 | –8 | μA |
| | Output leakage current high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | $\overline{\text{SCK}}$, SO/SB0, SB1, ports 2, 3, 6, 8, 9, port 5 (When N-ch open-drain) | | | | 3 | μA |
| | | $I_{LOH2}$ | $V_{OUT}$ = 13 V | Port 5 (When N-ch open-drain) | | | | 20 | μA |
| | Output leakage current low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | | –3 | μA |
| | On-chip pull-up resistor | $R_{L1}$ | $V_{IN}$ = 0 V | Ports 0 to 3, 6, 8, 9 (Excluding P00 pin) | | 50 | 100 | 200 | kΩ |
| | | $R_{L2}$ | | Port 5 (mask option) | | 15 | 30 | 60 | kΩ |

**DC CHARACTERISTICS ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| | Parameter | Symbol | Test conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| ★ | LCD drive voltage | $V_{LCD}$ | VAC0 = 0 | TA = –40 to +85 °C | | 2.7 | | $V_{DD}$ | V |
| | | | | TA = –10 to +85 °C | | 2.2 | | $V_{DD}$ | V |
| | | | VAC0 = 1 | | | 1.8 | | $V_{DD}$ | V |
| | VAC current Note 1 | $I_{VAC}$ | VAC0 = 1, $V_{DD}$ = 2.0 V ± 10% | | | | 1 | 4 | μA |
| | LCD split resistor Note 2 | $R_{LCD1}$ | | | | 50 | 100 | 200 | kΩ |
| | | $R_{LCD2}$ | | | | 5 | 10 | 20 | kΩ |
| ★ | LCD output voltage deviation Note 3 (common) | $V_{ODC}$ | $I_O$ = ±1.0 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD}$ x 2/3<br>$V_{LCD2} = V_{LCD}$ x 1/3<br>1.8 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | 0 | | ±0.2 | V |
| | | | $I_O$ = ±5.0 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD}$ x 2/3<br>$V_{LCD2} = V_{LCD}$ x 1/3<br>2.2 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | 0 | | ±0.2 | V |
| ★ | LCD output voltage deviation Note 3 (segment) | $V_{ODS}$ | $I_O$ = ±0.5 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD}$ x 2/3<br>$V_{LCD2} = V_{LCD}$ x 1/3<br>1.8 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | 0 | | ±0.2 | V |
| | | | $I_O$ = ±1.0 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD}$ x 2/3<br>$V_{LCD2} = V_{LCD}$ x 1/3<br>2.2 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | 0 | | ±0.2 | V |
| | Supply current Note 4 | $I_{DD1}$ | 6.0 MHz Note 5 Crystal oscillation | $V_{DD}$ = 5.0 V ± 10% Note 6 | | | 1.9 | 6.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ± 10% Note 7 | | | 0.4 | 1.3 | mA |
| | | $I_{DD2}$ | C1 = C2 = 22 pF | HALT mode | $V_{DD}$ = 5.0 V ± 10% | | 0.72 | 2.1 | mA |
| | | | | | $V_{DD}$ = 3.0 V ± 10% | | 0.27 | 0.8 | mA |
| | | $I_{DD1}$ | 4.19 MHz Note 5 Crystal oscillation | $V_{DD}$ = 5.0 V ± 10% Note 6 | | | 1.5 | 4.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ± 10% Note 7 | | | 0.25 | 0.75 | mA |
| | | $I_{DD2}$ | C1 = C2 = 22 pF | HALT mode | $V_{DD}$ = 5.0 V ± 10% | | 0.7 | 2.0 | mA |
| | | | | | $V_{DD}$ = 3.0 V ± 10% | | 0.23 | 0.7 | mA |
| | | $I_{DD3}$ | 32.768 kHz Note 8 Crystal oscillation | Low-voltage mode Note 9 | $V_{DD}$ = 3.0 V ± 10% | | 12 | 35.0 | μA |
| | | | | | $V_{DD}$ = 2.0 V ± 10% | | 4.5 | 12.0 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | 12 | 24.0 | μA |
| | | | | Low current consumption mode Note 10 | $V_{DD}$ = 3.0 V ± 10% | | 6.0 | 18.0 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | 6.0 | 12.0 | μA |
| | | $I_{DD4}$ | | HALT mode | Low-voltage mode Note 9 | $V_{DD}$ = 3.0 V ± 10% | | 8.5 | 25 | μA |
| | | | | | | $V_{DD}$ = 2.0 V ± 10% | | 3.0 | 9.0 | μA |
| | | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | 8.5 | 17 | μA |
| | | | | | Low current consumption mode Note 10 | $V_{DD}$ = 3.0 V ± 10% | | 3.5 | 12 | μA |
| | | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | 3.5 | 7.0 | μA |
| | | $I_{DD5}$ | XT1 = 0 V Note 11 STOP mode | $V_{DD}$ = 5.0 V ± 10% | | | 0.05 | 10 | μA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | | 0.02 | 5.0 | μA |
| | | | | | $T_A$ = 25 °C | | 0.02 | 3.0 | μA |

★ **Notes 1.** Clear VAC0 to 0 in the low current consumption mode and STOP mode. When VAC0 is set to 1, the current increases by about 1 μA.

**2.** Either $R_{LCD1}$ or $R_{LCD2}$ can be selected by the mask option.

**3.** The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs ($V_{LCDn}$; n = 0, 1, 2).

**4.** Not including currents flowing in on-chip pull-up resistors or LCD split resistors.

**5.** Including oscillation of the subsystem clock.

**6.** When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

**7.** When PCC is set to 0000 and the device is operated in the low-speed mode.

**8.** When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

★ **9.** When the sub-oscillator control register (SOS) is set to 0000.

★ **10.** When the SOS is set to 0010.

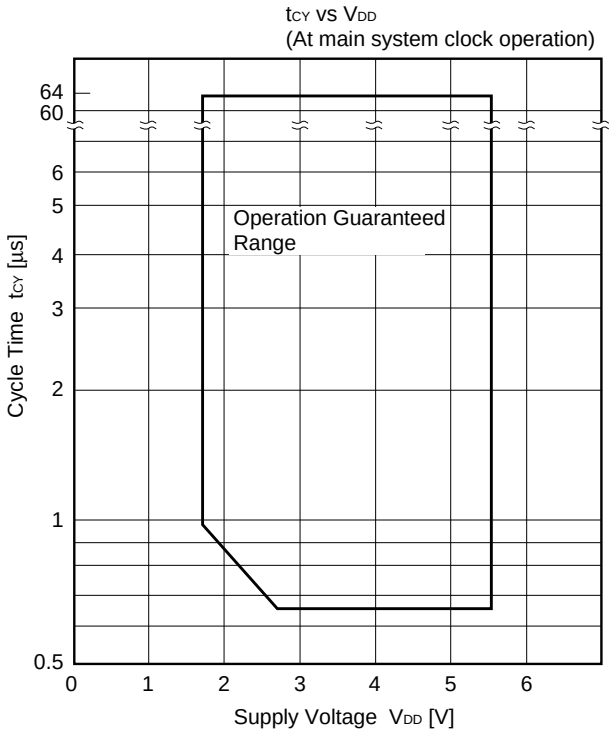
★ **11.** When the SOS is set to 00x1, and the sub-oscillator feedback resistor is not used (x : don't care).

**AC CHARACTERISTICS ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock cycle time Note 1 (minimum instruction execution time = 1 machine cycle) | $t_{CY}$ | Operating on main system clock | $V_{DD}$ = 2.7 to 5.5 V | 0.67 | | 64 | μs |
| | | | | 0.95 | | 64 | μs |
| | | Operating on subsystem clock | | 114 | 122 | 125 | μs |
| TI0, TI1, TI2 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0 | | 1.0 | MHz |
| | | | | 0 | | 275 | kHz |
| TI0, TI1, TI2 input high/low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.48 | | | μs |
| | | | | 1.8 | | | μs |
| Interrupt input high/low-level width | $t_{INTH}$, $t_{INTL}$ | INT0 | IM02 = 0 | **Note 2** | | | μs |
| | | | IM02 = 1 | 10 | | | μs |
| | | INT1, 2, 4 | | 10 | | | μs |
| | | KR0-KR3 | | 10 | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | μs |

**Notes 1.** The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time $t_{CY}$ versus supply voltage $V_{DD}$ characteristic with the main system clock operating.

**2.** $2t_{CY}$ or 128/fx is set by setting the interrupt mode register (IM0).



### SERIAL TRANSFER OPERATION

**2-Wire and 3-Wire Serial I/O Modes ($\overline{SCK}$...Internal clock output): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL1}$, $t_{KH1}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY1}$/2–50 | | | ns |
| | | | | $t_{KCY1}$/2–150 | | | ns |
| SI Note 1 setup time (to $\overline{SCK}$↑) | $t_{SIK1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SI Note 1 hold time (from $\overline{SCK}$↑) | $t_{KSI1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| SO Note 1 output delay time from $\overline{SCK}$↓ | $t_{KSO1}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF Note 2 | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |

**Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output line.

**2-Wire and 3-Wire Serial I/O Modes ($\overline{SCK}$...External clock input): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL2}$, $t_{KH2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 1600 | | | ns |
| SI Note 1 setup time (to $\overline{SCK}$↑) | $t_{SIK2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI Note 1 hold time (from $\overline{SCK}$↑) | $t_{KSI2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| SO Note 1 output delay time from $\overline{SCK}$↓ | $t_{KSO2}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF Note 2 | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |

**Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output line.

**SBI Mode ($\overline{SCK}$...Internal clock output (master)): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL3}$, $t_{KH3}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY3}/2-50$ | | | ns |
| | | | | $t_{KCY3}/2-150$ | | | ns |
| SB0, 1 setup time (to $\overline{SCK}\uparrow$) | $t_{SIK3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}\uparrow$) | $t_{KSI3}$ | | | $t_{KCY3}/2$ | | | ns |
| SB0, 1 output delay time from $\overline{SCK}\downarrow$ | $t_{KSO3}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}\uparrow$ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| $\overline{SCK}\downarrow$ from SB0, 1↓ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |

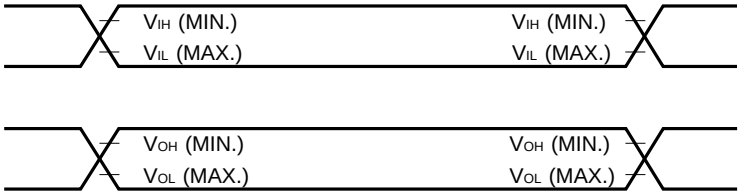
**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0, 1 output line.

**SBI Mode ($\overline{SCK}$...External clock input (slave)): ($T_A$ = –40 to +85 °C, $V_{DD}$ = 1.8 to 5.5 V)**

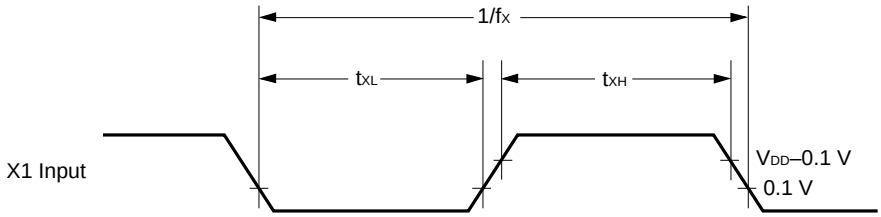
| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high/low-level width | $t_{KL4}$, $t_{KH4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 1600 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}\uparrow$) | $t_{SIK4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}\uparrow$) | $t_{KSI4}$ | | | $t_{KCY4}/2$ | | | ns |
| SB0, 1 output delay time from $\overline{SCK}\downarrow$ | $t_{KSO4}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}\uparrow$ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK}\downarrow$ from SB0, 1↓ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |

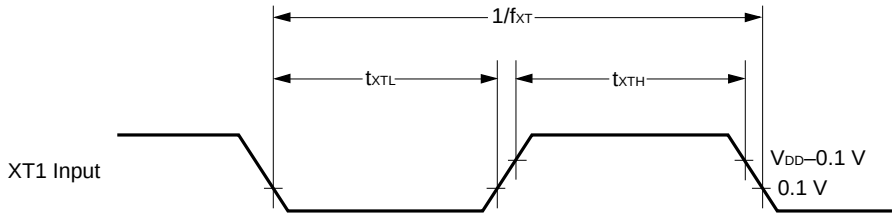
**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0, 1 output line.

★ **AC Timing Test Point (Excluding X1, XT1 inputs)**

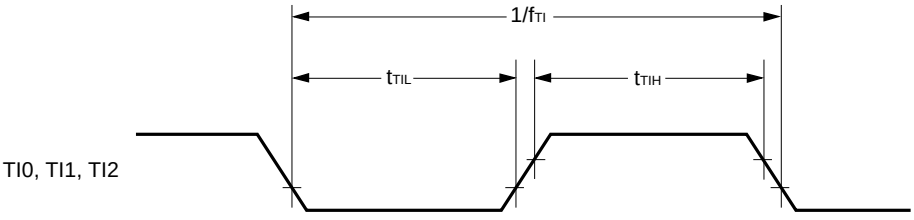



**Clock Timing**



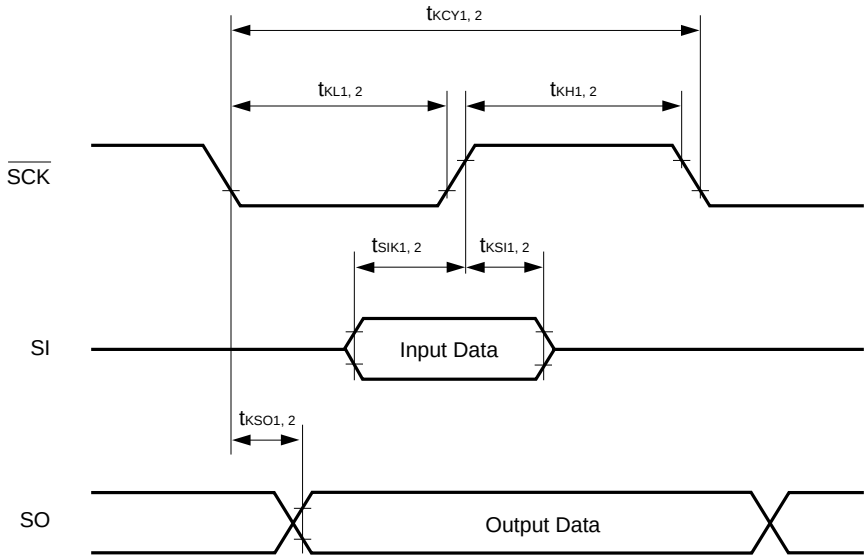




**TI0, TI1, TI2 Timing**

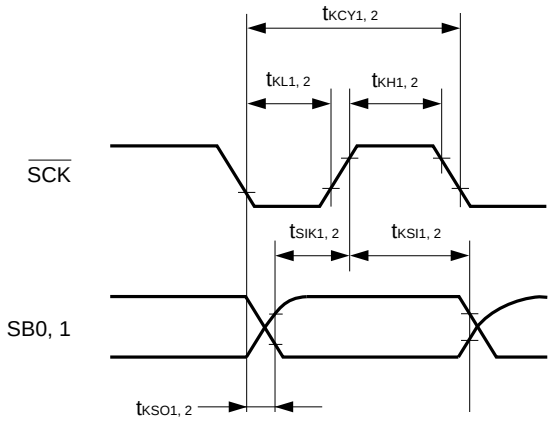


**Serial Transfer Timing**

**3-wire serial I/O mode**

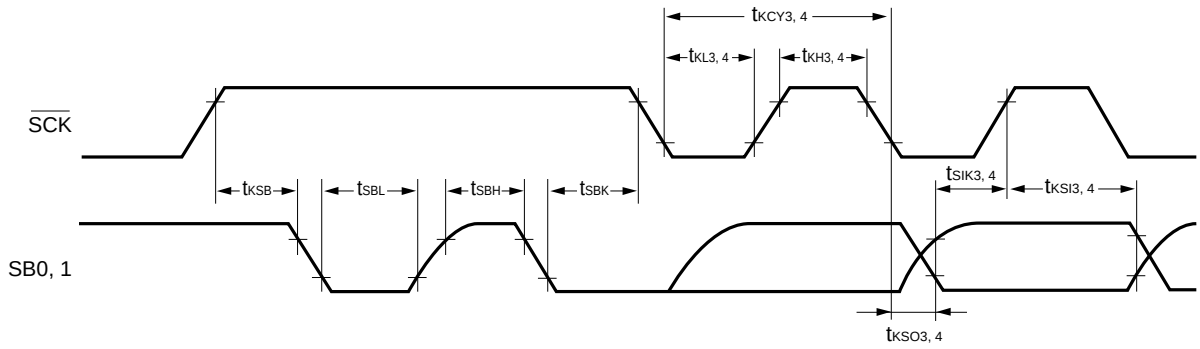



**2-wire serial I/O mode**

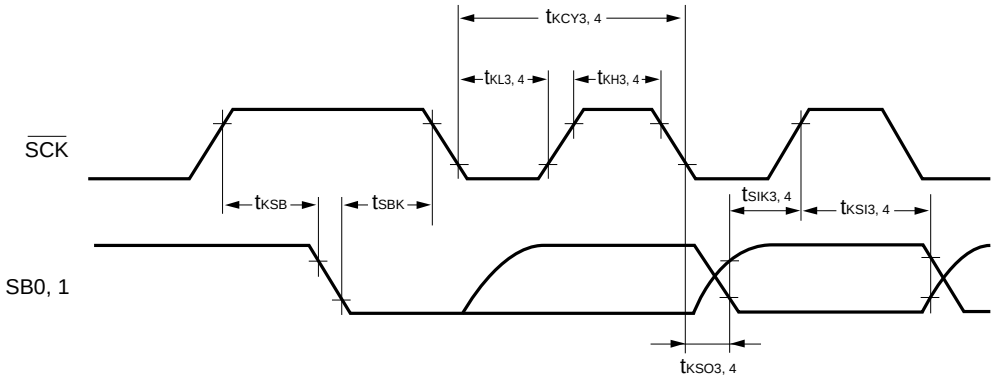


### Serial Transfer Timing

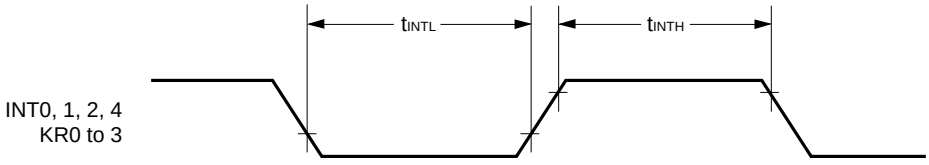
#### Bus release signal transfer



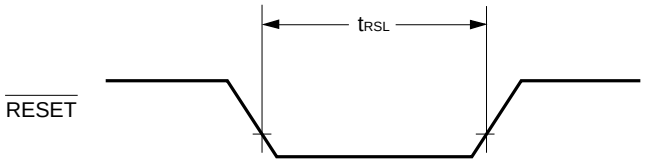

#### Command signal transfer




#### Interrupt input timing




#### $\overline{\text{RESET}}$ input timing



**DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS**

**($T_A$ = –40 to +85 °C)**

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Release signal set time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time Note 1 | $t_{WAIT}$ | Release by $\overline{RESET}$ | | **Note 2** | | ms |
| | | Release by interrupt request | | **Note 3** | | ms |

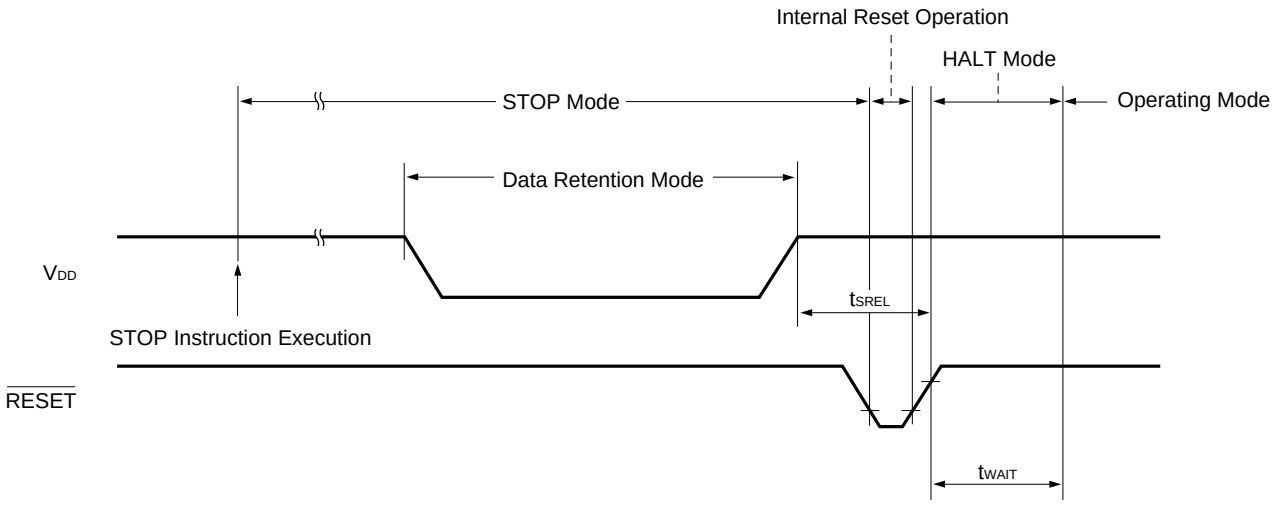
**Notes 1.** The oscillation stabillization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

**2.** Either $2^{17}/f_X$ or $2^{15}/f_X$ can be selected by the mask option.

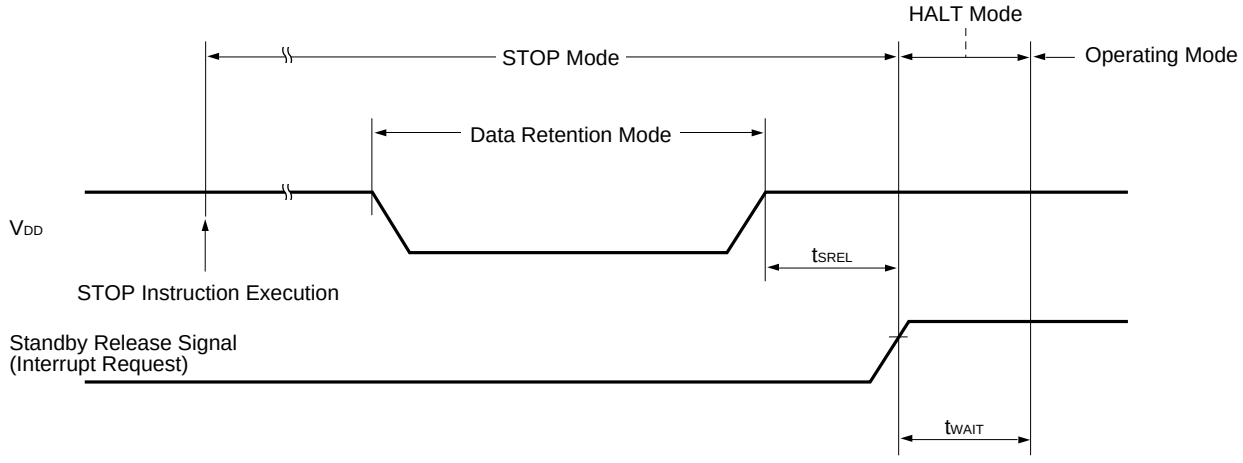
**3.** Depends on the basic interval timer mode register (BTM) settings (see the table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time | |
|---|---|---|---|---|---|
| | | | | fx = at 4.19 MHz | fx = at 6.0 MHz |
| — | 0 | 0 | 0 | $2^{20}/fx$ (approx. 250 ms) | $2^{20}/fx$ (approx. 175 ms) |
| — | 0 | 1 | 1 | $2^{17}/fx$ (approx. 31.3 ms) | $2^{17}/fx$ (approx. 21.8 ms) |
| — | 1 | 0 | 1 | $2^{15}/fx$ (approx. 7.81 ms) | $2^{15}/fx$ (approx. 5.46 ms) |
| — | 1 | 1 | 1 | $2^{13}/fx$ (approx. 1.95 ms) | $2^{13}/fx$ (approx. 1.37 ms) |

**Data Retention Timing (STOP Mode Release by $\overline{RESET}$)**

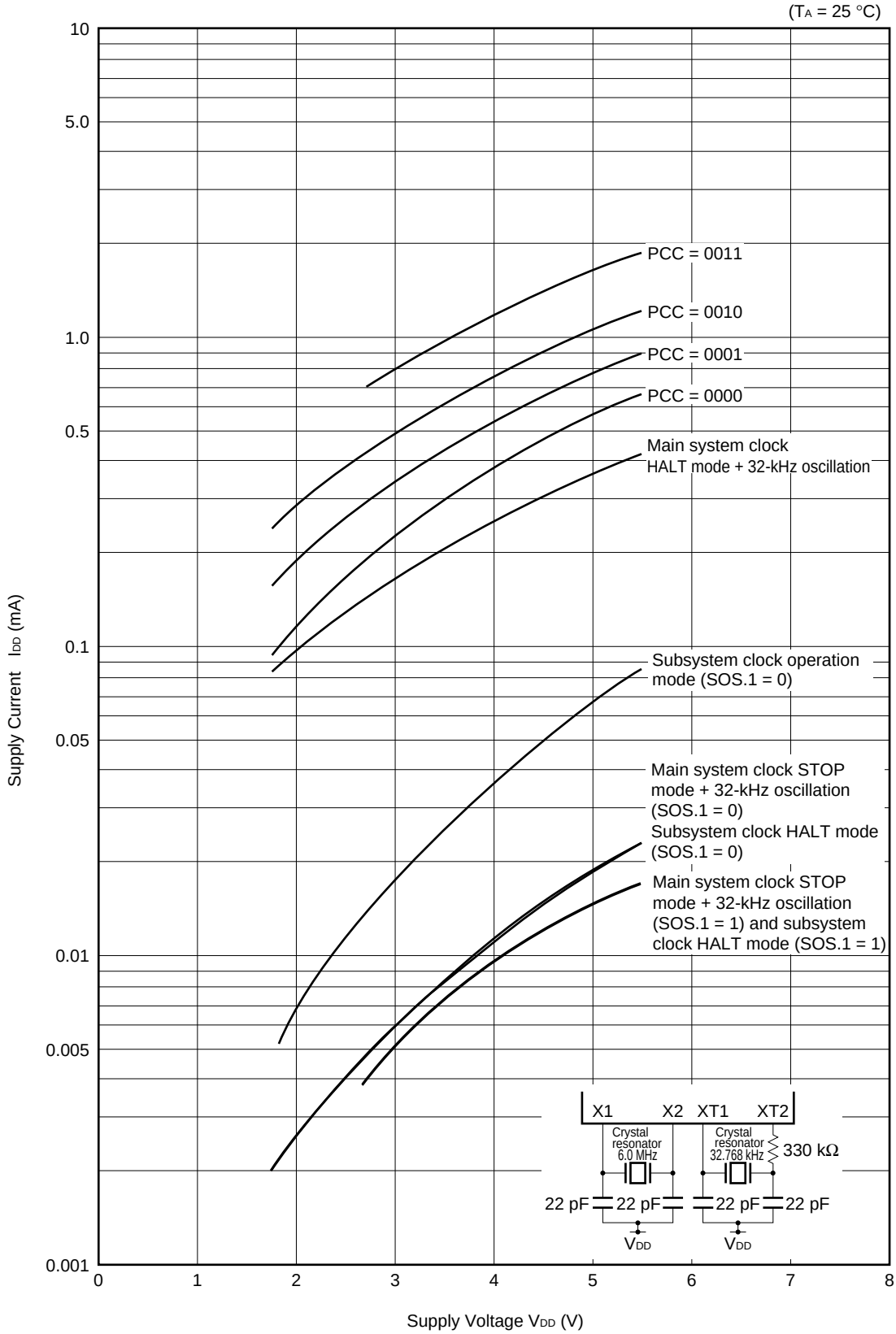



**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**

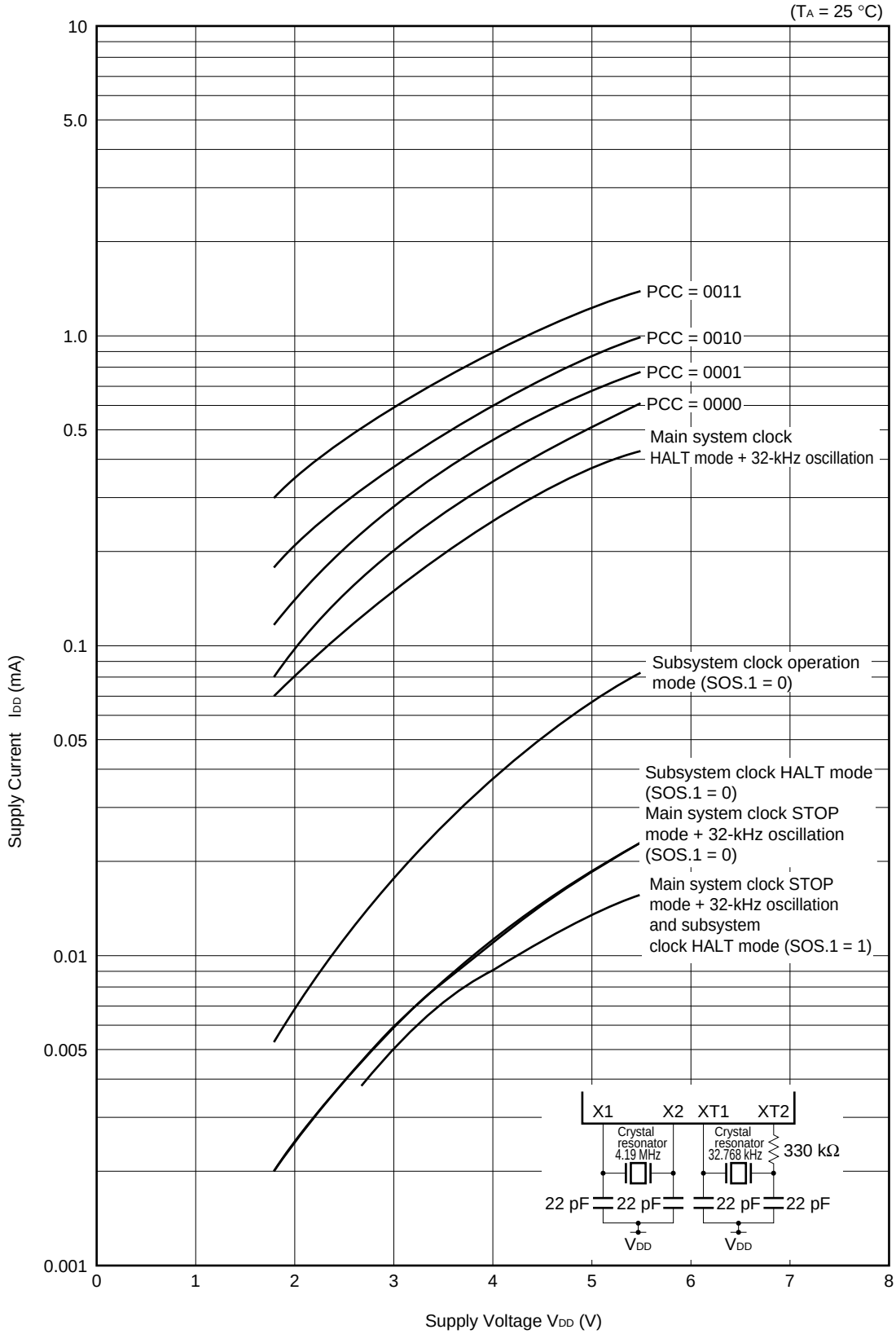


## 13. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

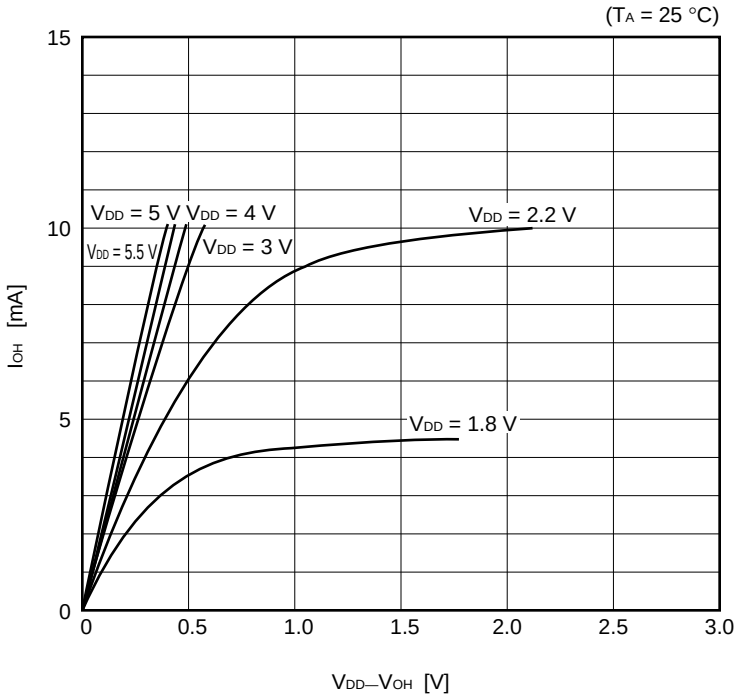
**$I_{DD}$ vs $V_{DD}$ (Main System Clock: 6.0-MHz Crystal Resonator)**



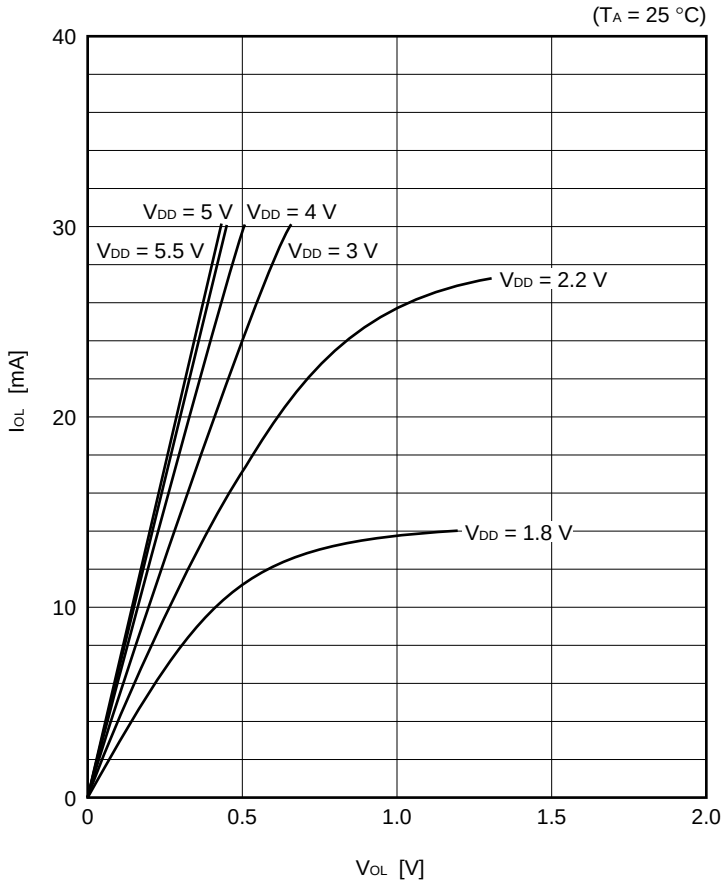
**$I_{DD}$ vs $V_{DD}$ (Main System Clock: 4.19-MHz Crystal Resonator)**



**$I_{OH}$ vs $V_{DD}$—$V_{OH}$ (Ports 2, 3, 6, 8 and 9)**

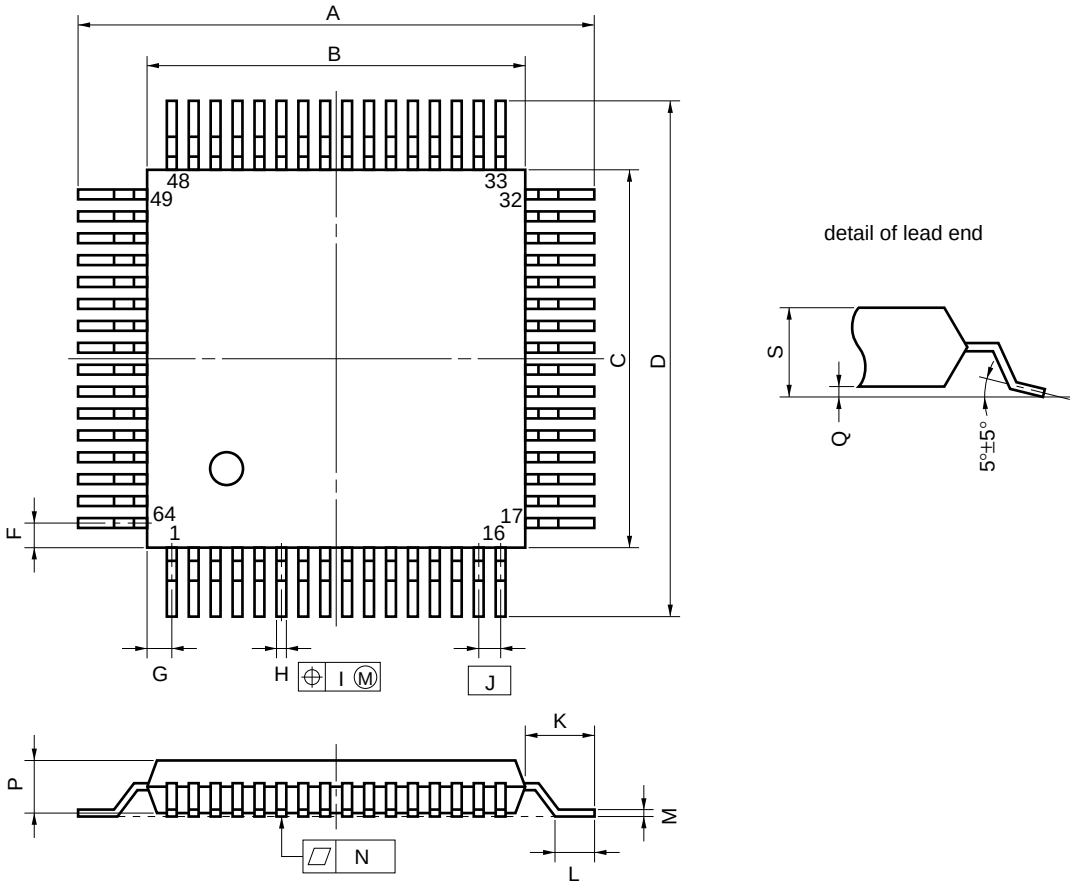



**$I_{OL}$ vs $V_{OL}$ (Ports 2, 3, 6, 8 and 9)**



## 14. PACKAGE DRAWINGS

### 64-PIN PLASTIC QFP (14 x 14 mm)



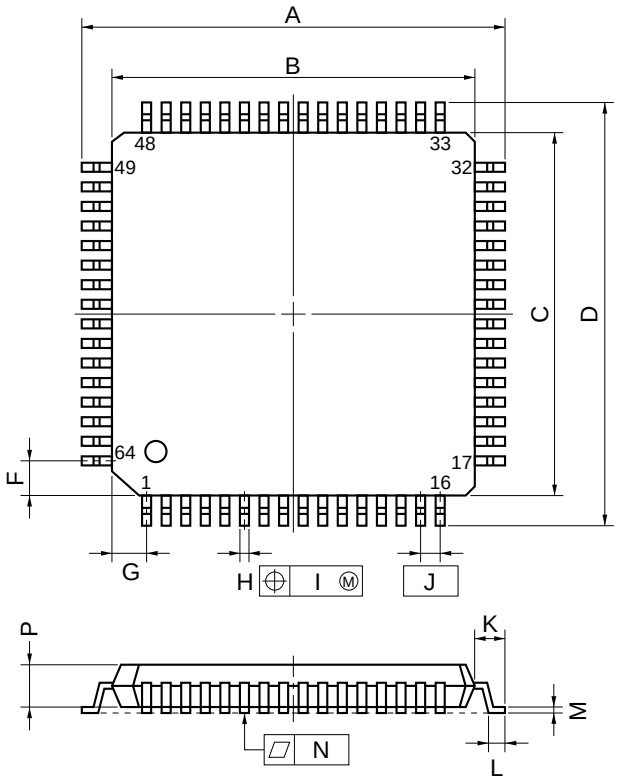

P64GC-80-AB8-3

**NOTE**

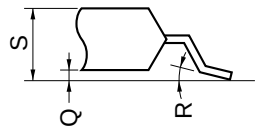
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 17.6±0.4 | 0.693±0.016 |
| B | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| C | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 1.0 | 0.039 |
| G | 1.0 | 0.039 |
| H | 0.35±0.10 | $0.014^{+0.004}_{-0.005}$ |
| I | 0.15 | 0.006 |
| J | 0.8 (T.P.) | 0.031 (T.P.) |
| K | 1.8±0.2 | 0.071±0.008 |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.003}$ |
| N | 0.10 | 0.004 |
| P | 2.55 | 0.100 |
| Q | 0.1±0.1 | 0.004±0.004 |
| S | 2.85 MAX. | 0.112 MAX. |

**64-PIN PLASTIC LQFP (12 x 12 mm)**




detail of lead end




**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 14.8±0.4 | 0.583±0.016 |
| B | 12.0±0.2 | $0.472^{+0.009}_{-0.008}$ |
| C | 12.0±0.2 | $0.472^{+0.009}_{-0.008}$ |
| D | 14.8±0.4 | 0.583±0.016 |
| F | 1.125 | 0.044 |
| G | 1.125 | 0.044 |
| H | 0.30±0.10 | $0.012^{+0.004}_{-0.005}$ |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.4±0.2 | 0.055±0.008 |
| L | 0.6±0.2 | $0.024^{+0.008}_{-0.009}$ |
| M | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.003}$ |
| N | 0.10 | 0.004 |
| P | 1.4 | 0.055 |
| Q | 0.125±0.075 | 0.005±0.003 |
| R | 5°±5° | 5°±5° |
| S | 1.7 MAX. | 0.067 MAX. |

**P64GK-65-8A8-1**

## 15. RECOMMENDED SOLDERING CONDITIONS

The μPD753108 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 15-1. Surface Mounting Type Soldering Conditions**

★ **(1) μPD753104GC-xxx-AB8 : 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)**
**μPD753106GC-xxx-AB8 : 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)**
**μPD753108GC-xxx-AB8 : 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Peak package's surface temperature: 235 ˚C, Reflow time: 30 seconds or less (at 210 ˚C or higher), Number of reflow processes: 3 max. | IR35-00-3 |
| VPS | Peak package's surface temperature: 215 ˚C, Reflow time: 40 seconds or less (at 200 ˚C or higher), Number of reflow processes: 3 max. | VP15-00-3 |
| Wave soldering | Solder temperature: 260 ˚C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120 ˚C or below (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300 ˚C or below, Time: 3 seconds or less (per device side) | — |

**Caution Use of more than one soldering method should be avoided (except for partial heating).**

**(2) μPD753104GK-xxx-8A8 : 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)**
**μPD753106GK-xxx-8A8 : 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)**
**μPD753108GK-xxx-8A8 : 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Peak package's surface temperature: 235 ˚C, Reflow time: 30 seconds or less (at 210 ˚C or higher), Number of reflow processes: 2 max. | IR35-00-2 |
| VPS | Peak package's surface temperature: 215 ˚C, Reflow time: 40 seconds or less (at 200 ˚C or higher), Number of reflow processes: 2 max. | VP15-00-2 |
| Wave soldering | Solder temperature: 260 ˚C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120 ˚C or below (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300 ˚C or below, Time: 3 seconds or less (per device side) | — |

**Caution Use of more than one soldering method should be avoided (except for partial heating).**

## APPENDIX A. μPD75308B, 753108 AND 75P3116 FUNCTIONAL LIST

| Parameter | | μPD75308B | μPD753108 | μPD75P3116 |
|---|---|---|---|---|
| Program memory | | Mask ROM<br>0000H to 1F7FH<br>(8064 x 8 bits) | Mask ROM<br>0000H to 1FFFH<br>(8192 x 8 bits) | One-time PROM<br>0000H to 3FFFH<br>(16384 x 8 bits) |
| Data memory | | 000H to 1FFH<br>(512 x 4 bits) | | |
| CPU | | 75X Standard | 75XL CPU | |
| Instruction execution time | When main system clock is selected | 0.95, 1.91, 15.3 μs<br>(during 4.19-MHz operation) | • 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation) | |
| | When subsystem clock is selected | 122 μs (32.768-kHz operation) | | |
| Stack | SBS register | None | SBS.3 = 1: Mk I mode selection<br>SBS.3 = 0: Mk II mode selection | |
| | Stack area | 000H to 0FFH | 000H to 1FFH | |
| | Subroutine call instruction stack operation | 2-byte stack | When Mk I mode: 2-byte stack<br>When Mk II mode: 3-byte stack | |
| Instruction | BRA !addr1<br>CALLA !addr1 | Unavailable | When Mk I mode: unavailable<br>When Mk II mode: available | |
| | MOVT XA, @BCDE<br>MOVT XA, @BCXA<br>BR BCDE<br>BR BCXA | | Available | |
| | CALL !addr | 3 machine cycles | Mk I mode: 3 machine cycles, Mk II mode: 4 machine cycles | |
| | CALLF !faddr | 2 machine cycles | Mk I mode: 2 machine cycles, Mk II mode: 3 machine cycles | |
| I/O port | CMOS input | 8 | 8 | |
| | CMOS input/output | 16 | 20 | |
| | Bit port output | 8 | 0 | |
| | N-ch open-drain input/output | 8 | 4 | |
| | Total | 40 | 32 | |
| LCD controller/driver | | Segment selection: 24/28/32 segments<br>(can be changed to CMOS input/output port in 4 time-unit; max. 8) | Segment selection: 16/20/24 segments<br>(can be changed to CMOS input/output port in 4 time-unit; max. 8) | |
| | | Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) | | |
| | | On-chip split resistor for LCD driver can be specified by using mask option. | | No on-chip split resistor for LCD driver |
| Timer | | 3 channels<br>• Basic interval timer: 1 channel<br>• 8-bit timer/event counter: 1 channel<br>• Watch timer: 1 channel | 5 channels<br>• Basic interval timer/watchdog timer: 1 channel<br>• 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter)<br>• Watch timer: 1 channel | |

| Parameter | | μPD75308B | μPD753108 | μPD75P3116 |
|---|---|---|---|---|
| Clock output (PCL) | | • Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation) | • Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation)<br>• Φ, 750, 375, 93.8 kHz (Main system clock: during 6.0-MHz operation) | |
| BUZ output (BUZ) | | • 2 kHz (Main system clock: during 4.19-MHz operation) | • 2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation)<br>• 2.93, 5.86, 46.9 kHz (Main system clock: 6.0-MHz operation) | |
| Serial interface | | 3 modes are available<br>• 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit<br>• 2-wire serial I/O mode<br>• SBI mode | | |
| SOS register | Feedback resistor cut flag (SOS.0) | None | Contained | |
| | Sub-oscillator current cut flag (SOS.1) | None | Contained | |
| Register bank selection register (RBS) | | None | Yes | |
| Standby release by INT0 | | Unavailable | Available | |
| Vectored interrupt | | External: 3, internal: 3 | External: 3, internal: 5 | |
| Supply voltage | | $V_{DD}$ = 2.0 to 6.0 V | $V_{DD}$ = 1.8 to 5.5 V | |
| Operating ambient temperature | | $T_A$ = –40 to +85 °C | | |
| Package | | • 80-pin plastic QFP (14 x 20 mm)<br>• 80-pin plastic QFP (14 x 14 mm)<br>• 80-pin plastic TQFP (Fine pitch) (12 x 12 mm) | • 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)<br>• 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) | |

## APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD753108.

In the 75XL Series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

### Language processor

| RA75X relocatable assembler | Host machine | OS | Supply media | Part number (product name) |
|---|---|---|---|---|
| | PC-9800 Series | MS-DOS™ Ver. 3.30 to Ver. 6.2 Note | 3.5-inch 2HD | μS5A13RA75X |
| | | | 5-inch 2HD | μS5A10RA75X |
| | IBM PC/AT™ and compatible machines | Refer to "**OS for IBM PC**" | 3.5-inch 2HC | μS7B13RA75X |
| | | | 5-inch 2HC | μS7B10RA75X |

| Device file | Host machine | OS | Supply media | Part number (product name) |
|---|---|---|---|---|
| | PC-9800 Series | MS-DOS Ver. 3.30 to Ver. 6.2 Note | 3.5-inch 2HD | μS5A13DF753108 |
| | | | 5-inch 2HD | μS5A10DF753108 |
| | IBM PC/AT and compatible machines | Refer to "**OS for IBM PC**" | 3.5-inch 2HC | μS7B13DF753108 |
| | | | 5-inch 2HC | μS7B10DF753108 |

**Note** Ver. 5.00 and later have the task swap function, but it cannot be used for this software.

**Remark** Operation of the assembler and the device file is guaranteed only on the above host machines and OSs.

**PROM write tools**

<table>
<tr><td>Hardware</td><td>PG-1500</td><td colspan="3">PG-1500 is a PROM programmer which enables you to program single-chip microcontrollers including PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256K bits to 4M bits.</td></tr>
<tr><td></td><td>PA-75P3116GC</td><td colspan="3">PROM programmer adapter for the μPD75P3116GC. Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td></td><td>PA-75P3116GK</td><td colspan="3">PROM programmer adapter for the μPD75P3116GK. Connect the programmer adapter to PG-1500 for use.</td></tr>
<tr><td>Software</td><td>PG-1500 controller</td><td colspan="3">PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine.</td></tr>
<tr><td></td><td></td><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Supply media</td><td rowspan="2">Part number (product name)</td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td><td>PC-9800 Series</td><td>MS-DOS<br>(Ver. 3.30 to Ver. 6.2 Note)</td><td>3.5-inch 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td></td><td></td><td></td><td></td><td>5-inch 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td></td><td></td><td>IBM PC/AT and compatible machines</td><td>Refer to “OS for IBM PC”</td><td>3.5-inch 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td></td><td></td><td></td><td></td><td>5-inch 2HC</td><td>μS7B10PG1500</td></tr>
</table>

**Note** Ver. 5.00 and later have the task swap function, but it cannot be used for this software.

**Remark** Operation of the PG-1500 controller is guaranteed only on the above host machines and OSs.

**Debugging tool**

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD753108.

The system configurations are described as follows.

| | | |
|---|---|---|
| Hardware | IE-75000-R Note 1 | In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X Series and 75XL Series. When developing a μPD753108 Subseries, the emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R) that are sold separately must be used with the IE-75000-R.<br>By connecting with the host machine and the PROM programmer, efficient debugging can be made.<br>It contains the emulation board (IE-75000-R-EM) which is connected. |
| | IE-75001-R | In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X Series and 75XL Series. When developing a μPD753108 Subseries, the emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R) that are sold separately must be used with the IE-75001-R.<br>It can debug the system efficiently by connecting the host machine and PROM programmer. |
| | IE-75300-R-EM | Emulation board for evaluating the application systems that use a μPD753108 Subseries.<br>It must be used with the IE-75000-R or IE-75001-R. |
| | EP-753108GC-R<br>EV-9200GC-64 | Emulation probe for the μPD753108GC.<br>It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 64-pin conversion socket EV-9200GC-64 which facilitates connection to a target system. |
| | EP-753108GK-R<br>★ TGK-064SBW Note 2 | Emulation probe for the μPD753108GK.<br>It must be connected to the IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 64-pin conversion adapter TGK-064SBW which facilitates connection to a target system. |
| Software | IE control program | Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronics interface and controls the IE-75000-R or IE-75001-R on a host machine. |

| Host machine | OS | Supply media | Part No. (product name) |
|---|---|---|---|
| PC-9800 Series | MS-DOS (Ver. 3.30 to Ver. 6.2 Note 3) | 3.5-inch 2HD | μS5A13IE75X |
| | | 5-inch 2HD | μS5A10IE75X |
| IBM PC/AT and compatible machines | Refer to "**OS for IBM PC**" | 3.5-inch 2HC | μS7B13IE75X |
| | | 5-inch 2HC | μS7B10IE75X |

**Notes 1.** Maintenance product.

★ **2.** This is a product of TOKYO ELETECH CORPORATION (Tokyo 03-5295-1661). For purchasing, contact an NEC sales representative.

**3.** Ver. 5.00 and later have the task swap function, but it cannot be used for this software.

**Remarks 1.** Operation of the IE control program is guaranteed only on the above host machines and OSs.

**2.** The μPD753104, 753106, 753108 and 75P3116 are commonly referred to as the μPD753108 Subseries.

**OS for IBM PC**

The following IBM PC OS's are supported.

| OS | Version |
|---|---|
| PC DOS™ | Ver. 3.1 to Ver. 6.3<br>J6.1/V Note to J6.3/V Note |
| MS-DOS | Ver. 5.0 to Ver. 6.22<br>5.0/V Note to 6.2/V Note |
| IBM DOS™ | J5.02/V Note |

**Note** Only the English mode is supported.

**Caution Ver. 5.0 and later have the task swap function, but it cannot be used for this software.**

## ★ APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Device Related Documents

| Document Name | Document No. | |
|---|---|---|
| | English | Japanese |
| μPD753104, 753106, 753108 Data Sheet | U10086E (This document) | U10086J |
| μPD75P3116 Data Sheet | U11369E | U11369J |
| μPD753108 User's Manual | U10890E | U10890J |
| μPD753108 Instruction Application Table | — | IEM-5600 |
| 75XL Series Selection Guide | U10453E | U10453J |

### Development Tool Related Documents

| Document Name | | | Document No. | |
|---|---|---|---|---|
| | | | English | Japanese |
| Hardware | IE-75000-R/IE-75001-R User's Manual | | EEU-1416 | EEU-846 |
| | IE-75300-R-EM User's Manual | | U11354E | U11354J |
| | EP-753108GC/GK-R User's Manual | | EEU-1495 | EEU-968 |
| | PG-1500 User's Manual | | EEU-1335 | U11940J |
| Software | RA75X Assembler Package User's Manual | Operation | EEU-1346 | EEU-731 |
| | | Language | EEU-1363 | EEU-730 |
| | PG-1500 Controller User's Manual | PC-9800 Series (MS-DOS) base | EEU-1291 | EEU-704 |
| | | IBM PC Series (PC DOS) base | U10540E | EEU-5008 |

### Other Related Documents

| Document Name | Document No. | |
|---|---|---|
| | English | Japanese |
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535E | C10535J |
| Quality Grades on NEC Semiconductor Devices | C11531E | C11531J |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E | C10983J |
| Electrostatic Discharge (ESD) Test | — | MEM-539 |
| Guide to Quality Assurance for Semiconductor Devices | MEI-1202 | C11893J |
| Microcomputer Product Series Guide | — | U11416J |

**Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.**

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

**NEC Electronics (Germany) GmbH**
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

**NEC Electronics (UK) Ltd.**
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

**NEC Electronics Italiana s.r.1.**
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

**NEC Electronics (Germany) GmbH**
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

**NEC Electronics (France) S.A.**
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

**NEC Electronics (France) S.A.**
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

**NEC Electronics (Germany) GmbH**
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

**NEC Electronics Hong Kong Ltd.**
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

**NEC Electronics Singapore Pte. Ltd.**
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

**NEC Electronics Taiwan Ltd.**
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

**NEC do Brasil S.A.**
Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

J96. 8

MS-DOS is either a registered trademark or a trademark of Microsoft Corporation in the United States and/or other countries.

IBM DOS, PC/AT, and PC DOS are trademarks of International Business Machines Corporation.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.



M4 96.5