

**$\mu$ PD75104, 75106, 75108****4-BIT SINGLE-CHIP MICROCOMPUTER****DESCRIPTION**

$\mu$ PD75108 is a 4-bit single-chip microcomputer integrating timer/event counters, serial interface, and vector interrupt function, in addition to a CPU, ROM, RAM, and I/O ports, on a single chip. Operating at high speeds, the microcomputer allows data to be manipulated in units of 1, 4, or 8 bits. In addition, various bit manipulation instructions are provided to reinforce I/O manipulation capability. Equipped with I/Os for interfacing with peripheral circuits operating on a different supply voltage, outputs that can directly drive LEDs, and analog inputs,  $\mu$ PD75108 is suitable for controlling such systems as VTRs, acoustic products, button telephones, radio communications equipment, and printers. A pin-compatible EPROM model is also available for evaluation of system development and small-scale production of application systems.

*Detailed functions are described in the following user's manual. Be sure to read it for designing.*

*$\mu$ PD751XX Series User's Manual: IEM-922*

**FEATURES**

- Internal memory
  - Program memory (ROM)
    - :  $8068 \times 8$  bits ( $\mu$ PD75108)
    - :  $6016 \times 8$  bits ( $\mu$ PD75106)
    - :  $4096 \times 8$  bits ( $\mu$ PD75104)
  - Data memory (RAM)
    - :  $512 \times 4$  bits ( $\mu$ PD75108)
    - :  $320 \times 4$  bits ( $\mu$ PD75106, 75104)
- New architecture "75X series" rivaling 8-bit microcomputers
- 43 systematically organized instructions
  - A wealth of bit manipulation instructions
  - 8-bit data transfer, compare, operation, increment, and decrement instructions
  - 1-byte relative branch instructions
  - GETI instruction executing 2-/3-byte instruction with one byte
- High speed. Minimum instruction execution time:  $0.95 \mu\text{s}$  (at 4.19 MHz), 5 V
- Power-saving, instruction time change function:  $0.95 \mu\text{s}/1.91 \mu\text{s}/15.3 \mu\text{s}$  (at 4.19 MHz)
- I/O port pins as many as 58
- Three channels of 8-bit timers
- 8-bit serial interface
- Multiplexed vector interrupt function
- Model with PROM is available:  $\mu$ PD75P108B (One-time PROM, EPROM)

Unless there are differences among  $\mu$ PD75104, 75106, and 75108 functions,  $\mu$ PD75108 is treated as the representative model throughout this manual.

The information in this document is subject to change without notice.

**ORDERING INFORMATION**

| Part Number        | Package                             | Quality Grade |
|--------------------|-------------------------------------|---------------|
| μPD75104CW-xxx     | 64-pin plastic shrink DIP (750 mil) | Standard      |
| μPD75104GF-xxx-3BE | 64-pin plastic QFP (14 × 20 mm)     | Standard      |
| μPD75106CW-xxx     | 64-pin plastic shrink DIP (750 mil) | Standard      |
| μPD75106GF-xxx-3BE | 64-pin plastic QFP (14 × 20 mm)     | Standard      |
| μPD75108CW-xxx     | 64-pin plastic shrink DIP (750 mil) | Standard      |
| μPD75108GF-xxx-3BE | 64-pin plastic QFP (14 × 20 mm)     | Standard      |

**Remarks:** xxx is ROM code number.

Please refer to “Quality Grade on NEC Semiconductor Devices” (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

## FUNCTIONAL OUTLINE

| Item                               |     | Specifications                                                                                                                                                                                                                                                       |
|------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of Basic Instructions       |     | 43                                                                                                                                                                                                                                                                   |
| Minimum Instruction Execution Time |     | Changeable in three steps: 0.95 $\mu$ s, 1.91 $\mu$ s, and 15.3 $\mu$ s at 4.19 MHz                                                                                                                                                                                  |
| Internal Memory                    | ROM | 8064 $\times$ 8 bits ( $\mu$ PD75108), 6016 $\times$ 8 bits ( $\mu$ PD75106), 4096 $\times$ 8 bits ( $\mu$ PD75104)                                                                                                                                                  |
|                                    | RAM | 512 $\times$ 4 bits ( $\mu$ PD75108), 320 $\times$ 4 bits ( $\mu$ PD75106, 75104)                                                                                                                                                                                    |
| General-Purpose Register           |     | 4 bits $\times$ 8 $\times$ 4 banks (memory mapped)                                                                                                                                                                                                                   |
| Accumulator                        |     | Three accumulators selectable according to the bit length of manipulated data:<br>• 1-bit accumulator (CY), 4-bit accumulator (A), and 8-bit accumulator (XA)                                                                                                        |
| I/O Port                           |     | 58 port pins<br>• CMOS input pins: 10<br>• CMOS I/O pins (can directly drive LEDs): 32<br>• Medium voltage N-ch open-drain I/O pins: 12<br>(can directly drive LEDs. Pull-up resistor can be connected to each bit)<br>• Comparator input pins (4-bit accuracy): 4   |
| Timer/Counter                      |     | • 8-bit timer/event counter $\times$ 2<br>• 8-bit basic interval timer (can be used as watchdog timer)                                                                                                                                                               |
| Serial Interface                   |     | • 8 bits<br>• LSB first/MSB first mode selectable<br>• Two transfer modes (transfer/reception and reception only modes)                                                                                                                                              |
| Vector Interrupt                   |     | External: 3, Internal: 4                                                                                                                                                                                                                                             |
| Test Input                         |     | External: 2                                                                                                                                                                                                                                                          |
| Standby                            |     | • STOP and HALT modes                                                                                                                                                                                                                                                |
| Instruction Set                    |     | • Various bit manipulation instructions (set, reset, test, Boolean operation)<br>• 8-bit data transfer, compare, operation, increment, and decrement<br>• 1-byte relative branch instructions<br>• GETI instruction constituting 2 or 3-byte instruction with 1 byte |
| Others                             |     | • Power-ON reset circuit (mask option)<br>• Bit manipulation memory (bit sequential buffer: 16 bits)                                                                                                                                                                 |
| Package                            |     | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 $\times$ 20 mm)                                                                                                                                                                                    |

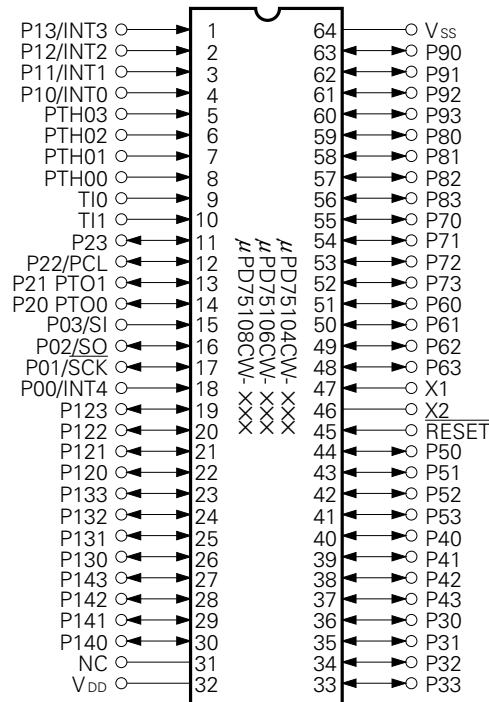
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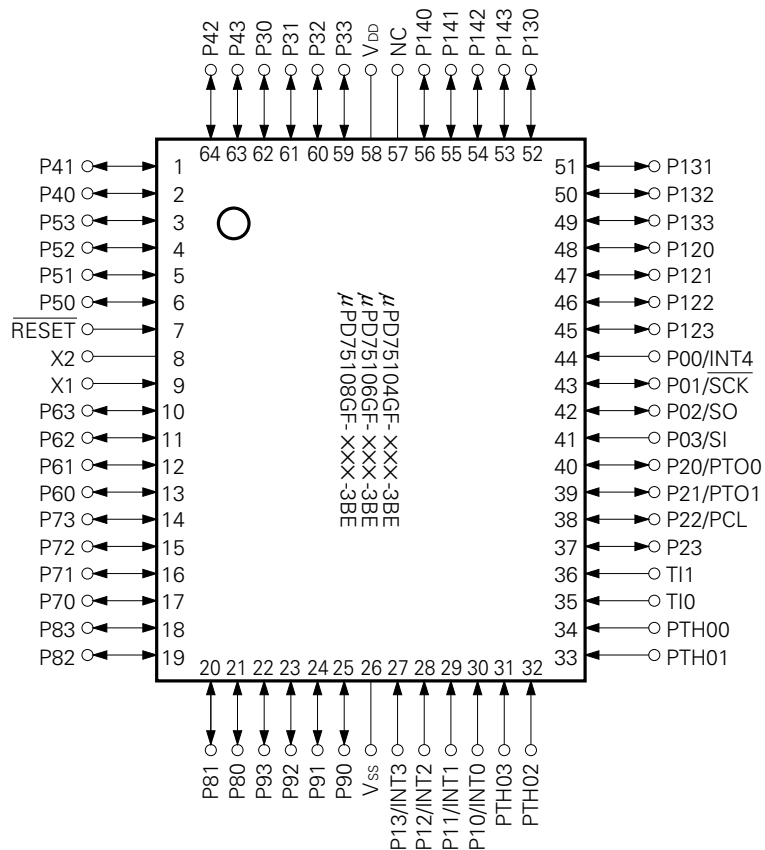
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## 1. PIN CONFIGURATION (Top View)

- 64-Pin Plastic Shrink DIP (750 mil)



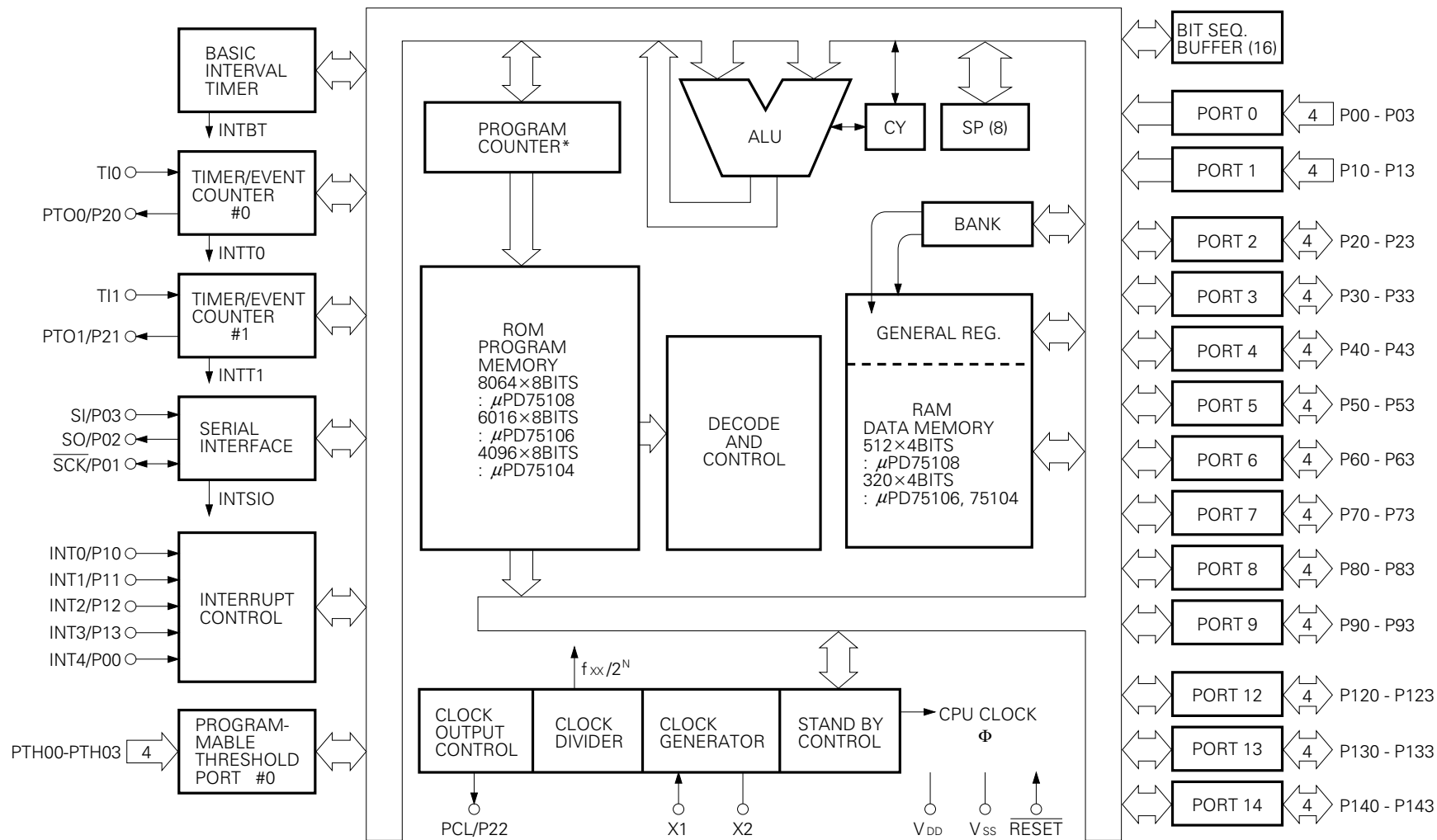
- 64-Pin Plastic QFP (14 × 20 mm)



**Pin names**

|           |           |                           |                                   |
|-----------|-----------|---------------------------|-----------------------------------|
| P00-P03   | : Port 0  | $\overline{\text{SCK}}$   | : Serial Clock Input/Output       |
| P10-P13   | : Port 1  | SO                        | : Serial Output                   |
| P20-P23   | : Port 2  | SI                        | : Serial Input                    |
| P30-P33   | : Port 3  | PTO0, PTO1                | : Timer Output                    |
| P40-P43   | : Port 4  | PCL                       | : Clock Output                    |
| P50-P53   | : Port 5  | PTH00-PTH03               | : Comparator Input                |
| P60-P63   | : Port 6  | INT0, INT1, INT4          | : External Vector Interrupt Input |
| P70-P73   | : Port 7  | INT2, INT3                | : External Test Input             |
| P80-P83   | : Port 8  | TI0, TI1                  | : Timer Input                     |
| P90-P93   | : Port 9  | X1, X2                    | : Clock Oscillation Pin           |
| P120-P123 | : Port 12 | $\overline{\text{RESET}}$ | : Reset Input                     |
| P130-P133 | : Port 13 | NC                        | : No Connection                   |
| P140-P143 | : Port 14 |                           |                                   |

## 2. BLOCK DIAGRAM



\*: 13 bits: μPD75106, 75108  
12 bits: μPD75104

### 3. PIN FUNCTIONS

#### 3.1 PORT PINS

| Pin Name    | I/O   | Shared with:            | Function                                                                                                                                                      | 8-Bit I/O | At Reset | I/O Circuit TYPE*1 |
|-------------|-------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|----------|--------------------|
| P00         | Input | INT4                    | 4-bit input port (PORT 0)                                                                                                                                     | x         | Input    | B                  |
| P01         | I/O   | $\overline{\text{SCK}}$ |                                                                                                                                                               |           |          | F                  |
| P02         | I/O   | SO                      |                                                                                                                                                               |           |          | E                  |
| P03         | Input | SI                      |                                                                                                                                                               |           |          | B                  |
| P10         | Input | INT0                    | 4-bit input port (PORT 1)                                                                                                                                     | x         | Input    | B                  |
| P11         |       | INT1                    |                                                                                                                                                               |           |          |                    |
| P12         |       | INT2                    |                                                                                                                                                               |           |          |                    |
| P13         |       | INT3                    |                                                                                                                                                               |           |          |                    |
| P20*3       | I/O   | PTO0                    | 4-bit I/O port (PORT 2)                                                                                                                                       | x         | Input    | E                  |
| P21*3       |       | PTO1                    |                                                                                                                                                               |           |          |                    |
| P22*3       |       | PCL                     |                                                                                                                                                               |           |          |                    |
| P23*3       |       | —                       |                                                                                                                                                               |           |          |                    |
| P30-P33*3   | I/O   | —                       | 4-bit programmable I/O port (PORT 3)<br>Can be specified for input or output bitwise.                                                                         | o         | Input    | E                  |
| P40-P43*3   | I/O   | —                       | 4-bit I/O port (PORT 4)                                                                                                                                       |           | Input    | E                  |
| P50-P53*3   | I/O   | —                       | 4-bit I/O port (PORT 5)                                                                                                                                       |           | Input    | E                  |
| P60-P63*3   | I/O   | —                       | 4-bit programmable I/O port (PORT 6)<br>Can be specified for input or output bitwise.                                                                         | o         | Input    | E                  |
| P70-P73*3   | I/O   | —                       | 4-bit I/O port (PORT 7)                                                                                                                                       |           | Input    | E                  |
| P80-P83*3   | I/O   | —                       | 4-bit I/O port (PORT 8)                                                                                                                                       | o         | Input    | E                  |
| P90-P93*3   | I/O   | —                       | 4-bit I/O port (PORT 9)                                                                                                                                       |           | Input    | E                  |
| P120-P123*3 | I/O   | —                       | 4-bit N-ch open-drain I/O port (PORT 12)<br>Built-in pull-up resistors can be specified in bit units by mask option.<br>Open-drain withstanding voltage: 12 V | o         | Input*2  | M                  |
| P130-P133*3 | I/O   | —                       | 4-bit N-ch open-drain I/O port (PORT 13)<br>Built-in pull-up resistors can be specified in bit units by mask option.<br>Open-drain withstanding voltage: 12 V |           | Input*2  | M                  |
| P140-P143*3 | I/O   | —                       | 4-bit N-ch open-drain I/O port (PORT 14)<br>Built-in pull-up resistors can be specified in bit units by mask option.<br>Open-drain withstanding voltage: 12 V | —         | Input*2  | M                  |

\*1: Circles indicate Schmitt trigger input pins.

2: With drain open: high impedance

With pull-up resistor connected: high level

3: Can directly drive LEDs.

## 3.2 PINS OTHER THAN PORTS

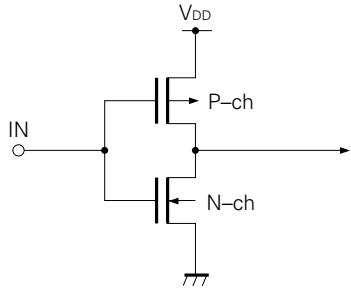
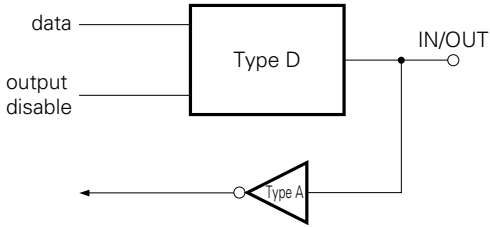
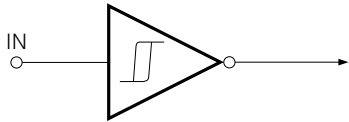
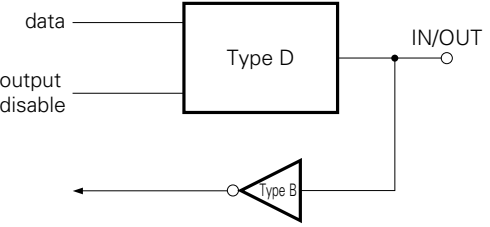
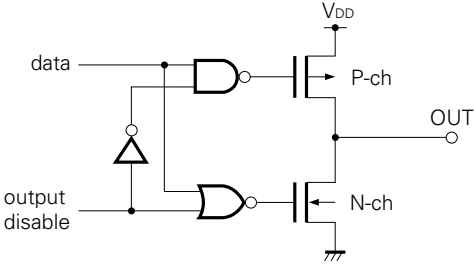
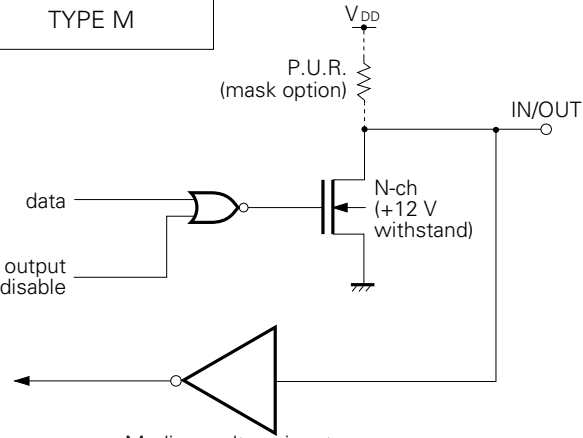
| Pin Name        | I/O   | Shared with: | Function                                                                                                                                   | At Reset | I/O Circuit TYPE*1 |
|-----------------|-------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------------|
| PTH00-PTH03     | Input | —            | 4-bit variable threshold voltage analog input port                                                                                         | —        | N                  |
| TI0             | Input | —            | External event pulse inputs for timer/event counter.<br>Also serves as edge-detected vector interrupt input.<br>1-bit input also possible. | —        | B                  |
| TI1             |       |              |                                                                                                                                            |          |                    |
| PTO0            | I/O   | P20          | Outputs for timer/event counter                                                                                                            | Input    | E                  |
| PTO1            |       | P21          |                                                                                                                                            |          |                    |
| SCK             | I/O   | P01          | Serial clock I/O                                                                                                                           | Input    | F                  |
| SO              | I/O   | P02          | Serial data output                                                                                                                         | Input    | E                  |
| SI              | Input | P03          | Serial data input                                                                                                                          | Input    | B                  |
| INT4            | Input | P00          | Edge-detected vectored interrupt input (both rising and falling edges detected)                                                            | Input    | B                  |
| INT0            | Input | P10          | Edge-detected vectored interrupt inputs (valid edge selectable)                                                                            | Input    | B                  |
| INT1            |       | P11          |                                                                                                                                            |          |                    |
| INT2            | Input | P12          | Edge-detected testable inputs (rising edge detected)                                                                                       | Input    | B                  |
| INT3            |       | P13          |                                                                                                                                            |          |                    |
| PCL             | I/O   | P22          | Clock output                                                                                                                               | Input    | E                  |
| X1, X2          | —     | —            | Crystal/ceramic system clock oscillator connections.<br>Input external clock to X1, and signal in reverse phase with X1 to X2.             | —        | —                  |
| RESET           | Input | —            | System reset input (low level active type)                                                                                                 | —        | B                  |
| NC*2            | —     | —            | No Connection                                                                                                                              | —        | —                  |
| V <sub>DD</sub> | —     | —            | Positive power supply                                                                                                                      | —        | —                  |
| V <sub>SS</sub> | —     | —            | GND                                                                                                                                        | —        | —                  |

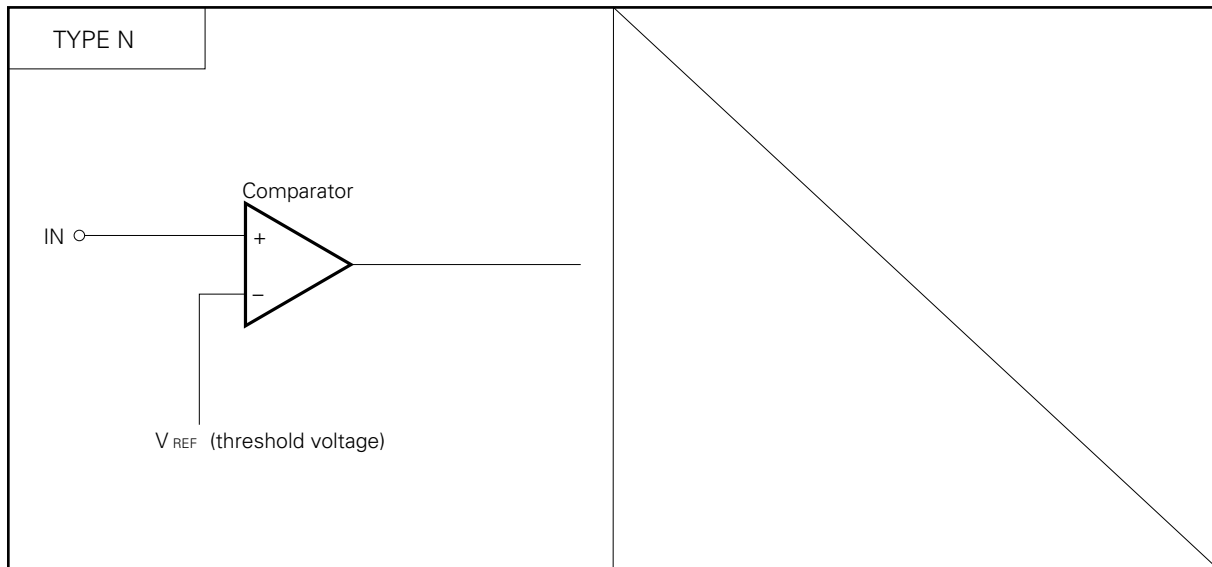
\*1: Circles indicate Schmitt trigger input pins.

2: Connect the NC pin directly to the V<sub>DD</sub> pin when  $\mu$ PD75P108B and a printed circuit board are shared.

### 3.3 PIN INPUT/OUTPUT CIRCUITS

The following shows a simplified input/output circuit diagram for each pin of the μPD75108.

|                                                                                                                                                                                                         |                                                                                                                                                                                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>TYPE A</p>  <p>Input buffer of CMOS standard</p>                                                                    | <p>TYPE E</p>  <p>I/O circuit consisting of Type D push-pull output circuit and Type A input buffer</p>   |
| <p>TYPE B</p>  <p>Schmitt trigger input with hysteresis characteristics</p>                                           | <p>TYPE F</p>  <p>I/O circuit consisting of Type D push-pull output and Type B Schmitt trigger input</p> |
| <p>TYPE D</p>  <p>Push-pull output that can be set in a output high-impedance state (both P-ch and N-ch are off)</p> | <p>TYPE M</p>  <p>Medium-voltage input buffer (+12 V withstand)<br/>P.U.R.: Pull-Up Resistor</p>        |



### 3.4 RECOMMENDED PROCESSING OF UNUSED PINS

| Pin                                                                                                                         | Recommended connections                                                  |
|-----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| PTH00-PTH03<br>TI0<br>TI1                                                                                                   | Connect to V <sub>SS</sub> or V <sub>DD</sub>                            |
| P00                                                                                                                         | Connect to V <sub>SS</sub>                                               |
| P01-P03                                                                                                                     | Connect to V <sub>SS</sub> or V <sub>DD</sub>                            |
| P10-P13                                                                                                                     | Connect to V <sub>SS</sub>                                               |
| P20-P23<br>P30-P33<br>P40-P43<br>P50-P53<br>P60-P63<br>P70-P73<br>P80-P83<br>P90-P93<br>P120-P123<br>P130-P133<br>P140-P143 | Input: Connect to V <sub>SS</sub> or V <sub>DD</sub><br><br>Output: Open |
| $\overline{\text{RESET}}^{*1}$                                                                                              | Connect to V <sub>DD</sub>                                               |
| NC <sup>*2</sup>                                                                                                            | Open                                                                     |

\*1: Connect this pin to the V<sub>DD</sub> pin only when a power-ON reset circuit is provided as a mask option.

2: Connect the NC pin to the V<sub>DD</sub> pin when  $\mu$ PD75P108 and a printed circuit board are shared.

### 3.5 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS

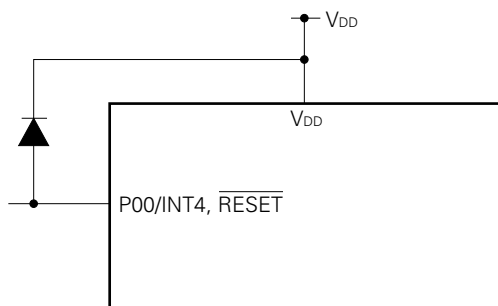
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal functions of the  $\mu$ PD75108 are tested (solely used for IC tests), is provided to the P00/INT4 and  $\overline{\text{RESET}}$  pins.

If a voltage exceeding  $V_{DD}$  is applied to either of these pins, the  $\mu$ PD75108 is put into test mode. Therefore, even when the  $\mu$ PD75108 is in normal operation, if noise exceeding the  $V_{DD}$  is input into any of these pins, the  $\mu$ PD75108 will enter the test mode, and this will cause problems for normal operation.

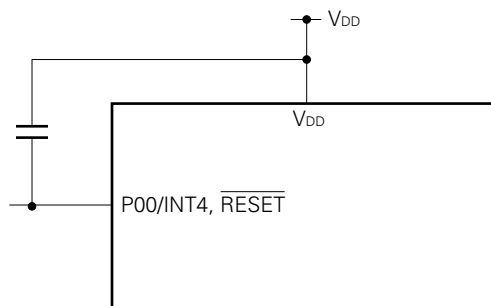
As an example, if the wiring to the P00/INT4 pin or the  $\overline{\text{RESET}}$  pin is long, stray noise may be picked up and the above mentioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode across P00/INT4 and  $\overline{\text{RESET}}$ , and  $V_{DD}$ .



- Connect a capacitor across P00/INT4 and  $\overline{\text{RESET}}$ , and  $V_{DD}$ .



#### 4. MEMORY CONFIGURATION

- Program memory (ROM) ...  $8064 \times 8$  bits (0000H-1F7FH) :  $\mu$ PD75108  
...  $6016 \times 8$  bits (0000H-177FH) :  $\mu$ PD75106  
...  $4096 \times 8$  bits (0000H-0FFFH) :  $\mu$ PD75104
- 0000H, 0001H : Vector table to which address from which program is started is written after reset
- 0002H-000BH: Vector table to which address from which program is started is written after interrupt
- 0020H-007FH: Table area referenced by GETI instruction
- Data memory (RAM)
  - Data area ....  $512 \times 4$  bits (000H-1FFH):  $\mu$ PD75108  
 $320 \times 4$  bits (000H-13FH) :  $\mu$ PD75106, 75104
  - Peripheral hardware area ....  $128 \times 4$  bits (F80H-FFFH)

| Address | 7                                           | 6   | 5 | 0                                           |
|---------|---------------------------------------------|-----|---|---------------------------------------------|
| 0000H   | MBE                                         | RBE | 0 | Internal reset start address (upper 5 bits) |
|         | Internal reset start address (lower 8 bits) |     |   |                                             |
| 0002H   | MBE                                         | RBE | 0 | INTBT/INT4 start address (upper 5 bits)     |
|         | INTBT/INT4 start address (lower 8 bits)     |     |   |                                             |
| 0004H   | MBE                                         | RBE | 0 | INT0/INT1 start address (upper 5 bits)      |
|         | INT0/INT1 start address (lower 8 bits)      |     |   |                                             |
| 0006H   | MBE                                         | RBE | 0 | INTSIO start address (upper 5 bits)         |
|         | INTSIO start address (lower 8 bits)         |     |   |                                             |
| 0008H   | MBE                                         | RBE | 0 | INTT0 start address (upper 5 bits)          |
|         | INTT0 start address (lower 8 bits)          |     |   |                                             |
| 000AH   | MBE                                         | RBE | 0 | INTT1 start address (upper 5 bits)          |
|         | INTT1 start address (lower 8 bits)          |     |   |                                             |
| 0020H   | GETI instruction reference table            |     |   |                                             |
| 007FH   |                                             |     |   |                                             |
| 0080H   |                                             |     |   |                                             |
| 07FFH   |                                             |     |   |                                             |
| 0800H   |                                             |     |   |                                             |
| 0FFFH   |                                             |     |   |                                             |
| 1000H   |                                             |     |   |                                             |
| 1F7FH   |                                             |     |   |                                             |

CALLF ! faddr  
instruction entry address

BRCB ! caddr  
instruction branch address

BRCB ! caddr  
instruction branch address

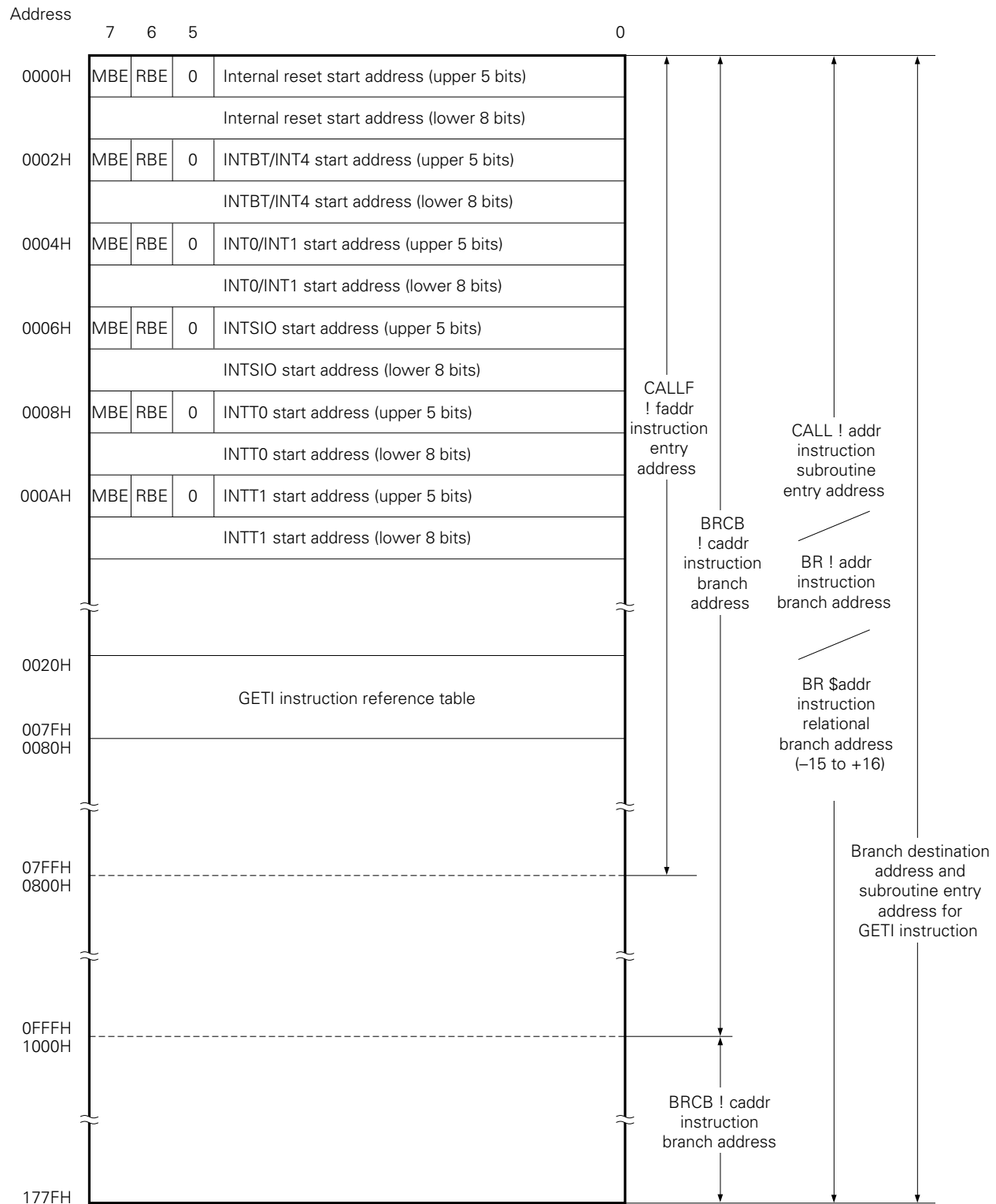
CALL ! addr  
instruction subroutine entry address

BR ! addr  
instruction branch address

BR \$addr  
instruction relational branch address (-15 to -1, +2 to +16)

Branch destination address and subroutine entry address for GETI instruction

**Remarks:** In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(b)  $\mu$ PD75106**Fig. 4-1 Program Memory Map (2/3)**

**Remarks:** In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(c) μPD75106

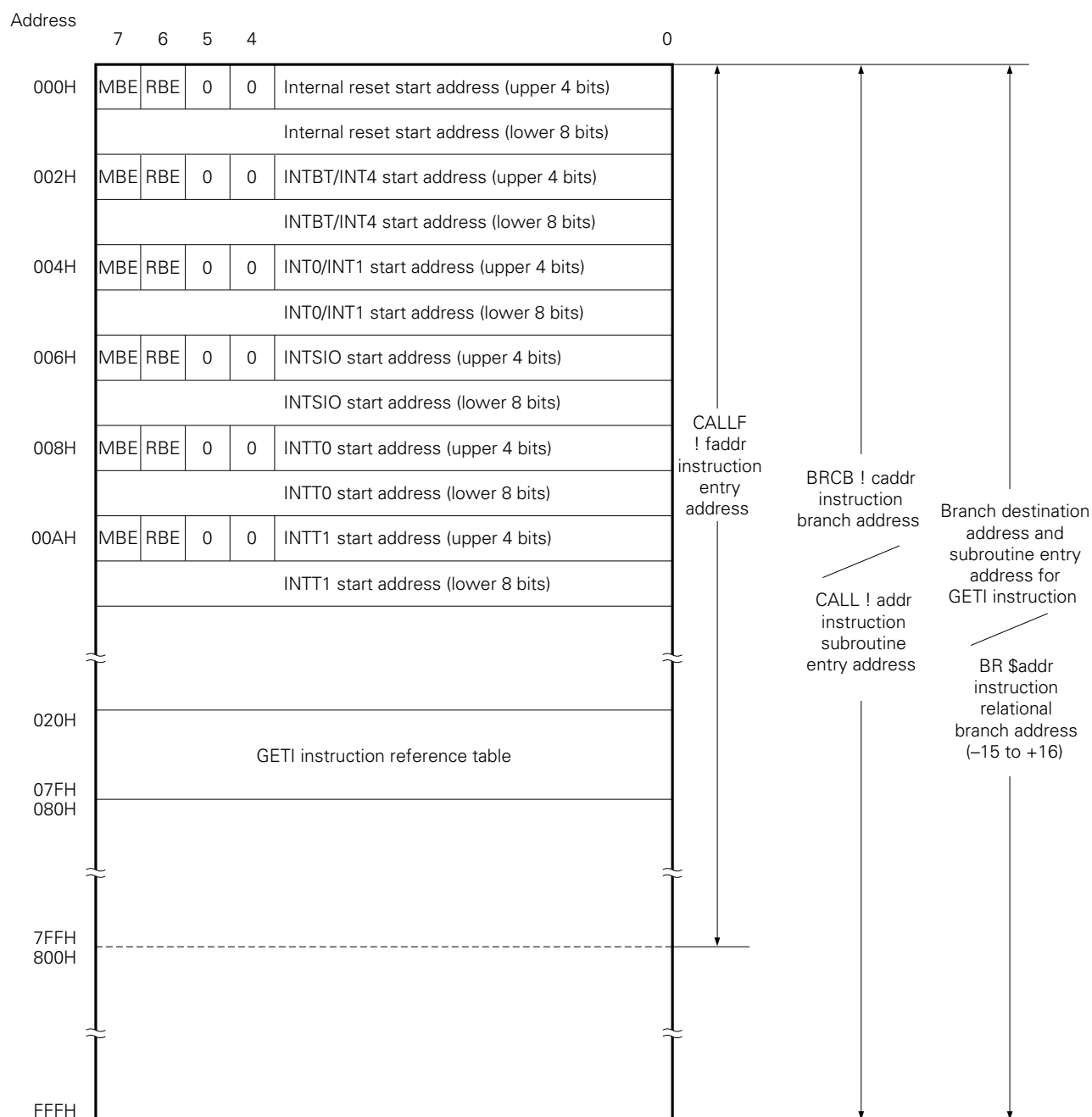


Fig. 4-1 Program Memory Map (3/3)

**Remarks:** In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(a) μPD75108

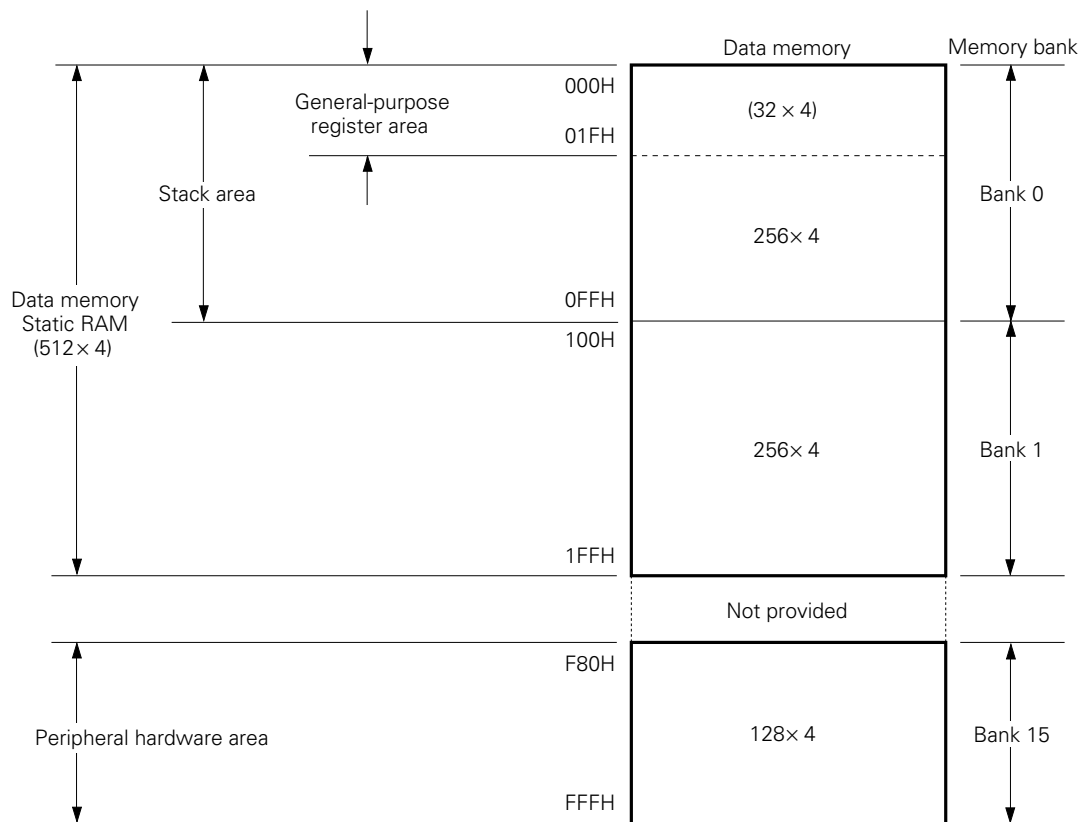


Fig. 4-2 Data Memory Map(1/2)

(b) μPD75106, 75104

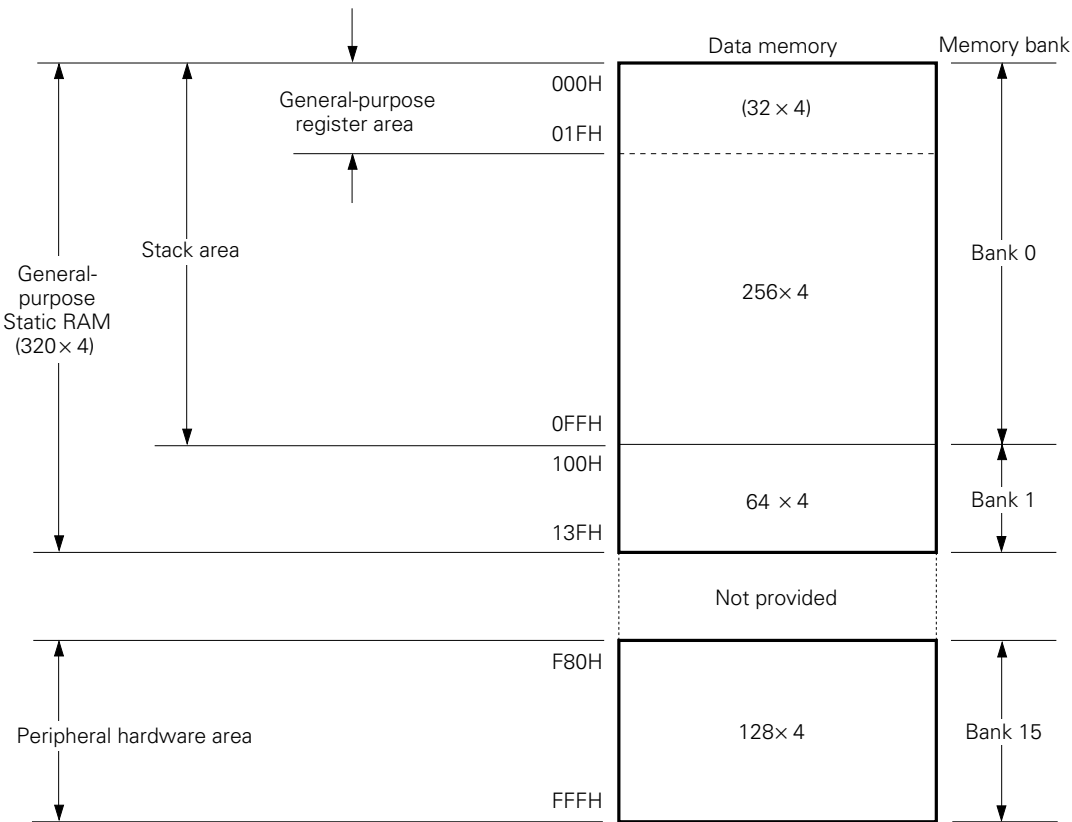


Fig. 4-2 Data Memory Map(2/2)

## 5. PERIPHERAL HARDWARE FUNCTIONS

### 5.1 PORTS

I/O ports are classified into the following 3 kinds:

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 4, 5, 6, 7, 8, 9): 32
- N-ch open-drain input/output (PORT12, 13, 14) : 12

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Total : 52

**Table 5-1 Port Function**

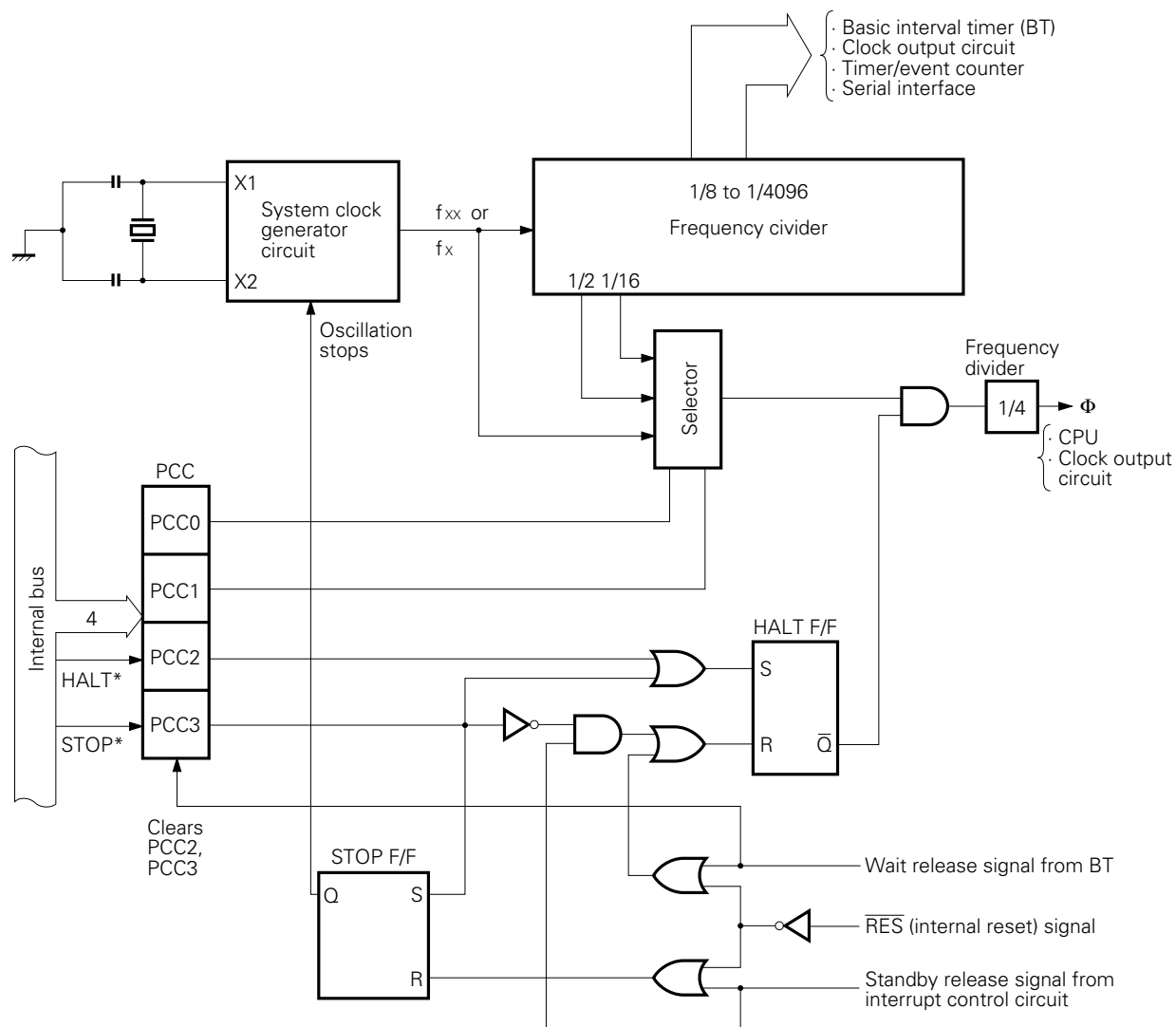
| Port<br>(Symbol)                                   | Function    | Operation and Features                                                                                                                    | Remarks                                                      |
|----------------------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| PORT0<br>PORT1                                     | 4-bit input | Can always be read or tested regardless of operation mode of shared pin                                                                   | Shared with SI, SO, $\overline{SCK}$ , and INT0 to 4 pins    |
| PORT3<br>PORT6                                     | 4-bit I/O*  | Can be set in input or output mode bitwise                                                                                                | —                                                            |
| PORT2<br>PORT4<br>PORT5<br>PORT7<br>PORT8<br>PORT9 |             | Can be set in input or output mode in units of 4 bits. Ports 4 and 5, 6 and 7, 8 and 9 can be used in pairs to input or output 8-bit data | Port 2 pins are shared with PTO0, PTO1, and PCL pins         |
| PORT12<br>PORT13<br>PORT14                         |             | Can be set in input or output mode in units of 4 bits. Ports 12 and 13 can be used in pairs to input or output 8-bit data                 | Each bit can be connected to pull-up resistor by mask option |

\*: Can directly drive LED.

## 5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit generates clocks to control CPU operation modes by supplying clocks to the CPU and peripheral hardware. In addition, this circuit can change the instruction execution time.

- 0.95  $\mu$ s/1.91  $\mu$ s/15.3  $\mu$ s (operating at 4.19 MHz)



\*: Execution of the instruction

**Remarks** 1: f<sub>xx</sub>= Crystal/ceramic oscillator

2: f<sub>x</sub> = External clock frequency

3: PCC: Processor clock control register

4: One clock cycle (t<sub>cy</sub>) of Φ is one machine cycle of an instruction. For t<sub>cy</sub>, refer to AC characteristics in 12. ELECTRICAL SPECIFICATIONS.

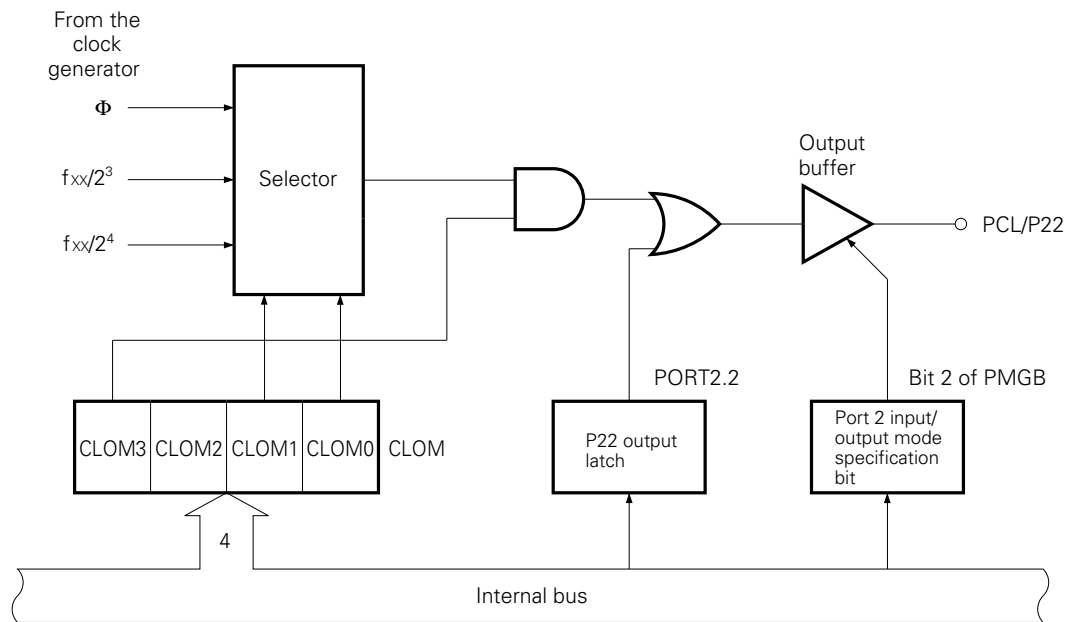
★

**Fig. 5-1 Clock Generator Block Diagram**

### 5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock output circuit is used to output clock pulses to the remote control output, peripheral LSIs, etc.

- Clock output (PCL) :  $\Phi$ , 524, 262 kHz (operating at 4.19 MHz)

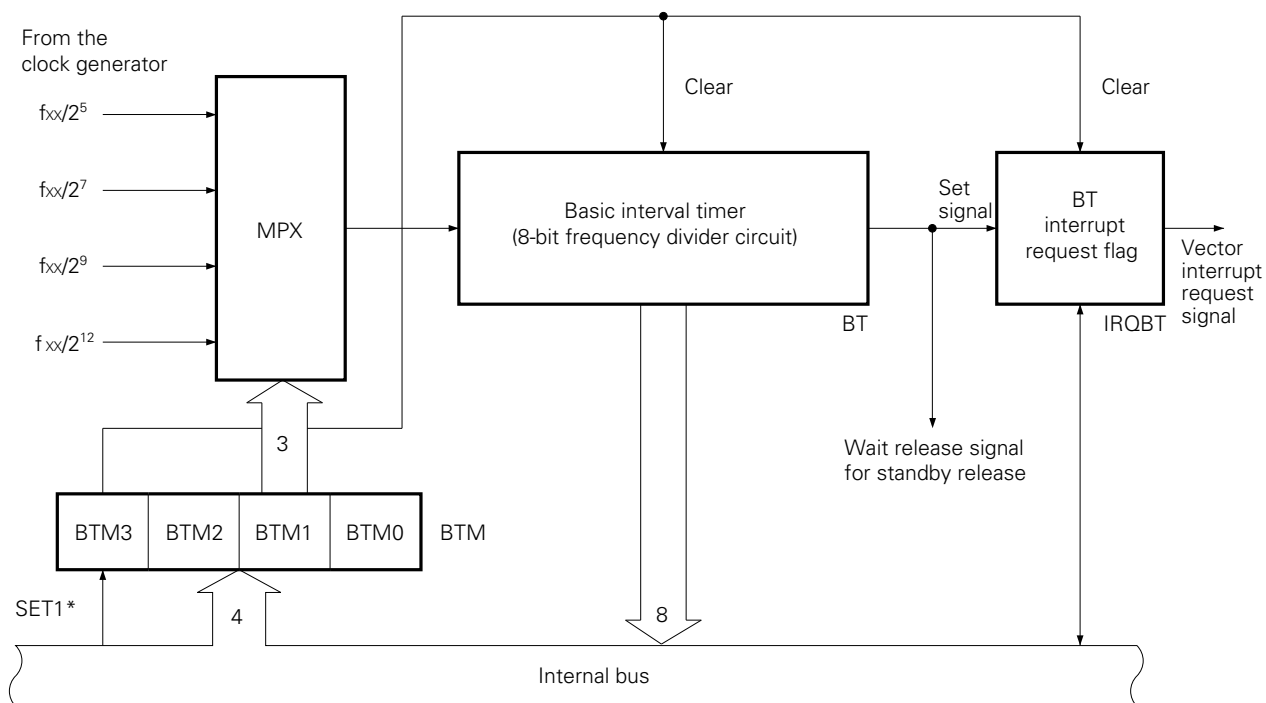


**Fig. 5-2 Clock Output Circuit Configuration**

## 5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



Remarks : \*: Instruction execution

**Fig. 5-3 Basic Interval Timer Configuration**

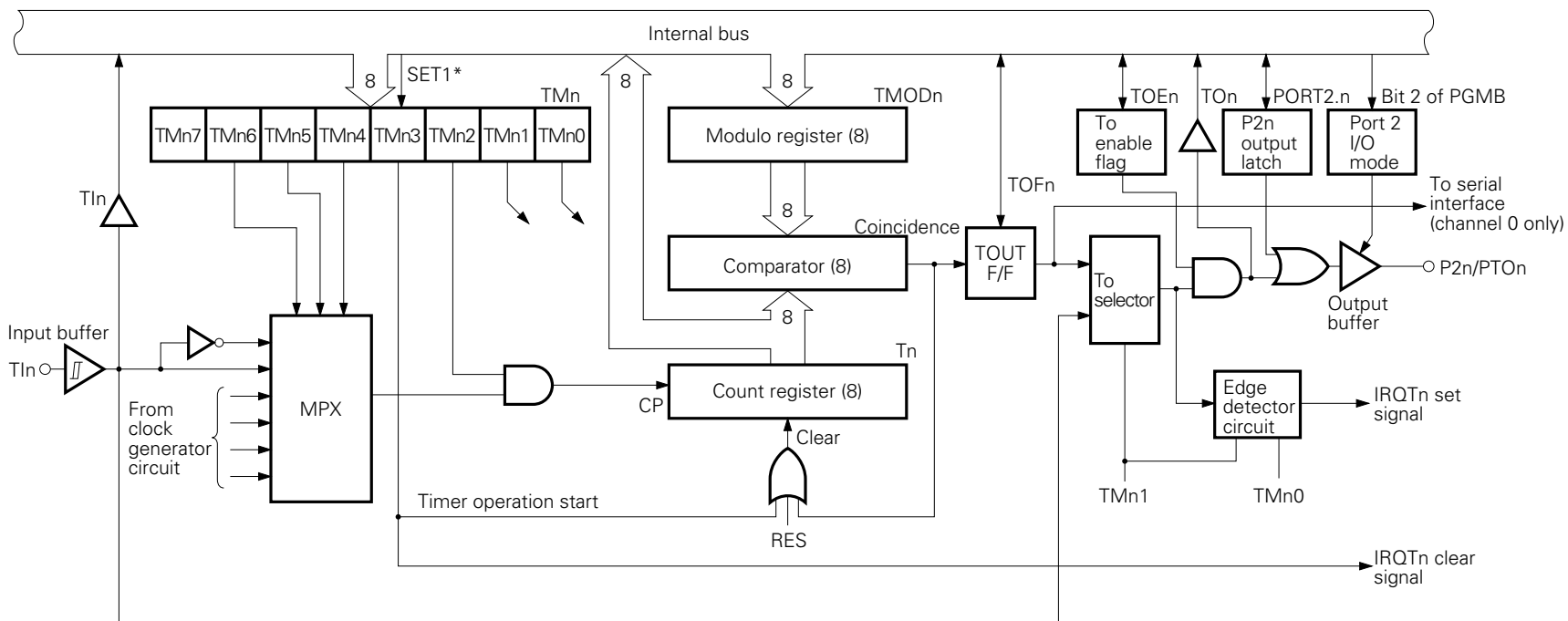
## 5.5 TIMER/EVENT COUNTER

$\mu$ PD75108 contains two channels of timer/event counters.

These two channels are almost identical in terms of configuration and function except the count pulse (CP) that can be selected and the function to supply clocks to the serial interface.

The functions of the timer/event counter include:

- Programmable interval timer operation
- Output of square wave at an arbitrary frequency to PTO<sub>n</sub> pin
- Event counter operation
- Input of TIn pin signal as external interrupt input signal
- Dividing TIn pin input by N to output to PTO<sub>n</sub> pin (frequency divider operation)
- Supply of serial shift clock to serial interface circuit (channel 0 only)
- Reading counting status



Remarks: \* indicates the instruction execution.

Fig. 5-4 Timer/Event Counter Block Diagram (n = 0, 1)

## 5.6 SERIAL INTERFACE

The  $\mu$ PD75108 is equipped with clock 8-bit serial interface that operates in the following two modes:

- Operation stop mode
- Three-line serial I/O mode

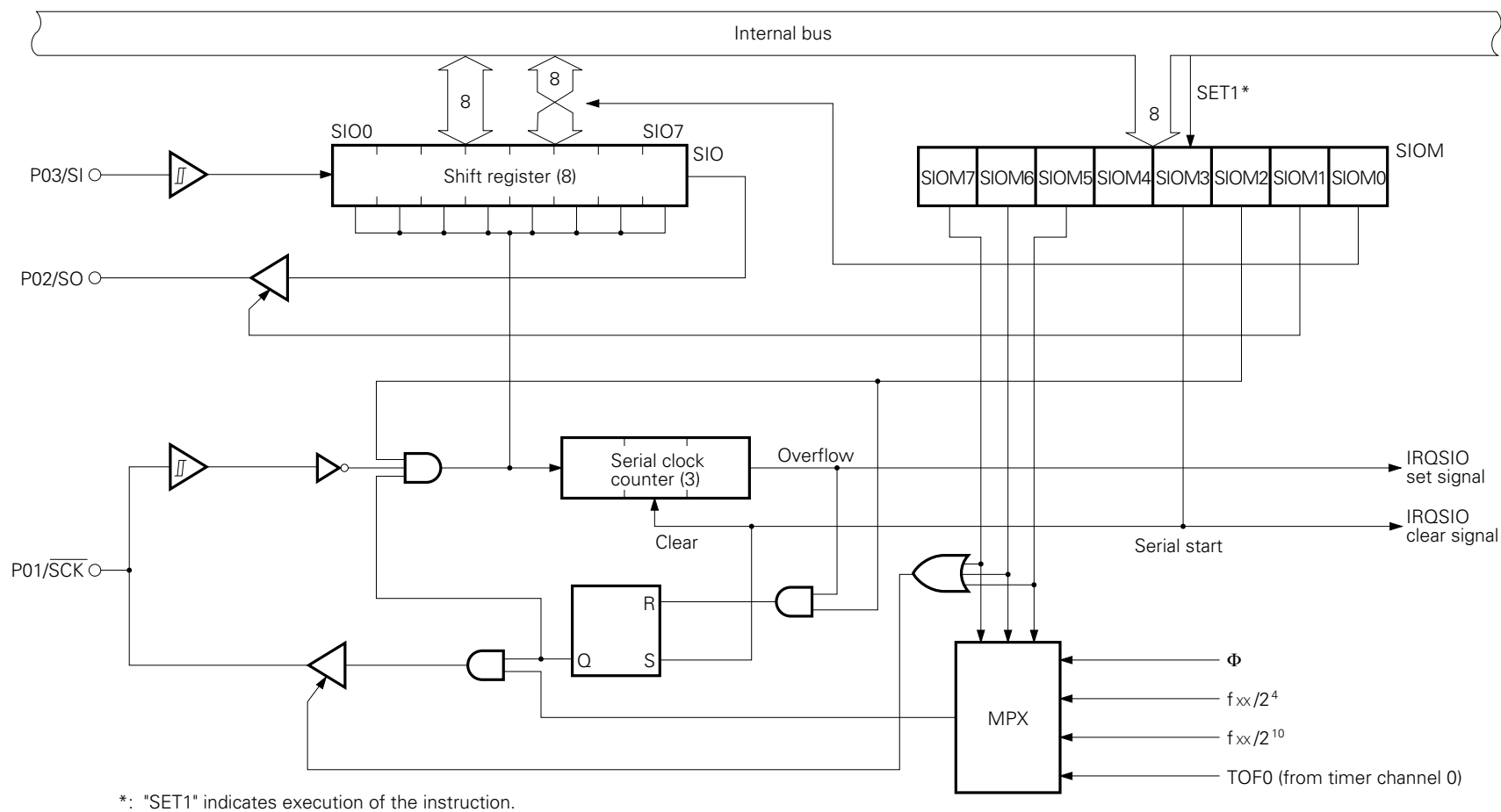


Fig. 5-5 Serial Interface Block Diagram

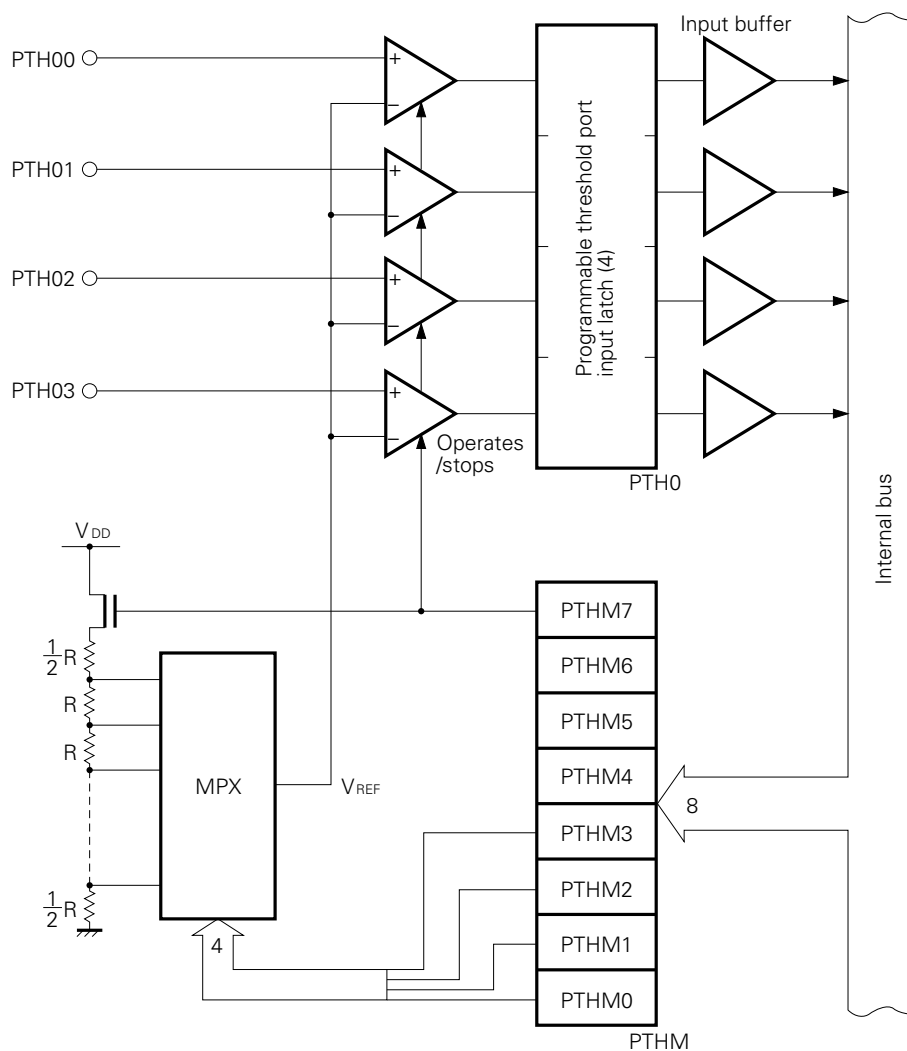
### 5.7 PROGRAMMABLE THRESHOLD PORT (ANALOG INPUT PORT)

$\mu$ PD75108 is equipped with a 4-bit analog input port (consisting of PTH00 to PTH03 pins) whose threshold voltage is programmable.

This programmable threshold port is configured as shown in Figure 5-6.

The threshold voltage ( $V_{REF}$ ) can be changed in 16 steps ( $V_{DD} \times 0.5/16 - V_{DD} \times 15.5/16$ ), and analog signals can be directly input.

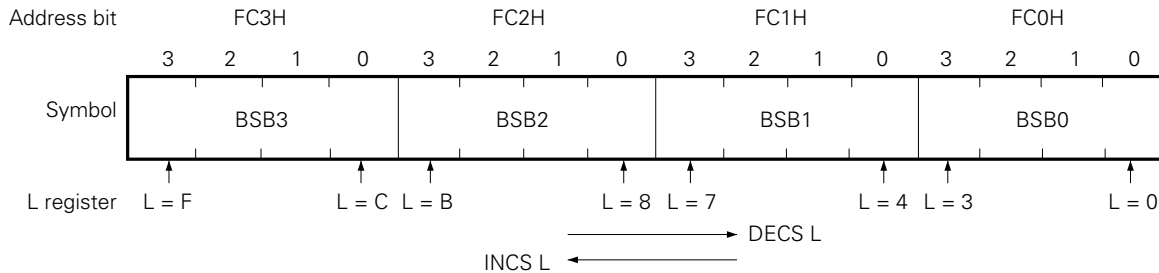
When  $V_{REF}$  is set to  $V_{DD} \times 7.5/16$ , the programmable threshold port can also be used as a digital signal input port.



**Fig. 5-6 Programmable Threshold Port Configuration**

### 5.8 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



*Remarks:* For the pmem.@L addressing, the specification bit is shifted according to the L register.

**Fig. 5-7 Bit Sequential Buffer Format**

### 5.9 POWER-ON FLAG (MASK OPTION)

The power-ON flag (PONF) is set to only when the power-ON reset circuit operates and power-ON reset signal has been generated (see Fig. 8-1).

The PONF flag is mapped at bit 0 of memory space address FD1H, and can be manipulated by a bit manipulation instruction. However, it cannot be set by the SET1 instruction.

## 6. INTERRUPT FUNCTIONS

The  $\mu$ PD75108 has 7 different interrupt sources and can perform multiplexed interrupt processing with priority assigned.

In addition to that, the  $\mu$ PD75108 is also provided with two types of edge detection testable inputs.

The interrupt control circuit of the  $\mu$ PD75108 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Multiplexed interrupt function that can specify priority by the interrupt priority selector register (IPS).
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

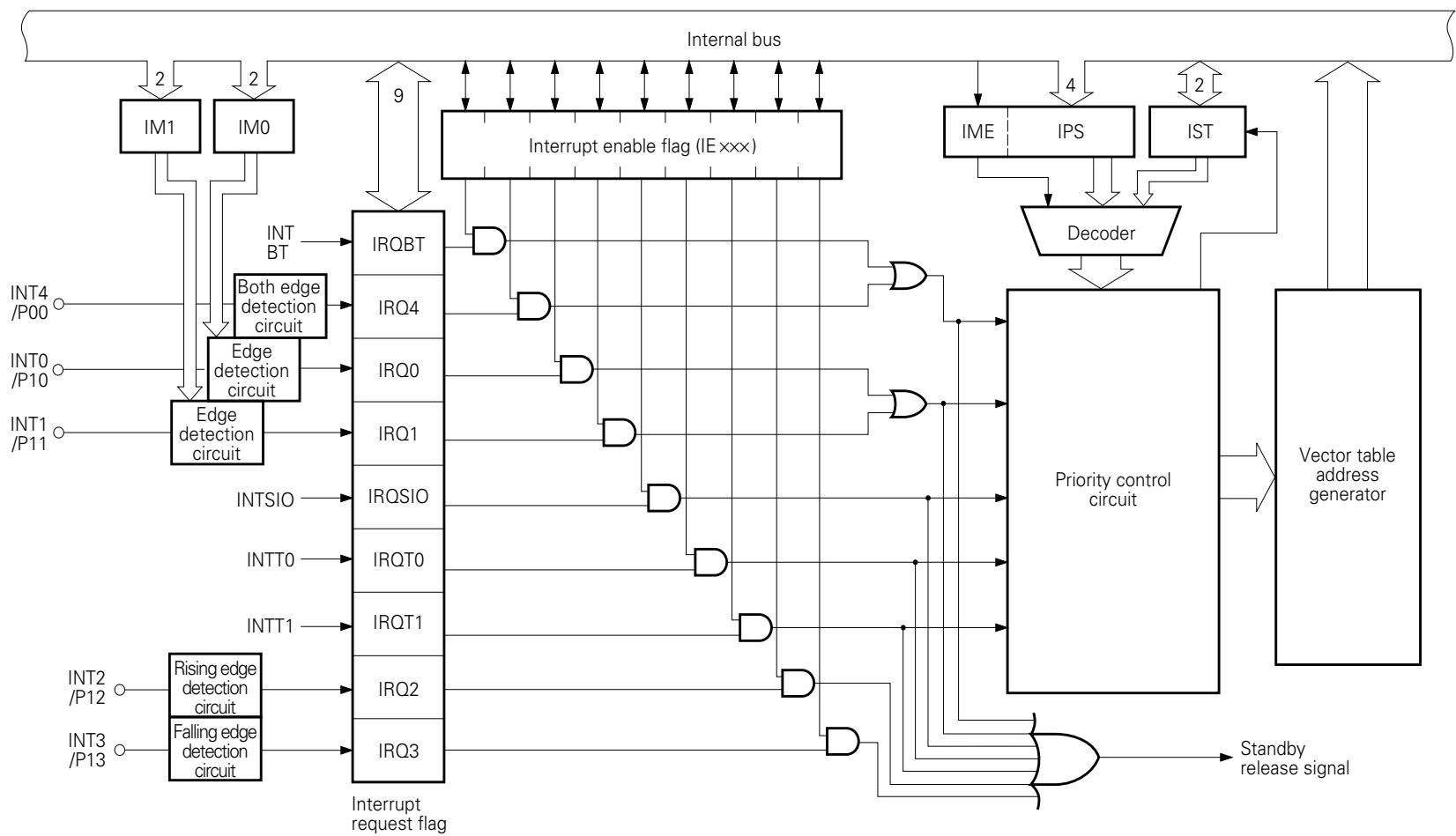


Fig. 6-1 Interrupt Control Block Diagram

## 7. STANDBY FUNCTIONS

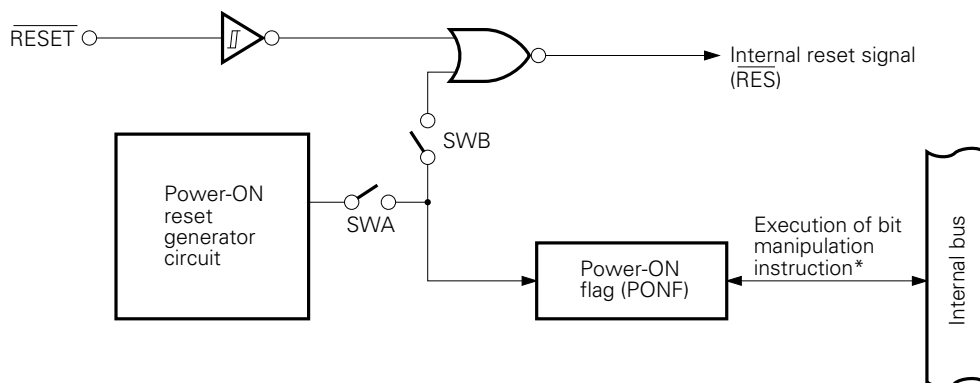
The μPD75108 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption of the microcomputer chip while waiting for program execution.

**Table 7-1 Each Status in Standby Mode**

|                     |                         | STOP Mode                                                                                                                                                        | HALT Mode                                                 |
|---------------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| Setting Instruction |                         | STOP instruction                                                                                                                                                 | HALT instruction                                          |
| Operation Status    | Clock Generator circuit | Clock oscillation stops                                                                                                                                          | Only CPU clock $\Phi$ is stopped                          |
|                     | Basic Interval Timer    | Stops                                                                                                                                                            | Operates (sets IRQBT at reference time intervals)         |
|                     | Serial Interface        | Operates only when input of external $\overline{\text{SCK}}$ or output of T00 is selected as serial clock (where external T10 is input to timer/event counter 0) | Operates when serial clock other than $\Phi$ is specified |
|                     | Timer/Event Counter     | Operates only when TIn pin input signal is specified as count clock                                                                                              | Operates                                                  |
|                     | Clock output circuit    | Stops                                                                                                                                                            | Operates when clock other than CPU clock $\Phi$ is used   |
|                     | CPU                     | Stops                                                                                                                                                            | Stops                                                     |
| Release Signal      |                         | Interrupt request signal enabled by interrupt enable flag, or $\overline{\text{RESET}}$ input                                                                    |                                                           |

## 8. RESET FUNCTION

The reset ( $\overline{\text{RES}}$ ) signal generator circuit is configured as shown in Figure 8-1.

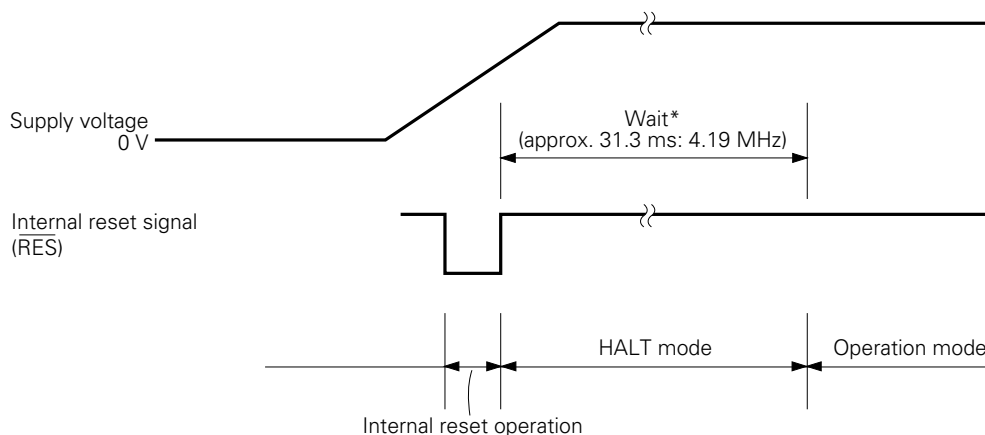


\*: PONF cannot be set to 1 by SET1 instruction.

**Fig. 8-1 Reset Signal Generator Circuit**

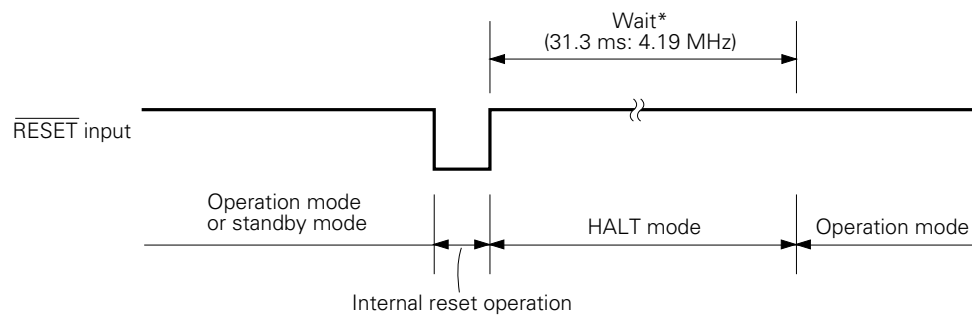
The Power-ON reset generator circuit generates an internal reset signal when the supply voltage rises. This pulse can be used in three ways by specifying a mask option through SWA and SWB shown in Fig. 8-1. (Refer to 11. MASK OPTION SELECTION.)

The reset operations performed by the Power-ON reset circuit and the RESET input signal are illustrated in Figs. 8-2 and 8-3, respectively.



\*: The wait time does not include the time required after the  $\overline{\text{RES}}$  signal has been generated until the oscillation starts.

**Fig. 8-2 Reset by Power-ON Reset Circuit**



\*: The wait time does not include the time required after the  $\overline{\text{RES}}$  signal has been generated until the oscillation starts.

**Fig. 8-3 Reset by  $\overline{\text{RESET}}$  Signal**

The status of each internal hardware device after the reset operation has been performed is shown in Table 8-1.

Table 8-1 Hardware Device Status After Reset

| Hardware                                      |                                        | RESET input during standby mode                                                                                                           | Power-ON Reset or RESET Input during Operation                                                                                            |
|-----------------------------------------------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Program Counter (PC)                          |                                        | Lower 4 bits of program memory address 000H are set to PC <sub>12-8</sub> ,*1 and contents of address 001H are set to PC <sub>7-0</sub> . | Lower 4 bits of program memory address 000H are set to PC <sub>12-8</sub> ,*1 and contents of address 001H are set to PC <sub>7-0</sub> . |
| PSW                                           | Carry Flag (CY)                        | Retained                                                                                                                                  | Undefined                                                                                                                                 |
|                                               | Skip Flags (SK0-SK2)                   | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | Interrupt Status Flags (IST0, 1)       | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | Bank Enable Flags (MBE, RBE)           | Bit 6 of program memory address 000H is set in RBE, and bit 7 is set in MBE.                                                              | Bit 6 of program memory address 000H is set in RBE, and bit 7 is set in MBE.                                                              |
| Stack Pointer (SP)                            |                                        | Undefined                                                                                                                                 | Undefined                                                                                                                                 |
| Data Memory (RAM)                             |                                        | Retained*2                                                                                                                                | Undefined                                                                                                                                 |
| General-Purpose Registers (X,A,H,L,D,E,B,C)   |                                        | Retained                                                                                                                                  | Undefined                                                                                                                                 |
| Bank Selector Registers (MBS, RBS)            |                                        | 0, 0                                                                                                                                      | 0, 0                                                                                                                                      |
| Basic interval timer                          | Counter (BT)                           | Undefined                                                                                                                                 | Undefined                                                                                                                                 |
|                                               | Mode Register (BTM)                    | 0                                                                                                                                         | 0                                                                                                                                         |
| Timer/Event Counter (n = 0, 1)                | Counter (Tn)                           | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | Modulo Register (TMODn)                | FFH                                                                                                                                       | FFH                                                                                                                                       |
|                                               | Mode Register (TMn)                    | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | TOEn, TOFn                             | 0, 0                                                                                                                                      | 0, 0                                                                                                                                      |
| Serial Interface                              | Shift Register (SIO)                   | Retained                                                                                                                                  | Undefined                                                                                                                                 |
|                                               | Mode Register (SIOM)                   | 0                                                                                                                                         | 0                                                                                                                                         |
| Clock Generator Circuit, Clock Output Circuit | Processor Clock Control Register (PCC) | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | Clock Output Mode Register (CLOM)      | 0                                                                                                                                         | 0                                                                                                                                         |
| Interrupt                                     | Interrupt Request Rlags (IRQxxx)       | Reset (0)                                                                                                                                 | Reset (0)                                                                                                                                 |
|                                               | Interrupt Enable Flags (IExxx)         | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | Priority Selector Register (IPS)       | 0                                                                                                                                         | 0                                                                                                                                         |
|                                               | INT0, 1 Mode Registers (IM0, IM1)      | 0, 0                                                                                                                                      | 0, 0                                                                                                                                      |
| Digital Port                                  | Output Buffer                          | OFF                                                                                                                                       | OFF                                                                                                                                       |
|                                               | Output Latch                           | Cleared (0)                                                                                                                               | Cleared (0)                                                                                                                               |
|                                               | I/O Mode Registers (PMGA, PMGB, PMGC)  | 0                                                                                                                                         | 0                                                                                                                                         |
| Analog Port                                   | PTH00-PTH03 Input Latches              | Undefined                                                                                                                                 | Undefined                                                                                                                                 |
|                                               | Mode Register (PTHM)                   | 0                                                                                                                                         | 0                                                                                                                                         |
| Power-ON Flag (PONF)                          |                                        | Retained                                                                                                                                  | 1 or undefined*2                                                                                                                          |
| Bit Sequential Buffer (BSB0-BSB3)             |                                        | 0                                                                                                                                         | 0                                                                                                                                         |

\*1: PC<sub>11-8</sub> for μPD75104

2: Power-ON reset: 1

RESET input during operation: undefined

**Note:** Data at data memory addresses 0F8H to 0FDH become undefined when the RESET signal has been input.

## 9. INSTRUCTION SET

### (1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD751XX Series User's Manual (IEM-922)). However, fmem and pmem restricts the label that can be described.

| Representation | Description                                         |                                        |
|----------------|-----------------------------------------------------|----------------------------------------|
| reg            | X, A, B, C, D, E, H, L                              |                                        |
| reg1           | X, B, C, D, E, H, L                                 |                                        |
| rp             | XA, BC, DE, HL                                      |                                        |
| rp1            | BC, DE, HL                                          |                                        |
| rp2            | BC, DE                                              |                                        |
| rp'            | XA, BC, DE, HL, XA', BC', DE', HL'                  |                                        |
| rp'1           | BC, DE, HL, XA', BC', DE', HL'                      |                                        |
| rpa            | HL, HL+, HL–, DE, DL                                |                                        |
| rpa1           | DE, DL                                              |                                        |
| n4             | 4-bit immediate data or label                       |                                        |
| n8             | 8-bit immediate data or label                       |                                        |
| mem            | 8-bit immediate data or label*                      |                                        |
| bit            | 2-bit immediate data or label                       |                                        |
| fmem           | FB0H to FBFH, FF0H to FFFH immediate data or label  |                                        |
| pmem           | FC0H to FFFH immediate data or label                |                                        |
| addr           | μPD75104                                            | 0000H to 0FFFH immediate data or label |
|                | μPD75106                                            | 0000H to 177FH immediate data or label |
|                | μPD75108                                            | 0000H to 1F7FH immediate data or label |
| caddr          | 12-bit immediate data or label                      |                                        |
| faddr          | 11-bit immediate data or label                      |                                        |
| taddr          | 20H to 7FH immediate data (where bit0 = 0) or label |                                        |
| PORTn          | PORT0 - PORT9, PORT12 - PORT14                      |                                        |
| IExxx          | IEBT, IESIO, IET0, IET1, IE0 - IE4                  |                                        |
| RBn            | RB0 - RB3                                           |                                        |
| MBn            | MB0, MB1, MB15                                      |                                        |

\*: Only even address can be described as mem for 8-bit data processing.

## (2) Legend of operation field

|                   |                                         |
|-------------------|-----------------------------------------|
| A                 | : A register; 4-bit accumulator         |
| B                 | : B register; 4-bit accumulator         |
| C                 | : C register; 4-bit accumulator         |
| D                 | : D register; 4-bit accumulator         |
| E                 | : E register; 4-bit accumulator         |
| H                 | : H register; 4-bit accumulator         |
| L                 | : L register; 4-bit accumulator         |
| X                 | : X register; 4-bit accumulator         |
| XA                | : Register pair (XA); 8-bit accumulator |
| BC                | : Register pair (BC); 8-bit accumulator |
| DE                | : Register pair (DE); 8-bit accumulator |
| HL                | : Register pair (HL); 8-bit accumulator |
| XA'               | : Expansion register pair (XA')         |
| BC'               | : Expansion register pair (BC')         |
| DE'               | : Expansion register pair (DE')         |
| HL'               | : Expansion register pair (HL')         |
| PC                | : Program counter                       |
| SP                | : Stack pointer                         |
| CY                | : Carry flag; or bit accumulator        |
| PSW               | : Program status word                   |
| MBE               | : Memory bank enable flag               |
| RBE               | : Register bank enable flag             |
| PORT <sub>n</sub> | : Port n (n = 0 - 9, 12 - 14)           |
| IME               | : Interrupt mask enable flag            |
| IPS               | : Interrupt priority selection register |
| IE <sub>xxx</sub> | : Interrupt enable flag                 |
| RBS               | : Register bank selection register      |
| MBS               | : Memory bank selection register        |
| PCC               | : Processor clock control register      |
| .                 | : Delimiter of address and bit          |
| (xx)              | : Contents addressed by xx              |
| xxH               | : Hexadecimal data                      |

(3) Symbols in addressing area field

|     |                                                                                        |                                                                                  |                              |
|-----|----------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------------------------|
| *1  | MB = MBE · MBS<br>(MBS = 0, 1, 15)                                                     |                                                                                  | Data memory<br>addressing    |
| *2  | MB = 0                                                                                 |                                                                                  |                              |
| *3  | MBE = 0 : MB = 0 (00H-7FH)<br>MB = 15 (80H-FFH)<br>MBE = 1 : MB = MBS (MBS = 0, 1, 15) |                                                                                  |                              |
| *4  | MB = 15, fmem = FB0H-FBFH,<br>FF0H-FFFH                                                |                                                                                  |                              |
| *5  | MB = 15, pmem = FC0H-FFFH                                                              |                                                                                  |                              |
| *6  | μPD75104                                                                               | addr = 0000H-0FFFH                                                               | Program memory<br>addressing |
|     | μPD75106                                                                               | addr = 0000H-177FH                                                               |                              |
|     | μPD75108                                                                               | addr = 0000H-1F7FH                                                               |                              |
| *7  | addr = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16  |                                                                                  |                              |
| *8  | μPD75104                                                                               | caddr = 0000H-0FFFH (PC <sub>11</sub> = 0)                                       |                              |
|     | μPD75106                                                                               | caddr = 0000H-0FFFH (PC <sub>12</sub> = 0) or 1000H-177FH (PC <sub>12</sub> = 1) |                              |
|     | μPD75108                                                                               | caddr = 0000H-0FFFH (PC <sub>12</sub> = 0) or 1000H-1F7FH (PC <sub>12</sub> = 1) |                              |
| *9  | faddr = 000H-7FFH                                                                      |                                                                                  |                              |
| *10 | taddr = 020H-07FH                                                                      |                                                                                  |                              |

- Remarks**
- MB indicates memory bank that can be accessed.
  - In \*2, MB = 0 regardless of MBE and MBS.
  - In \*4 and \*5, MB = 15 regardless of MBE and MBS.
  - \*6 to \*10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR ! adder or CALL ! adder) is skipped ..... S = 2

*Note* : The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock  $\Phi$ , (= tcy), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

| Instructions            | Mne-<br>monics | Operand   | Bytes | Ma-<br>chine<br>Cyc-<br>les | Operation                                                      | Addressing<br>Area | Skip<br>Conditions |
|-------------------------|----------------|-----------|-------|-----------------------------|----------------------------------------------------------------|--------------------|--------------------|
| Transfer                | MOV            | A, #n4    | 1     | 1                           | $A \leftarrow n4$                                              |                    | String effect A    |
|                         |                | reg1, #n4 | 2     | 2                           | $reg1 \leftarrow n4$                                           |                    |                    |
|                         |                | XA, #n8   | 2     | 2                           | $XA \leftarrow n8$                                             |                    | String effect A    |
|                         |                | HL, #n8   | 2     | 2                           | $HL \leftarrow n8$                                             |                    | String effect B    |
|                         |                | rp2, #n8  | 2     | 2                           | $rp2 \leftarrow n8$                                            |                    |                    |
|                         |                | A, @HL    | 1     | 1                           | $A \leftarrow (HL)$                                            | *1                 |                    |
|                         |                | A, @HL+   | 1     | 2+S                         | $A \leftarrow (HL)$ , then $L \leftarrow L+1$                  | *1                 | L = 0              |
|                         |                | A, @HL-   | 1     | 2+S                         | $A \leftarrow (HL)$ , then $L \leftarrow L-1$                  | *1                 | L = FH             |
|                         |                | A, @rpa1  | 1     | 1                           | $A \leftarrow (rpa1)$                                          | *2                 |                    |
|                         |                | XA, @HL   | 2     | 2                           | $XA \leftarrow (HL)$                                           | *1                 |                    |
|                         |                | @HL, A    | 1     | 1                           | $(HL) \leftarrow A$                                            | *1                 |                    |
|                         |                | @HL, XA   | 2     | 2                           | $(HL) \leftarrow XA$                                           | *1                 |                    |
|                         |                | A, mem    | 2     | 2                           | $A \leftarrow (mem)$                                           | *3                 |                    |
|                         |                | XA, mem   | 2     | 2                           | $XA \leftarrow (mem)$                                          | *3                 |                    |
|                         |                | mem, A    | 2     | 2                           | $(mem) \leftarrow A$                                           | *3                 |                    |
|                         |                | mem, XA   | 2     | 2                           | $(mem) \leftarrow XA$                                          | *3                 |                    |
|                         |                | A, reg    | 2     | 2                           | $A \leftarrow reg$                                             |                    |                    |
|                         |                | XA, rp'   | 2     | 2                           | $XA \leftarrow rp'$                                            |                    |                    |
|                         |                | reg1, A   | 2     | 2                           | $reg1 \leftarrow A$                                            |                    |                    |
|                         |                | rp'1, XA  | 2     | 2                           | $rp'1 \leftarrow XA$                                           |                    |                    |
|                         | XCH            | A, @HL    | 1     | 1                           | $A \leftrightarrow (HL)$                                       | *1                 |                    |
|                         |                | A, @HL+   | 1     | 2+S                         | $A \leftrightarrow (HL)$ , then $L \leftarrow L+1$             | *1                 | L = 0              |
|                         |                | A, @HL-   | 1     | 2+S                         | $A \leftrightarrow (HL)$ , then $L \leftarrow L-1$             | *1                 | L = FH             |
|                         |                | A, @rpa1  | 1     | 1                           | $A \leftrightarrow (rpa1)$                                     | *2                 |                    |
|                         |                | XA, @HL   | 2     | 2                           | $XA \leftrightarrow (HL)$                                      | *1                 |                    |
|                         |                | A, mem    | 2     | 2                           | $A \leftrightarrow (mem)$                                      | *3                 |                    |
|                         |                | XA, mem   | 2     | 2                           | $XA \leftrightarrow (mem)$                                     | *3                 |                    |
|                         |                | A, reg1   | 1     | 1                           | $A \leftrightarrow reg1$                                       |                    |                    |
|                         |                | XA, rp'   | 2     | 2                           | $XA \leftrightarrow rp'$                                       |                    |                    |
| Table<br>Refer-<br>ence | MOVT           | XA, @PCDE | 1     | 3                           | • $\mu$ PD75104<br>$XA \leftarrow (PC_{11-8}+DE)_{ROM}$        |                    |                    |
|                         |                |           |       |                             | • $\mu$ PD75106, 75108<br>$XA \leftarrow (PC_{12-8}+DE)_{ROM}$ |                    |                    |
|                         |                | XA, @PCXA | 1     | 3                           | • $\mu$ PD75104<br>$XA \leftarrow (PC_{11-8}+XA)_{ROM}$        |                    |                    |
|                         |                |           |       |                             | • $\mu$ PD75106, 75108<br>$XA \leftarrow (PC_{12-8}+XA)_{ROM}$ |                    |                    |

| Instruc-<br>tions                 | Mne-<br>monics | Operand           | Bytes | Ma-<br>chine<br>Cyc-<br>les | Operation                                                      | Addressing<br>Area | Skip<br>Conditions |
|-----------------------------------|----------------|-------------------|-------|-----------------------------|----------------------------------------------------------------|--------------------|--------------------|
| Bit<br>transfer                   | MOV1           | CY,fmem.bit       | 2     | 2                           | $CY \leftarrow (fmem.bit)$                                     | *4                 |                    |
|                                   |                | CY,pmem.@L        | 2     | 2                           | $CY \leftarrow (pmem_{7-2+L_{3-2}.bit(L_{1-0})})$              | *5                 |                    |
|                                   |                | CY,@H+mem.<br>bit | 2     | 2                           | $CY \leftarrow (H+mem_{3-0}.bit)$                              | *1                 |                    |
|                                   |                | fmem.bit,CY       | 2     | 2                           | $(fmem.bit) \leftarrow CY$                                     | *4                 |                    |
|                                   |                | pmem.@L,CY        | 2     | 2                           | $(pmem_{7-2+L_{3-2}.bit(L_{1-0})}) \leftarrow CY$              | *5                 |                    |
|                                   |                | @H+mem.bit,<br>CY | 2     | 2                           | $(H+mem_{3-0}.bit) \leftarrow CY$                              | *1                 |                    |
| Arith-<br>metic<br>opera-<br>tion | ADDS           | A, #n4            | 1     | 1+S                         | $A \leftarrow A+n4$                                            |                    | carry              |
|                                   |                | XA, #n8           | 2     | 2+S                         | $XA \leftarrow XA+n8$                                          |                    | carry              |
|                                   |                | A, @HL            | 1     | 1+S                         | $A \leftarrow A+(HL)$                                          | *1                 | carry              |
|                                   |                | XA, rp'           | 2     | 2+S                         | $XA \leftarrow XA+rp'$                                         |                    | carry              |
|                                   |                | rp'1, XA          | 2     | 2+S                         | $rp'1 \leftarrow rp'1+XA$                                      |                    | carry              |
|                                   | ADDC           | A, @HL            | 1     | 1                           | $A, CY \leftarrow A+(HL)+CY$                                   | *1                 |                    |
|                                   |                | XA, rp'           | 2     | 2                           | $XA, CY \leftarrow XA+rp'+CY$                                  |                    |                    |
|                                   |                | rp'1, XA          | 2     | 2                           | $rp'1, CY \leftarrow rp'1+XA+CY$                               |                    |                    |
|                                   | SUBS           | A, @HL            | 1     | 1+S                         | $A \leftarrow A-(HL).$                                         | *1                 | borrow             |
|                                   |                | XA, rp'           | 2     | 2+S                         | $XA \leftarrow XA-rp'$                                         |                    | borrow             |
|                                   |                | rp'1, XA          | 2     | 2+S                         | $rp'1 \leftarrow rp'1-XA$                                      |                    | borrow             |
|                                   | SUBC           | A, @HL            | 1     | 1                           | $A, CY \leftarrow A-(HL)-CY$                                   | *1                 |                    |
|                                   |                | XA, rp'           | 2     | 2                           | $XA, CY \leftarrow XA-rp'-CY$                                  |                    |                    |
|                                   |                | rp'1, XA          | 2     | 2                           | $rp'1, CY \leftarrow rp'1-XA-CY$                               |                    |                    |
|                                   | AND            | A, #n4            | 2     | 2                           | $A \leftarrow A \wedge n4$                                     |                    |                    |
|                                   |                | A, @HL            | 1     | 1                           | $A \leftarrow A \wedge (HL)$                                   | *1                 |                    |
|                                   |                | XA, rp'           | 2     | 2                           | $XA \leftarrow XA \wedge rp'$                                  |                    |                    |
|                                   |                | rp'1, XA          | 2     | 2                           | $rp'1 \leftarrow rp'1 \wedge XA$                               |                    |                    |
|                                   | OR             | A, #n4            | 2     | 2                           | $A \leftarrow A \vee n4$                                       |                    |                    |
|                                   |                | A, @HL            | 1     | 1                           | $A \leftarrow A \vee (HL)$                                     | *1                 |                    |
|                                   |                | XA, rp'           | 2     | 2                           | $XA \leftarrow XA \vee rp'$                                    |                    |                    |
|                                   |                | rp'1, XA          | 2     | 2                           | $rp'1 \leftarrow rp'1 \vee XA$                                 |                    |                    |
|                                   | XOR            | A, #n4            | 2     | 2                           | $A \leftarrow A \nabla n4$                                     |                    |                    |
|                                   |                | A, @HL            | 1     | 1                           | $A \leftarrow A \nabla (HL)$                                   | *1                 |                    |
|                                   |                | XA, rp'           | 2     | 2                           | $XA \leftarrow XA \nabla rp'$                                  |                    |                    |
|                                   |                | rp'1, XA          | 2     | 2                           | $rp'1 \leftarrow rp'1 \nabla XA$                               |                    |                    |
| Accumulator<br>Manipulation       | RORC           | A                 | 1     | 1                           | $CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$ |                    |                    |
|                                   | NOT            | A                 | 2     | 2                           | $A \leftarrow \bar{A}$                                         |                    |                    |
| Incre-<br>ment/<br>decre-<br>ment | INCS           | reg               | 1     | 1+S                         | $reg \leftarrow reg+1$                                         |                    | reg = 0            |
|                                   |                | rp1               | 1     | 1+S                         | $rp1 \leftarrow rp1+1$                                         |                    | rp1 = 00H          |
|                                   |                | @HL               | 2     | 2+S                         | $(HL) \leftarrow (HL)+1$                                       | *1                 | (HL) = 0           |
|                                   |                | mem               | 2     | 2+S                         | $(mem) \leftarrow (mem)+1$                                     | *3                 | (mem) = 0          |
|                                   | DECS           | reg               | 1     | 1+S                         | $reg \leftarrow reg-1$                                         |                    | reg = FH           |
|                                   |                | rp'               | 2     | 2+S                         | $rp' \leftarrow rp'-1$                                         |                    | rp' = FFH          |

| Instruc-<br>tions                   | Mne-<br>monics | Operand       | Bytes | Ma-<br>chine<br>Cyc-<br>les | Operation                                                                   | Addressing<br>Area | Skip<br>Conditions |
|-------------------------------------|----------------|---------------|-------|-----------------------------|-----------------------------------------------------------------------------|--------------------|--------------------|
| Com-<br>pare                        | SKE            | reg, #n4      | 2     | 2+S                         | Skip if reg = n4                                                            |                    | reg = n4           |
|                                     |                | @HL, #n4      | 2     | 2+S                         | Skip if (HL) = n4                                                           | *1                 | (HL) = n4          |
|                                     |                | A, @HL        | 1     | 1+S                         | Skip if A = (HL)                                                            | *1                 | A = (HL)           |
|                                     |                | XA, @HL       | 2     | 2+S                         | Skip if XA = (HL)                                                           | *1                 | XA = (HL)          |
|                                     |                | A, reg        | 2     | 2+S                         | Skip if A = reg                                                             |                    | A = reg            |
|                                     |                | XA, rp'       | 2     | 2+S                         | Skip if XA = rp'                                                            |                    | XA = rp'           |
| Carry<br>flag<br>Manipu-<br>lation  | SET1           | CY            | 1     | 1                           | $CY \leftarrow 1$                                                           |                    |                    |
|                                     | CLR1           | CY            | 1     | 1                           | $CY \leftarrow 0$                                                           |                    |                    |
|                                     | SKT            | CY            | 1     | 1+S                         | Skip if CY = 1                                                              |                    | CY = 1             |
|                                     | NOT1           | CY            | 1     | 1                           | $CY \leftarrow \overline{CY}$                                               |                    |                    |
| Memory/<br>Bit<br>Manipu-<br>lation | SET1           | mem.bit       | 2     | 2                           | $(\text{mem.bit}) \leftarrow 1$                                             | *3                 |                    |
|                                     |                | fmem.bit      | 2     | 2                           | $(\text{fmem.bit}) \leftarrow 1$                                            | *4                 |                    |
|                                     |                | pmem.@L       | 2     | 2                           | $(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) \leftarrow 1$            | *5                 |                    |
|                                     |                | @H+mem.bit    | 2     | 2                           | $(H + \text{mem}_{3-0}.\text{bit}) \leftarrow 1$                            | *1                 |                    |
|                                     | CLR1           | mem.bit       | 2     | 2                           | $(\text{mem.bit}) \leftarrow 0$                                             | *3                 |                    |
|                                     |                | fmem.bit      | 2     | 2                           | $(\text{fmem.bit}) \leftarrow 0$                                            | *4                 |                    |
|                                     |                | pmem.@L       | 2     | 2                           | $(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) \leftarrow 0$            | *5                 |                    |
|                                     |                | @H+mem.bit    | 2     | 2                           | $(H + \text{mem}_{3-0}.\text{bit}) \leftarrow 0$                            | *1                 |                    |
|                                     | SKT            | mem.bit       | 2     | 2+S                         | Skip if (mem.bit) = 1                                                       | *3                 | (mem.bit) = 1      |
|                                     |                | fmem.bit      | 2     | 2+S                         | Skip if (fmem.bit) = 1                                                      | *4                 | (fmem.bit) = 1     |
|                                     |                | pmem.@L       | 2     | 2+S                         | Skip if $(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) = 1$             | *5                 | (pmem.@L) = 1      |
|                                     |                | @H+mem.bit    | 2     | 2+S                         | Skip if $(H + \text{mem}_{3-0}.\text{bit}) = 1$                             | *1                 | (@H+mem.bit) = 1   |
|                                     | SKF            | mem.bit       | 2     | 2+S                         | Skip if (mem.bit) = 0                                                       | *3                 | (mem.bit) = 0      |
|                                     |                | fmem.bit      | 2     | 2+S                         | Skip if (fmem.bit) = 0                                                      | *4                 | (fmem.bit) = 0     |
|                                     |                | pmem.@L       | 2     | 2+S                         | Skip if $(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) = 0$             | *5                 | (pmem.@L) = 0      |
|                                     |                | @H+mem.bit    | 2     | 2+S                         | Skip if $(H + \text{mem}_{3-0}.\text{bit}) = 0$                             | *1                 | (@H+mem.bit) = 0   |
|                                     | SKTCLR         | fmem.bit      | 2     | 2+S                         | Skip if (fmem.bit) = 1 and clear                                            | *4                 | (fmem.bit) = 1     |
|                                     |                | pmem.@L       | 2     | 2+S                         | Skip if $(\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0})) = 1$ and clear   | *5                 | (pmem.@L) = 1      |
|                                     |                | @H+mem.bit    | 2     | 2+S                         | Skip if $(H + \text{mem}_{3-0}.\text{bit}) = 1$ and clear                   | *1                 | (@H+mem.bit) = 1   |
|                                     | AND1           | CY,fmem.bit   | 2     | 2                           | $CY \leftarrow CY \wedge (\text{fmem.bit})$                                 | *4                 |                    |
|                                     |                | CY,pmem.@L    | 2     | 2                           | $CY \leftarrow CY \wedge (\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0}))$ | *5                 |                    |
|                                     |                | CY,@H+mem.bit | 2     | 2                           | $CY \leftarrow CY \wedge (H + \text{mem}_{3-0}.\text{bit})$                 | *1                 |                    |
|                                     | OR1            | CY,fmem.bit   | 2     | 2                           | $CY \leftarrow CY \vee (\text{fmem.bit})$                                   | *4                 |                    |
|                                     |                | CY,pmem.@L    | 2     | 2                           | $CY \leftarrow CY \vee (\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0}))$   | *5                 |                    |
|                                     |                | CY,@H+mem.bit | 2     | 2                           | $CY \leftarrow CY \vee (H + \text{mem}_{3-0}.\text{bit})$                   | *1                 |                    |
|                                     | XOR1           | CY,fmem.bit   | 2     | 2                           | $CY \leftarrow CY \nabla (\text{fmem.bit})$                                 | *4                 |                    |
|                                     |                | CY,pmem.@L    | 2     | 2                           | $CY \leftarrow CY \nabla (\text{pmem}_{7-2} + L_{3-2}.\text{bit}(L_{1-0}))$ | *5                 |                    |
|                                     |                | CY,@H+mem.bit | 2     | 2                           | $CY \leftarrow CY \nabla (H + \text{mem}_{3-0}.\text{bit})$                 | *1                 |                    |

| Instructions                                                                                                                          | Mne-<br>monics                                                                                                                                       | Operand | Bytes   | Ma-<br>chine<br>Cyc-<br>les | Operation                                                                                                                                                                                                                                                                      | Addressing<br>Area                                                                                                                  | Skip<br>Conditions |
|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| Branch                                                                                                                                | BR                                                                                                                                                   | addr    | —       | —                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>PC_{11-0} \leftarrow \text{addr}</math><br/><div>(The most suitable instruction is selectable from among BRCB ! caddr, and BR \$ addr depending on the assembler.)</div></li></ul>                   | *6                                                                                                                                  |                    |
|                                                                                                                                       |                                                                                                                                                      |         |         |                             | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow \text{addr}</math><br/><div>(The most suitable instruction is selectable from among BR ! addr, BRCB ! caddr, and BR \$ addr depending on the assembler.)</div></li></ul> |                                                                                                                                     |                    |
|                                                                                                                                       |                                                                                                                                                      | ! addr  | 3       | 3                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow \text{addr}</math></li></ul>                                                                                                                                             | *6                                                                                                                                  |                    |
|                                                                                                                                       |                                                                                                                                                      | \$ addr | 1       | 2                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>PC_{11-0} \leftarrow \text{addr}</math></li></ul>                                                                                                                                                    | *7                                                                                                                                  |                    |
|                                                                                                                                       |                                                                                                                                                      |         |         |                             | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow \text{addr}</math></li></ul>                                                                                                                                             |                                                                                                                                     |                    |
|                                                                                                                                       |                                                                                                                                                      | BRCB    | ! caddr | 2                           | 2                                                                                                                                                                                                                                                                              | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>PC_{11-0} \leftarrow \text{caddr}_{11-0}</math></li></ul> | *8                 |
|                                                                                                                                       | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow PC_{12} + \text{caddr}_{11-0}</math></li></ul> |         |         |                             |                                                                                                                                                                                                                                                                                |                                                                                                                                     |                    |
|                                                                                                                                       | BR                                                                                                                                                   | PCDE    | 2       | 3                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>PC_{11-0} \leftarrow PC_{11-8} + DE</math></li></ul>                                                                                                                                                 |                                                                                                                                     |                    |
|                                                                                                                                       |                                                                                                                                                      |         |         |                             | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow PC_{12-8} + DE</math></li></ul>                                                                                                                                          |                                                                                                                                     |                    |
|                                                                                                                                       |                                                                                                                                                      | PCXA    | 2       | 3                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>PC_{11-0} \leftarrow PC_{11-8} + XA</math></li></ul>                                                                                                                                                 |                                                                                                                                     |                    |
| <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>PC_{12-0} \leftarrow PC_{12-8} + XA</math></li></ul> |                                                                                                                                                      |         |         |                             |                                                                                                                                                                                                                                                                                |                                                                                                                                     |                    |
| Subrou-<br>tine/<br>Stack<br>Control                                                                                                  | CALL                                                                                                                                                 | ! addr  | 3       | 3                           | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75104<br/><math>(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}</math><br/><math>(SP-3) \leftarrow MBE, RBE, 0, 0</math><br/><math>PC_{11-0} \leftarrow \text{addr}, SP \leftarrow SP-4</math></li></ul>                     | *6                                                                                                                                  |                    |
|                                                                                                                                       |                                                                                                                                                      |         |         |                             | <ul style="list-style-type: none"><li>• <math>\mu</math>PD75106, 75108<br/><math>(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}</math><br/><math>(SP-3) \leftarrow MBE, RBE, 0, PC_{12}</math><br/><math>PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4</math></li></ul>        |                                                                                                                                     |                    |

| Instructions                                     | Mne-<br>monics | Operand | Bytes | Ma-<br>chine<br>Cyc-<br>les | Operation                                                                                                                                                                                                                                                                   | Addressing<br>Area | Skip<br>Conditions |
|--------------------------------------------------|----------------|---------|-------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------|
| Subrou-<br>tine/<br>Stack<br>Control<br>(Cont'd) | CALLF          | ! faddr | 2     | 2                           | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75104<br/> <math>(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}</math><br/> <math>(SP-3) \leftarrow MBE, RBE, 0, 0</math><br/> <math>PC_{11-0} \leftarrow 0, faddr, SP \leftarrow SP-4</math> </li> </ul>               | *9                 |                    |
|                                                  |                |         |       |                             | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75106, 75108<br/> <math>(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}</math><br/> <math>(SP-3) \leftarrow MBE, RBE, 0, PC_{12}</math><br/> <math>PC_{12-0} \leftarrow 00, faddr, SP \leftarrow SP-4</math> </li> </ul> |                    |                    |
|                                                  | RET            |         | 1     | 3                           | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75104<br/> <math>MBE, RBE, x, x \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>SP \leftarrow SP+4</math> </li> </ul>                                                |                    |                    |
|                                                  |                |         |       |                             | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75106, 75108<br/> <math>MBE, RBE, x, PC_{12} \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>SP \leftarrow SP+4</math> </li> </ul>                                   |                    |                    |
|                                                  | RETS           |         | 1     | 3+S                         | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75104<br/> <math>MBE, RBE, x, x \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>SP \leftarrow SP+4</math>, then skip unconditionally </li> </ul>                     |                    | Unconditioned      |
|                                                  |                |         |       |                             | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75106, 75108<br/> <math>MBE, RBE, x, PC_{12} \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>SP \leftarrow SP+4</math>, then skip unconditionally </li> </ul>        |                    |                    |
|                                                  | RETI           |         | 1     | 3                           | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75104<br/> <math>MBE, RBE, x, x \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>PSW \leftarrow (SP+4)(SP+5), SP \leftarrow SP+6</math> </li> </ul>                   |                    |                    |
|                                                  |                |         |       |                             | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75106, 75108<br/> <math>MBE, RBE, x, PC_{12} \leftarrow (SP+1)</math><br/> <math>PC_{11-0} \leftarrow (SP)(SP+3)(SP+2)</math><br/> <math>PSW \leftarrow (SP+4)(SP+5), SP \leftarrow SP+6</math> </li> </ul>      |                    |                    |
|                                                  | PUSH           | rp      | 1     | 1                           | $(SP-1)(SP-2) \leftarrow rp, SP \leftarrow SP-2$                                                                                                                                                                                                                            |                    |                    |
|                                                  |                | BS      | 2     | 2                           | $(SP-1) \leftarrow MBS, (SP-2) \leftarrow RBS,$<br>$SP \leftarrow SP-2$                                                                                                                                                                                                     |                    |                    |
|                                                  | POP            | rp      | 1     | 1                           | $rp \leftarrow (SP+1)(SP), SP \leftarrow SP+2$                                                                                                                                                                                                                              |                    |                    |
|                                                  |                | BS      | 2     | 2                           | $MBS \leftarrow (SP+1), RBS \leftarrow (SP),$<br>$SP \leftarrow SP+2$                                                                                                                                                                                                       |                    |                    |

| Instructions              | Mne-<br>monics | Operand                | Bytes | Ma-<br>chine<br>Cyc-<br>les | Operation                                                                                                                                                                                                                                                                                                                       | Addressing<br>Area | Skip<br>Conditions                |
|---------------------------|----------------|------------------------|-------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------|
| Inter-<br>rupt<br>Control | EI             |                        | 2     | 2                           | IME (IPS.3) $\leftarrow$ 1                                                                                                                                                                                                                                                                                                      |                    |                                   |
|                           |                | IExxx                  | 2     | 2                           | IExxx $\leftarrow$ 1                                                                                                                                                                                                                                                                                                            |                    |                                   |
|                           | DI             |                        | 2     | 2                           | IME (IPS.3) $\leftarrow$ 0                                                                                                                                                                                                                                                                                                      |                    |                                   |
|                           |                | IExxx                  | 2     | 2                           | IExxx $\leftarrow$ 0                                                                                                                                                                                                                                                                                                            |                    |                                   |
| I/O                       | IN*            | A, PORT <sub>n</sub>   | 2     | 2                           | A $\leftarrow$ PORT <sub>n</sub> (n = 0-9, 12-14)                                                                                                                                                                                                                                                                               |                    |                                   |
|                           |                | XA, PORT <sub>n</sub>  | 2     | 2                           | XA $\leftarrow$ PORT <sub>n+1</sub> , PORT <sub>n</sub> (n = 4, 6, 8, 12)                                                                                                                                                                                                                                                       |                    |                                   |
|                           | OUT*           | PORT <sub>n</sub> , A  | 2     | 2                           | PORT <sub>n</sub> $\leftarrow$ A (n = 2-9, 12-14)                                                                                                                                                                                                                                                                               |                    |                                   |
|                           |                | PORT <sub>n</sub> , XA | 2     | 2                           | PORT <sub>n+1</sub> , PORT <sub>n</sub> $\leftarrow$ XA (n = 4, 6, 8, 12)                                                                                                                                                                                                                                                       |                    |                                   |
| CPU<br>Control            | HALT           |                        | 2     | 2                           | Set HALT Mode (PCC.2 $\leftarrow$ 1)                                                                                                                                                                                                                                                                                            |                    |                                   |
|                           | STOP           |                        | 2     | 2                           | Set STOP Mode (PCC.3 $\leftarrow$ 1)                                                                                                                                                                                                                                                                                            |                    |                                   |
|                           | NOP            |                        | 1     | 1                           | No Operation                                                                                                                                                                                                                                                                                                                    |                    |                                   |
| Special                   | SEL            | RB <sub>n</sub>        | 2     | 2                           | RBS $\leftarrow$ n (n = 0-3)                                                                                                                                                                                                                                                                                                    |                    |                                   |
|                           |                | MB <sub>n</sub>        | 2     | 2                           | MBS $\leftarrow$ n (n = 0, 1, 15)                                                                                                                                                                                                                                                                                               |                    |                                   |
|                           | GETI           | taddr                  | 1     | 3                           | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75104</li> <li>• Where TBR instruction,<br/>PC<sub>11-0</sub> <math>\leftarrow</math> (taddr)<sub>3-0</sub>+(taddr+1)</li> </ul>                                                                                                                                     | *10                |                                   |
|                           |                |                        |       |                             | <ul style="list-style-type: none"> <li>• Where TCALL instruction,<br/>(SP-4)(SP-1)(SP-2) <math>\leftarrow</math> PC<sub>11-0</sub><br/>(SP-3) <math>\leftarrow</math> MBE, RBE, 0, 0<br/>PC<sub>11-0</sub> <math>\leftarrow</math> (taddr)<sub>3-0</sub>+(taddr+1)<br/>SP <math>\leftarrow</math> SP-4</li> </ul>               |                    |                                   |
|                           |                |                        |       |                             | <ul style="list-style-type: none"> <li>• Except for TBR and TCALL instructions,<br/>Instruction execution of (taddr)(taddr+1)</li> </ul>                                                                                                                                                                                        |                    | Depends on referenced instruction |
|                           |                |                        |       |                             | <ul style="list-style-type: none"> <li>• <math>\mu</math>PD75106, 75108</li> <li>• Where TBR instruction,<br/>PC<sub>12-0</sub> <math>\leftarrow</math> (taddr)<sub>4-0</sub>+(taddr+1)</li> </ul>                                                                                                                              |                    |                                   |
|                           |                |                        |       |                             | <ul style="list-style-type: none"> <li>• Where TCALL instruction,<br/>(SP-4)(SP-1)(SP-2) <math>\leftarrow</math> PC<sub>11-0</sub><br/>(SP-3) <math>\leftarrow</math> MBE, RBE, 0, PC<sub>12</sub><br/>PC<sub>12-0</sub> <math>\leftarrow</math> (taddr)<sub>4-0</sub>+(taddr+1)<br/>SP <math>\leftarrow</math> SP-4</li> </ul> |                    |                                   |
|                           |                |                        |       |                             | <ul style="list-style-type: none"> <li>• Except for TBR and TCALL instructions,<br/>Instruction execution of (taddr)(taddr+1)</li> </ul>                                                                                                                                                                                        |                    | Depends on referenced instruction |

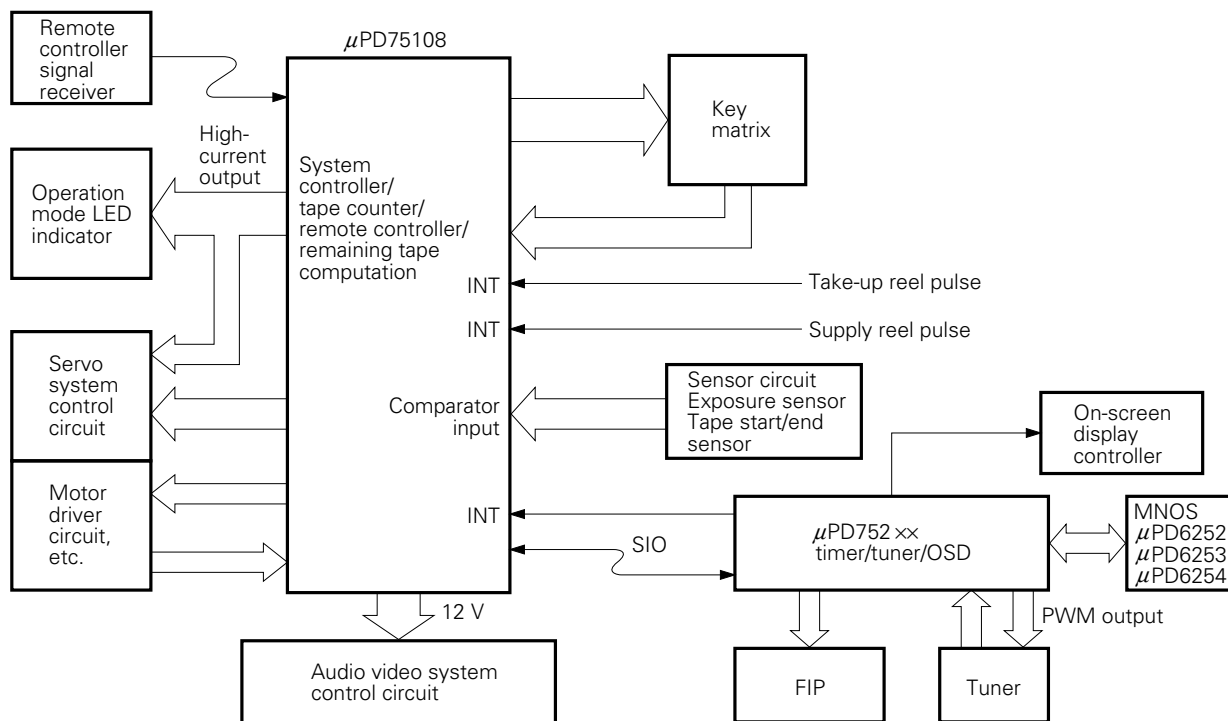
\*: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.



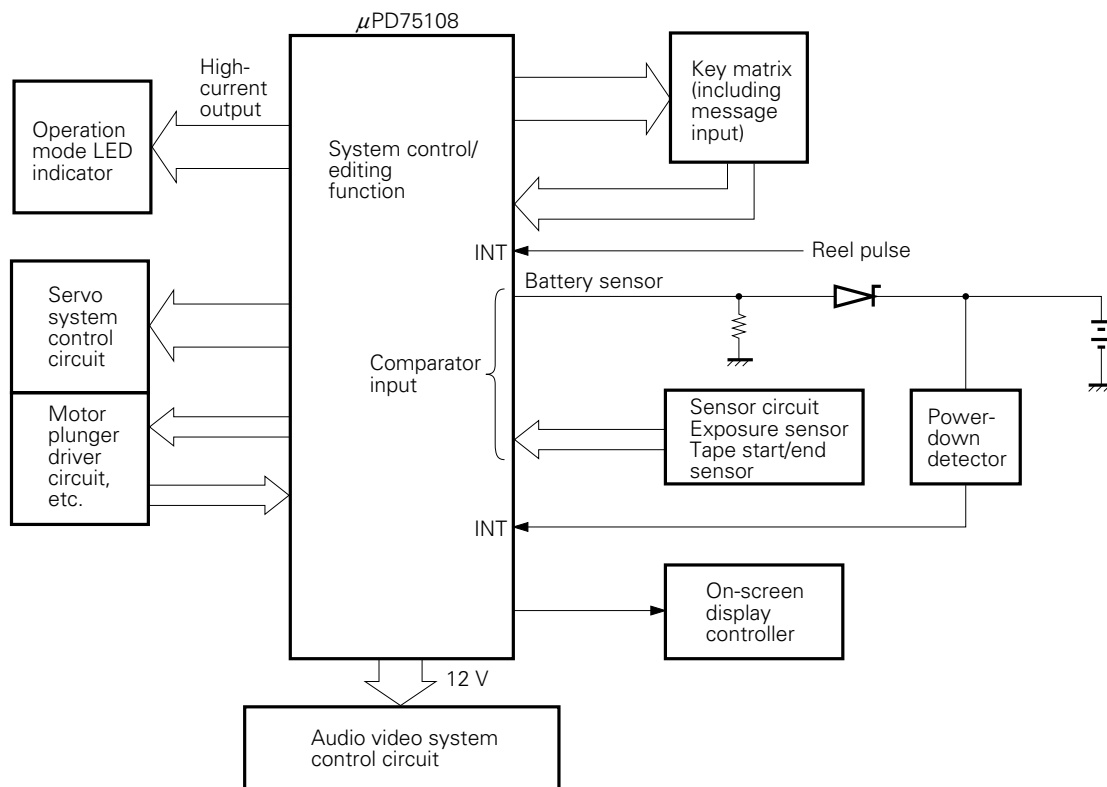
**Remarks:** TBR and TCALL instructions are assembler instructions for GETI instruction table definition.

## 10. APPLICATION EXAMPLES

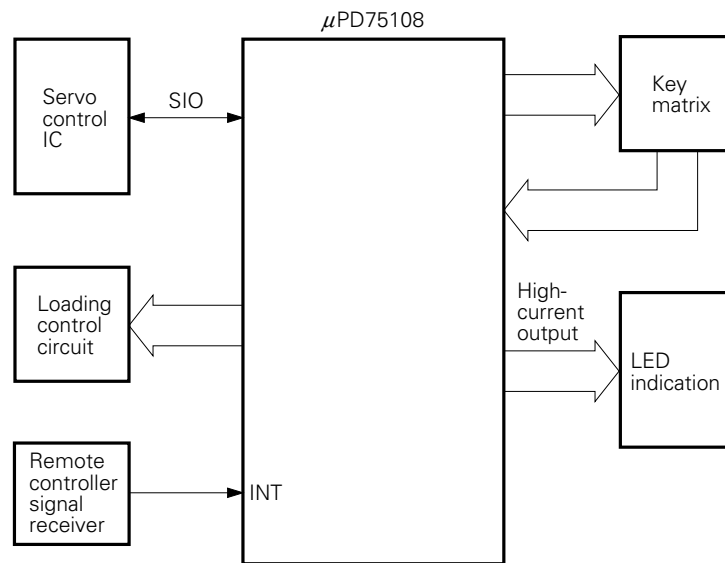
### 10.1 VTR SYSTEM CONTROLLER



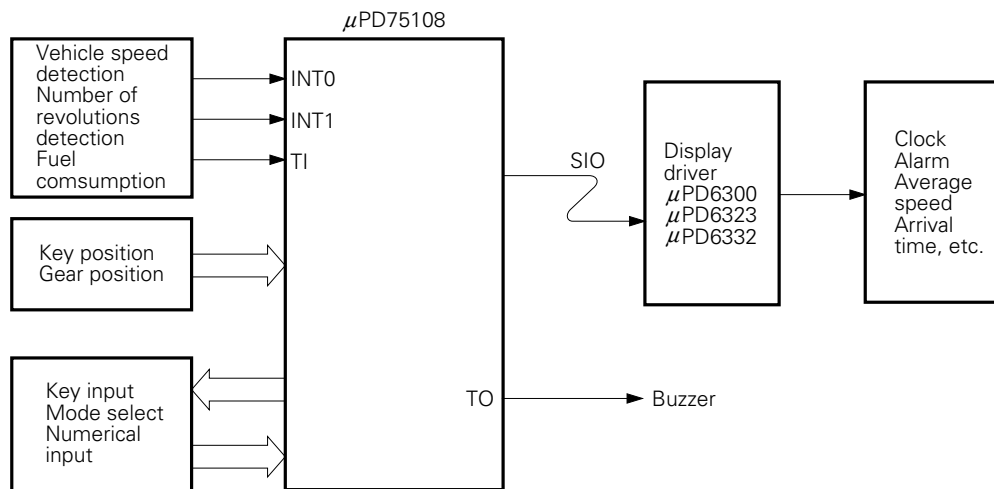
### 10.2 VTR CAMERA



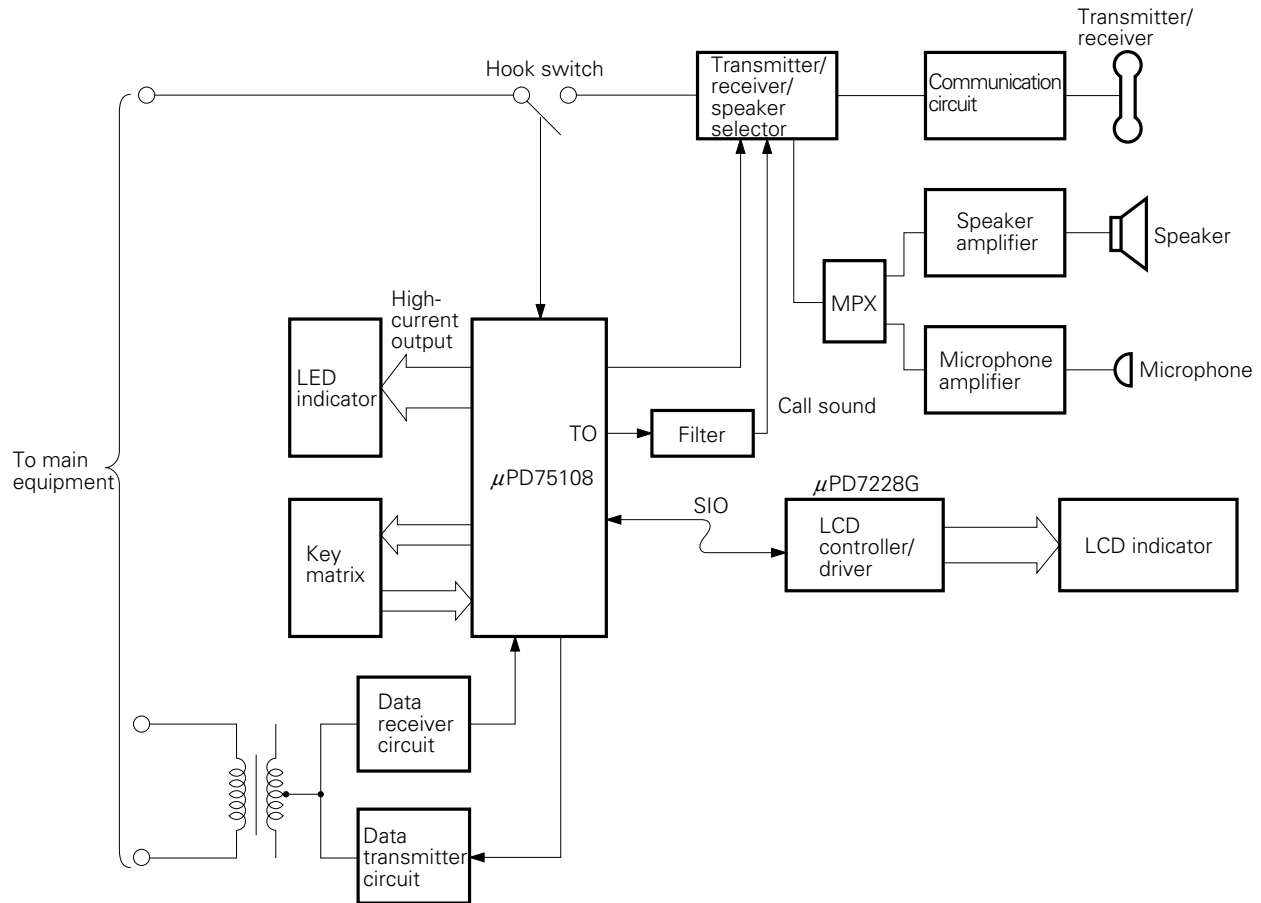
### 10.3 COMPACT DISC PLAYER



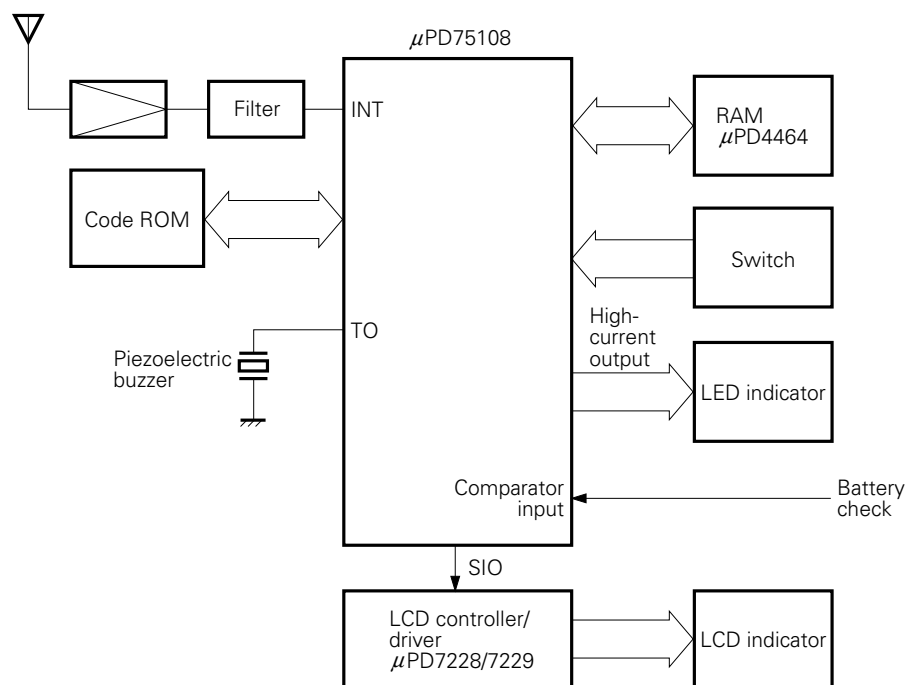
### 10.4 AUTOMOBILE APPLICATIONS (TRIP COMPUTER)



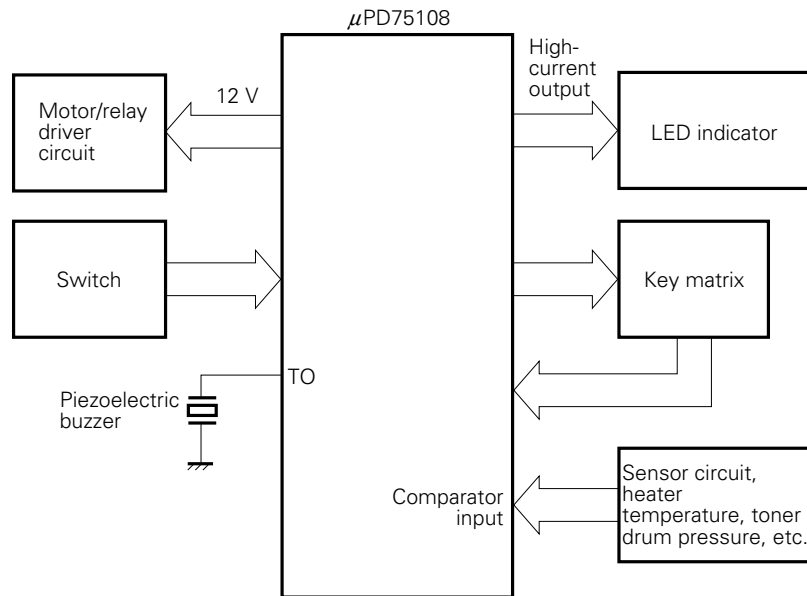
## 10.5 PUSHBUTTON TELEPHONE



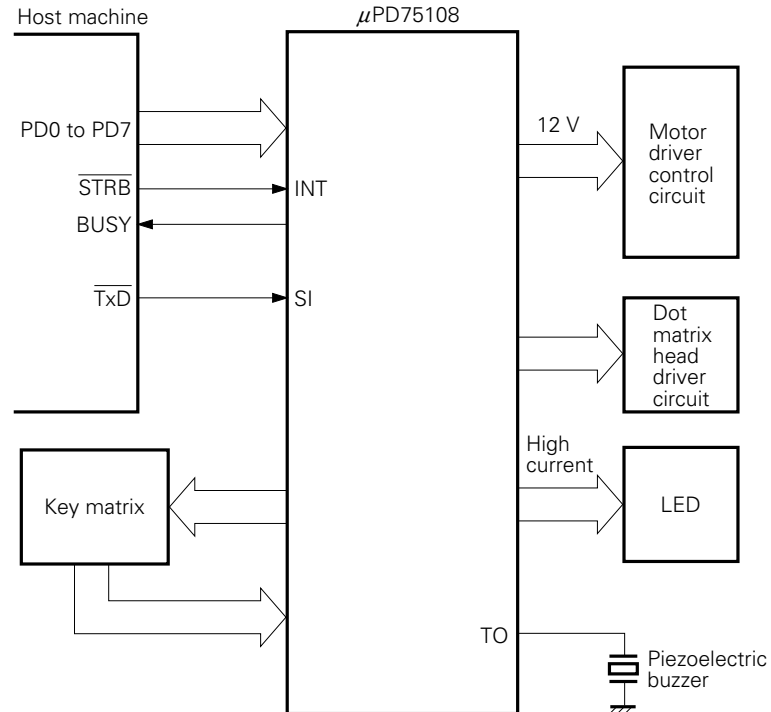
## 10.6 DISPLAY PAGER



## 10.7 PLAIN PAPER COPIER (PPC)



## 10.8 PRINTER CONTROLLER



## 11. MASK OPTION SELECTION

$\mu$ PD75108 has the following mask options. Options to be built in can be selected.

(1) Pin

| Pin         | Mask Option                                 |
|-------------|---------------------------------------------|
| P120 - P123 | Pull-down resistor can be built in bitwise. |
| P130 - P133 |                                             |
| P140 - P143 |                                             |

(2) Power-ON reset generation circuit, power-ON flag (PONF)

One from the following three ways can be selected.

| Switching Selection<br>(Refer to Fig. 8-1.) |     | Power-On Reset<br>Generation Circuit | Power-On Flag<br>(PONF) | Internal Reset Signal<br>( $\overline{\text{RES}}$ ) |
|---------------------------------------------|-----|--------------------------------------|-------------------------|------------------------------------------------------|
| SWA                                         | SWB |                                      |                         |                                                      |
| ON                                          | ON  | Provided                             | Provided                | Generates automatically                              |
| ON                                          | OFF | Provided                             | Provided                | Not generates autoamtically                          |
| OFF                                         | OFF | Not provided                         | Not provided            | —                                                    |

## 12. ELECTRICAL SPECIFICATIONS

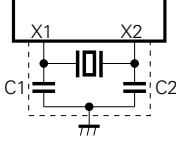
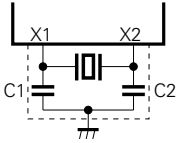
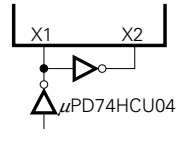
### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

| Parameter                 | Symbol        | Conditions                         |                    | Ratings              | Unit             |
|---------------------------|---------------|------------------------------------|--------------------|----------------------|------------------|
| Supply Voltage            | $V_{DD}$      |                                    |                    | -0.3 to +7.0         | V                |
| Input Voltage             | $V_{I1}$      | Other than ports 12, 13, 14        |                    | -0.3 to $V_{DD}+0.3$ | V                |
|                           | $V_{I2}^{*1}$ | Ports 12 to 14                     | w/pull-up resistor | -0.3 to $V_{DD}+0.3$ | V                |
|                           |               |                                    | Open drain         | -0.3 to +13          | V                |
| Output Voltage            | $V_O$         |                                    |                    | -0.3 to $V_{DD}+0.3$ | V                |
| High-Level Output Current | $I_{OH}$      | 1 pin                              |                    | -15                  | mA               |
|                           |               | All pins                           |                    | -30                  | mA               |
| Low-Level Output Current  | $I_{OL}^{*2}$ | 1 pin                              | Peak               | 30                   | mA               |
|                           |               |                                    | rms                | 15                   | mA               |
|                           |               | Total of ports 0, 2 to 4, 12 to 14 | Peak               | 100                  | mA               |
|                           |               |                                    | rms                | 60                   | mA               |
|                           |               | Total of ports 5 to 9              | Peak               | 100                  | mA               |
|                           |               |                                    | rms                | 60                   | mA               |
| Operating Temperature     | $T_{opt}$     |                                    |                    | -40 to +85           | $^\circ\text{C}$ |
| Storage Temperature       | $T_{stg}$     |                                    |                    | -65 to +150          | $^\circ\text{C}$ |

\*1: The power supply impedance (pull-up resistance) must be 50 k $\Omega$  or higher when a voltage higher than 10 V is applied to ports 12, 13, and 14.

2:  $\text{rms} = \text{Peak value} \times \sqrt{\text{Duty}}$

**OSCILLATOR CIRCUIT CHARACTERISTICS**(T<sub>a</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 6.0 V)

| Oscillator     | Recommended Constants                                                             | Item                                                                  | Conditions                                                      | MIN. | TYP. | MAX.              | Unit |
|----------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------|------|------|-------------------|------|
| Ceramic        |  | Oscillation frequency(f <sub>xx</sub> )* <sup>1</sup>                 | V <sub>DD</sub> = Oscillation voltage range                     | 2.0  |      | 5.0* <sup>3</sup> | MHz  |
|                |                                                                                   | Oscillation stabilization time* <sup>2</sup>                          | After V <sub>DD</sub> come to MIN. of oscillation voltage range |      |      | 4                 | ms   |
| Crystal        |  | Oscillation frequency (f <sub>xx</sub> )* <sup>1</sup>                |                                                                 | 2.0  | 4.19 | 5.0* <sup>3</sup> | MHz  |
|                |                                                                                   | Oscillation stabilization time* <sup>2</sup>                          | V <sub>DD</sub> = 4.5 to 6.0 V                                  |      |      | 10                | ms   |
| External Clock |  | X1 input frequency (f <sub>x</sub> )* <sup>1</sup>                    |                                                                 | 2.0  |      | 5.0* <sup>3</sup> | MHz  |
|                |                                                                                   | X1 input high-, low-level widths (t <sub>xH</sub> , t <sub>xL</sub> ) |                                                                 | 100  |      | 250               | ns   |

\*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V<sub>DD</sub> has come to MIN. of oscillation voltage range or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < f<sub>x</sub> ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

**Note:** When using the oscillation circuit of the system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity: ★

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Also, do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V<sub>SS</sub>. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

**RECOMMENDED OSCILLATOR CIRCUITS CONSTANTS****RECOMMENDED CERAMIC OSCILLATORS**

| Manufacturer               | Product Name | External Capacitance (pF) |          | Oscillation Voltage Range (V) |      |
|----------------------------|--------------|---------------------------|----------|-------------------------------|------|
|                            |              | C1                        | C2       | MIN.                          | MAX. |
| Murata Mfg.<br>Co., Ltd.   | CSA 2.00MG   | 30                        | 30       | 2.7                           | 6.0  |
|                            | CSA 4.19MG   | 30                        | 30       | 3.0                           | 6.0  |
|                            | CSA 4.19MGU  | 30                        | 30       | 2.7                           | 6.0  |
|                            | CST 4.19T    | Provided                  | Provided | 3.0                           | 6.0  |
| Kyoto Ceramic<br>Co., Ltd. | KBR-2.0MS    | 100                       | 100      | 3.0                           | 6.0  |
|                            | KBR-4.0MS    | 33                        | 33       | 3.0                           | 6.0  |
|                            | KBR-4.19MS   | 33                        | 33       | 3.0                           | 6.0  |
|                            | KBR-4.9152M  | 33                        | 33       | 3.0                           | 6.0  |

**RECOMMENDED CRYSTAL OSCILLATOR**

| Manufacturer | Product Name | External Capacitance (pF) |    | Oscillation Voltage Range (V) |      |
|--------------|--------------|---------------------------|----|-------------------------------|------|
|              |              | C1                        | C2 | MIN.                          | MAX. |
| Kinseki      | HC-49/U      | 22                        | 22 | 2.7                           | 6.0  |

**DC CHARACTERISTICS** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $6.0$  V)

| Item                              | Symbol     | Conditions                                   |                                   | MIN.                    | TYP. | MAX.         | Unit          |
|-----------------------------------|------------|----------------------------------------------|-----------------------------------|-------------------------|------|--------------|---------------|
| High-Level Input Voltage          | $V_{IH1}$  | Other than below                             |                                   | $0.7V_{DD}$             |      | $V_{DD}$     | V             |
|                                   | $V_{IH2}$  | Ports 0, 1, TI0, 1, RESET                    |                                   | $0.8 V_{DD}$            |      | $V_{DD}$     | V             |
|                                   | $V_{IH3}$  | Ports 12 to 14                               | Pull-up resistor                  | $0.7 V_{DD}$            |      | $V_{DD}$     | V             |
|                                   |            |                                              | Open drain                        | $0.7 V_{DD}$            |      | 12           | V             |
|                                   | $V_{IH4}$  | X1, X2                                       |                                   | $V_{DD}-0.5$            |      | $V_{DD}$     | V             |
| Low-Level Input Voltage           | $V_{IL1}$  | Other than below                             |                                   | 0                       |      | $0.3 V_{DD}$ | V             |
|                                   | $V_{IL2}$  | Ports 0, 1, TI0, 1, RESET                    |                                   | 0                       |      | $0.2 V_{DD}$ | V             |
|                                   | $V_{IL3}$  | X1, X2                                       |                                   | 0                       |      | 0.4          | V             |
| High-Level Output Voltage         | $V_{OH}$   | $V_{DD} = 4.5$ to $6.0$ V, $I_{OH} = -1$ mA  |                                   | $V_{DD}-1.0$            |      |              | V             |
|                                   |            | $I_{OH} = -100 \mu\text{A}$                  |                                   | $V_{DD}-0.5$            |      |              | V             |
| Low-Level Output Voltage          | $V_{OL}$   | $V_{DD} = 4.5$ to $6.0$ V                    | Ports 0, 2 to 9, $I_{OL} = 15$ mA |                         | 0.35 | 2.0          | V             |
|                                   |            |                                              | Ports 12 to 14, $I_{OL} = 10$ mA  |                         | 0.35 | 2.0          | V             |
|                                   |            | $V_{DD} = 4.5$ to $6.0$ V, $I_{OL} = 1.6$ mA |                                   |                         |      | 0.4          | V             |
|                                   |            | $I_{OL} = 400 \mu\text{A}$                   |                                   |                         |      | 0.5          | V             |
| High-Level Input Leakage Current  | $I_{LIH1}$ | $V_{IN} = V_{DD}$                            | Other than below                  |                         |      | 3            | $\mu\text{A}$ |
|                                   | $I_{LIH2}$ |                                              | X1,X2                             |                         |      | 20           | $\mu\text{A}$ |
|                                   | $I_{LIH3}$ | $V_{IN} = 12$ V                              | Ports 12 to 14 (open drain)       |                         |      | 20           | $\mu\text{A}$ |
| Low-Level Input Leakage Current   | $I_{LIL1}$ | $V_{IN} = 0$ V                               | Other than X1, X2                 |                         |      | -3           | $\mu\text{A}$ |
|                                   | $I_{LIL2}$ |                                              | X1, X2                            |                         |      | -20          | $\mu\text{A}$ |
| High-Level Output Leakage Current | $I_{LOH1}$ | $V_{OUT} = V_{DD}$                           | Other than below                  |                         |      | 3            | $\mu\text{A}$ |
|                                   | $I_{LOH2}$ | $V_{OUT} = 12$ V                             | Ports 12 to 14 (open drain)       |                         |      | 20           | $\mu\text{A}$ |
| Low-Level Output Leakage Current  | $I_{LOL}$  | $V_{OUT} = 0$ V                              |                                   |                         |      | -3           | $\mu\text{A}$ |
| Internal Pull-Up Resistor*1       | $R_L$      | Ports 12 to 14                               | $V_{DD} = 5 V \pm 10\%$           | 15                      | 40   | 70           | k $\Omega$    |
|                                   |            |                                              |                                   | 10                      |      | 80           | k $\Omega$    |
| Supply Current*1                  | $I_{DD1}$  | 4.19MHz crystal                              | $V_{DD} = 5 V \pm 10\%^{*2}$      |                         | 3    | 9            | mA            |
|                                   |            |                                              | $V_{DD} = 3 V \pm 10\%^{*3}$      |                         | 0.55 | 1.5          | mA            |
|                                   | $I_{DD2}$  | oscillator<br>C1 = C2 = 22pF                 | HALT                              | $V_{DD} = 5 V \pm 10\%$ | 600  | 1800         | $\mu\text{A}$ |
|                                   |            |                                              | mode                              | $V_{DD} = 3 \pm 10\%$   | 200  | 600          | $\mu\text{A}$ |
|                                   | $I_{DD3}$  | STOP mode, $V_{DD} = 3 V \pm 10\%$           |                                   |                         | 0.1  | 10           | $\mu\text{A}$ |

\*1: The current flowing into the internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included.

2: When the high-speed mode is set by setting the processor clock control register (PCC) to 0011.

3: When the low-speed mode is set by setting the PCC to 0000.

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 0\text{ V}$ )

| Parameter                | Symbol    | Conditions                                | MIN. | TYP. | MAX. | Unit |
|--------------------------|-----------|-------------------------------------------|------|------|------|------|
| Input Capacitance        | $C_{IN}$  | $f = 1\text{ MHz}$                        |      |      | 15   | pF   |
| Output Capacitance       | $C_{OUT}$ | Pins other than those measured are at 0 V |      |      | 15   | pF   |
| Input/Output Capacitance | $C_{IO}$  |                                           |      |      | 15   | pF   |

**COMPARATOR CHARACTERISTICS** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $6.0\text{ V}$ )

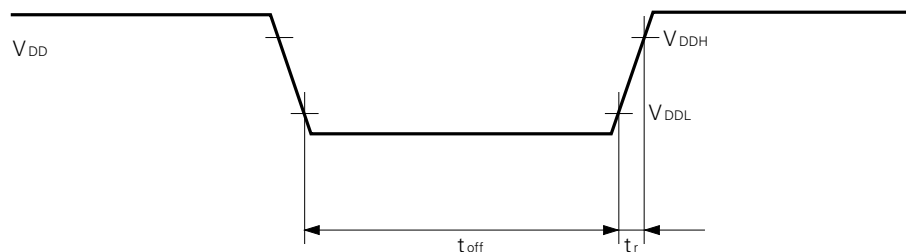
| Parameter                              | Symbol      | Conditions          | MIN. | TYP. | MAX.      | Unit |
|----------------------------------------|-------------|---------------------|------|------|-----------|------|
| Comparison Accuracy                    | $V_{ACOMP}$ |                     |      |      | $\pm 100$ | mV   |
| Threshold Voltage                      | $V_{TH}$    |                     | 0    |      | $V_{DD}$  | V    |
| PTH Input voltage                      | $V_{IPTH}$  |                     | 0    |      | $V_{DD}$  | V    |
| Comparator circuit current dissipation |             | PTHM7 is set to "1" |      | 1    |           | mA   |

**POWER-ON RESET CIRCUIT CHARACTERISTICS (MASK OPTION)** ( $T_a = -40$  to  $+85^\circ\text{C}$ )

| Parameter                                    | Symbol     | Conditions                     | MIN. | TYP. | MAX. | Unit          |
|----------------------------------------------|------------|--------------------------------|------|------|------|---------------|
| Power-On Reset High-Level Operating Voltage  | $V_{DDH}$  |                                | 4.5  |      | 6.0  | V             |
| Power-On Reset Low-Level Operating Voltage   | $V_{DDL}$  |                                | 0    |      | 0.2  | V             |
| Supply Voltage Rise Time                     | $t_r$      |                                | 10   |      | *1   | $\mu\text{s}$ |
| Supply Voltage Off Time                      | $t_{off}$  |                                | 1    |      |      | s             |
| Power-On Reset Circuit Current Dissipation*2 | $I_{DDPR}$ | $V_{DD} = 5\text{ V} \pm 10\%$ |      | 10   | 100  | $\mu\text{A}$ |
|                                              |            | $V_{DD} = 2.5\text{ V}$        |      | 2    | 20   | $\mu\text{A}$ |

\*1:  $2^{17}/f_{xx}$  (31.3 ms at  $f_{xx} = 4.19\text{ MHz}$ )

2: Current flowing when power-ON reset circuit or power-ON Flag is incorporated.

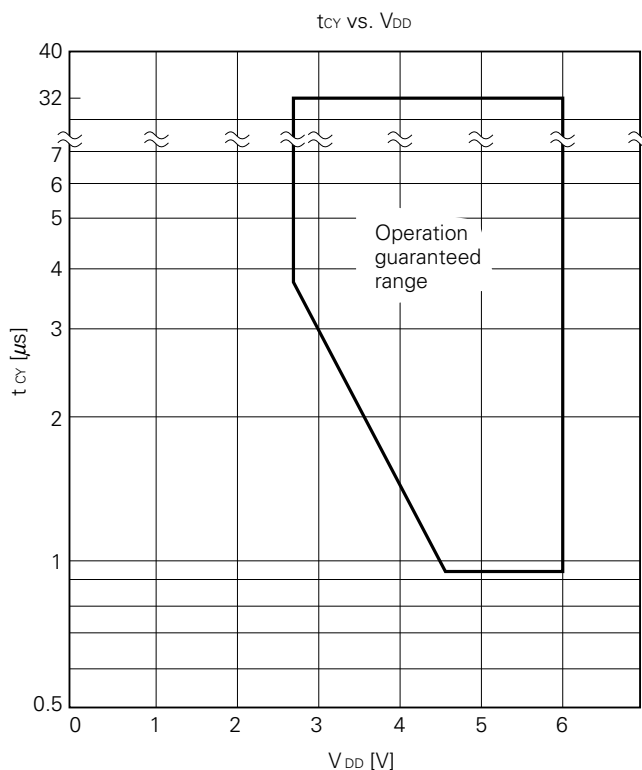


**Note:** Apply power gradually and smoothly.

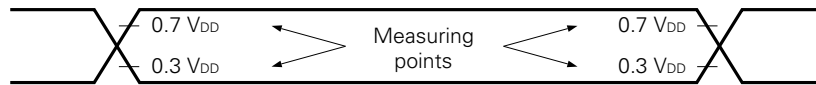
**AC CHARACTERISTICS** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $6.0$  V)

| Parameter                                                                             | Symbol                   | Conditions                | MIN.   | TYP.            | MAX. | Unit          |
|---------------------------------------------------------------------------------------|--------------------------|---------------------------|--------|-----------------|------|---------------|
| CPU Clock Cycle Time*<br>(Minimum Instruction<br>Execution Time = 1<br>Machine Cycle) | $t_{CY}$                 | $V_{DD} = 4.5$ to $6.0$ V | 0.95   |                 | 32   | $\mu\text{s}$ |
|                                                                                       |                          |                           | 3.8    |                 | 32   | $\mu\text{s}$ |
| TI0, TI1 Input Frequency                                                              | $f_{TI}$                 | $V_{DD} = 4.5$ to $6.0$ V | 0      |                 | 1    | MHz           |
|                                                                                       |                          |                           | 0      |                 | 275  | kHz           |
| TI0, TI1 Input High-/<br>Low-Level Width                                              | $t_{TIH}$ ,<br>$t_{TIL}$ | $V_{DD} = 4.5$ to $6.0$ V | 0.48   |                 |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | 1.8    |                 |      | $\mu\text{s}$ |
| $\overline{\text{SCK}}$ Cycle Time                                                    | $t_{KCY}$                | $V_{DD} = 4.5$ to $6.0$ V | Input  | 0.8             |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | Output | 0.95            |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | Input  | 3.2             |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | Output | 3.8             |      | $\mu\text{s}$ |
| $\overline{\text{SCK}}$ High-/Low-Level<br>Width                                      | $t_{KH}$ ,<br>$t_{KL}$   | $V_{DD} = 4.5$ to $6.0$ V | Input  | 0.4             |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | Output | $t_{KCY}/2-50$  |      | ns            |
|                                                                                       |                          |                           | Input  | 1.6             |      | $\mu\text{s}$ |
|                                                                                       |                          |                           | Output | $t_{KCY}/2-150$ |      | ns            |
| SI Setup Time<br>(vs. $\overline{\text{SCK}}\uparrow$ )                               | $t_{SIK}$                |                           | 100    |                 |      | ns            |
| SI Hold Time<br>(vs. $\overline{\text{SCK}}\uparrow$ )                                | $t_{KSI}$                |                           | 400    |                 |      | ns            |
| $\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ Output<br>delay Time         | $t_{KSO}$                | $V_{DD} = 4.5$ to $6.0$ V |        |                 | 300  | ns            |
|                                                                                       |                          |                           |        |                 | 1000 | ns            |
| INT0 to 4                                                                             | $t_{INTH}$ ,             |                           | 5      |                 |      | $\mu\text{s}$ |
| High-/Low-Level Width                                                                 | $t_{INTL}$               |                           |        |                 |      |               |
| $\overline{\text{RESET}}$ Low-Level Width                                             | $t_{RSL}$                |                           | 5      |                 |      | $\mu\text{s}$ |

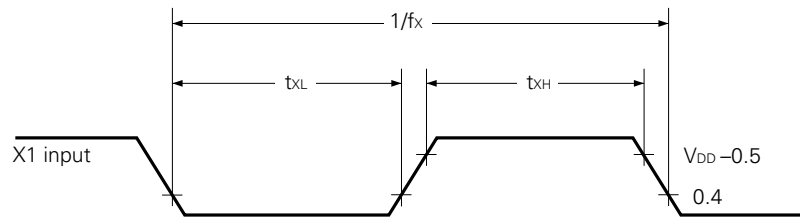
\*: The cycle time of the CPU clock ( $\Phi$ ) is determined by the input frequency of the ceramic or crystal oscillator circuit and the set value of the processor clock control register. The  $t_{CY}$  vs.  $V_{DD}$  characteristics are as shown on the right.



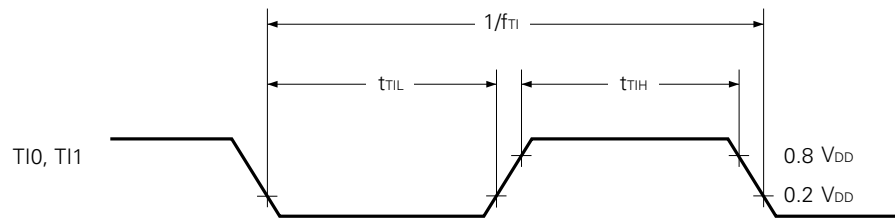
**AC TIMING MEASURING POINTS** (excluding Ports 0, 1, TI0, TI1, X1, X2, and RESET)



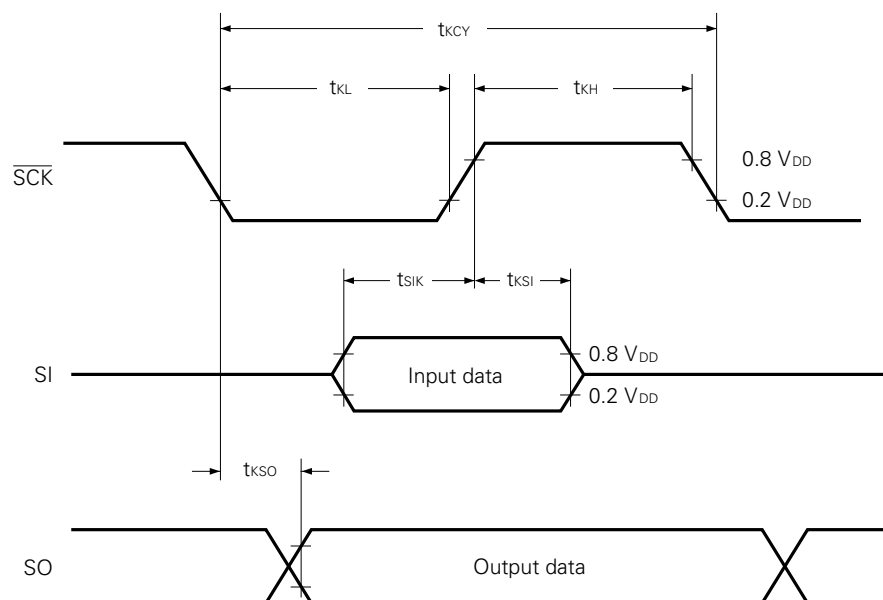
**CLOCK TIMING**



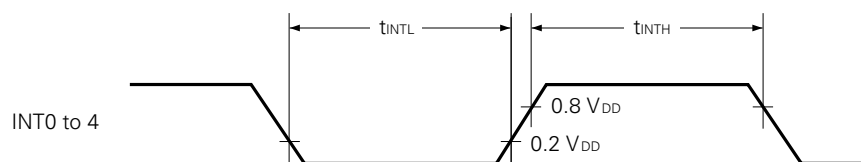
**TI TIMING**



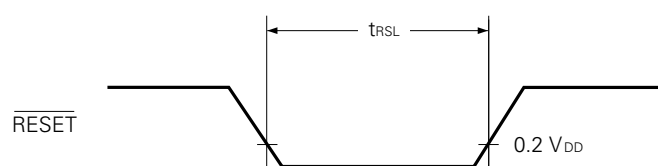
# SERIAL TRANSFER TIMING



# INTERRUPT INPUT TIMING



# RESET INPUT TIMING



**LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE**(T<sub>a</sub> = -40 to +85°C)

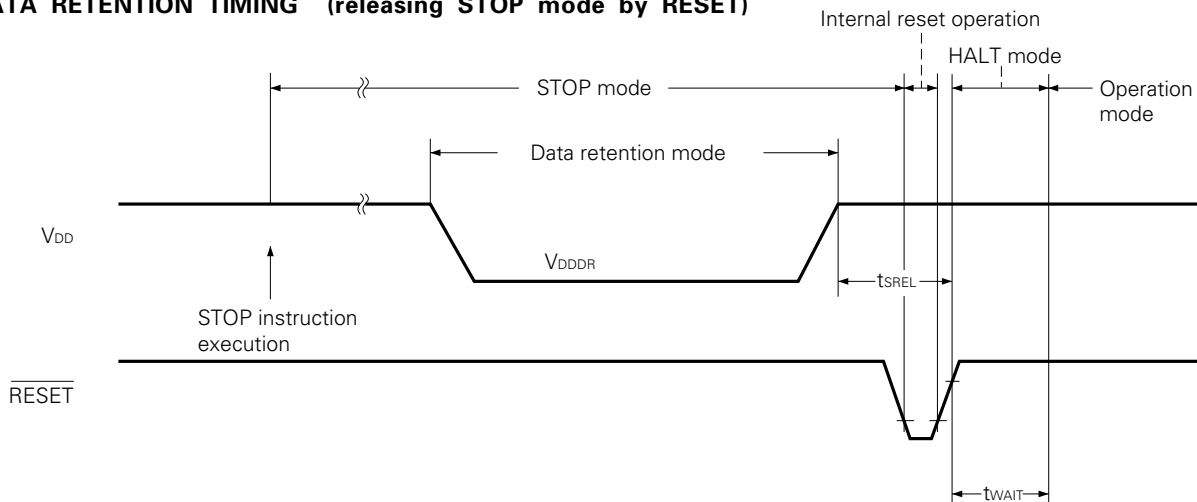
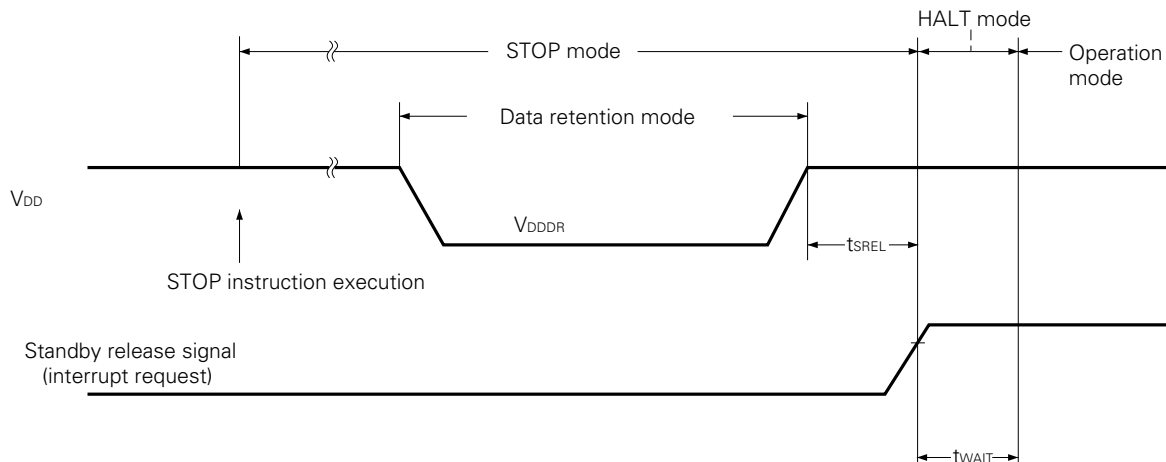
| Parameter                             | Symbol            | Conditions                            | MIN. | TYP.                            | MAX. | Unit |
|---------------------------------------|-------------------|---------------------------------------|------|---------------------------------|------|------|
| Data Retention Supply Voltage         | V <sub>DDDR</sub> |                                       | 2.0  |                                 | 6.0  | V    |
| Data Retention Supply Current*1       | I <sub>DDDR</sub> | V <sub>DDDR</sub> = 2.0 V             |      | 0.1                             | 10   | μA   |
| Release Signal Set Time               | t <sub>SREL</sub> |                                       | 0    |                                 |      | μs   |
| Oscillation Stabilization Wait Time*2 | t <sub>WAIT</sub> | Released by $\overline{\text{RESET}}$ |      | 2 <sup>17</sup> /f <sub>x</sub> |      | ms   |
|                                       |                   | Released by interrupt request         |      | *3                              |      | ms   |

\*1: The current flowing through internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included

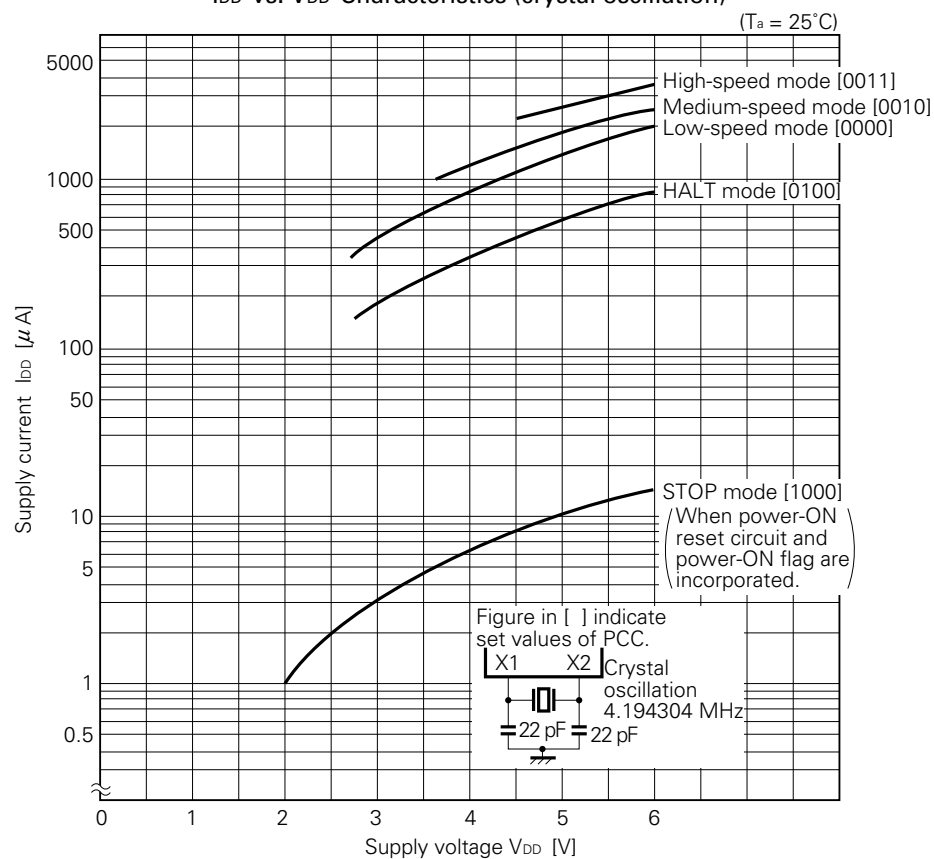
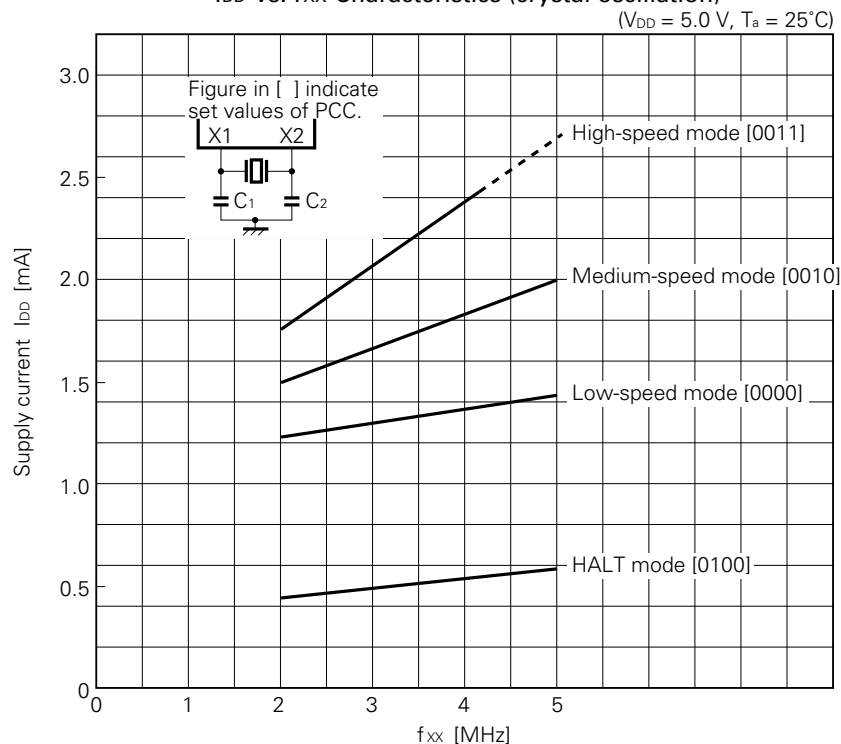
2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

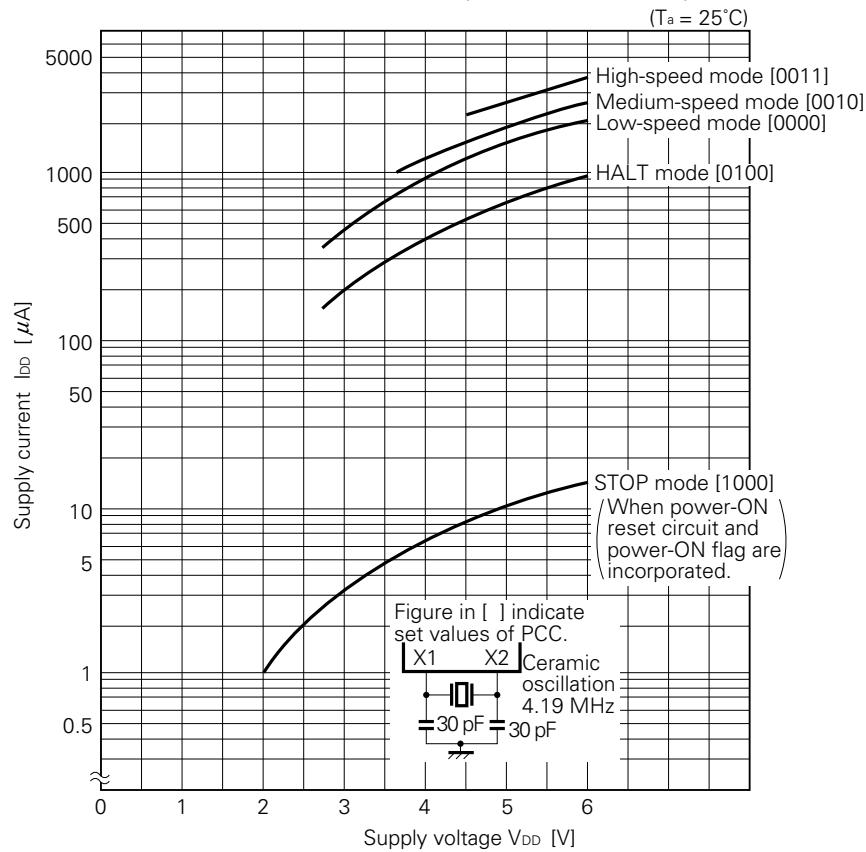
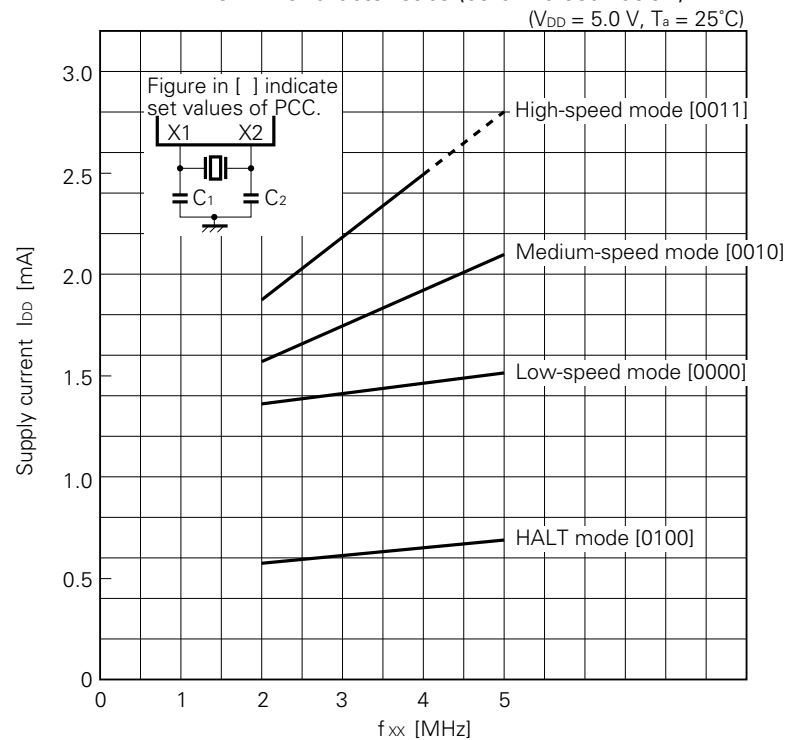
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

| BTM3 | BTM2 | BTM1 | BTM0 | Wait time ( ): f <sub>xx</sub> = 4.19 MHz          |
|------|------|------|------|----------------------------------------------------|
| –    | 0    | 0    | 0    | 2 <sup>20</sup> /f <sub>xx</sub> (approx. 250 ms)  |
| –    | 0    | 1    | 1    | 2 <sup>17</sup> /f <sub>xx</sub> (approx. 31.3 ms) |
| –    | 1    | 0    | 1    | 2 <sup>15</sup> /f <sub>xx</sub> (approx. 7.82 ms) |
| –    | 1    | 1    | 1    | 2 <sup>13</sup> /f <sub>xx</sub> (approx. 1.95 ms) |

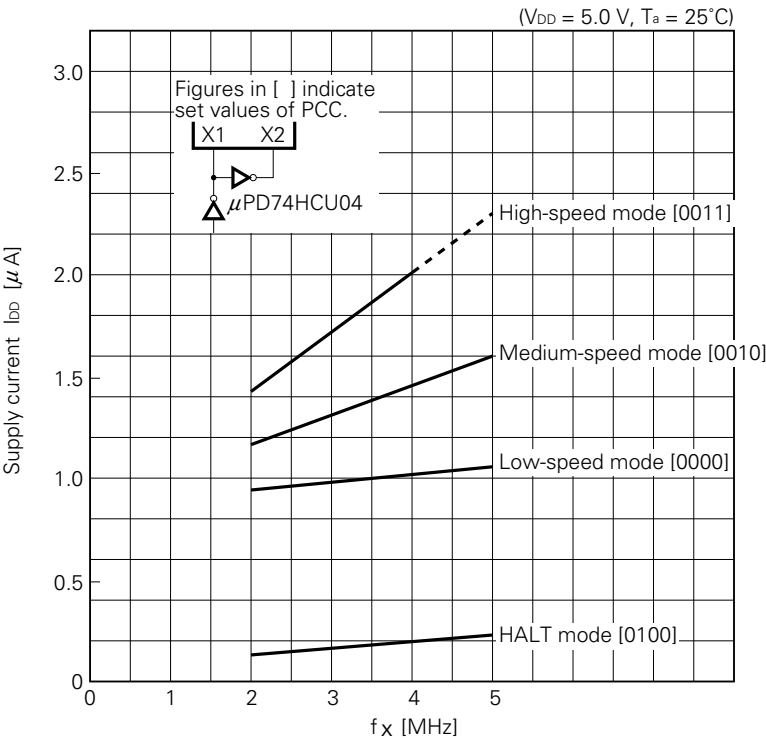
**DATA RETENTION TIMING (releasing STOP mode by  $\overline{\text{RESET}}$ )****DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)**

## 13. CHARACTERISTIC DATA

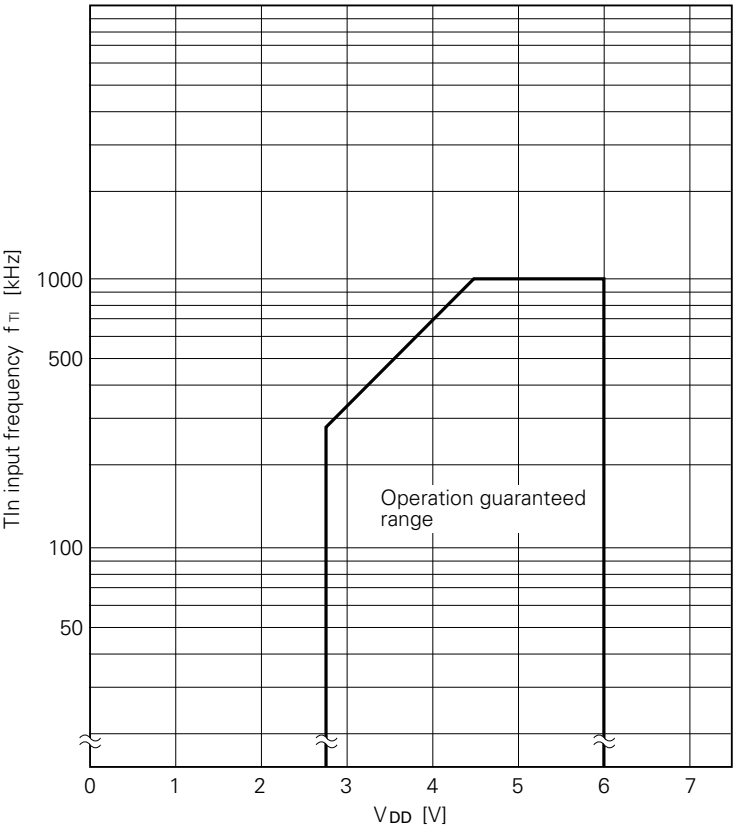
I<sub>DD</sub> vs. V<sub>DD</sub> Characteristics (crystal oscillation)I<sub>DD</sub> vs. f<sub>xx</sub> Characteristics (crystal oscillation)

$I_{DD}$  vs.  $V_{DD}$  Characteristics (ceramic oscillation) $I_{DD}$  vs.  $f_{xx}$  Characteristics (ceramic oscillation)

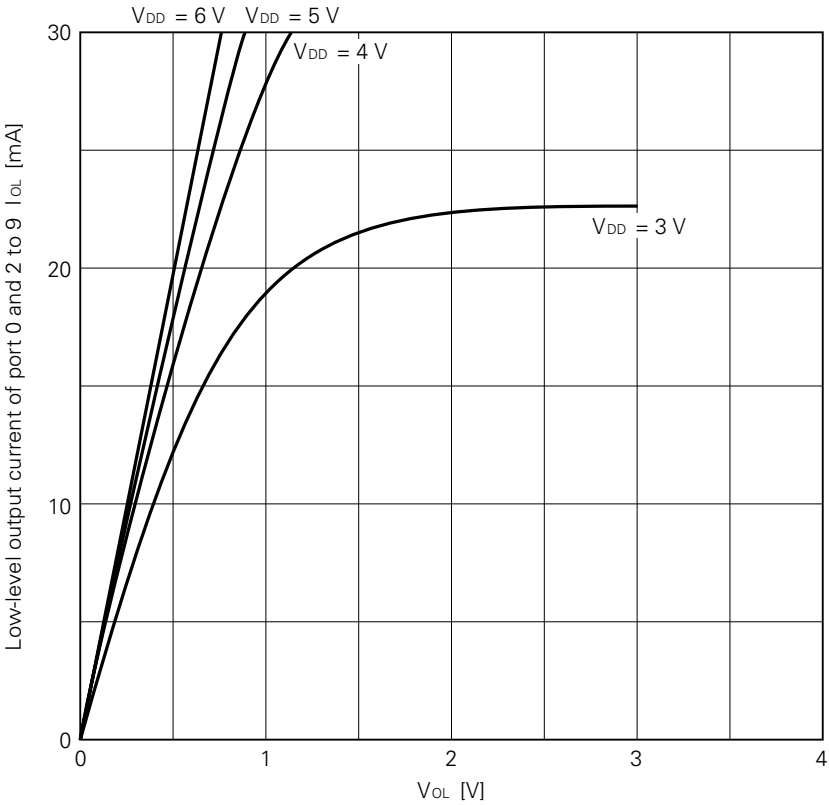
$I_{DD}$  vs.  $f_X$  Characteristics (external clock)



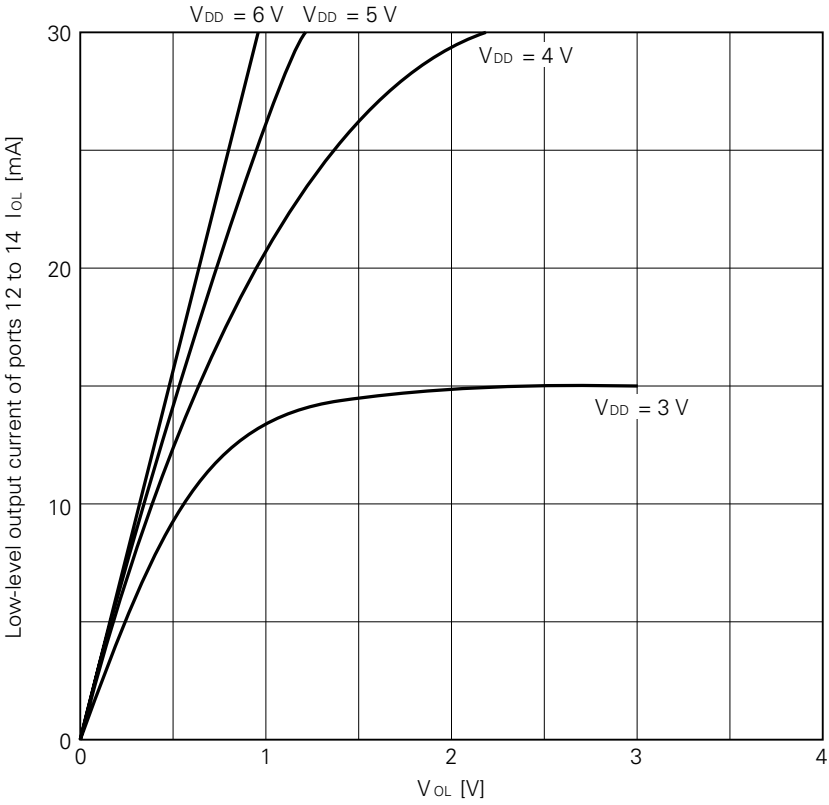
$f_{TI}$  vs.  $V_{DD}$  Characteristics

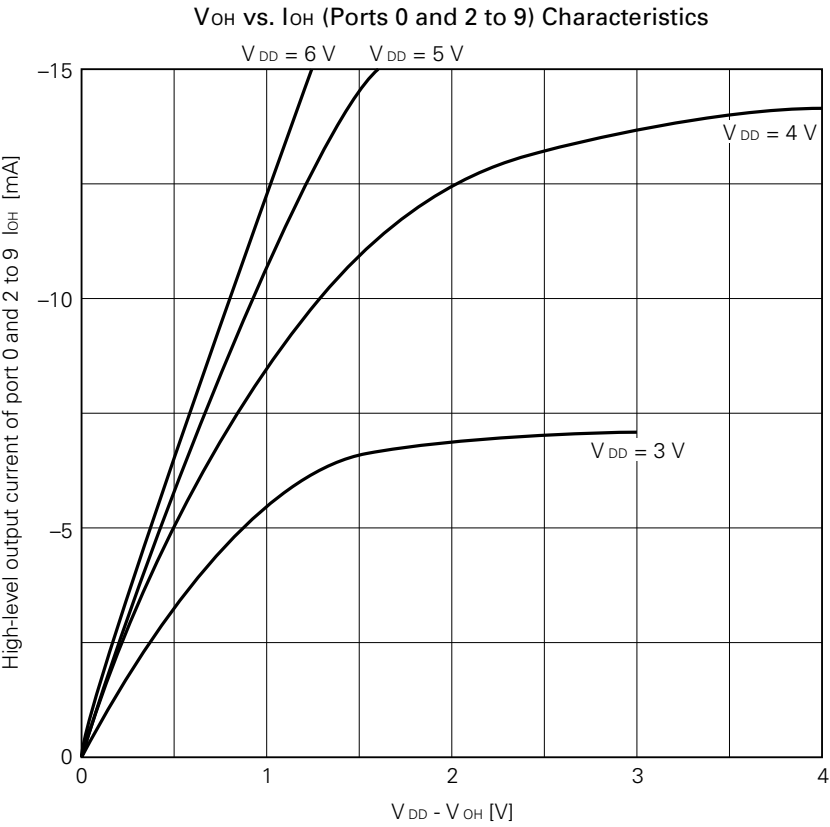


V<sub>OL</sub> vs. I<sub>OL</sub> (Ports 0 and 2 to 9) Characteristics



V<sub>OL</sub> vs. I<sub>OL</sub> (Ports 12 to 14) Characteristics

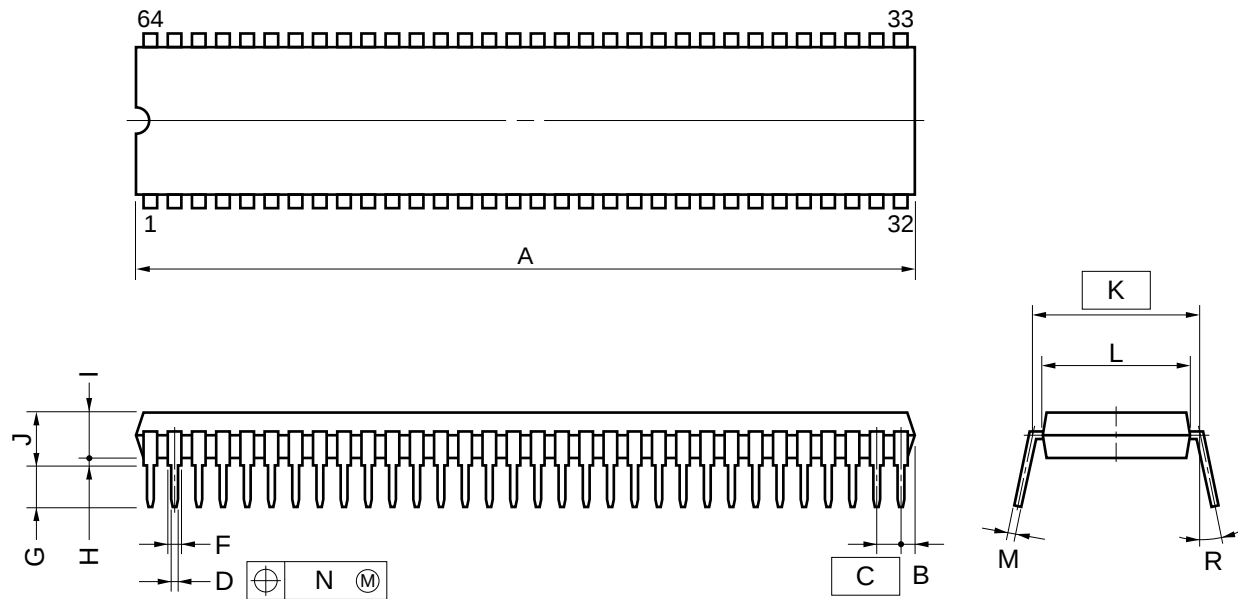




**Remarks:** Unless otherwise specified, all the characteristic data shown are reference values.

14. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)

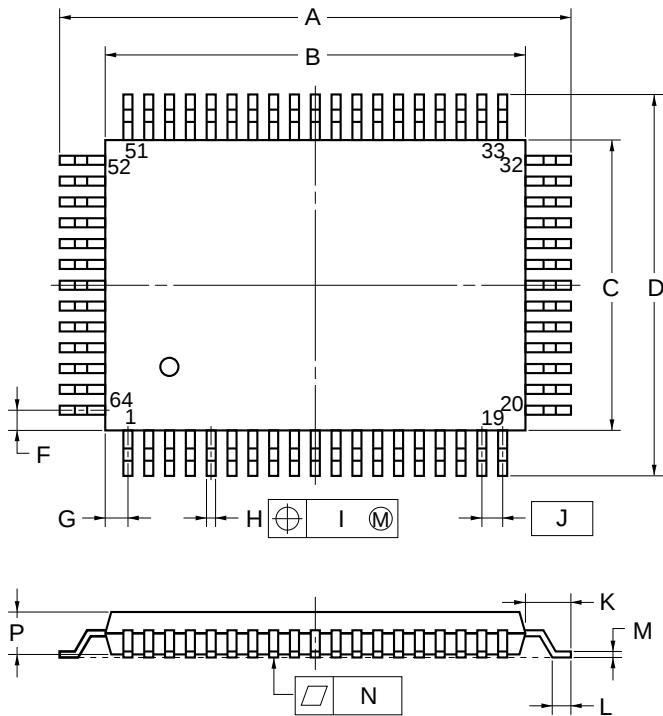


- NOTE**
- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
  - 2) Item "K" to center of leads when formed parallel.

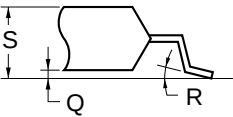
| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 58.68 MAX.                             | 2.311 MAX.                                |
| B    | 1.78 MAX.                              | 0.070 MAX.                                |
| C    | 1.778 (T.P.)                           | 0.070 (T.P.)                              |
| D    | 0.50±0.10                              | 0.020 <sup>+0.004</sup> <sub>-0.005</sub> |
| F    | 0.9 MIN.                               | 0.035 MIN.                                |
| G    | 3.2±0.3                                | 0.126±0.012                               |
| H    | 0.51 MIN.                              | 0.020 MIN.                                |
| I    | 4.31 MAX.                              | 0.170 MAX.                                |
| J    | 5.08 MAX.                              | 0.200 MAX.                                |
| K    | 19.05 (T.P.)                           | 0.750 (T.P.)                              |
| L    | 17.0                                   | 0.669                                     |
| M    | 0.25 <sup>+0.10</sup> <sub>-0.05</sub> | 0.010 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.17                                   | 0.007                                     |
| R    | 0~15°                                  | 0~15°                                     |

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



detail of lead end

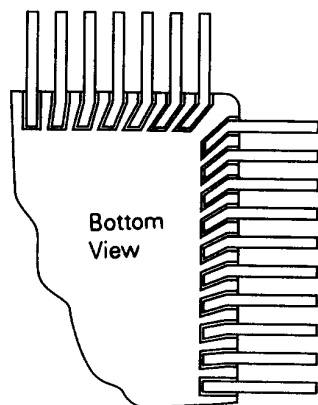
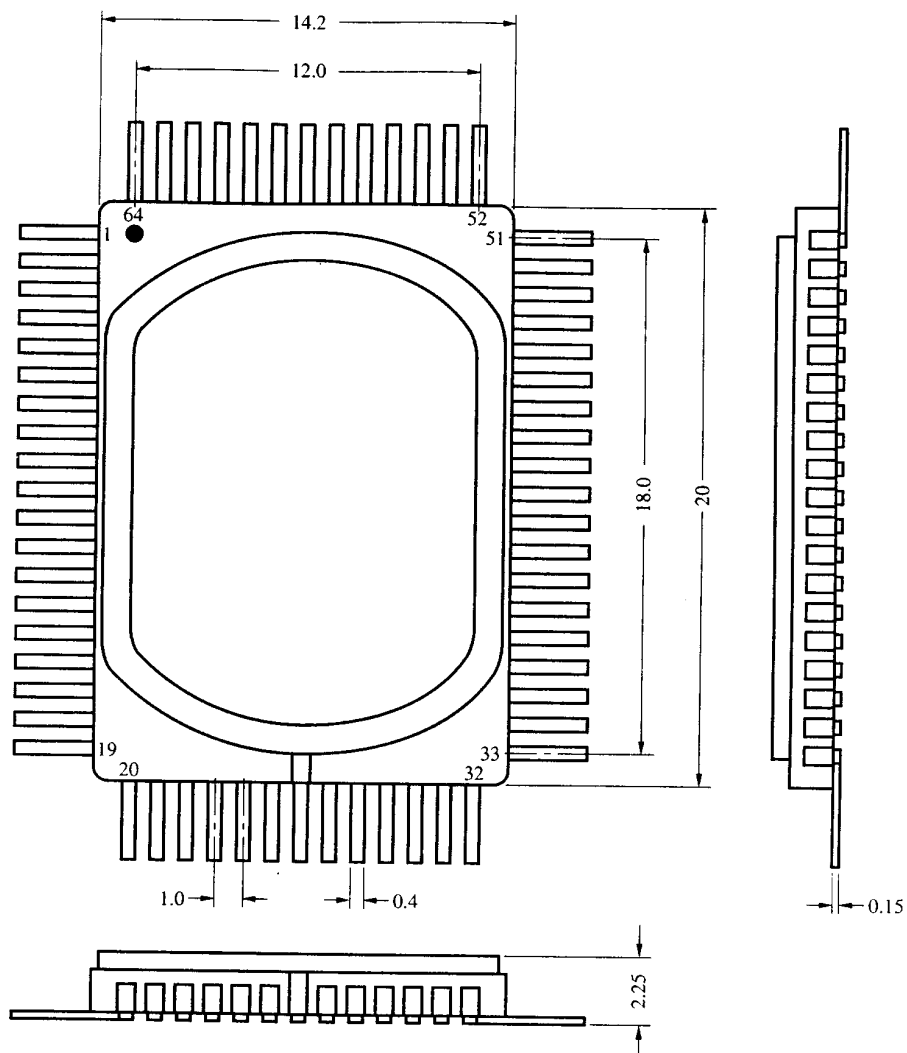


**NOTE**  
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 23.6±0.4                               | 0.929±0.016                               |
| B    | 20.0±0.2                               | 0.795 <sup>+0.008</sup> <sub>-0.009</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 17.6±0.4                               | 0.693±0.016                               |
| F    | 1.0                                    | 0.039                                     |
| G    | 1.0                                    | 0.039                                     |
| H    | 0.40±0.10                              | 0.016 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.20                                   | 0.008                                     |
| J    | 1.0 (T.P.)                             | 0.039 (T.P.)                              |
| K    | 1.8±0.2                                | 0.071 <sup>+0.008</sup> <sub>-0.009</sub> |
| L    | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 2.7                                    | 0.106                                     |
| Q    | 0.1±0.1                                | 0.004±0.004                               |
| R    | 5°±5°                                  | 5°±5°                                     |
| S    | 3.0 MAX.                               | 0.119 MAX.                                |

P64GF-100-3B8,3BE,3BR-2

ES 64-Pin Ceramic QFP (Reference) (unit in mm)



- Note 1.** The metal cap is connected to pin 26, at the V<sub>SS</sub> (GND) level.
- 2.** The leads are molded diagonally at the bottom.
- 3.** The lead lengths are not specified, as the lead cutting process is not controlled.

## 15. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75104, 75106, and 75108 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

For other soldering methods and conditions, please consult NEC.

**Table 15-1 Soldering Conditions of Surface Mount Type**

μPD75108GF - xxx - 3BE: 64-pin plastic QFP (14 x 20 mm)

| Soldering Method    | Soldering Conditions                                                                                                                                 | Symbol for Recommended Condition |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Infrared Reflow     | Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1                                                              | IR30-00-1                        |
| VPS                 | Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1                                                              | VP15-00-1                        |
| Wave Soldering      | Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature) | WS60-00-1                        |
| Pin Partial Heating | Pin temperature: 300°C max., time: 3 seconds max. (per side)                                                                                         | —                                |

**Caution:** Do not use two or more soldering methods in combination (except the pin partial heating method).

**Table 15-2 Soldering Conditions of Through-Hole Type**

μPD75108CW - xxx : 64-pin plastic shrink DIP (750 mil)

| Soldering Method                    | Soldering Conditions                                          |
|-------------------------------------|---------------------------------------------------------------|
| Wave Soldering (Only for lead part) | Soldering bath temperature: 260°C max., Time: 10 seconds max. |
| Pin Partial Heating                 | Pin temperature: 260°C max., Time: 10 seconds max.            |

**Caution:** The wave soldering must be performed at the lead part only. Note that the solder must not be directly contacted to the package body.

# APPENDIX A. FUNCTIONAL DIFFERENCES AMONG PRODUCTS IN $\mu$ PD751XX SERIES

| Item                               | μPD75104                                                                       | μPD75106                                                                                                     | μPD75108                                          | μPD75112                                                                   | μPD75116                 | μPD75104A                                                                                                                                             | μPD75108A                                                                  | μPD75108F                                                                                                    | μPD75112F                | μPD75116F                | μPD75P108B                                                                                                           | μPD75P116                                                                      |
|------------------------------------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| ROM Configuration                  | Mask ROM                                                                       |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            |                                                                                                              |                          |                          | PROM                                                                                                                 |                                                                                |
| ROM (Bits)                         | 000H-FFFH<br>4096 × 8                                                          | 0000H-177FH<br>6016 × 8                                                                                      | 0000H-1F7FH<br>8064 × 8                           | 0000H-2F7FH<br>12160 × 8                                                   | 0000H-3F7FH<br>16256 × 8 | 000H-FFFH<br>4096 × 8                                                                                                                                 | 0000H-1F7FH<br>8064 × 8                                                    | 0000H-1F7FH<br>8064 × 8                                                                                      | 0000H-2F7FH<br>12160 × 8 | 0000H-3F7FH<br>16256 × 8 | 0000H-1F7FH<br>8064 × 8                                                                                              | 0000H-3F7FH<br>16256 × 8                                                       |
| RAM (Bits)                         | 320 × 4<br>(Bank 0: 256 × 4)<br>(Bank 1: 64 × 4)                               |                                                                                                              | 512 × 4<br>(Bank 0: 256 × 4)<br>(Bank 1: 256 × 4) |                                                                            |                          | 320 × 4<br>(Bank 0: 256 × 4)<br>(Bank 1: 64 × 4)                                                                                                      | 512 × 4<br>(Bank 0: 256 × 4)<br>(Bank 1: 256 × 4)                          | 512 × 4<br>(Bank 0: 256 × 4)<br>(Bank 1: 256 × 4)                                                            |                          |                          |                                                                                                                      |                                                                                |
| Instruction Set                    | High-end (Only μPD75104 and 75104A are not provided with BR!addr instruction.) |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | High end                                                                                                     |                          |                          |                                                                                                                      |                                                                                |
| I/O Lines                          | Total                                                                          | 58                                                                                                           |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            |                                                                                                              |                          |                          |                                                                                                                      |                                                                                |
|                                    | I/O                                                                            | • CMOS I/O: 32<br>• +12 V open-drain output: 12<br>(pull-up resistor as mask option)<br>LED direct drive: 44 |                                                   |                                                                            |                          | • CMOS I/O: 32<br>(pull-up resistor as mask option: 24)<br>• +12 V open-drain output: 12<br>(pull-up resistor as mask option)<br>LED direct drive: 44 |                                                                            | • CMOS I/O: 32<br>• +10 V open-drain output: 12<br>(pull-up resistor as mask option)<br>LED direct drive: 44 |                          |                          | • CMOS I/O: 32<br>• +12 V open-drain output: 12<br>LED direct drive: 44                                              |                                                                                |
|                                    | Input                                                                          | • CMOS input: 10<br>• Comparator input: 4                                                                    |                                                   |                                                                            |                          | • CMOS input: 10<br>(pull-up resistor as mask option: 4)<br>• Comparator input: 44                                                                    |                                                                            | • CMOS input: 10<br>• Comparator input: 4                                                                    |                          |                          |                                                                                                                      |                                                                                |
| Power-ON Reset Circuit             | Provided (mask option)                                                         |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | None                                                                                                         |                          |                          |                                                                                                                      |                                                                                |
| Power-ON Flag                      |                                                                                |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            |                                                                                                              |                          |                          |                                                                                                                      |                                                                                |
| Operating Voltage Range            | 2.7 to 6.0 V                                                                   |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | 2.7 to 5.0 V (T <sub>a</sub> = -40 to +50°C)<br>2.8 to 5.0 V (T <sub>a</sub> = -40 to +60°C)                 |                          |                          | 2.7 to 6.0 V                                                                                                         | 5 V ± 10%                                                                      |
| Minimum Instruction Execution Time | 0.95 μs (at 5 V)<br>3 μs (at 3 V)                                              |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | 0.95 μs (at 4.5 V to 5.0 V)                                                                                  |                          |                          | 0.95 μs (at 5 V)<br>3 μs (at 3 V)                                                                                    | 0.95 μs (at 5 V)                                                               |
|                                    |                                                                                |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | 1.91 μs (at 3 V)                                                                                             |                          |                          |                                                                                                                      |                                                                                |
| Pin Connections                    | Depends on package                                                             |                                                                                                              |                                                   |                                                                            |                          |                                                                                                                                                       |                                                                            | Depends on package. Only μPD75P108, and 75P116 are provided with V <sub>PP</sub> pin.                        |                          |                          |                                                                                                                      |                                                                                |
| Package                            | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 × 20 mm)     |                                                                                                              |                                                   | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 × 20 mm) |                          | • 64-pin plastic QFP (14 × 14 mm)                                                                                                                     | • 64-pin plastic QFP (14 × 14 mm)<br><br>• 64-pin plastic QFP (14 × 14 mm) | • 64-pin plastic QFP (14 × 20 mm)                                                                            |                          |                          | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin ceramic shrink DIP (w/window)<br>• 64-pin plastic QFP (14 × 20 mm) | • 64-pin plastic shrink DIP (750 mil)<br><br>• 64-pin plastic QFP (14 × 20 mm) |

**APPENDIX B. DEVELOPMENT TOOLS**

The following development support tools are readily available to support development of systems using  $\mu$ PD75108:

|          |                                        |                                                                                                  |
|----------|----------------------------------------|--------------------------------------------------------------------------------------------------|
| Hardware | IE-75000-R* <sup>1</sup><br>IE-75001-R | In-circuit emulator for 75X series                                                               |
|          | IE-75000-R-EM* <sup>2</sup>            | Emulation board for IE-75000-R and IE-75001-R                                                    |
|          | EP-75108CW-R                           | Emulation probe for $\mu$ PD75108CW                                                              |
|          | EP-75108GF-R<br>EV-9200G-64            | Emulation probe for $\mu$ PD75108GF. It is provided with a 64-pin conversion socket, EV-9200G-64 |
|          | PG-1500                                | PROM programmer                                                                                  |
|          | PA-75P108CW                            | PROM programmer adapter for $\mu$ PD75P108BCW and 75P108BDW. It is connected to PG-1500.         |
|          | PA-75P116GF                            | Programmer adapter for $\mu$ PD75P108BGF. It is connected to PG-1500.                            |
| Software | IE Control Program                     | Host machine                                                                                     |
|          | PG-1500 Controller                     | PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A* <sup>3</sup> )                                    |
|          | RA75X Relocatable Assembler            | IBM PC/AT™ (PC DOS™ Ver.3.1)                                                                     |

\*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

**Remarks:** For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

**APPENDIX C. RELATED DOCUMENTS**

## GENERAL NOTES ON CMOS DEVICES

### ① STATIC ELECTRICITY (ALL MOS DEVICES)

**Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.**

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

### ② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

**Fix the input level of CMOS devices.**

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to  $V_{DD}$  or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

### ③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

**The initial status of MOS devices is undefined upon power application.**

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

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