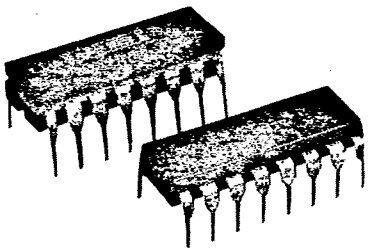
BURR-BROWN®



HI-508A
HI-509A

Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- ESD RESISTANT
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

DESCRIPTION

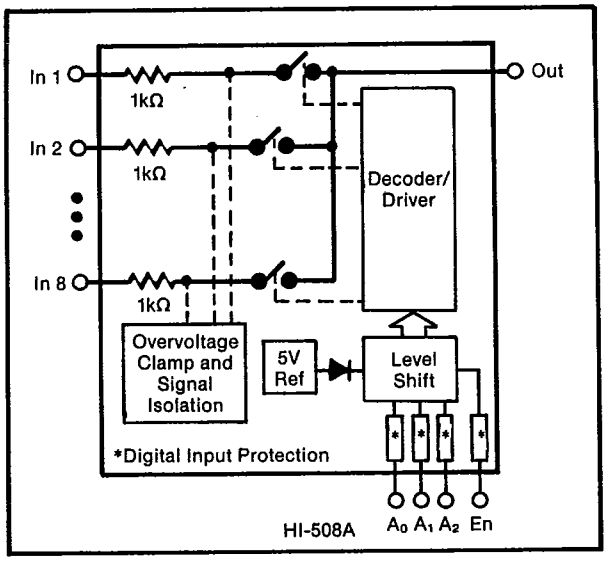
The HI-508A is an 8-channel single-ended analog multiplexer and the HI-509A is a 4-channel differential multiplexer.

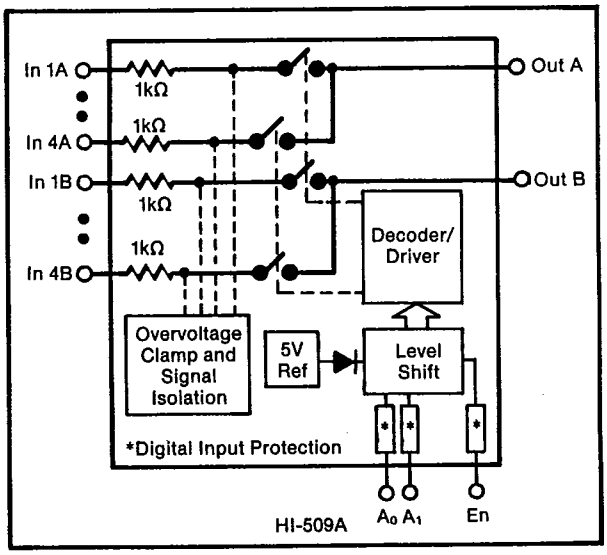
The HI-508A and HI-509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the HI-508A and HI-509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The HI-508A and HI-509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic DIP or plastic DIP. Commercial (0°C to +75°C) and military (−55°C to +125°C) versions are available.

FUNCTIONAL DIAGRAMS





International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

Printed in U.S.A. February, 1988

SPECIFICATIONS

ELECTRICAL

Supplies = +15V, −15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V unless otherwise specified.

PARAMETER	TEMP	HI-508/HI-509A-2 MIN	HI-508/HI-509A-2 TYP	HI-508/HI-509A-2 MAX	HI-508/HI-509A-5 MIN	HI-508/HI-509A-5 TYP	HI-508/HI-509A-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
R_{ON}, On Resistance[1]	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_D (OFF) with Input Overvoltage Applied[2]	+25°C		4.0			4.0		nA
	Full			2.0				µA
I_D (ON), On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF} Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold[3]	Full	4.0			4.0			V
I_A, Input Leakage Current (High or Low)[4]	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time: (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"OFF Isolation"[5]	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance: HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current[6]	Full		0.5	2.0		0.5	2.0	mA
I−, Current[6]	Full		0.02	1.0		0.02	1.0	mA

NOTES: (1) $V_{OUT} = \pm 10V$, $I_{OUT} = -100\mu A$. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended. (4) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (5) $V_{EN} = 0.8V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 7Vrms$, f = 100kHz. Worst-case isolation occurs on channel 4 due to proximity of the output pins. (6) V_{EN}, $V_A = 0V$ or 4.0V.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS[1]

Voltage between supply pins 44V
V+ to ground 22V
V− to ground 25V
Digital input overvoltage V_{EN}, V_A: V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (−) ..... −4V
or 20mA, whichever occurs first.
Analog input overvoltage V_S: V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (−) ..... −20V
Continuous current, S or D 20mA
Peak current, S or D (pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 1.28W
Operating temperature range: HI-508A/509A-2 ... −55°C to +125°C
HI-508A/509A-5 ..... 0°C to +75°C
Storage temperature range ..... −65°C to +150°C
*Derate 12.8mW/°C above $T_A = +75°C$.

NOTE: (1). Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

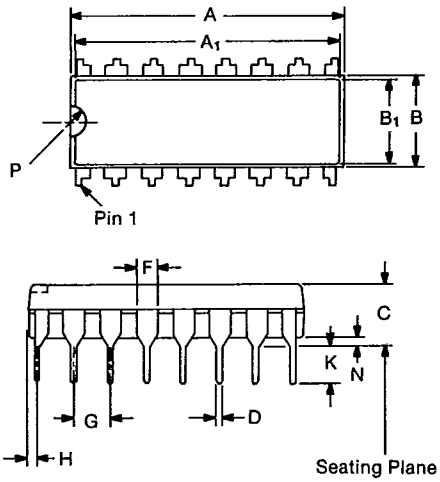
PRICES

MODEL	1-24	25-99	100+
HI3-0508A-5	$10.45	$ 8.20	$ 7.35
HI1-0508A-5	11.15	9.20	8.25
HI1-0508A-2	25.15	20.85	17.35
HI3-0509A-5	10.45	8.20	7.35
HI1-0509A-5	11.15	9.20	8.25
HI1-0509A-2	25.15	20.85	17.35

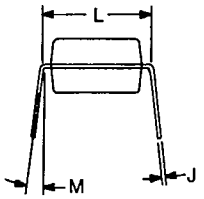
ORDERING INFORMATION

MODEL	DESCRIPTION	TEMP RANGE	PACKAGE
HI3-0508A-5	8-Channel Single-Ended	0°C to +75°C	16-Pin Plastic DIP
HI1-0508A-5	8-Channel Single-Ended	0°C to +75°C	16-Pin CERDIP
HI1-0508A-2	8-Channel Single-Ended	−55°C to +125°C	16-Pin CERDIP
HI3-0509A-5	4-Channel Differential	0°C to +75°C	16-Pin Plastic DIP
HI1-0509A-5	4-Channel Differential	0°C to +75°C	16-Pin CERDIP
HI1-0509A-2	4-Channel Differential	−55°C to +125°C	16-Pin CERDIP

MECHANICAL



Plastic DIP Package

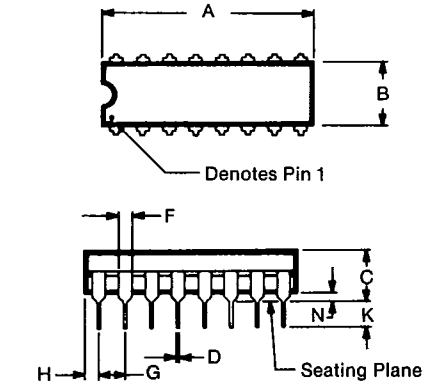


NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

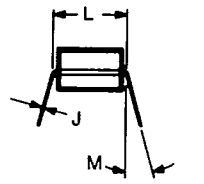
PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CASE: Plastic

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.02	0.05	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27



Ceramic DIP Package

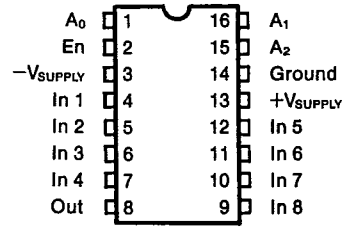


NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC		7.62 BASIC	
M	—	15°	—	15°
N	.020	.050	0.51	1.27

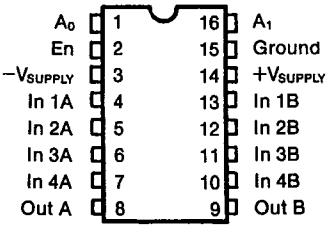
PIN CONFIGURATIONS

Top View



HI1-508A (ceramic)
HI3-508A (plastic)

Top View



HI1-509A (ceramic)
HI3-509A (plastic)

DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resisitive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.001% loading error and 10kΩ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20μV if a 1kΩ source is used. In general, for the HI-508A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differenital impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differenital errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications. Refer to Figure 2.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load Impedances, differenital and common-mode, should be $10^{10}\Omega$ or higher.

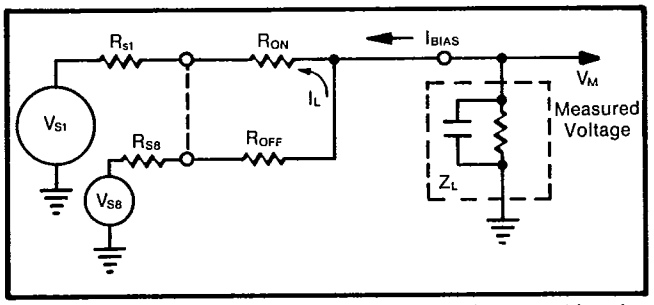


FIGURE 1. HI-508A DC Accuracy Equivalent Circuit.

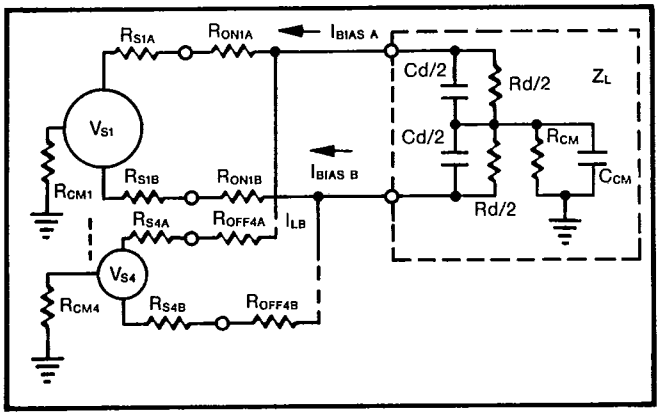


FIGURE 2. HI-509A DC Accuracy Equivalent Circuit.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the HI-509A is used for multiplexing high-level signals of ±1V to ±10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients, seen at the source and load, decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\,dt$$

where $i = C\,(dV/dt)$ of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

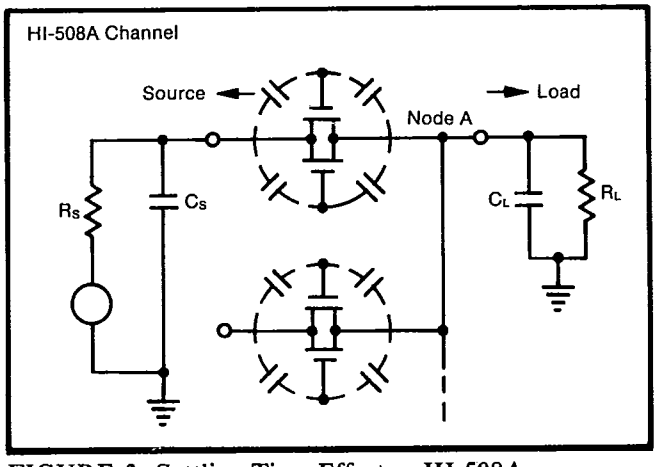


FIGURE 3. Settling Time Effects—HI-508A.

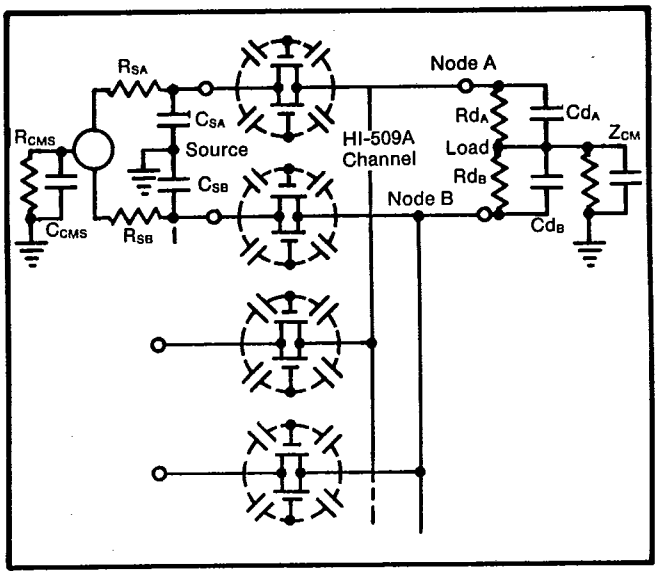


FIGURE 4. Settling and Common-Mode Effects—HI-509A.

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feethrough from the three (HI-509A) or seven (HI-508A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1kHz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (HI-509A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the HI-509A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the HI-509A and Burr-Brown's INA110 Instrumentation Amplifier is 110dB at DC to 10Hz (G = 100) with a 6dB/octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model INA110 Instrumentation Amplifier connected for gains of 10, 100, and 500.

Factors which will degrade multiplexer and system DC CMR are:

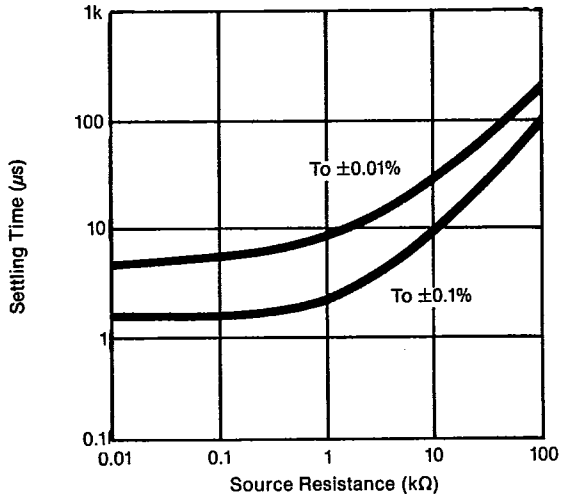
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer-to-amplifier wiring must be minimized. Use twisted-shielded-pair signal lines wherever possible.

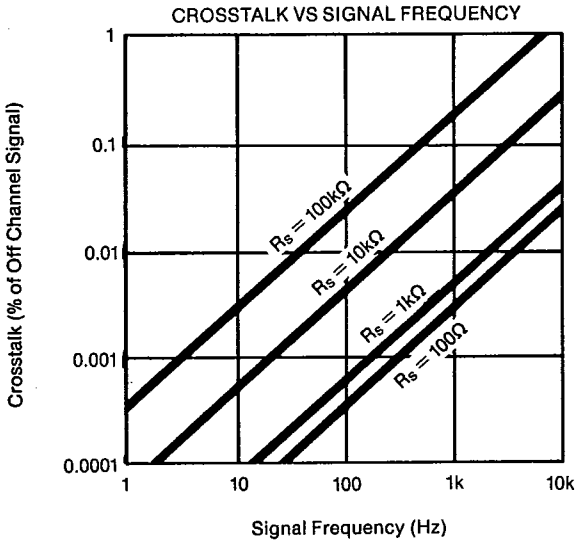
TYPICAL DYNAMIC PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

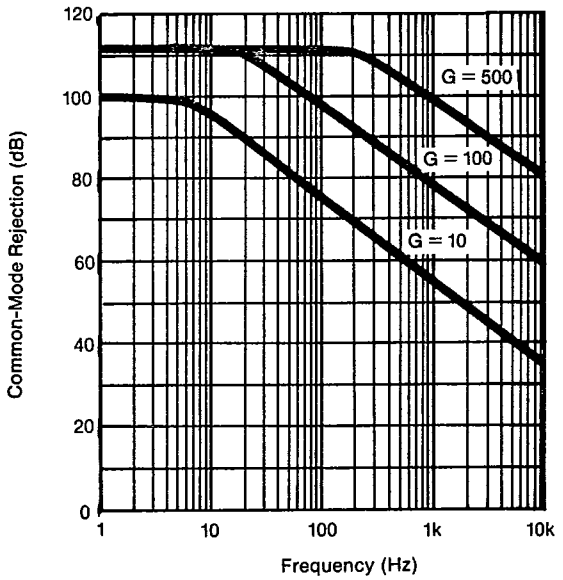
SETTLING TIME VS SOURCE RESISTANCE FOR 20V STEP CHANGE



CROSSTALK VS SIGNAL FREQUENCY



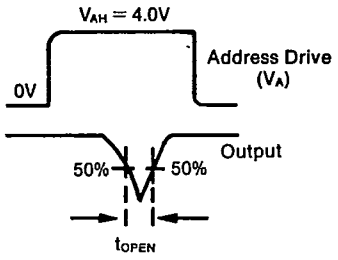
COMBINED CMR VS FREQUENCY HI-509A AND INA110

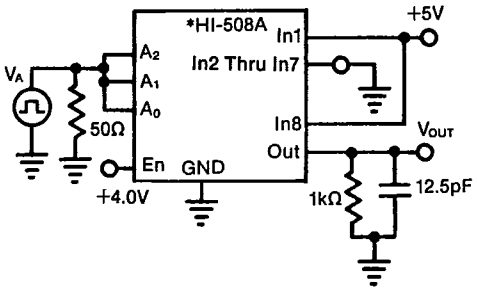


SWITCHING WAVEFORMS

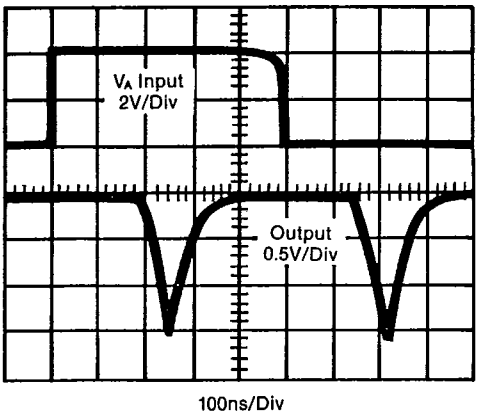
Typical at +25°C unless otherwise noted.

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

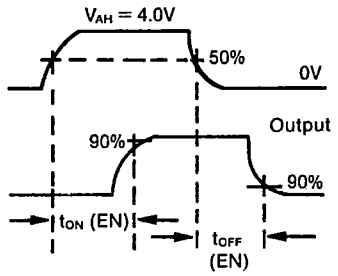


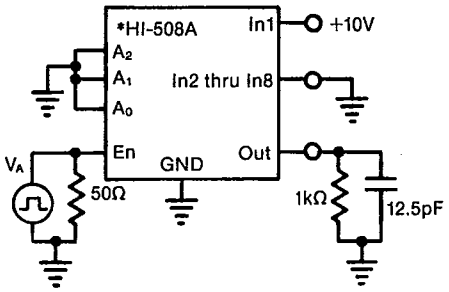


*Similar connection for HI-509A.

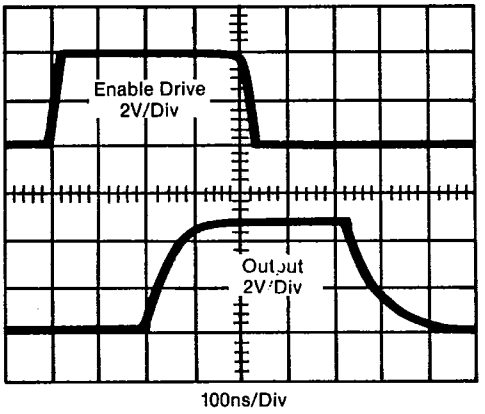


ENABLE DELAY (t_{ON} ($\overline{EN}$), t_{OFF} (EN))





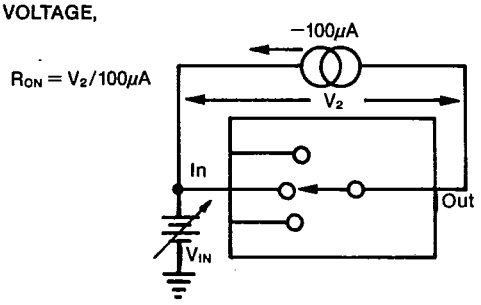
*Similar connection for HI-509A.



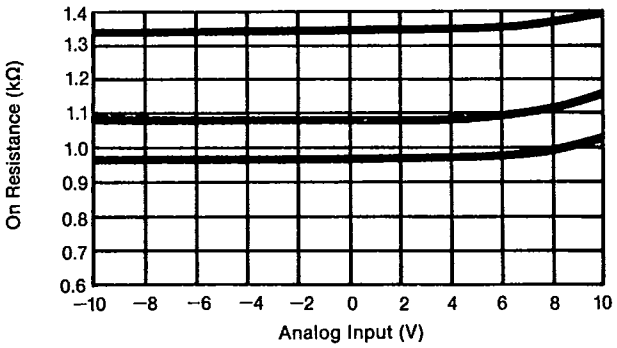
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless otherwise specified: T_A = +25, V_S = ±15V, V_{AH} = +4V, V_{AL} = 0.8V and V_{REF} = Open.

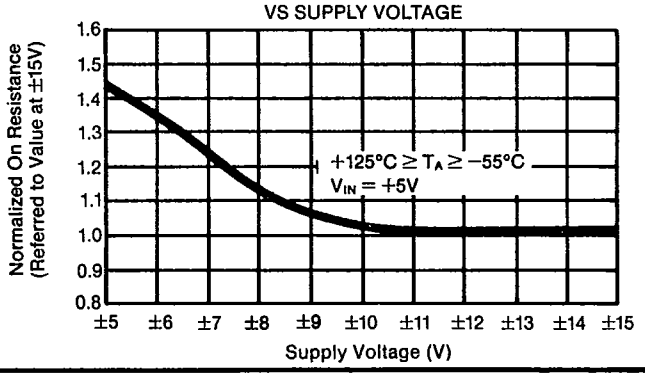
ON RESISTANCE VS ANALOG INPUT VOLTAGE, SUPPLY VOLTAGE



ON RESISTANCE VS ANALOG INPUT VOLTAGE

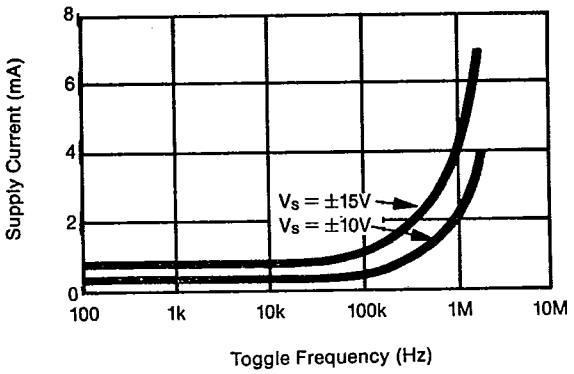


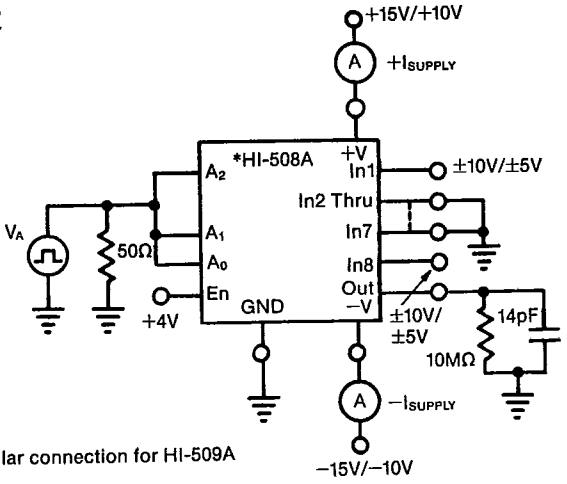
NORMALIZED ON RESISTANCE VS SUPPLY VOLTAGE



PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

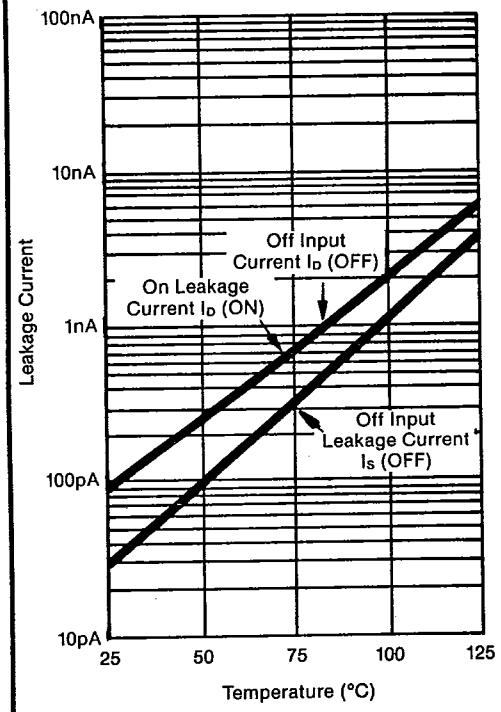
SUPPLY CURRENT VS TOGGLE FREQUENCY

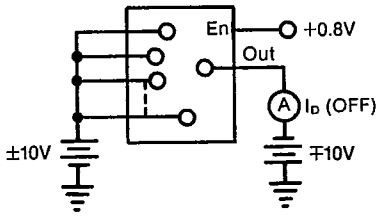


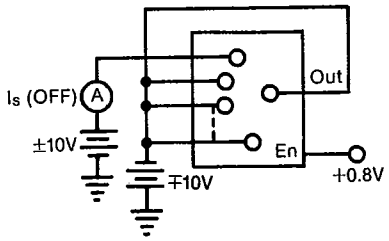


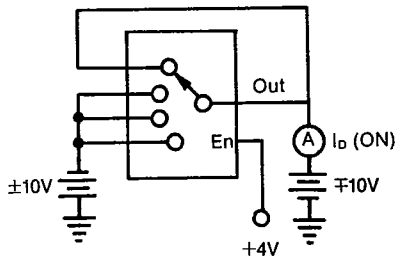
*Similar connection for HI-509A

LEAKAGE CURRENT VS TEMPERATURE



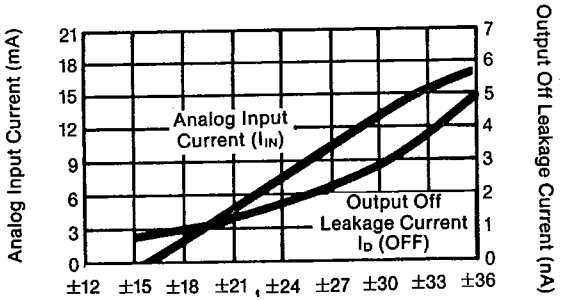


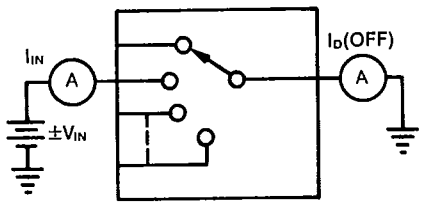




NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V. (Two measurements per device for I_D(OFF): +10V/–10V and –10V/+10V).

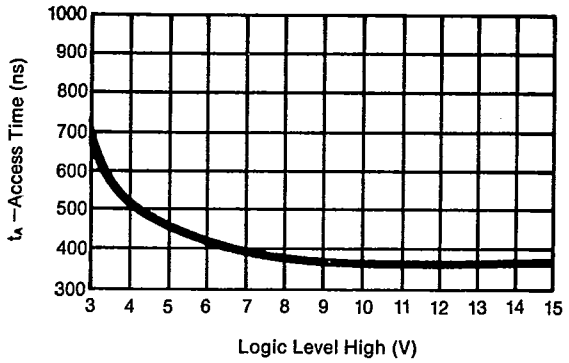
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

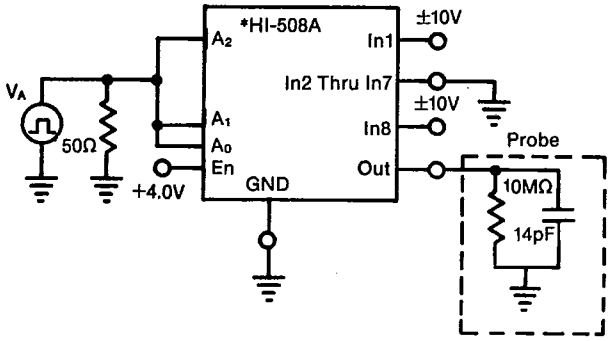




PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

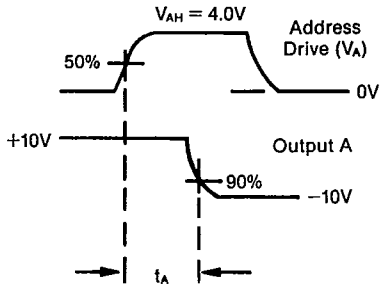
ACCESS TIME VS
LOGIC LEVEL (High)

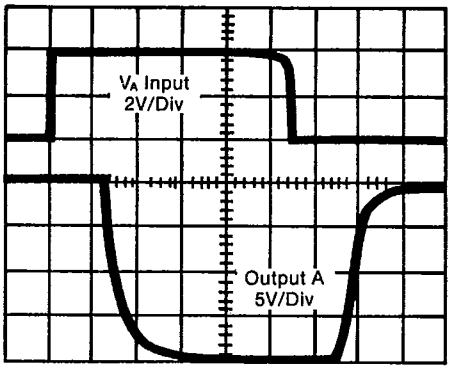




*Similar connection for HI-509A

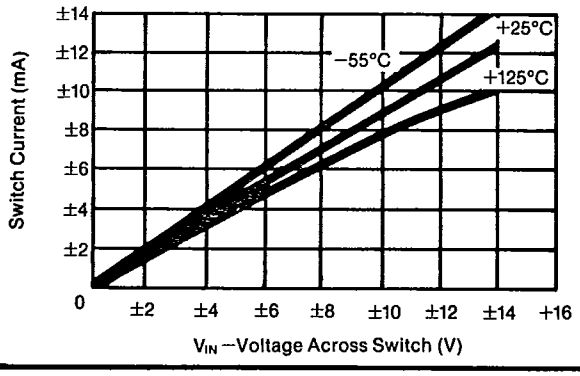
ACCESS TIME

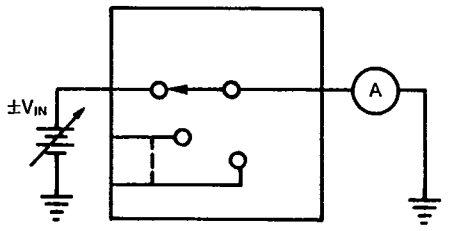




200ns/Div

ON-CHANNEL CURRENT
VS VOLTAGE





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (HI-509A) or 3-bit (HI-508A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Adddress Lines are active. If the ENABLE line is not to be used, simply tie it to $+V_{SUPPLY}$.

If the +15V and/or −15V supply voltage is absent or shorted to ground, the HI-509A and HI-508A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended.

To preserve common-mode rejection of the HI-509A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

Single-Ended Multiplexer (HI-508A)

Up to 32 channels (four multiplexers) can be connected to a single node, or up to 64 channels using nine HI-508A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

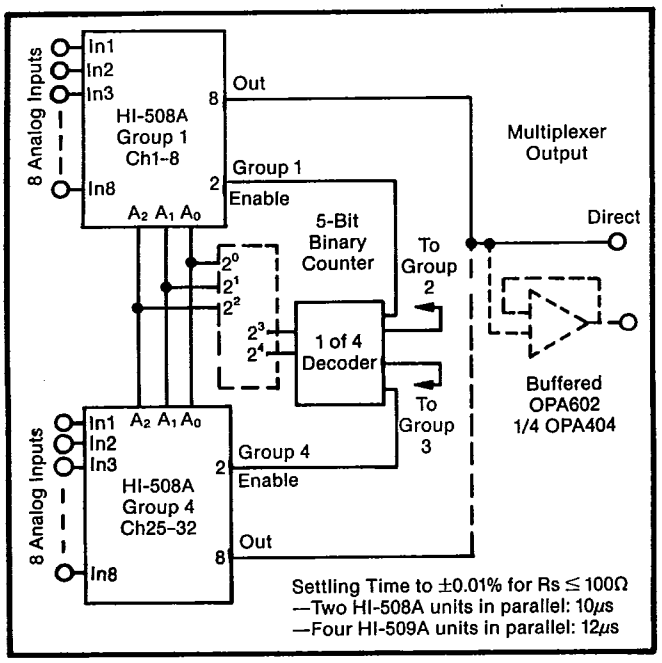


FIGURE 5. 32-Channel, Single-Tier Expansion.

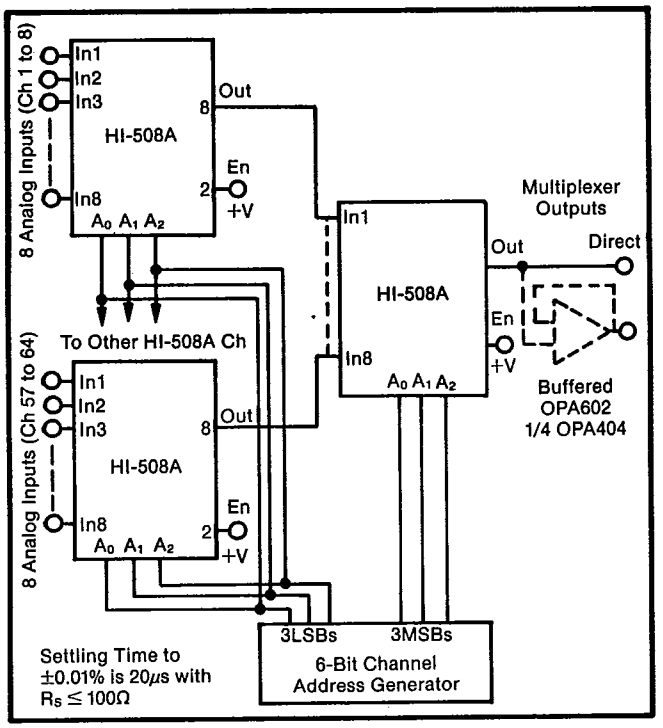


FIGURE 6. Channel Expansion Up to 64 Channels Using 8 × 8 Two-Tiered Expansion.

Differential Multiplexer (HI-509A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 × 1 or 16 channels using a 4 × 4 configuration.

Single-Node Expansion

The 32 × 1 configuration is simply eight (HI-509A) units tied to a single node. Programming is accomplished with a 5-bit counter, using the 2LSBs of the counter to control Channel Address inputs A_0 and A_1 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 2) of the HI-509A multiplexers.

Two-Tier Expansion

Using a 4 × 4 two-tier structure for expansion to 16 channels, the programming is simplified. A 4-bit counter output does not require a 1-of-8 decoder. The 2LSBs of the counter drive the A_0 and A_1 inputs of the four first-tier multiplexers and the 2MSBs of the counter are applied to the A_0 and A_1 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.