HD404369 Series

HITACHI

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Description

The HD404369 Series is a 4-bit HMCS400-Series microcomputer designed to increase program productivity and also incorporate large-capacity memory. Each microcomputer has an A/D converter, input capture timer, 32-kHz oscillator for clock, and four low-power dissipation modes.

The HD404369 Series includes nine chips: the HD404364, HD40A4364 with 4-kword ROM; the HD404368, HD40A4368 with 8-kword ROM; the HD4043612, HD40A43612 with 12-kword ROM; the HD404369, HD40A4369 with 16-kword ROM; the HD407A4369 with 16-kword PROM.

The HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369 are high speed versions (minimum instruction cycle time: 0.47 μs).

The HD407A4369 is a PROM version (ZTAT™ microcomputer). A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™ version is 27256-compatible.)

Features

- 512-digit × 4-bit RAM
- 54 I/O pins
  - — One input-only pin
  - — 53 input/output pins: 8 pins are intermediate-voltage NMOS open drain with high-current pins (15 mA, max.)
- On-chip A/D converter (8-bit × 12-channel)
  - — Low power voltage 2.7 V to 6.0 V
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- Eight-bit clock-synchronous serial interface (1 channel)
- Alarm output

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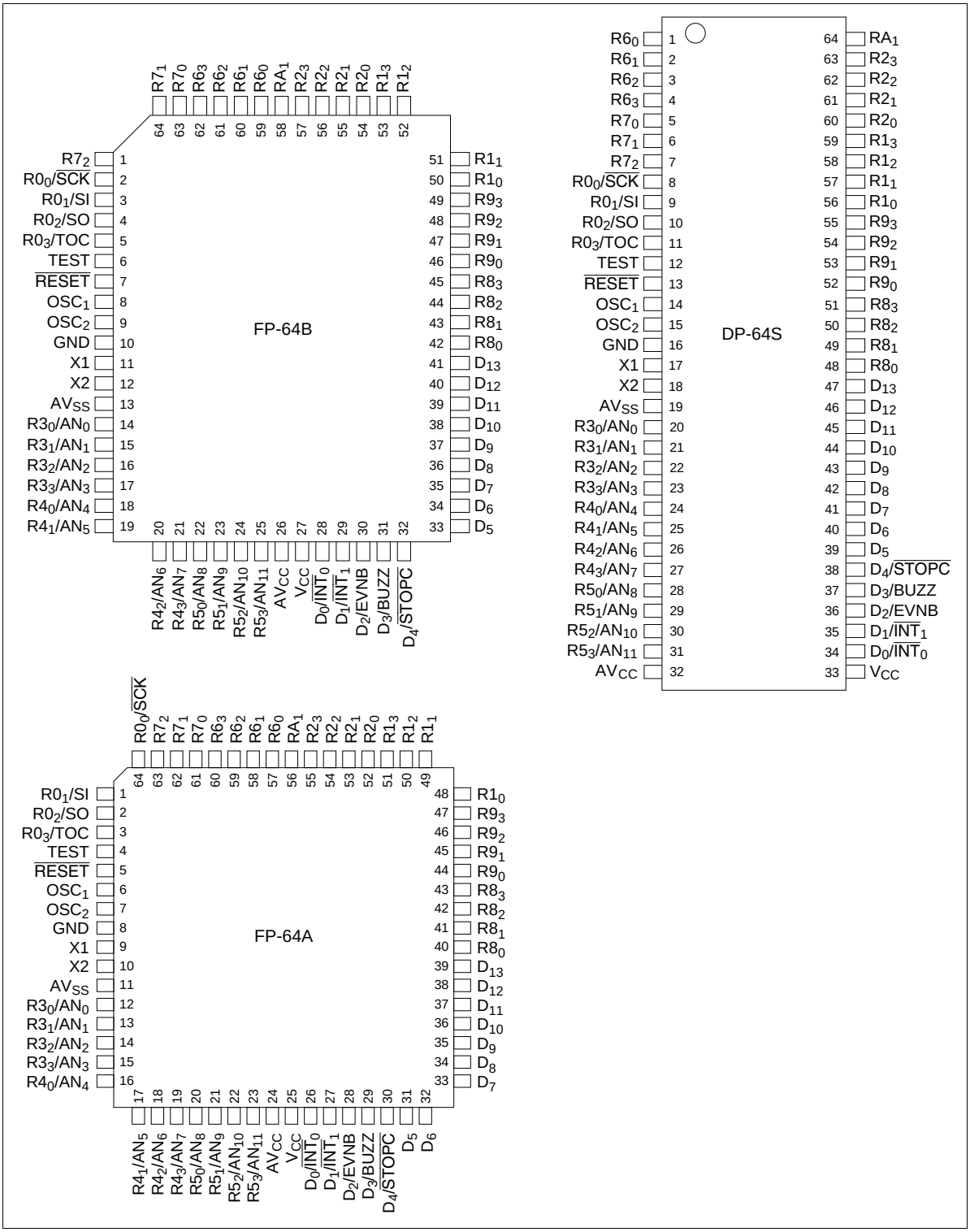
- Built-in oscillators
  - — Ceramic oscillator or crystal
  - — External clock drive is also possible
  - — Subclock: 32.768-kHz crystal oscillator
- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One by A/D converter
  - — One by serial interface
- Four low-power dissipation modes
  - — Standby mode
  - — Stop mode
  - — Watch mode
  - — Subactive mode
- Instruction cycle time
  - — 0.47 µs (f_{OSC} = 8.5 MHz, 1/4 division ratio):
    HD40A4364, HD40A4368, HD40A43612, HD40A4369, HD407A4369
  - — 0.8 µs (f_{OSC} = 5 MHz, 1/4 division ratio):
    HD404364, HD404368, HD4043612, HD404369
  - — 1/4, 1/8, 1/16, 1/32 system clock division ratio can be selecte

Ordering Information

Type	Instruction Cycle Time	Product Name	Model Name	ROM (Words)	Package
Mask ROM	Standard version (f_{osc}= 5 MHz)	HD404364	HD404364S	4,096	DP-64S
			HD404364F		FP-64B
			HD404364H		FP-64A
		HD404368	HD404368S	8,192	DP-64S
			HD404368F		FP-64B
			HD404368H		FP-64A
		HD4043612	HD4043612S	12,288	DP-64S
			HD4043612F		FP-64B
			HD4043612H		FP-64A
		HD404369	HD404369S	16,384	DP-64S
			HD404369F		FP-64B
			HD404369H		FP-64A
	High speed versions	HD40A4364	HD40A4364S	4,096	DP-64S
	(f_{osc} = 8.5 MHz)		HD40A4364F		FP-64B
			HD40A4364H		FP-64A
		HD40A4368	HD40A4368S	8,192	DP-64S
			HD40A4368F		FP-64B
			HD40A4368H		FP-64A
		HD40A43612	HD40A43612S	12,288	DP-64S
			HD40A43612F		FP-64B
			HD40A43612H		FP-64A
		HD40A4369	HD40A4369S	16,384	DP-64S
			HD40A4369F		FP-64B
			HD40A4369H		FP-64A
ZTAT™	(f_{osc} = 8.5 MHz)	HD407A4369	HD407A4369S	16,384	DP-64S
			HD407A4369F		FP-64B
			HD407A4369H		FP-64A

Pin Arrangement



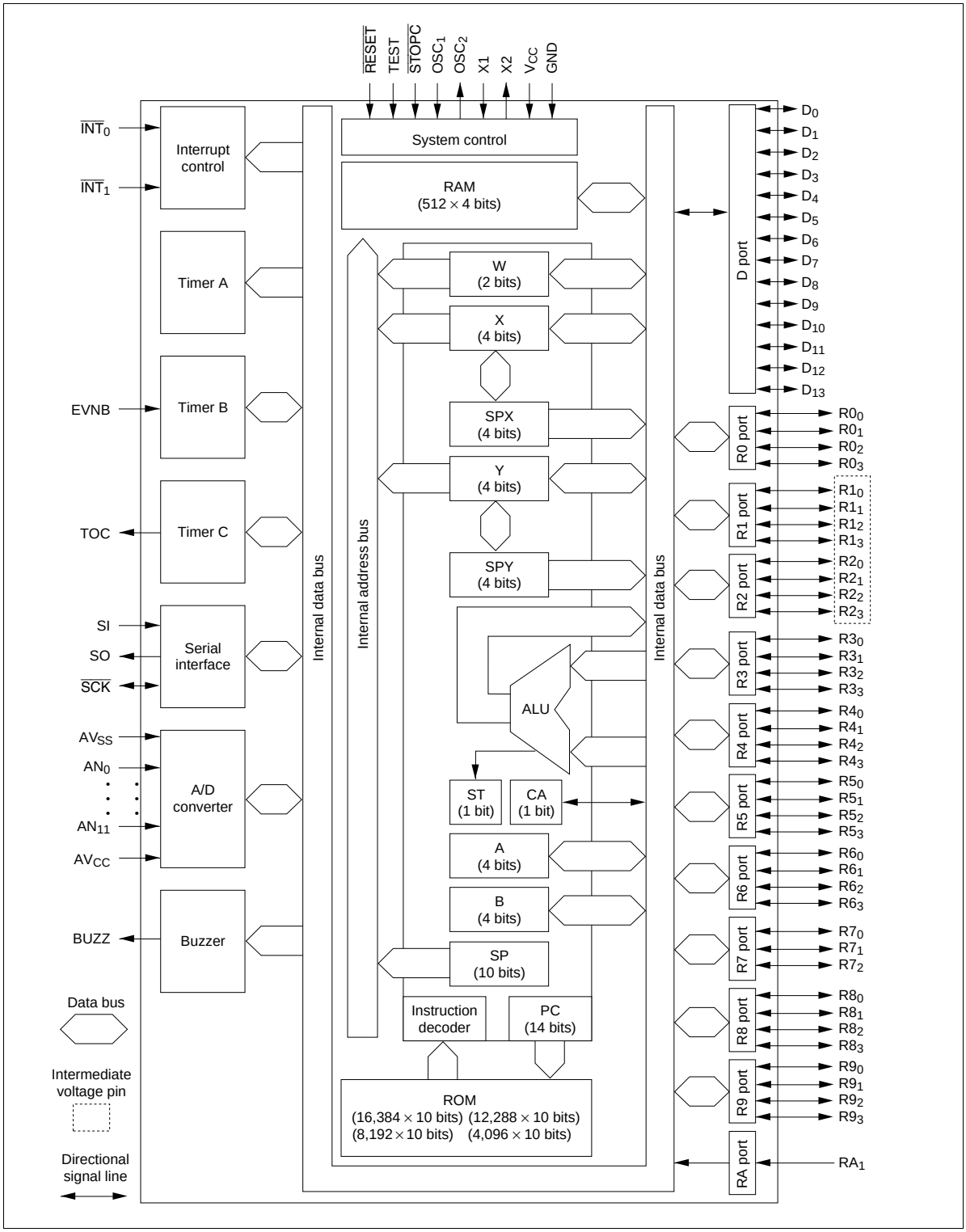
Pin Description

Item	Symbol	Pin Number DP-64S	FP-64B	FP-64A	I/O	Function
Power	V_{CC}	33	27	25		Applies power voltage
Supply	GND	16	10	8		Connected to ground
Test	TEST	12	6	4	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	13	7	5	I	Resets the MCU
Oscillator	OSC_1	14	8	6	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic oscillator or crystal oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	15	9	7	O	
	X1	17	11	9	I	Used with a 32.768-kHz crystal ocillator for clock purposes
	X2	18	12	10	O	
Port	D_0–D_{13}	34–47	28–41	26–39	I/O	Input/output pins consisting of standard voltage pins addressed individually by bits
	RA_1	64	58	56	I	One-bit standard-voltage input port pin
	$R0_0$–$R0_3$, $R3_0$–$R9_3$	1–11, 20–31, 48–55	1–5, 14–25, 42–49, 59–64	1–3, 12–23, 40–47, 57–64	I/O	Four-bit input/output pins consisting of standard voltage pins
	$R1_0$–$R2_3$	56–63	50–57	48–55	I/O	Four-bit input/output pins consisting of intermediate voltage pins
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	34, 35	28, 29	26, 27	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	38	32	30	I	Input pin for transition from stop mode to active mode
Serial Interface	$\overline{SCK}$	8	2	64	I/O	Serial interface clock input/output pin
	SI	9	3	1	I	Serial interface receive data input pin
	SO	10	4	2	O	Serial interface transmit data output pin
Timer	TOC	11	5	3	O	Timer output pin
	EVNB	36	30	28	I	Event count input pin
Alarm	BUZZ	37	31	29	O	Square waveform output pin

Pin Description (cont)

Item	Symbol	Pin Number DP-64S	FP-64B	FP-64A	I/O	Function
A/D converter	AV_{CC}	32	26	24		Power supply for the A/D converter. Connect this pin as close as possible to the V_{CC} pin and at the same voltage as V_{CC}. If the power supply voltage to be used for the A/D converter is not equal to V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
	AV_{SS}	19	13	11		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN_0–AN_{11}	20–31	14–25	12–23	I	Analog input pins for the A/D converter

Block Diagram



Memory Map

ROM Memory Map

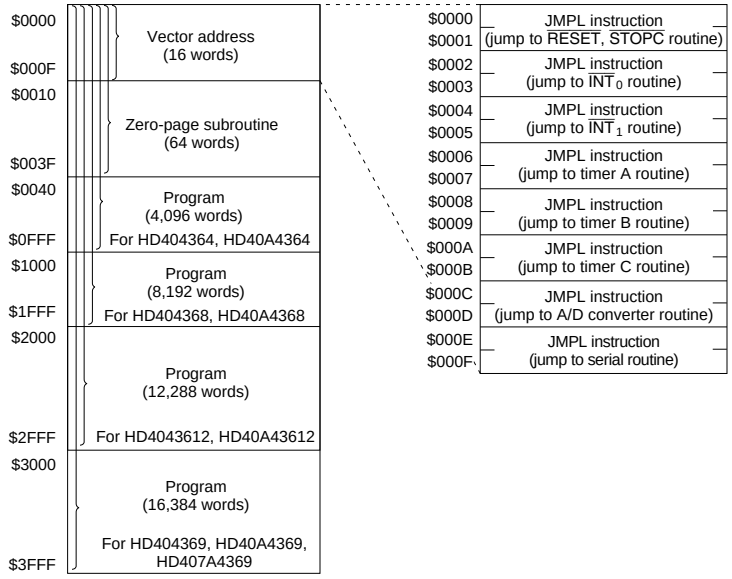
The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000-$0FFF (HD404364, HD40A4364), $0000–$1FFF (HD404368, HD40A4368), $0000–$2FFF (HD4043612, HD40A43612), $0000–$3FFF (HD404369, HD40A4369, HD407A4369)): The entire ROM area can be used for program coding.



Note: Since the ROM address areas between $0000–$0FFF overlap, the user can determine how these areas are to be used.

Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains 512-digit × 4 bit RAM areas. These RAM areas consist of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special function register area, and register flag area are mapped onto the same RAM memory space labeled as a RAM-mapped register area. The RAM memory map is shown in figure 2 and described below.

RAM Memory Map

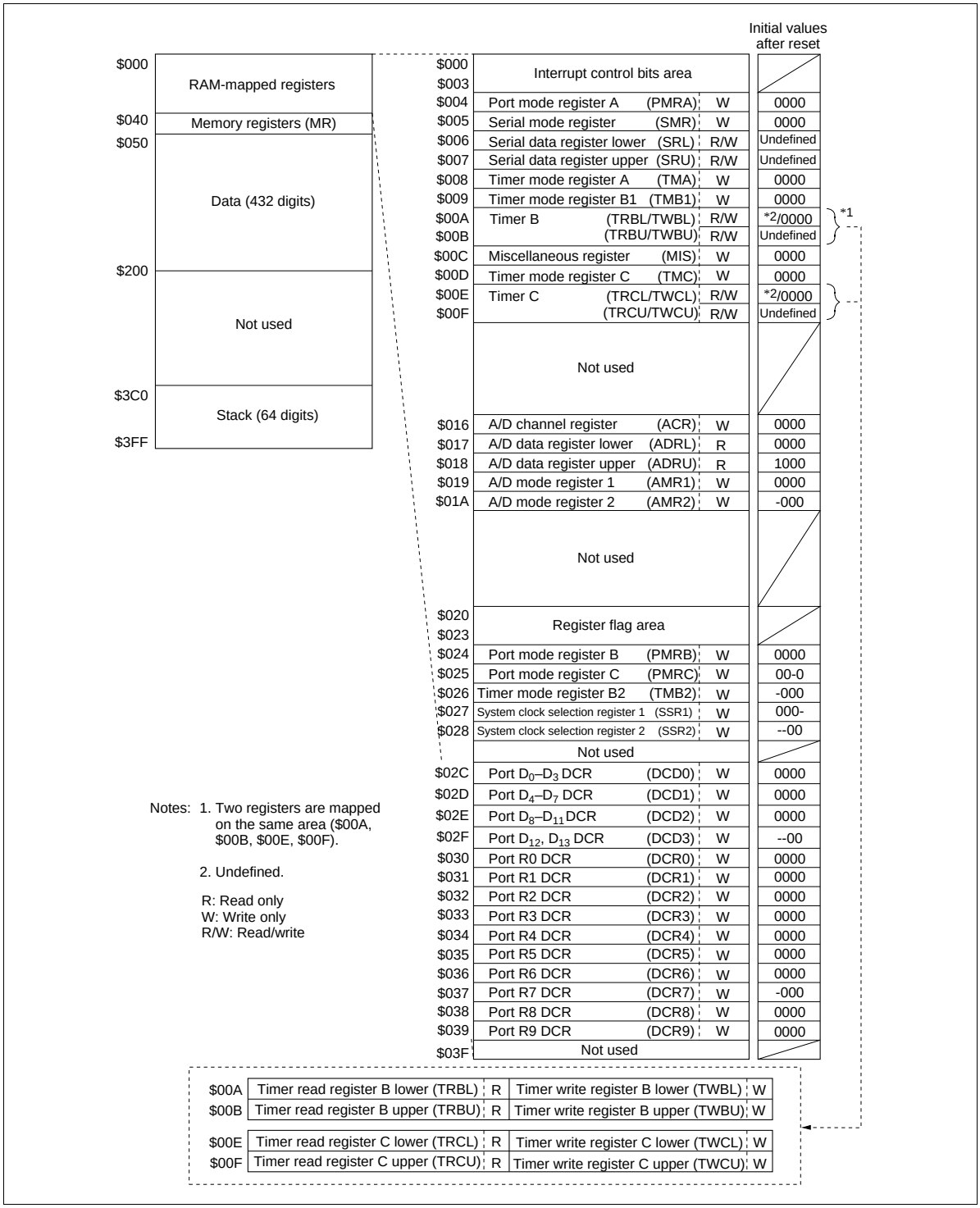


Figure 2 RAM Memory Map

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$01F, $024–$03F)

  This area is used as mode registers and data registers for external interrupts, serial interface, timer/counters, A/D converter, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($050–$1FF)

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

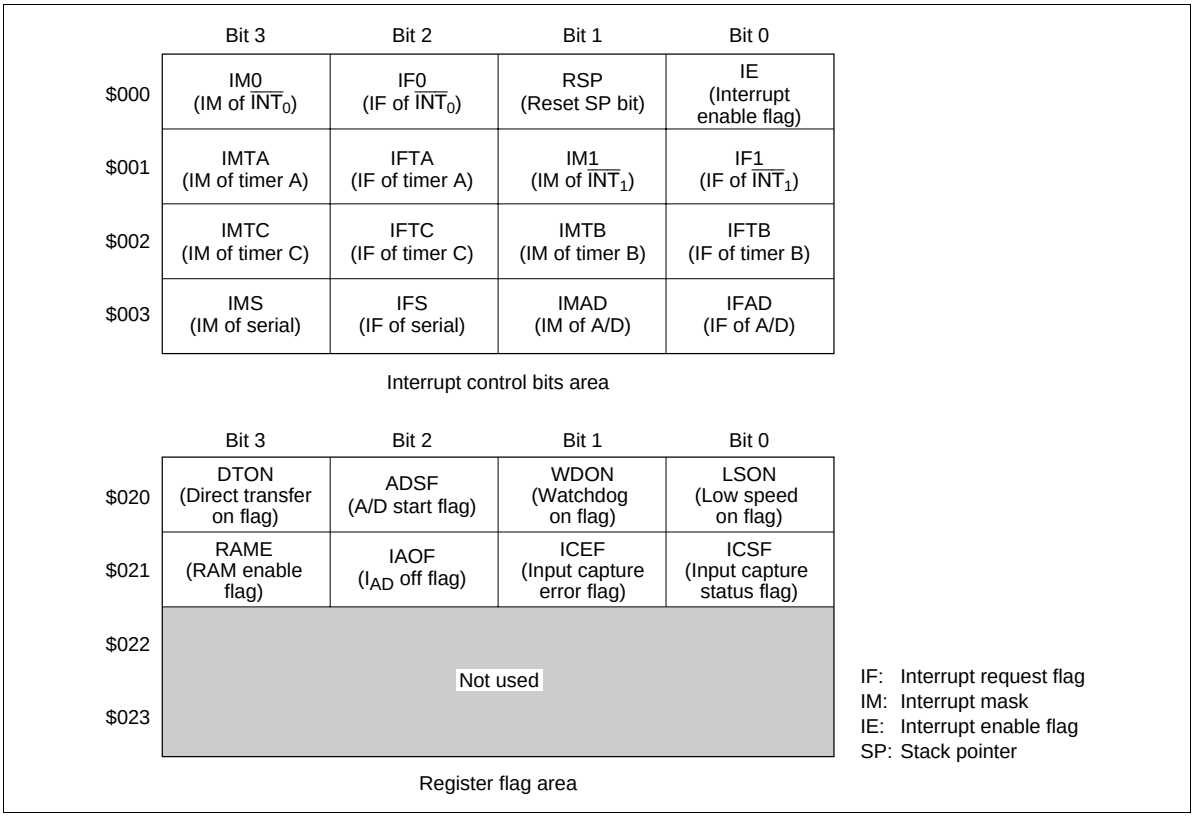


Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
LSON			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{STOPC}$ enable for stop mode cancellation.
The REM or REMD instuction must not be executed for ADSF during A/D conversion.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000	Interrupt control bits area			
$003				
PMRA $004	D_3/BUZZ	$R0_3$/TOC	$R0_1$/SI	$R0_2$/SO
SMR $005	$R0_0$/$\overline{SCK}$	Serial transmit clock speed selection		
SRL $006	Serial data register (lower digit)			
SRU $007	Serial data register (upper digit)			
TMA $008	*1	Clock source selection (timer A)		
TMB1 $009	*2	Clock source selection (timer B)		
TRBL/TWBL $00A	Timer B register (lower digit)			
TRBU/TWBU $00B	Timer B register (upper digit)			
MIS $00C	*3	SO PMOS control	Interrupt frame period selection	
TMC $00D	*2	Clock source selection (timer C)		
TRCL/TWCL $00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
	Not used			
ACR $016	Analog channel selection			
ADRL $017	A/D data register (lower digit)			
ADRU $018	A/D data register (upper digit)			
AMR1$019	$R3_3$/AN_3	$R3_2$/AN_2	$R3_1$/AN_1	$R3_0$/AN_0
AMR2 $01A	Not used	R5/AN_8–AN_{11}	R4/AN_4–AN_7	*4
	Not used			
$020	Register flag area			
$023				
PMRB $024	D_4/$\overline{STOPC}$	D_2/EVNB	D_1/$\overline{INT_1}$	D_0/$\overline{INT_0}$
PMRC $025	Buzzer output		*5	*6
TMB2 $026	Not used	*7	EVNB detection edge selection	
SSR1 $027	*8	*9	Clock select	Not used
SSR2 $028	Not used		Clock division ratio selection	
	Not used			
DCD0 $02C	Port D_3 DCD	Port D_2 DCD	Port D_1 DCD	Port D_0 DCD
DCD1 $02D	Port D_7 DCD	Port D_6 DCD	Port D_5 DCD	Port D_4 DCD
DCD2 $02E	Port D_{11} DCD	Port D_{10} DCD	Port D_9 DCD	Port D_8 DCD
DCD3 $02F	Not used		Port D_{13} DCD	Port D_{12} DCD
DCR0 $030	Port $R0_3$ DCR	Port $R0_2$ DCR	Port $R0_1$ DCR	Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
DCR5 $035	Port $R5_3$ DCR	Port $R5_2$ DCR	Port $R5_1$ DCR	Port $R5_0$ DCR
DCR6 $036	Port $R6_3$ DCR	Port $R6_2$ DCR	Port $R6_1$ DCR	Port $R6_0$ DCR
DCR7 $037	Not used	Port $R7_2$ DCR	Port $R7_1$ DCR	Port $R7_0$ DCR
DCR8 $038	Port $R8_3$ DCR	Port $R8_2$ DCR	Port $R8_1$ DCR	Port $R8_0$ DCR
DCR9 $039	Port $R9_3$ DCR	Port $R9_2$ DCR	Port $R9_1$ DCR	Port $R9_0$ DCR
	Not used			
$03F				

Notes:
1. Timer-A/time-base
2. Auto-reload on/off
3. Pull-up MOS control
4. A/D conversion time
5. SO output level control in idle states
6. Serial clock source selection
7. Input capture selection
8. 32-kHz oscillation stop
9. 32-kHz oscillation division ratio

Figure 5 Special Function Register Area

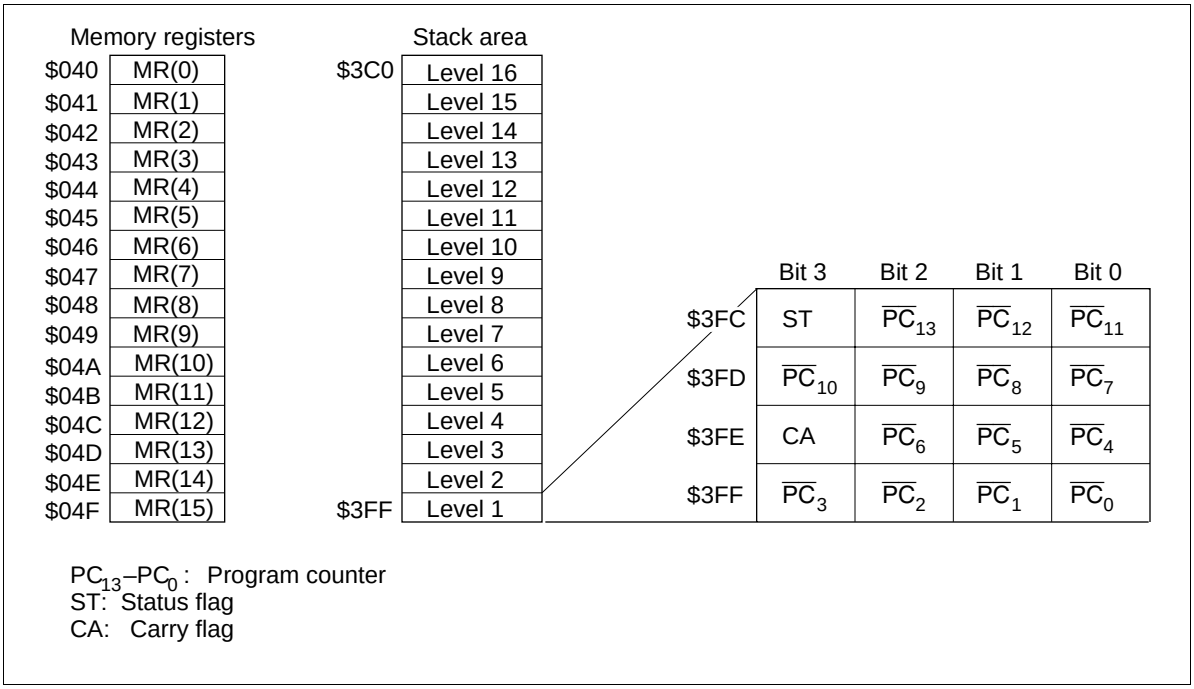


Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 7 and described below.

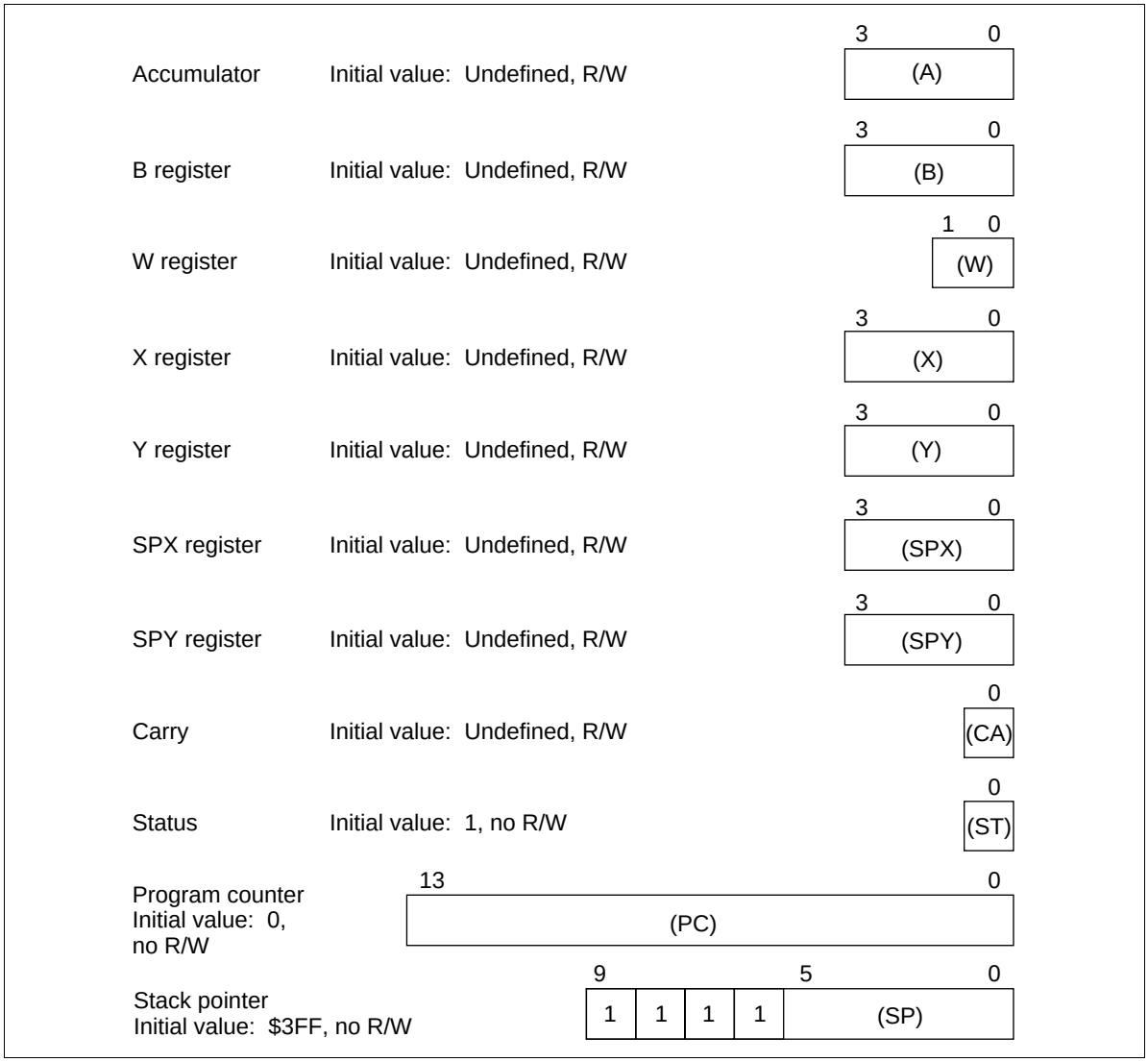


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a low-level voltage to the $\overline{\text{RESET}}$ pin. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ must be low for at least one t_{RC} to enable the oscillator to stabilize. During operation, $\overline{\text{RESET}}$ must be low for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Interrupts

The MCU has 7 interrupt sources: two external signals ($\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$), three timer/counters (timers A, B, and C), serial interface, and A/D converter.

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations $000 to $003 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 7 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 9 and an interrupt processing flowchart is shown in figure 10. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0-DCD2)	All bits 0	Turns output buffer off (to high impedance)
		(DCD3)	- - 00	
		(DCR0–DCR6, DCR8, DCR9)	All bits 0	
		(DCR7)	- 000	
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B bits 2–0	(PMRB2–PMRB0)	000	Refer to description of port mode register B
	Port mode register C	(PMRC)	00 - 0	Refer to description of port mode register C
Timer/counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- 000	Refer to description of timer mode register B2
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S	(PSS)	$000	—
	Prescaler W	(PSW)	$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Octal counter		000	—

Item		Abbr.	Initial Value	Contents
A/D	A/D mode register 1	(AMR1)	0000	Refer to description of A/D mode register
	A/D mode register 2	(AMR2)	- 000	
	A/D channel register	(ACR)	0000	Refer to description of A/D channel register
	A/D data register	(ADRL)	0000	Refer to description of A/D data register
		(ADRU)	1000	
Bit registers	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	I_{AD} off flag	(IAOF)	0	Refer to the description of A/D converter
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
	Input capture status flag	(ICSF)	0	Refer to description of timer B
	Input capture error flag	(ICEF)	0	Refer to description of timer B
Others	Miscellaneous register	(MIS)	0000	Refer to description of operating modes, I/O, and serial interface
	System clock select register 1	(SSR1)	000 -	Refer to description of operating modes, and oscillation circuits
	System clock select register 2	(SSR2)	- - 00	Refer to description of oscillation circuits

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program	Pre-mcu-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SRL, SRU)		
RAM		Pre-stop-mode values are retained	
RAM enable flag	(RAME)	1	0
Port mode register B bit 3	(PMRB3)	Pre-stop-mode values are retained	0
System clock select register 1 bit 3	(SSR13)		

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
$\overline{\text{RESET}}$, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
A/D	6	$000C
Serial	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.

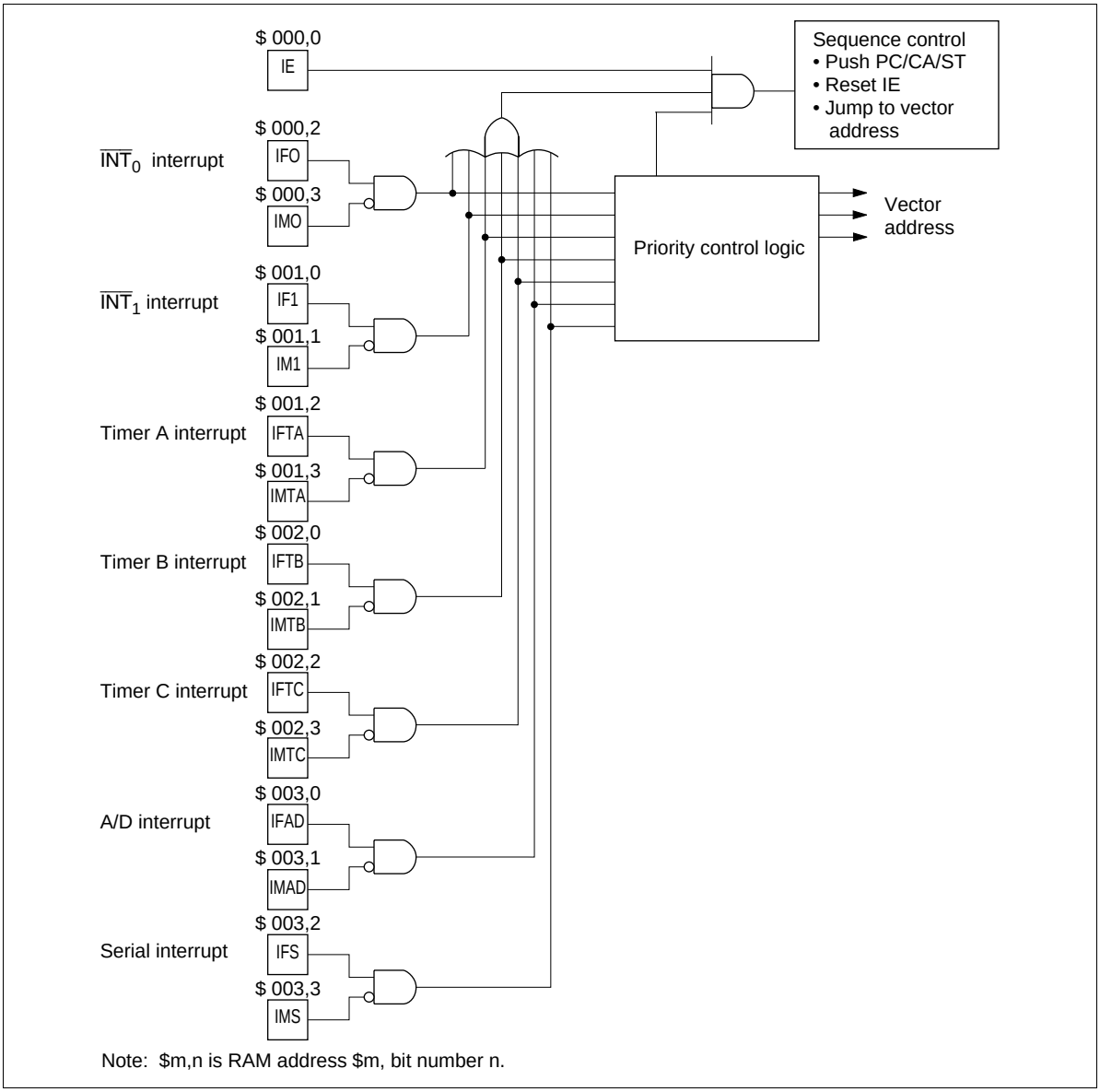


Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source						
	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C	A/D	Serial
IE	1	1	1	1	1	1	1
IF0 $\overline{IM0}$	1	0	0	0	0	0	0
IF1 $\overline{IM1}$	*	1	0	0	0	0	0
IFTA $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC $\overline{IMTC}$	*	*	*	*	1	0	0
IFAD $\overline{IMAD}$	*	*	*	*	*	1	0
IFS $\overline{IMS}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

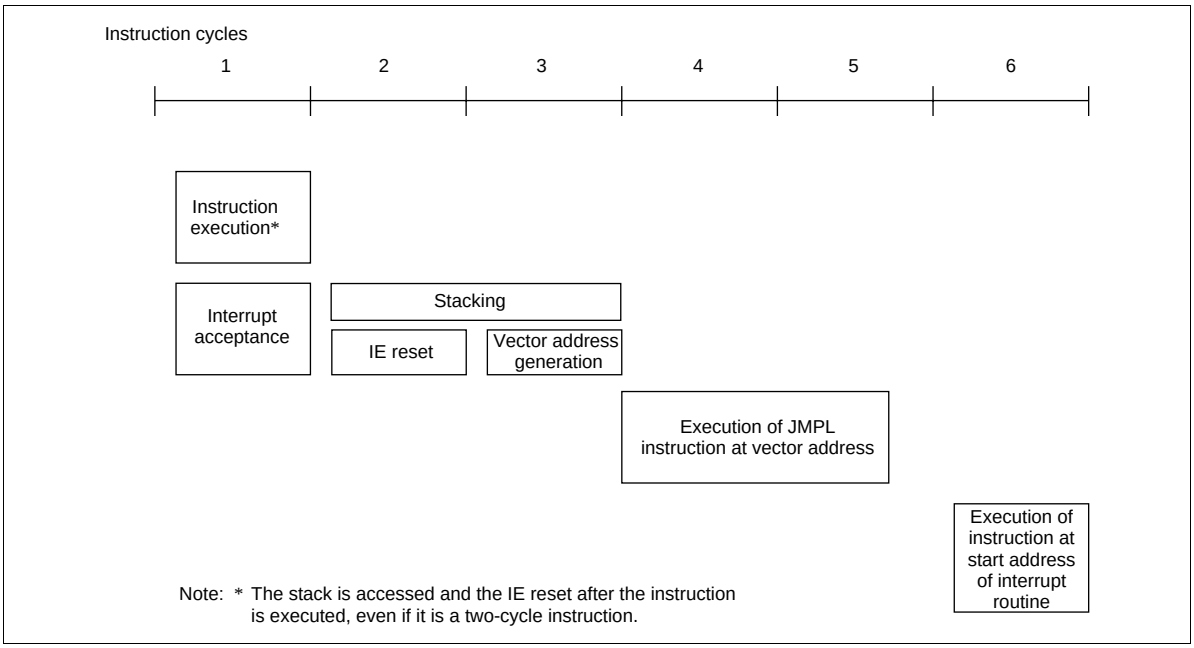


Figure 9 Interrupt Processing Sequence

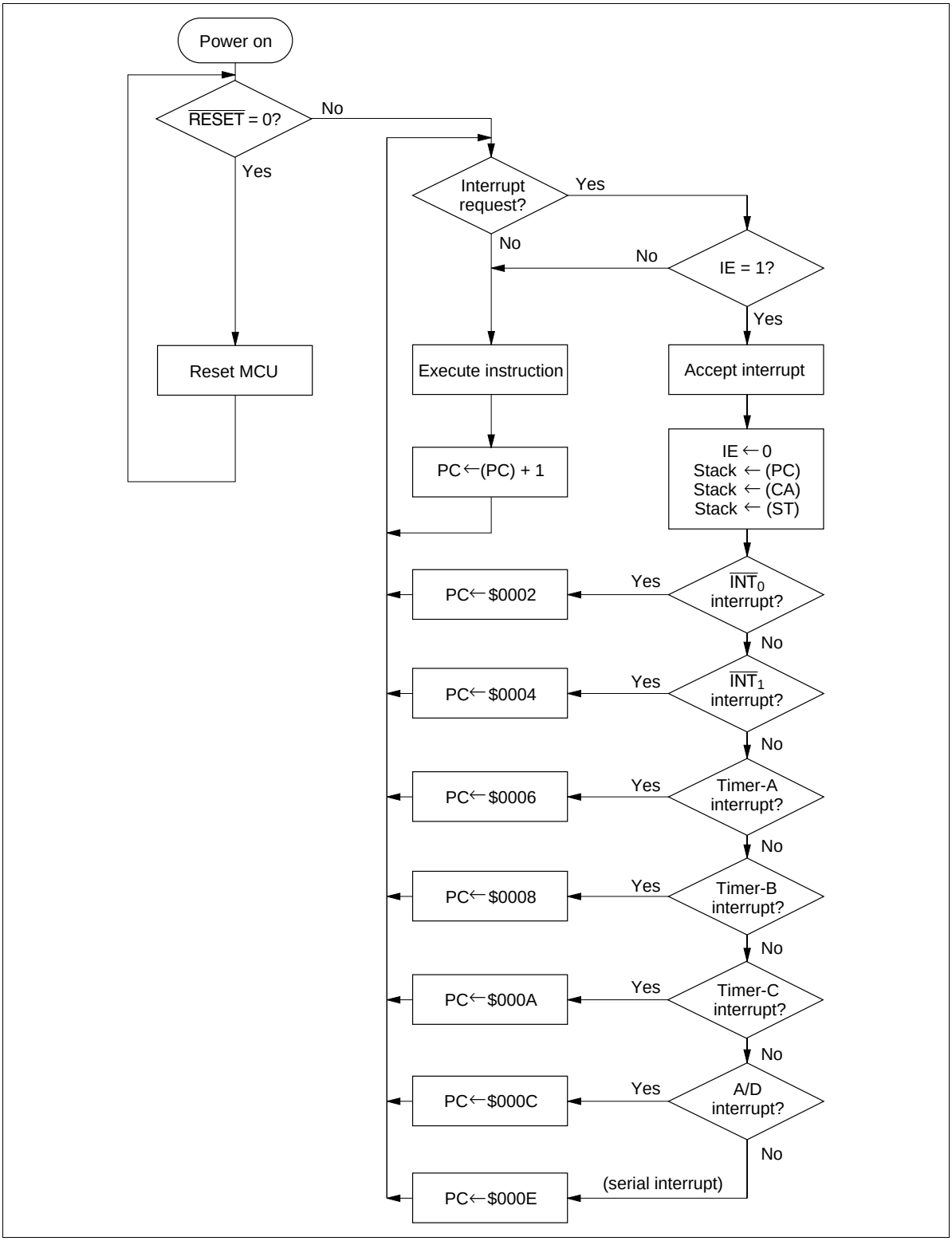


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT}_0$, $\overline{INT}_1$): Two external interrupt signals.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): IF0 and IF1 are set at the rising edge of signals input to $\overline{INT}_0$ and $\overline{INT}_1$, as listed in table 5.

Table 5 External Interrupt Request Flags (IF0: $000, Bit2; IF1: $001, Bit 0)

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1)

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: 001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B, as listed in table 9.

Table 9 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as listed in table 10.

Table 10 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 11.

Table 11 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 12.

Table 12 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 13.

Table 13 Serial Interrupt Request Flag (IFS: $003, Bit 2)

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 14.

Table 14 Serial Interrupt Mask (IMS: $003, Bit 3)

Mask IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 0): Set at the completion of A/D conversion, as listed in table 15.

Table 15 A/D Interrupt Request Flag (IFAD: $003, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 1): Prevents (masks) an interrupt request caused by the A/D interrupt request flag, as listed in table 16.

Table 16 A/D Interrupt Mask (IMAD: $003, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has five operating modes as shown in table 17. The operations in each mode are listed in tables 18 and 19. Transitions between operating modes are shown in figure 11.

Active Mode: All MCU functions operate according to the clock generated by the system oscillator OSC_1 and OSC_2.

Table 17 Operating Modes and Clock Status

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*[2]**
Activation method		$\overline{\text{RESET}}$ cancellation, interrupt $\overline{\text{STOPC}}$ cancellation in stop mode, STOP/SBY instruction in subactive mode (when direct transfer is selected)	SBY instruction	STOP instruction when TMA3 = 0	STOP instruction when TMA3 = 1	$\overline{\text{INT}_0}$ or timer A interrupt request from watch mode
Status	System oscillator	OP	OP	Stopped	Stopped	Stopped
	Subsystem oscillator	OP	OP	*[1] OP	OP	OP
Cancellation method		$\overline{\text{RESET}}$ input, STOP/SBY instruction	$\overline{\text{RESET}}$ input, interrupt request	$\overline{\text{RESET}}$ input, $\overline{\text{STOPC}}$ input in stop mode	$\overline{\text{RESET}}$ input, $\overline{\text{INT}_0}$ or timer A interrupt request	$\overline{\text{RESET}}$ input, STOP/SBY instruction

Notes: OP implies in operation

1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register 1 (SSR1: $027).
2. Subactive mode is an optional function; specify it on the function option list.

Table 18 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode	Standby Mode	Subactive Mode
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Serial	Reset	Stopped	OP	OP
A/D	Reset	Stopped	OP	Stopped
I/O	Reset	Retained	Retained	OP

Note: OP implies in operation

Table 19 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch mode	Stop Mode	Active Mode, Subactive mode
RA_1	—	—	Input enabled
D_0–D_{13}, R0–R9	Retained or output of peripheral functions	High impedance	Input enabled

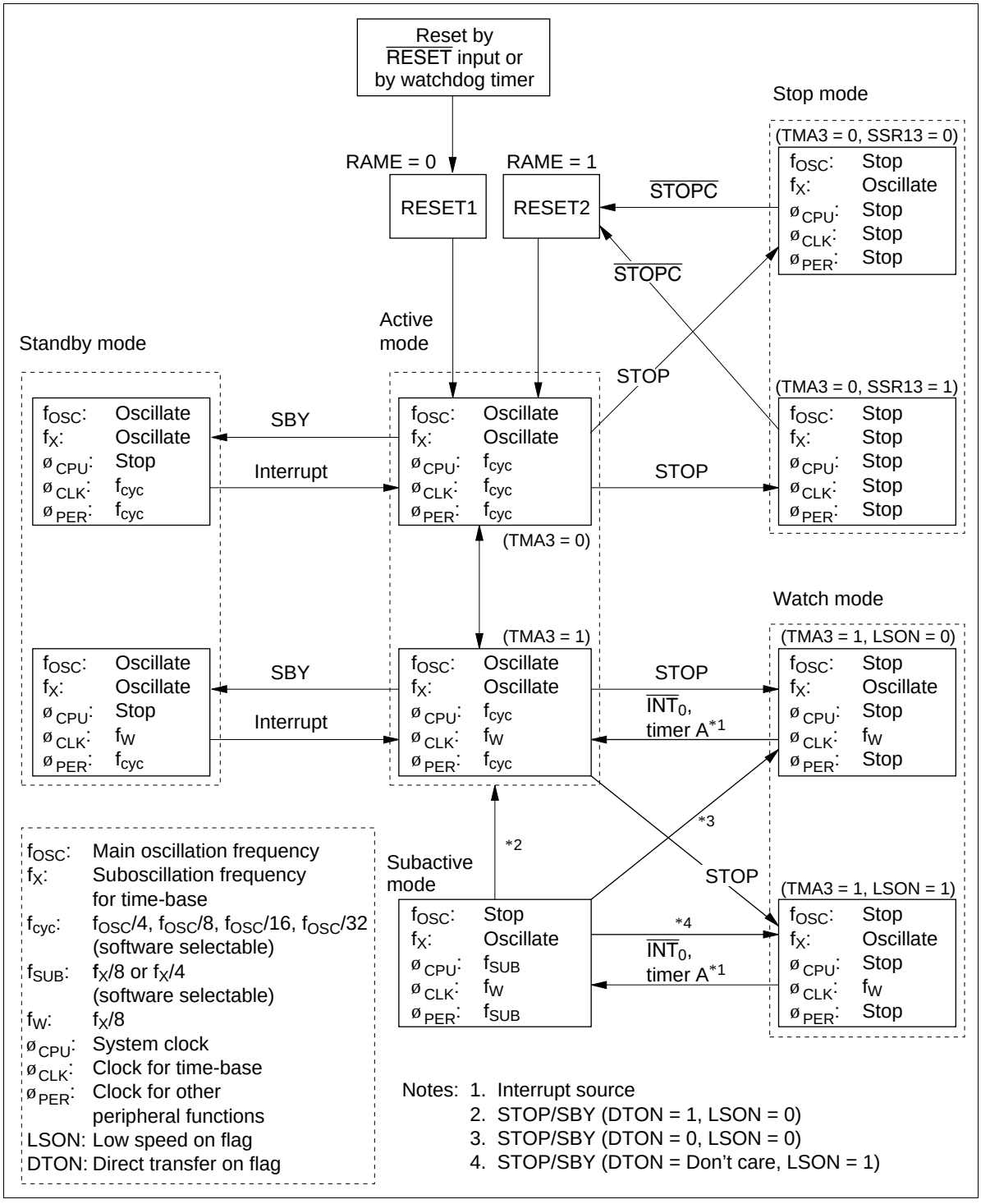


Figure 11 MCU Status Transitions

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a $\overline{\text{RESET}}$ input or an interrupt request. If it is terminated by $\overline{\text{RESET}}$ input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 12.

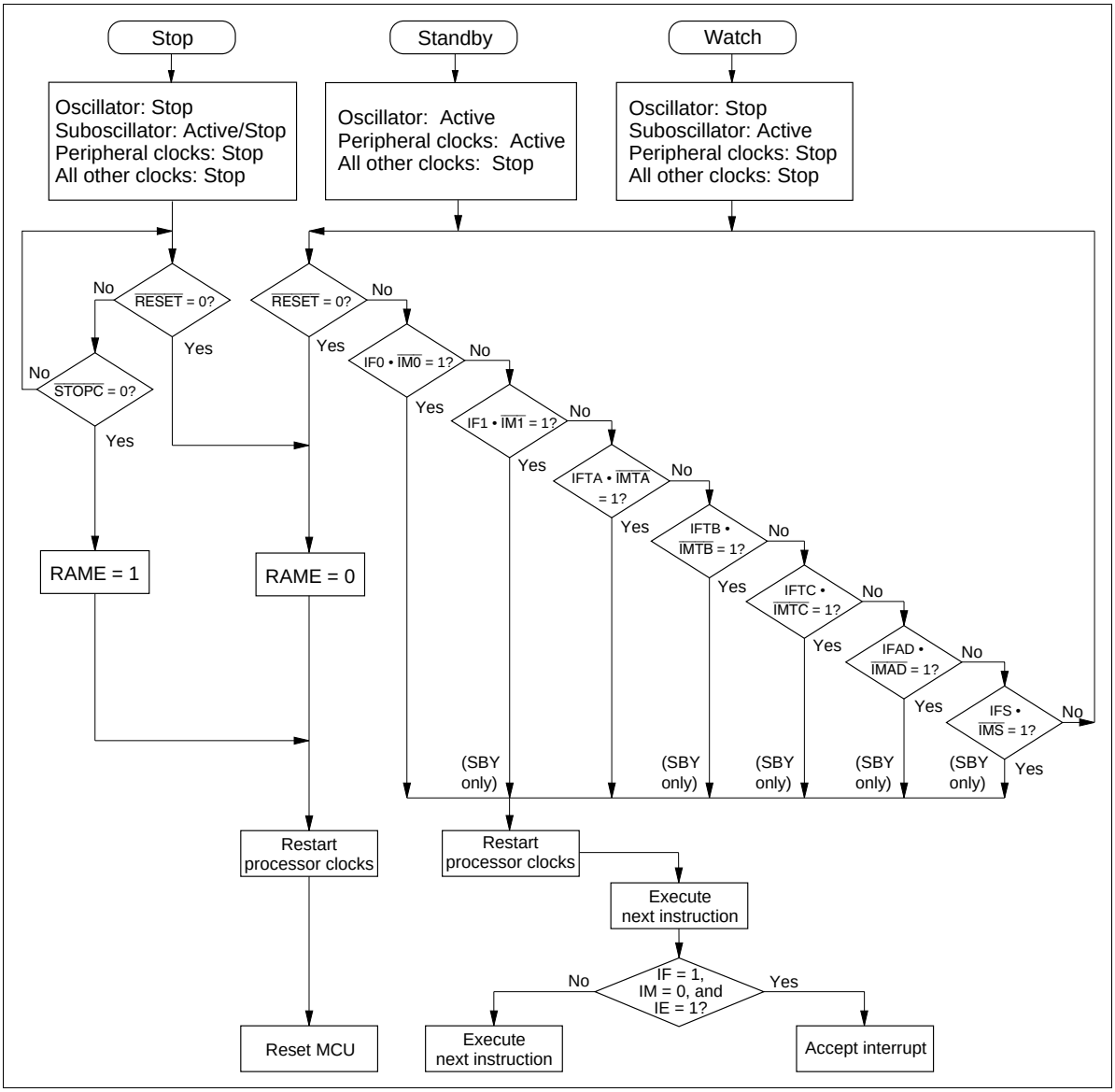


Figure 12 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. For the X1 and X2 oscillator to operate or stop can be selected by setting bit 3 of the system clock select register 1 (SSR1: $027; operating: SSR13 = 0, stop: SSR13 = 1) (figure 23). The MCU enters stop mode if the STOP instruction is executed in active mode when bit 3 of timer mode register A (TMA: $008) is set to 0 (TMA3 = 0) (figure 37).

Stop mode is terminated by a $\overline{\text{RESET}}$ input or a $\overline{\text{STOPC}}$ input as shown in figure 13. $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained,

but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: In watch mode, the clock function (timer A) using the X1 and X2 oscillator operates, but other function operations stop. Therefore, the power dissipation in this mode is the second least to stop mode, and this mode is convenient when only clock display is used. In this mode, the OSC_1 and OSC_2 oscillator stops, but the X1 and X2 oscillator operates. The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruction is executed in subactive mode.

Watch mode is terminated by a $\overline{\text{RESET}}$ input or a timer-A/$\overline{\text{INT}_0}$ interrupt request. For details of $\overline{\text{RESET}}$ input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{\text{INT}_0}$ interrupt request, the MCU enters active mode if LSON = 0, or subactive mode if LSON = 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{\text{INT}_0}$ interrupt, as shown in figures 14 and 15.

Operation during mode transition is the same as that at standby mode cancellation (figure 12).

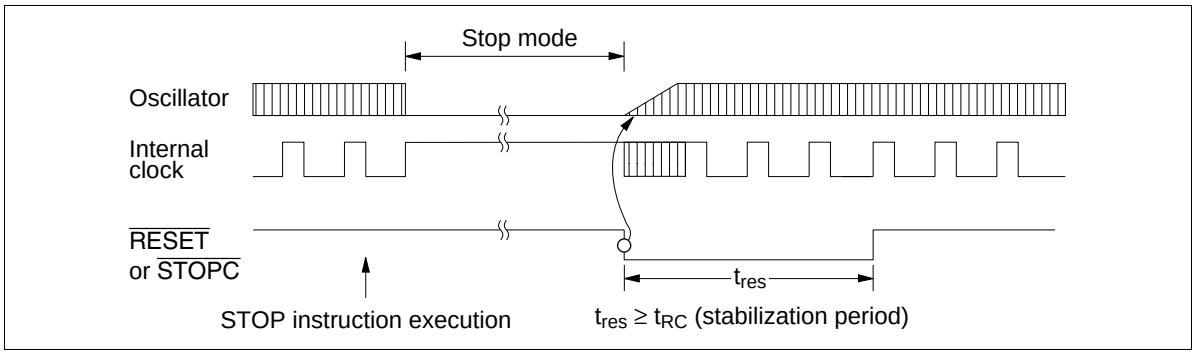


Figure 13 Timing of Stop Mode Cancellation

Subactive Mode: The OSC_1 and OSC_2 oscillator stops and the MCU operates with a clock generated by the X1 and X2 oscillator. In this mode, functions except the A/D conversion operate. However, because the operating clock is slow, the power dissipation becomes low, next to watch mode.

The CPU instruction execution speed can be selected as 244 µs or 122 µs by setting bit 2 (SSR12) of the system clock select register 1 (SSR1: $027). Note that the SSR12 value must be changed in active mode. If the value is changed in subactive mode, the MCU may malfunction.

When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of the low speed on flag (LSON: $020, bit 0) and the direct transfer on flag (DTON: $020, bit 3).

Interrupt Frame: In watch and subactive modes, $ø_{CLK}$ is applied to timer A and the $\overline{\text{INT}_0}$ circuit. Prescaler W and timer A operate as the time-base and generate the timing clock for the interrupt frame. Three interrupt frame lengths (T) can be selected by setting the miscellaneous register (MIS: $00C) (figure 15).

In watch and subactive modes, the timer-A/$\overline{\text{INT}_0}$ interrupt is generated synchronously with the interrupt frame. The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. The falling edge of the $\overline{\text{INT}_0}$ signal is input asynchronously with the interrupt

frame timing, but it is regarded as input synchronously with the second interrupt strobe clock after the falling edge. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

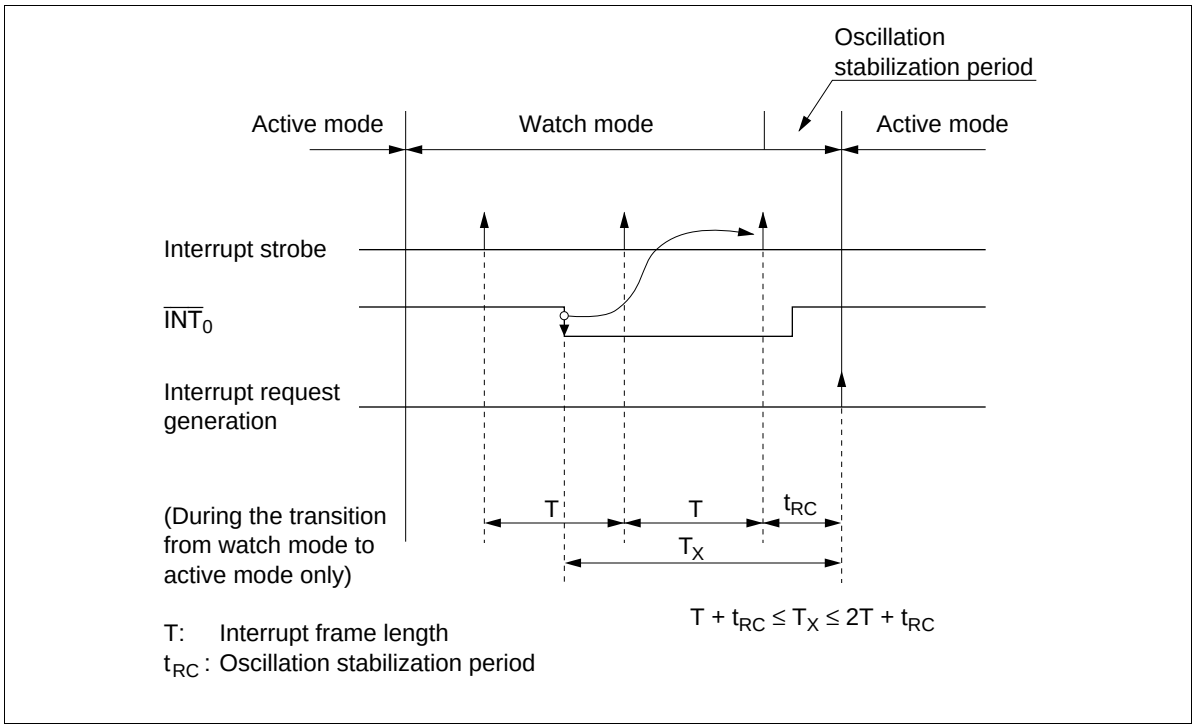


Figure 14 Interrupt Frame

Direct Transition from Subactive Mode to Active Mode: Available by controlling the direct transfer on flag (DTON: $020, bit 3) and the low speed on flag (LSON: $020, bit 0). The procedures are described below:

- Set LSON to 0 and DTON to 1 in subactive mode.
- Execute the STOP or SBY instruction.
- The MCU automatically enters active mode from subactive mode after waiting for the MCU internal processing time and oscillation stabilization time (figure 16).

Notes: 1. The DTON flag ($020, bit 3) can be set only in subactive mode. It is always reset in active mode.

2. The transition time (T_D) from subactive mode to active mode:
   $t_{RC} < T_D < T + t_{RC}$

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	MIS2
Buffer control. Refer to figure 34.	

MIS1	MIS0	T*1	t_{RC}*1	Oscillation Circuit Conditions
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms*2	
0	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
1	1	Not used		—

Notes: 1. The values of T and t_{RC} are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

Figure 15 Miscellaneous Register (MIS)

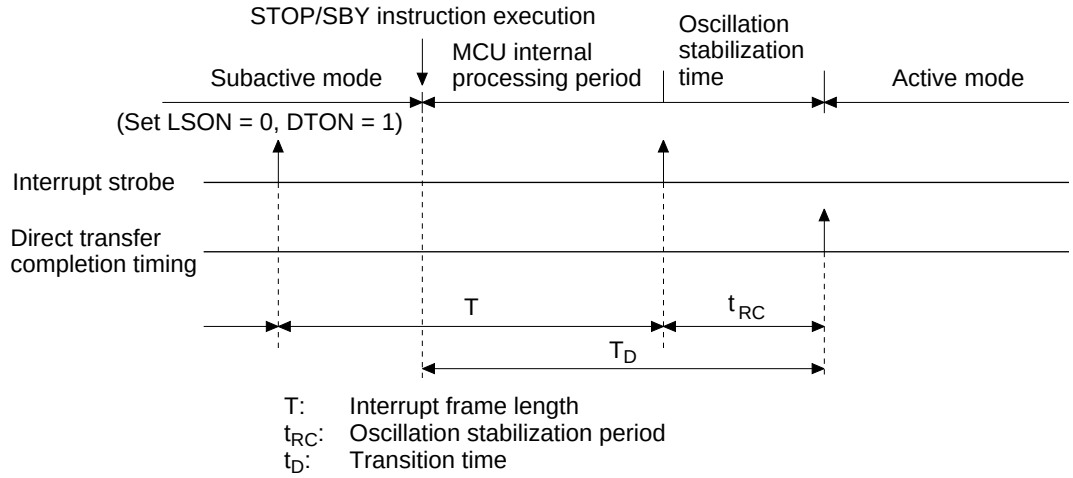


Figure 16 Direct Transition Timing

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by inputting $\overline{\text{STOPC}}$ as well as by $\overline{\text{RESET}}$. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by $\overline{\text{RESET}}$. When stop mode is cancelled by $\overline{\text{RESET}}$, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. $\overline{\text{RESET}}$ can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode is

used after transition to active mode), execute the TEST instruction to the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequence shown in figures 17 to 19. It is reset by an asynchronous $\overline{\text{RESET}}$ input, regardless of its status.

The low-power mode operation sequence is shown in figure 19. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBYinstruction, make sure all interrupt flags are cleared or all interrupts are masked.

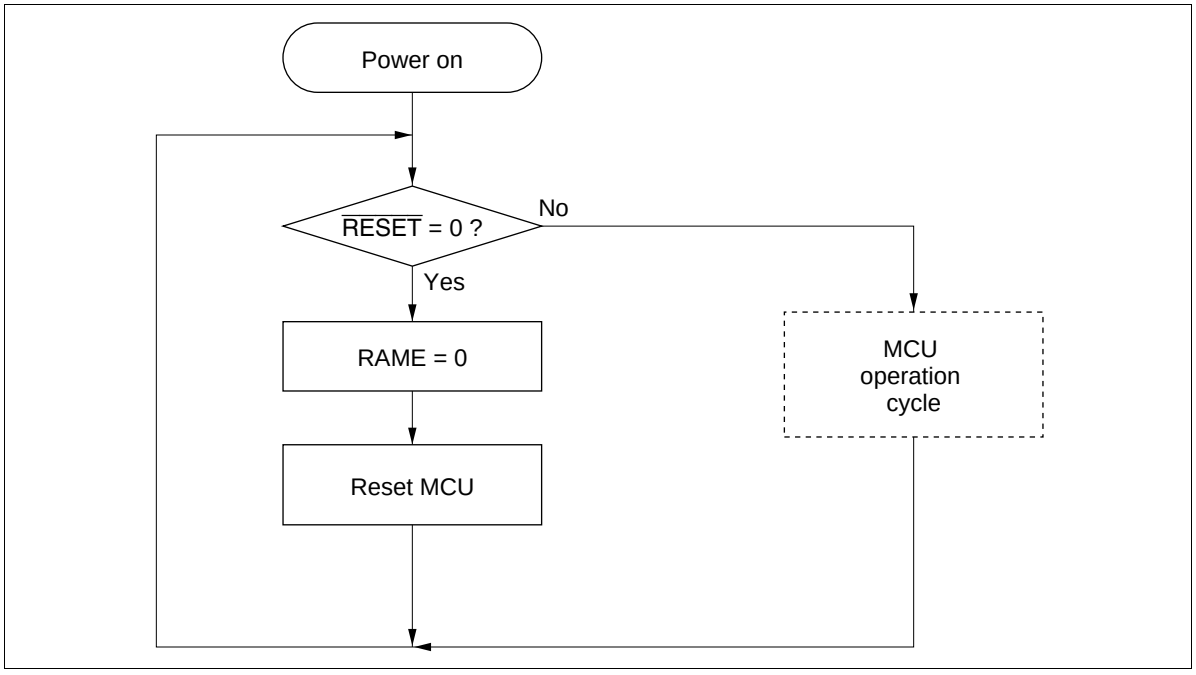


Figure 17 MCU Operating Sequence (Power On)

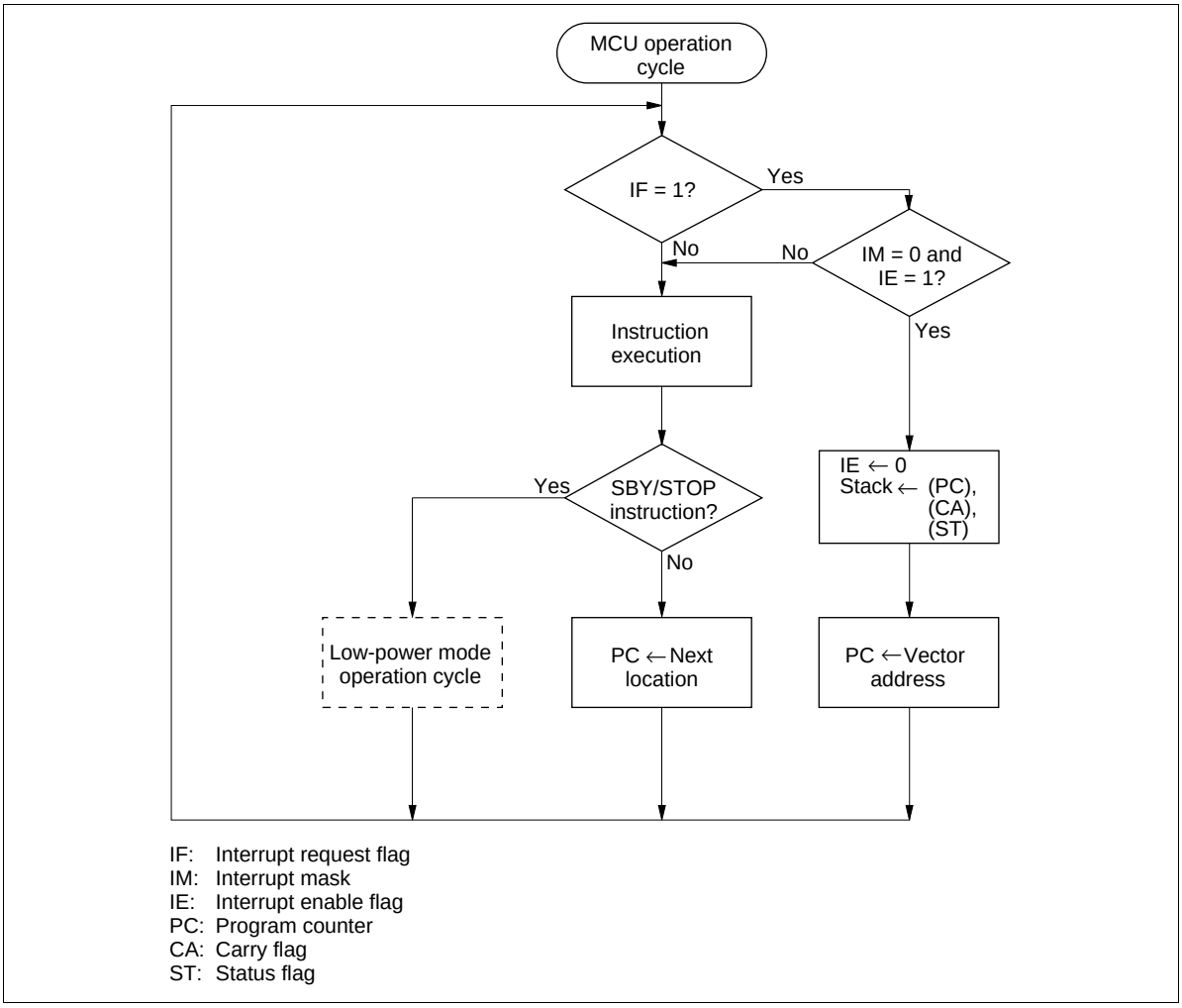


Figure 18 MCU Operating Sequence (MCU Operation Cycle)

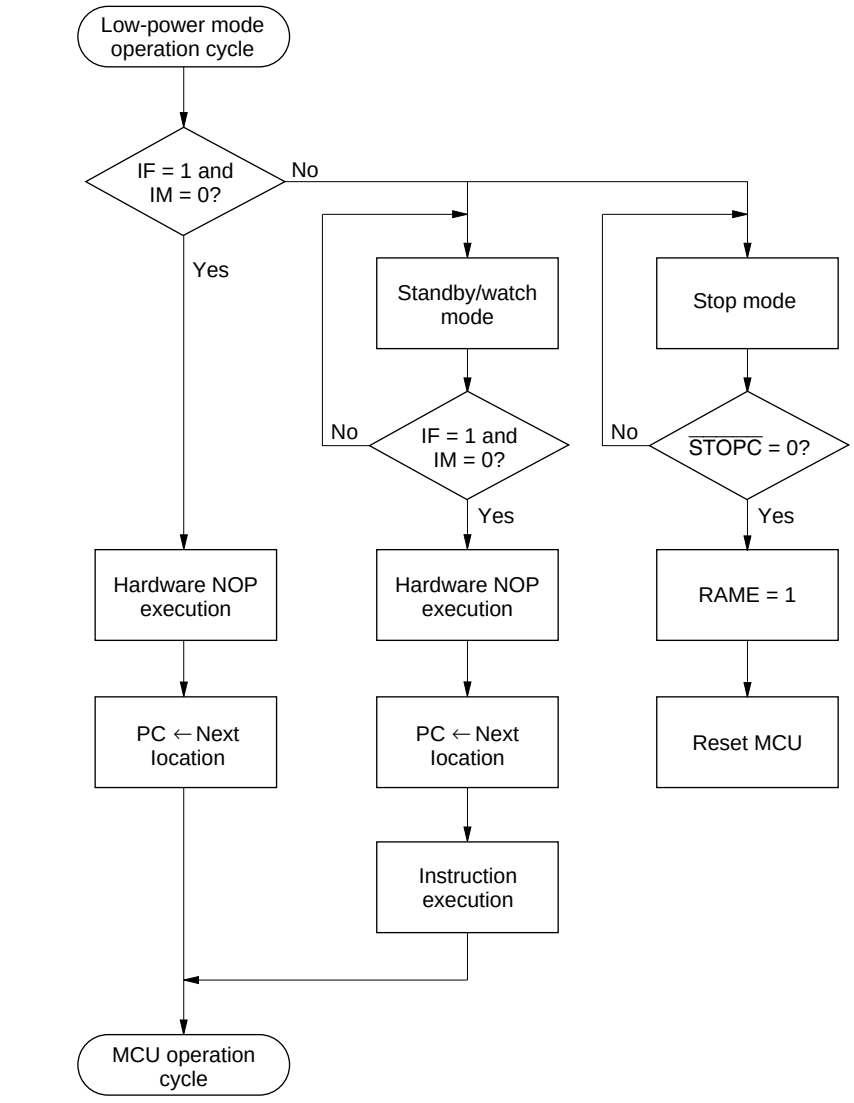


Figure 19 MCU Operating Sequence (Low-Power Mode Operation)

Note: When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Edge detection is shown in figure 20. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected. In figure 21, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either. When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT_0}$ longer than the interrupt frame

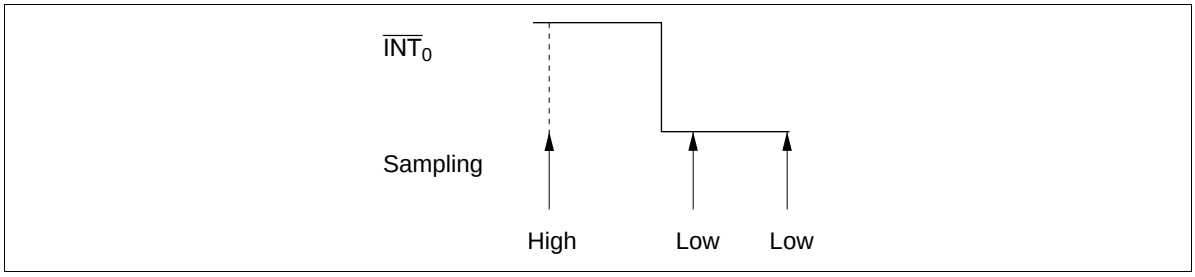


Figure 20 Edge Detection

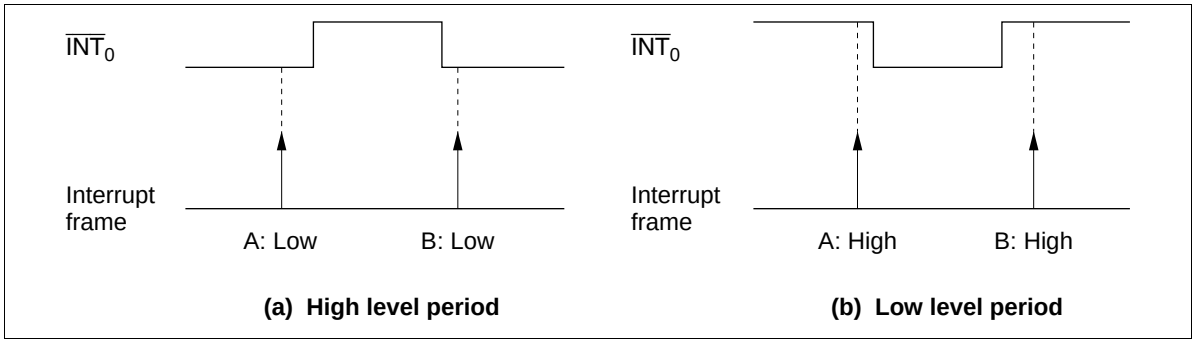


Figure 21 Sampling Example

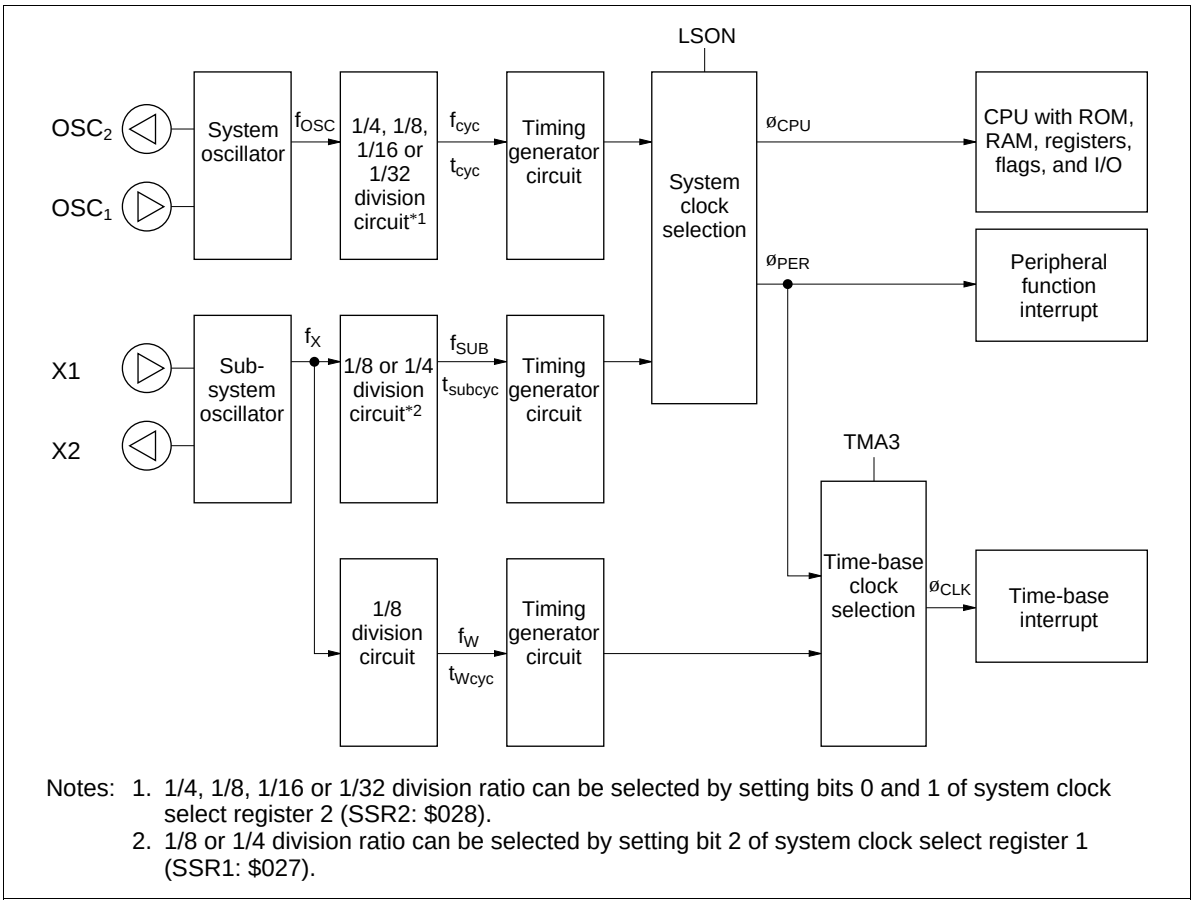
Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 22. As shown in table 20, a ceramic oscillator or crystal oscillator can be connected to OSC_1 and OSC_2, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock.

Registers for Oscillator Circuit Operation

System Clock Selection Register 1 (SSR1: $027): Four bit write-only register which sets the subsystem clock frequency (f_{SUB}) division ratio, and sets the subsystem clock oscillation in stop mode. Bit 1 (SSR11) of system clock select register 1 must be set according to the frequency of the oscillator connected to OSC_1 and OSC_2 (figure 23).

Bit 1 (SSR11) and bit 2 (SSR12) are initialized to 0 on reset and in stop mode. Bit 3 (SSR13) is initialized to 0 only on reset.



Notes: 1. 1/4, 1/8, 1/16 or 1/32 division ratio can be selected by setting bits 0 and 1 of system clock select register 2 (SSR2: $028).
2. 1/8 or 1/4 division ratio can be selected by setting bit 2 of system clock select register 1 (SSR1: $027).

Figure 22 Clock Generation Circuit

System clock selection register 1 (SSR1: $027)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	SSR13*1	SSR12	SSR11*2	Not used

SSR11	System Clock Selection
0	0.4 to 1.0 MHz
1	1.6 to 5.0 MHz (HD404369 Series)
	1.6 to 8.5 MHz (HD40A4369 Series)

SSR12	32-kHz Oscillation Division Ratio Selection
0	$f_{SUB} = f_X/8$
1	$f_{SUB} = f_X/4$

SSR13	32-kHz Oscillation Stop
0	Oscillation operates in stop mode
1	Oscillation stops in stop mode

Notes:
1. SSR13 will only be cleared to 0 by a $\overline{\text{RESET}}$ input. A $\overline{\text{STOPC}}$ input during stop mode will not clear SSR13. Also note that SSR13 will not be cleared upon transition to stop mode.
2. If f_{OSC} = 0.4 to 1.0 MHz, SSR11 must be set 0; if f_{OSC} = 1.6 to 8.5 MHz, SSR11 must be set to 1. Do not use f_{OSC} = 1.0 to 1.6 MHz with 32-kHz oscillation.

Figure 23 System Clock Selection Register 1 (SSR1)

System Clock Selection Register 2 (SSR2: $028): Four bit write-only register which is used to select the system clock divisor (figure 24).

The division ratio of the system clock can be selected as 1/4, 1/8, 1/16, or 1/32 by setting bits 0 and 1 (SSR20, SSR21) of system clock select register 2 (SSR2).

The values of SSR20 and SSR21 are valid after the MCU enters watch mode. The system clock must be stopped when the division ratio is to be changed.

There are two methods for changing the system clock divisor, as follows.

- In active mode, set the divisor by writing to SSR20 and SSR21. At this point, the prior divisor setting will remain in effect. Now, switch to watch mode, and then return to active mode. When active mode resumes, the system clock divisor will have switched to the new value.
- In subactive mode, set the divisor by writing to SSR20 and SSR21. Then return to active mode through watch mode. When active mode resumes, the system clock divisor will have switched to the new value. (The change will also take effect for direct transition to active mode.)

SSR2 is initialized to $0 on reset or in stop mode.

Notes on Usage

If the system clock select register 1 (SSR1: $027) setting does not match the oscillator frequency, the subsystem using the 32.768-kHz oscillation will malfunction.

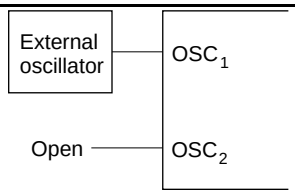
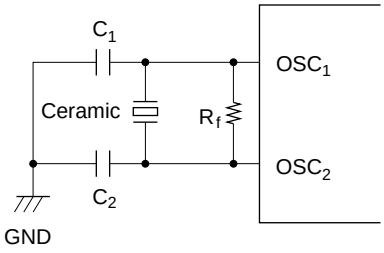
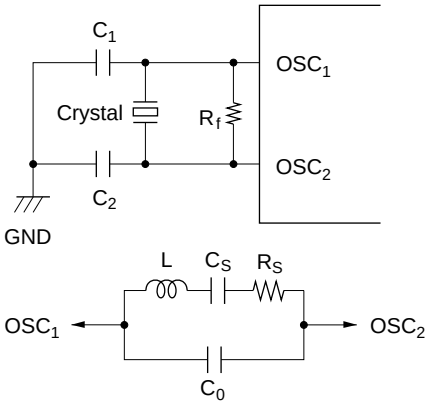
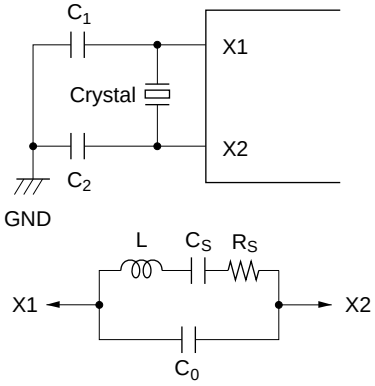
System clock selection register 2 (SSR2: $028)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SSR21	SSR20

SSR21	SSR20	System Clock Division Ratio
0	0	1/4 division
0	1	1/8 division
1	0	1/16 division
1	1	1/32 division

Figure 24 System Clock Selection Register 2 (SSR2)

Table 20 Oscillator Circuit Examples

	Circut Configuration	Circut Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal: Equivalent to circuit shown below C_0 = 7 pF max. R_S = 100 Ω max.
Crystal oscillator (X1, X2)		Crystal: 32.768 kHz: MX38T (Nippon Denpa) $C_1 = C_2$ = 20 pF ±20% R_S = 14 kΩ C_0 = 1.5 pF

Notes: 1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, X1, X2 and elements should be as short as possible, and must not cross other wiring (see figure 25).

3. When a 32.768-kHz crystal oscillator is not used, fix pin X1 to GND and leave pin X2 open.

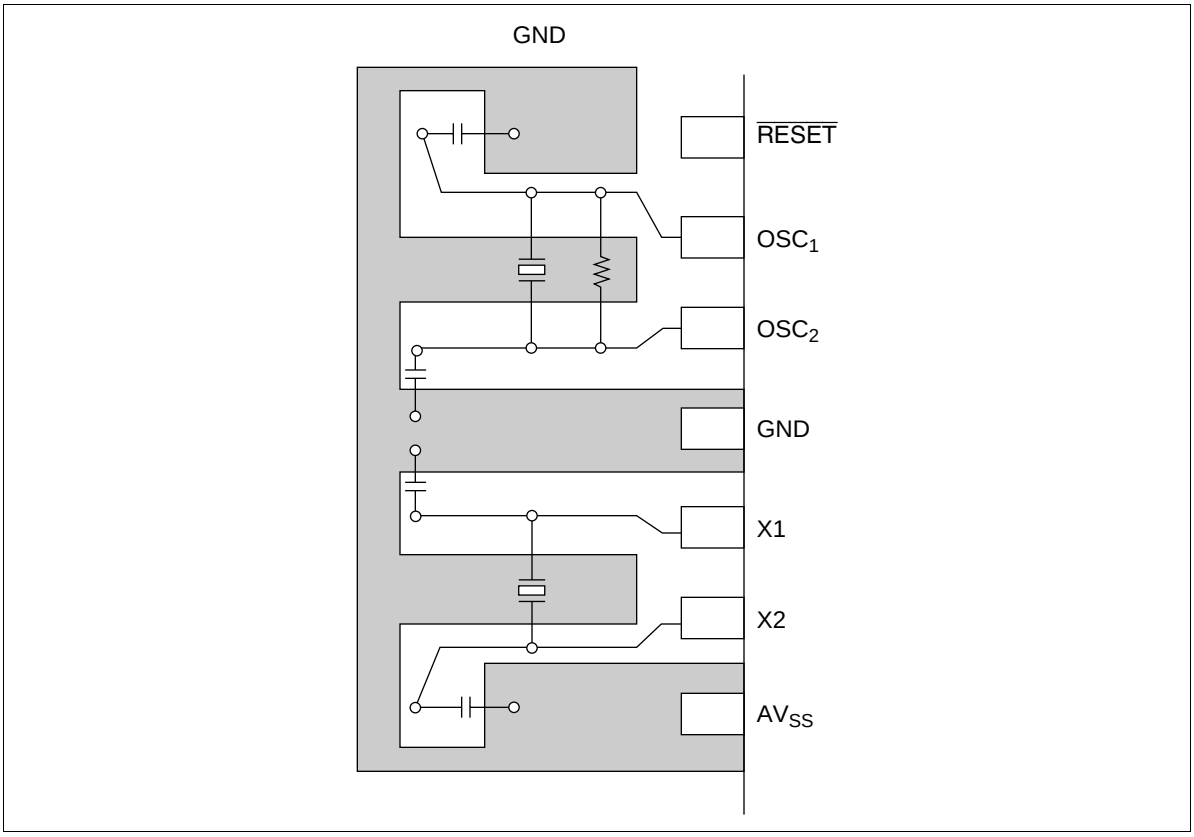


Figure 25 Typical Layout of Crystal and Ceramic Oscillators

Input/Output

The MCU has 53 input/output pins (D_0–D_{13}, R0–R9) and an input pin (RA_1). The features are described below.

- Eight pins (R1–R2) are high-current (15 mA max) input/output with intermediate voltage NMOS open drain pins.
- The D_0–D_4, R0, R3–R5 input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R0_2$/SO pin can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Each input/output pin except for R1 and R2 has a built-in pull-up MOS, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 26, programmable I/O circuits are listed in table 21, and I/O pin circuit types are shown in table 22.

Table 21 Programmable I/O Circuits

MIS3 (bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

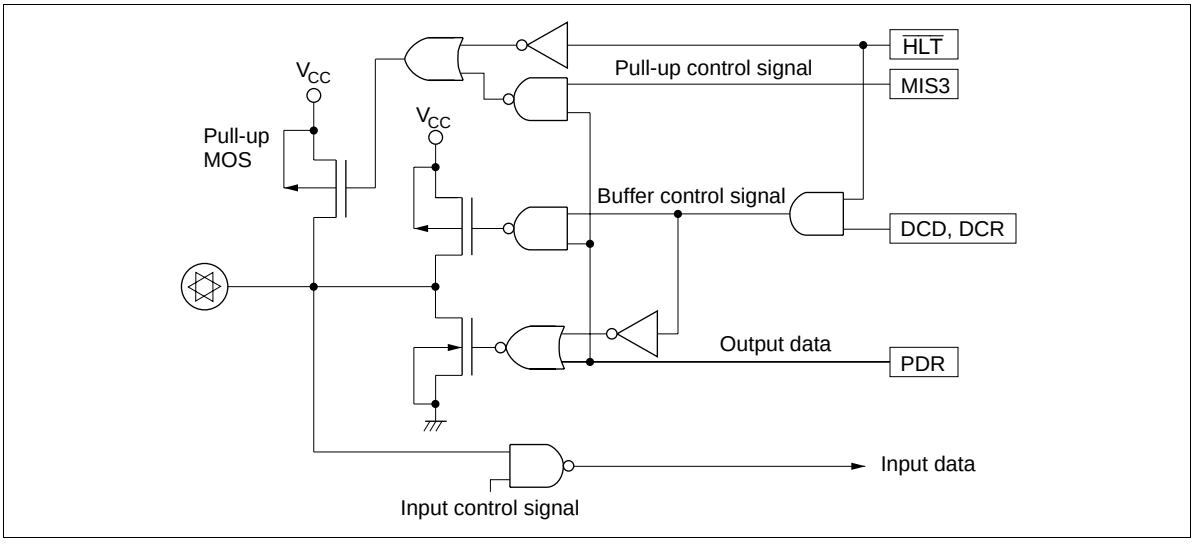
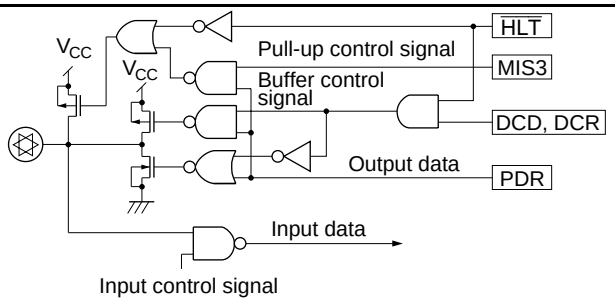
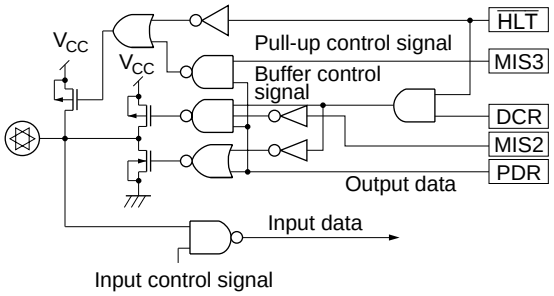
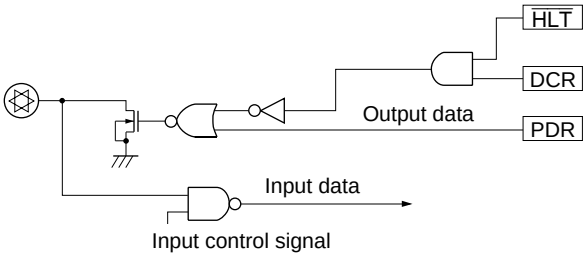
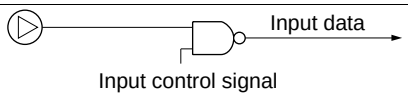
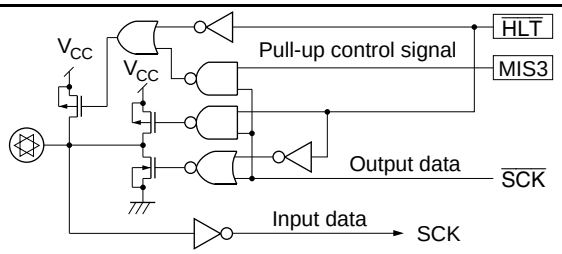
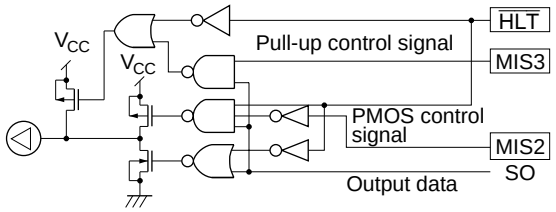
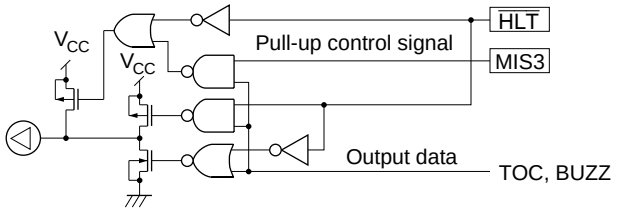
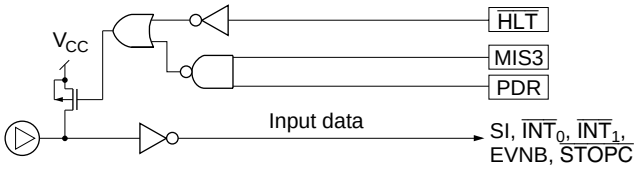
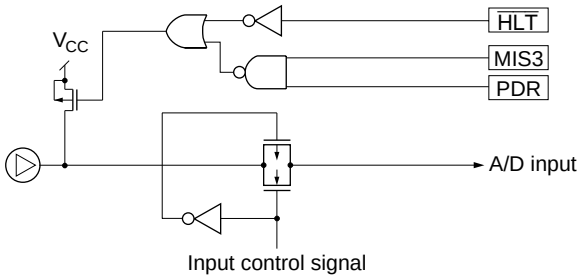


Figure 26 I/O Buffer Configuration

Table 22 Circuit Configuration of I/O Pins

I/O Pin Type	Circuit	Pins
Input/output pins		D_0–D_{13}, $R0_0$, $R0_1$, $R0_3$ $R3_0$–$R9_3$
		$R0_2$
		$R1_0$–$R2_3$
Input pins		RA_1

Notes on next page.

I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/output pins		$\overline{SCK}$
	Output pins		SO
			TOC, BUZZ
	Input pins		SI, $\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
			AN_0–AN_{11}

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins enter the high-impedance state.

2. The $\overline{HLT}$ signal is 1 in active, standby, watch, and subactive modes.

Evaluation Chip Set and ZTAT™/Mask ROM Product Differences

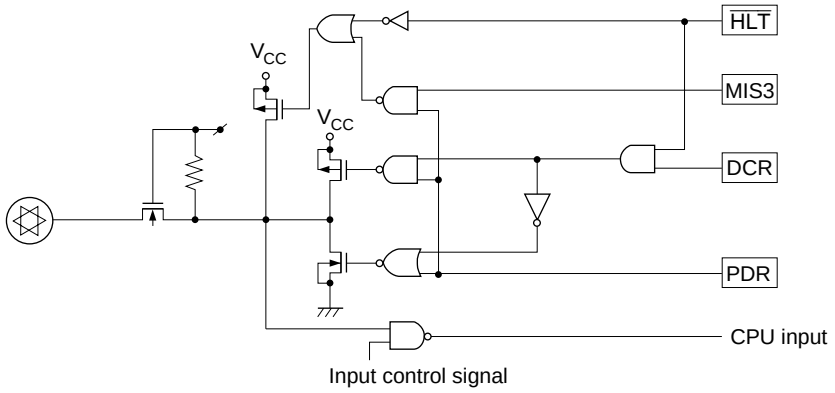
As shown in figure 27, the NMOS intermediate-voltage open drain pin circuit in the evaluation chip set differs from that used in the ZTAT™ microcomputer and built-in mask ROM microcomputer products.

Please note that although these outputs in the ZTAT™ microcomputer and built-in mask ROM microcomputer products can be set to high impedance by the combinations shown in table 23, these outputs cannot be set to high impedance in the evaluation chip set.

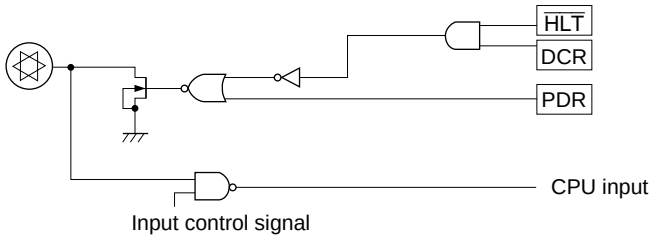
Table 23 Program Control of High Impedance States

Register	Set Value	
DCR	0	1
PDR	*	1

Notes: * An asterisk indicates that the value may be either 0 or 1 and has no influence on circuit operation. This applies to the ZTAT™ and built-in mask ROM microcomputer NMOS open drain pins.



(a) Evaluation Chip Set Circuit Structure



(b) ZTAT™ and Built-In Mask ROM Microcomputer Circuit Structure

Figure 27 NMOS Intermediate-Voltage Open Drain Pin Circuits

D Port (D_0–D_{13}): Consist of 14 input/output pins addressed by one bit.

Pins D_0–D_{13} are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{13} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD3: $02C–$02F) that are mapped to memory addresses (figure 28).

Pins D_0–D_2, D_4 are multiplexed with peripheral function pins $\overline{INT}_0$, $\overline{INT}_1$, EVNB, and $\overline{STOPC}$, respectively. The peripheral function modes of these pins are selected by bits 0–3 (PMRB0– PMRB3) of port mode register B (PMRB: $024) (figure 29).

Pin D_3 is multiplexed with peripheral function pin BUZZ. The peripheral function mode of this pin is selected by bit 3 (PMRA3) of port mode register A (PMRA: $004) (figure 30).

R Ports ($R0_0$–$R9_3$): 39 input/output pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR9: $030–$039) that are mapped to memory addresses (figure 28).

Pin $R0_0$ is multiplexed with peripheral function pin $\overline{SCK}$. The peripheral function mode of this pin is selected by bit 3 (SMR3) of serial mode register (SMR: $005) (figure 31).

Pins $R0_1$–$R0_3$ are multiplexed with peripheral pins SI, SO and TOC, respectively. The peripheral function modes of these pins are selected by bits 0–2 (PMRA0–PMRA2) of port mode register A (PMRA: $004), as shown in figure 30.

Port R3 is multiplexed with peripheral function pins AN_0–AN_3, respectively. The peripheral function modes of these pins can be selected by individual pins, by setting A/D mode register 1 (AMR1: $019) (figure 32).

Ports R4 and R5 are multiplexed with peripheral function pins AN_4–AN_{11}, respectively. The peripheral function modes of these pins can be selected in 4-pin units by setting bits 1 and 2 (AMR21, AMR22) of A/D mode register 2 (AMR2: $01A) (figure 33).

Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 21 and figure 34).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ.

Data control register (DCD0 to 3: $02C to $02F)
(DCR0 to 9: $030 to $039)

DCD0 to DCD3, DCR0 to DCR9

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03–DCD23, DCR03–DCR63, DCR83–DCR93	DCD02–DCD22, DCR02–DCR92	DCD01–DCD31, DCR01–DCR91	DCD00–DCD30, DCR00–DCR90

Bits 0 to 3	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	D_{11}	D_{10}	D_9	D_8
DCD3	Not used	Not used	D_{13}	D_{12}
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	Not used	$R7_2$	$R7_1$	$R7_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$
DCR9	$R9_3$	$R9_2$	$R9_1$	$R9_0$

Figure 28 Data Control Registers (DCD, DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	$D_4/\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

PMRB0	$D_0/\overline{INT}_0$ Mode Selection
0	D_0
1	$\overline{INT}_0$

PMRB1	$D_1/\overline{INT}_1$ Mode Selection
0	D_1
1	$\overline{INT}_1$

Note: * PMRB3 is reset to 0 only by $\overline{RESET}$ input. When $\overline{STOPC}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 29 Port Mode Register B (PMRB)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 30 Port Mode Register A (PMRA)

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0
Transmit clock selection. Refer to figure 62 in the serial interface section.		

Figure 31 Serial Mode Register (SMR)

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR10	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

Figure 32 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	AMR22	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR22	$R5/AN_8$–AN_{11} Pin Selection
0	R5
1	AN_8–AN_{11}

AMR21	$R4/AN_4$–AN_7 Pin Selection
0	R4
1	AN_4–AN_7

Figure 33 A/D Mode Register 2 (AMR2)

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on (refer to table 21)

MIS2	CMOS Buffer On/Off Selection for Pin $R0_2$/SO
0	PMOS active
1	PMOS off

MIS1	MIS0
t_{RC} selection. Refer to figure 15 in the operation modes section.	

Figure 34 Miscellaneous Register (MIS)

Prescalers

The MCU has the following two prescalers, S and W.

The prescaler operating conditions are listed in table 24, and the prescaler output supply is shown in figure 35. The timer A–C input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs the system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and subactive modes and at MCU reset.

Prescaler W: Five-bit counter that inputs the X1 input clock signal (32-kHz crystal oscillation) divided by eight. After being reset to $00 by MCU reset, prescaler W divides the input clock. Prescaler W can be reset by software.

Table 24 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Conditions	Stop Conditions
Prescaler S	System clock (in active and standby mode), subsystem clock (in subactive mode)	MCU reset	MCU reset, stop mode, watch mode
Prescaler W	32-kHz crystal oscillation	MCU reset, software	MCU reset, stop mode

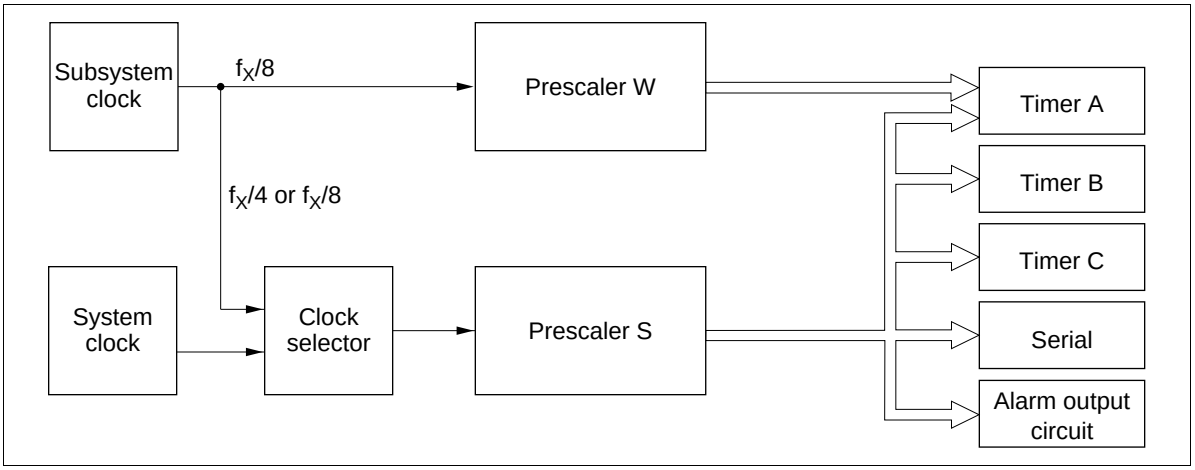


Figure 35 Prescaler Output Supply

Timers

The MCU has four timer/counters (A to C).

- Timer A: Free-running timer
- Timer B: Multifunction timer
- Timer C: Multifunction timer

Timer A is an 8-bit free-running timer. Timers B and C are 8-bit multifunction timers, whose functions are listed in table 25. The operating modes are selected by software.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
- Clock time-base

The block diagram of timer A is shown in figure 36.

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).

  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

- Clock time-base operation: Timer A is used as a clock time-base by setting bit 3 (TMA3) of timer mode register A (TMA: $008) to 1. The prescaler W output is applied to timer A, and timer A generates interrupts at the correct timing based on the 32.768-kHz crystal oscillation. In this case, prescaler W and timer A can be reset to $00 by software.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A’s operating mode and input clock source as shown in figure 37.

Table 25 Timer Functions

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	Prescaler W	Available	—	—
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Time-base	Available	—	—
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available

Note: — implies not available.

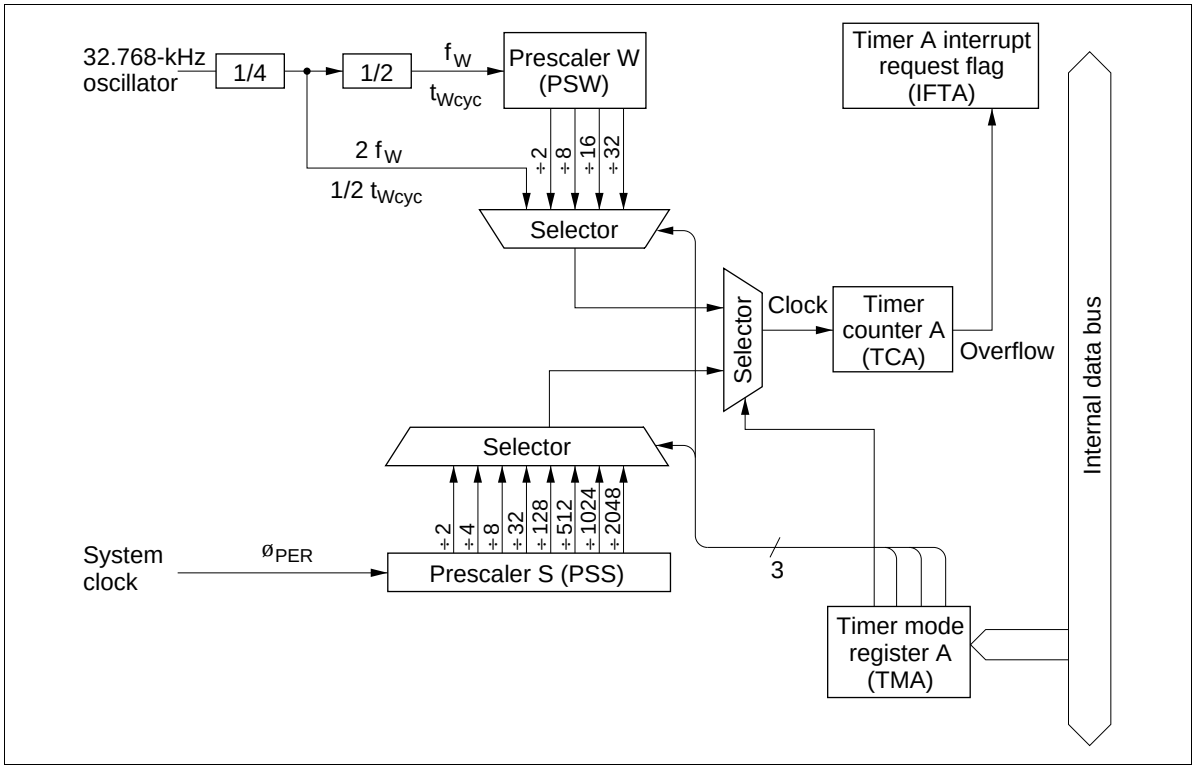


Figure 36 Timer A Block Diagram

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMA3	TMA2	TMA1	TMA0

TMA3	TMA2	TMA1	TMA0	Source Prescaler	Input Clock Frequency	Operating Mode
0	0	0	0	PSS	$2048t_{cyc}$	Timer A mode
			1	PSS	$1024t_{cyc}$	
		1	0	PSS	$512t_{cyc}$	
			1	PSS	$128t_{cyc}$	
	1	0	0	PSS	$32t_{cyc}$	
			1	PSS	$8t_{cyc}$	
		1	0	PSS	$4t_{cyc}$	
			1	PSS	$2t_{cyc}$	
1	0	0	0	PSW	$32t_{Wcyc}$	Time-base mode
			1	PSW	$16t_{Wcyc}$	
		1	0	PSW	$8t_{Wcyc}$	
			1	PSW	$2t_{Wcyc}$	
	1	0	0	PSW	$1/2t_{Wcyc}$	
			1	Inhibited		
		1	Don't care	PSW and TCA reset		

Notes: 1. t_{Wcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 37 Timer Mode Register A (TMA)

Timer B

Timer B Functions: Timer B has the following functions.

- Free-running/reload timer
- External event counter
- Input capture timer

The block diagram for each operation mode of timer B is shown in figures 38 and 39.

Timer B Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the value set in timer write register B (TWBL: $00A, TWBU: $00B) by software and incremented by one at each clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer B is initialized to its initial value set in timer write register B; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0). IFTB is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer B is used as an external event counter by selecting the external event input as an input clock source. In this case, pin D_2/EVNB must be set to EVNB by port mode register B (PMRB: $024).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by timer mode register 2 (TMB2: $026). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer B is incremented by one at each detection edge selected by timer mode register 2 (TMB2: $026). The other operation is basically the same as the free-running/reload timer operation.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVNB.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by timer mode register 2 (TMB2: $026).

  When a trigger edge is input to EVNB, the count of timer B is written to timer read register B (TRBL: $00A, TRBU: $00B), and the timer B interrupt request flag (IFTB: $002, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer B is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer B, or if timer B generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

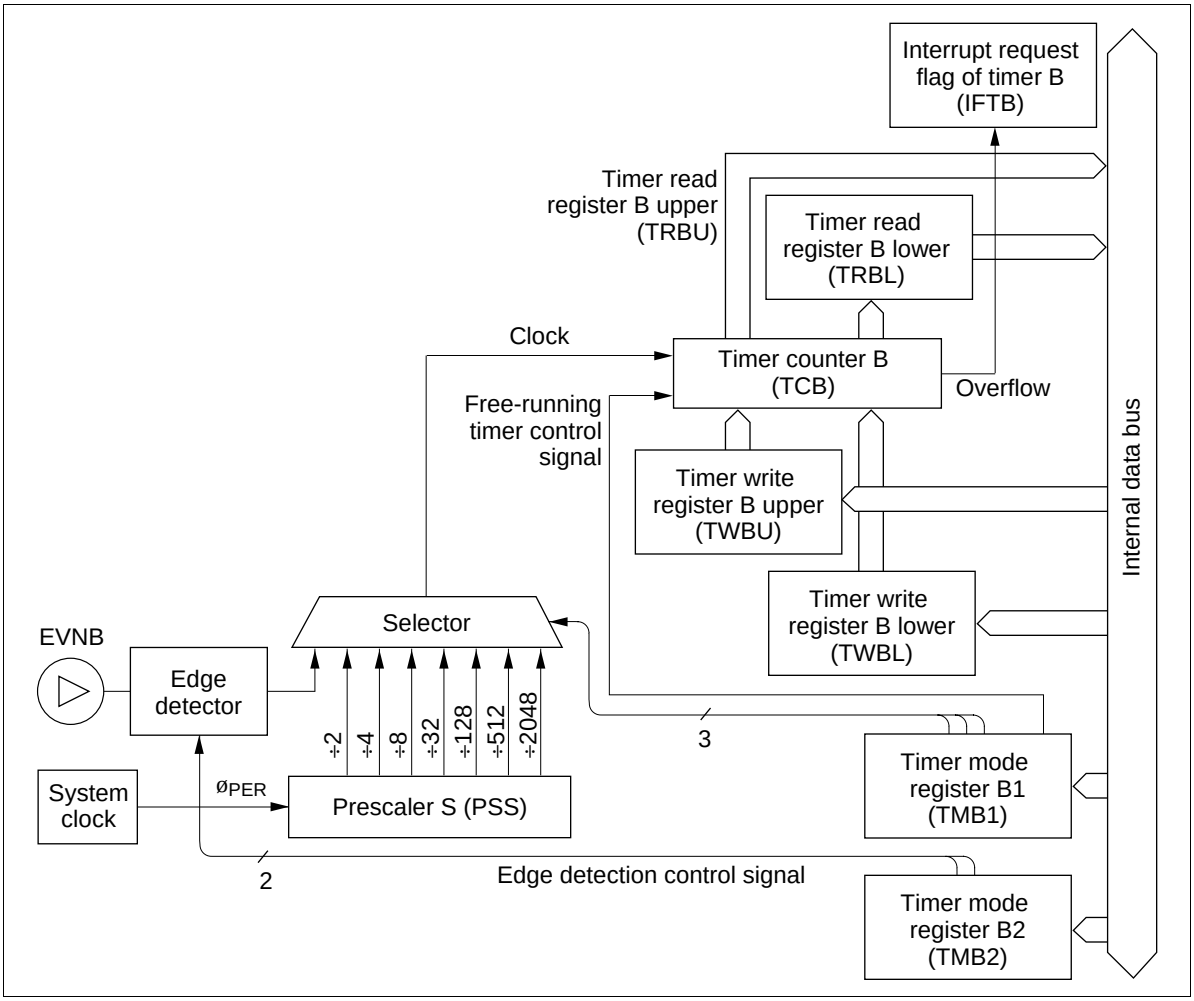


Figure 38 Timer B Free-Running and Reload Operation Block Diagram

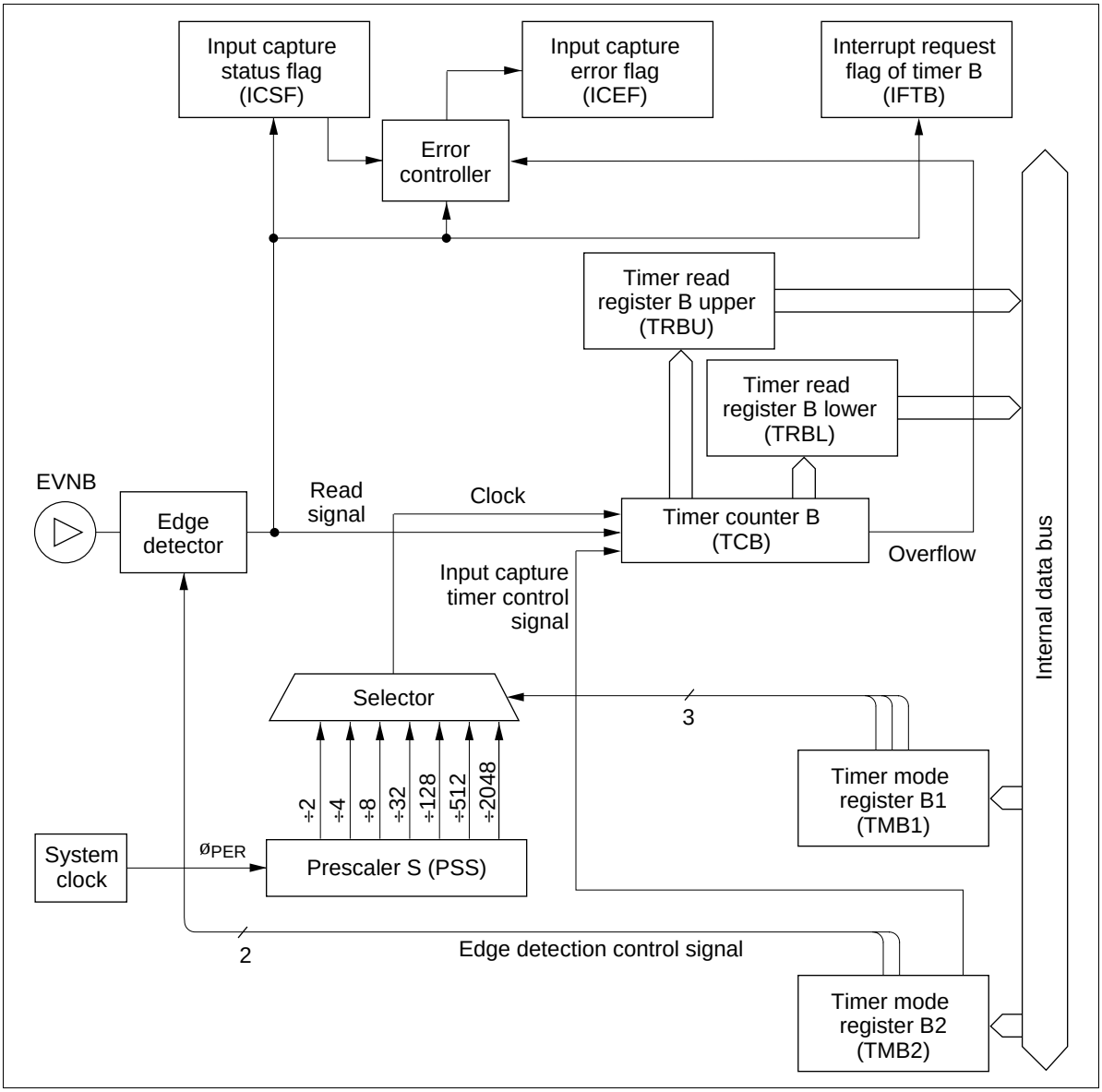


Figure 39 Timer B Input Capture Operation Block Diagram

Registers for Timer B Operation: By using the following registers, timer B operation modes are selected and the timer B count is read and written.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $026)
- Timer write register B (TWBL: $00A, TWBU: $00B)
- Timer read register B (TRBL: $00A, TRBU: $00B)
- Port mode register B (PMRB: $024)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 40. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register B1 write instruction. Setting timer B's initialization by writing to timer write register B (TWBL: $00A, TWBU: $00B) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	D_2/EVNB (external event input)

Figure 40 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $026): Three-bit write-only register that selects the detection edge of signals input to pin EVNB and input capture operation as shown in figure 41. It is reset to $0 by MCU reset.

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU). The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid (figures 42 and 43).

  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit (figures 44 and 45).

  The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

  When the input capture timer operation is selected and if the count of timer B is read after a trigger is input, either the lower or upper digit can be read first.

- Port mode register B (PMRB: $024): Write-only register that selects D_2/EVNB pin function as shown in figure 46. It is reset to $0 by MCU reset.

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-running/reload
1	Input capture

Figure 41 Timer Mode Register B2 (TMB2)

Timer write register B (lower digit) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 42 Timer Write Register B Lower Digit (TWBL)

Timer write register B (upper digit) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 43 Timer Write Register B Upper Digit (TWBU)

Timer read register B (lower digit) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 44 Timer Read Register B Lower Digit (TRBL)

Timer read register B (upper digit) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 45 Timer Read Register B Upper Digit (TRBU)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRB3*	PMRB2	PMRB1	PMRB0

PMRB2	D_2/EVNB Mode Selection
0	D_2
1	EVNB

PMRB3	$D_4/\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

PMRB0	$D_0/\overline{INT}_0$ Mode Selection
0	D_0
1	$\overline{INT}_0$

PMRB1	$D_1/\overline{INT}_1$ Mode Selection
0	D_1
1	$\overline{INT}_1$

Note: * PMRB3 is reset to 0 only by $\overline{RESET}$ input. When $\overline{STOPC}$ is input in stop mode, PMRB3 is not reset but retains its value.

Figure 46 Port Mode Register B (PMRB)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (PWM output)

The block diagram of timer C is shown in figure 47.

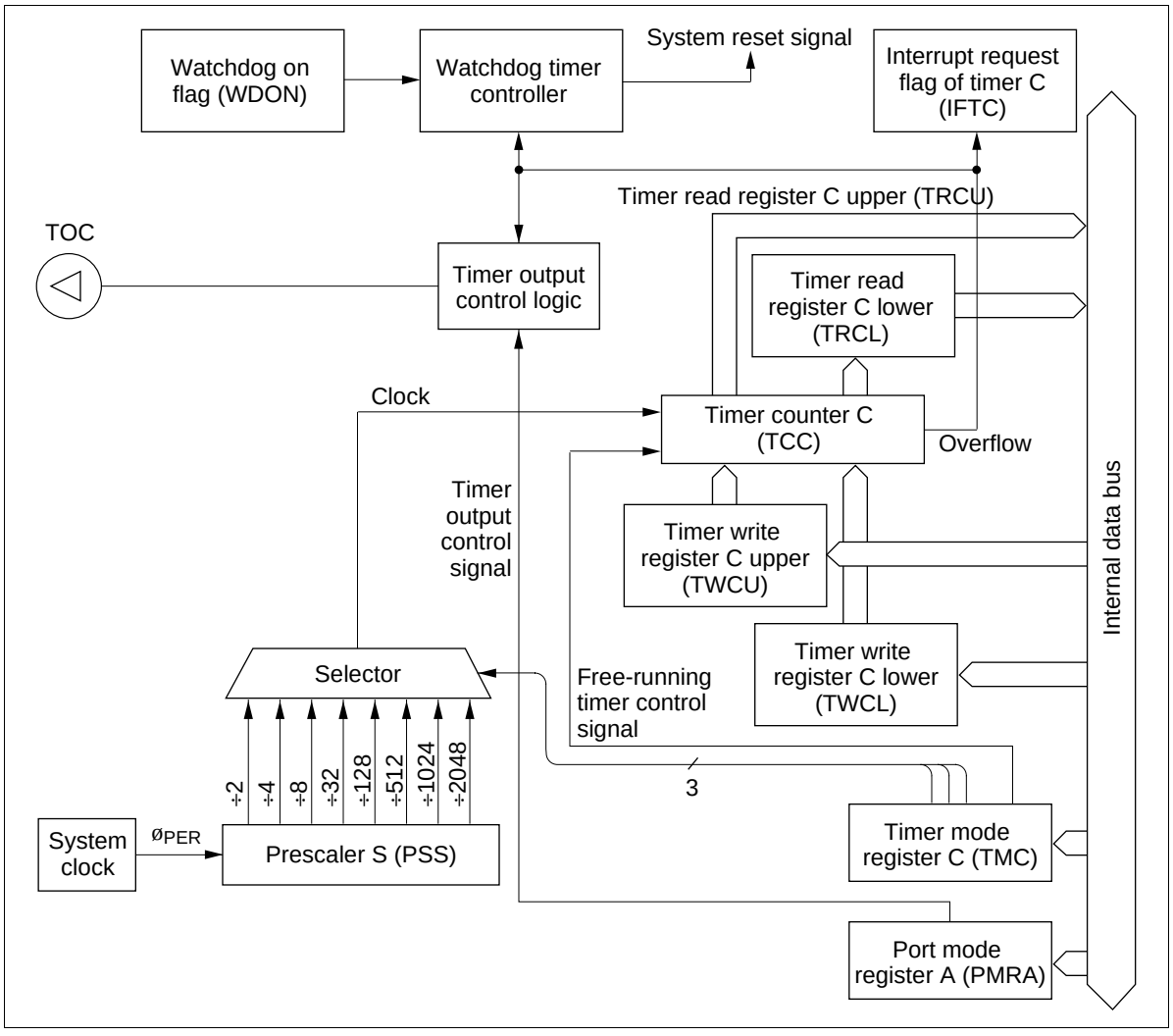


Figure 47 Timer C Block Diagram

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C (TMC: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. The watchdog timer operation flowchart is shown in figure 48. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The PWM output modes can be selected for timer C by setting port mode register A (PMRA: $004).

  By selecting the timer output mode, pin $R0_3$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

  PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C (TMC: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 49.

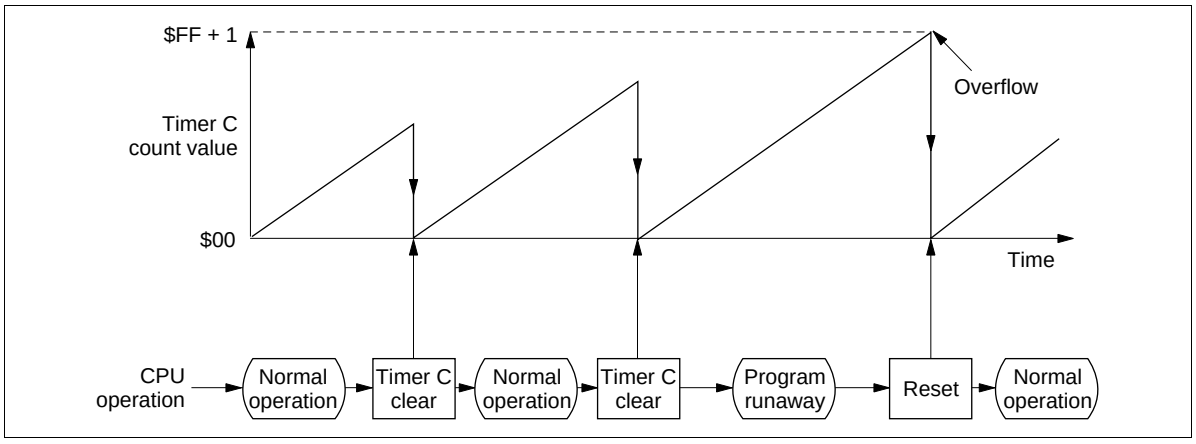
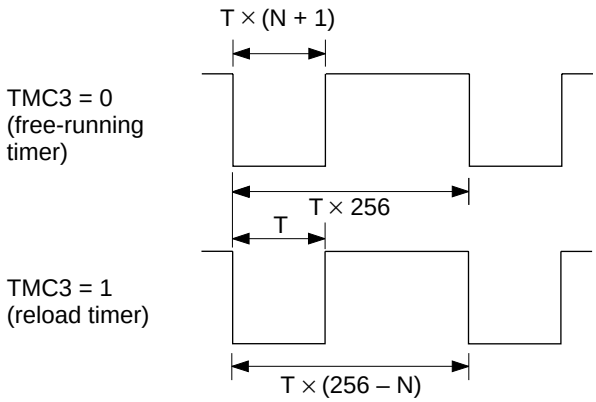


Figure 48 Watchdog Timer Operation Flowchart



Notes: T: Input clock period supplied to counter. (The clock source and system clock division ratio are determined by timer mode register C.)

N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 49 PWM Output Waveform

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

- Timer mode register C (TMC: $00D)
- Port mode register A (PMRA: $004)
- Timer write register C (TWCL: $00E, TWCU: $00F)
- Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C (TMC: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 50. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 50 Timer Mode Register C (TMC)

- Port mode register A (PMRA: $004): Write-only register that selects $R0_3$/TOC pin function as shown in figure 51. It is reset to $0 by MCU reset.
- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of the lower digit (TWCL) and the upper digit (TWCU) as shown in figures 52 and 53. The operation of timer write register C is basically the same as that of timer write register B (TWBL: $00A, TWBU: $00B).
- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of the lower digit (TRCL) and the upper digit (TRCU) that holds the count of the timer C upper digit (figures 54 and 55). The operation of timer read register C is basically the same as that of timer read register B (TRBL: $00A, TRBU: $00B).

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	PMRA3	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA3	D_3/BUZZ Mode Selection
0	D_3
1	BUZZ

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 51 Port Mode Register A (PMRA)

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 52 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 53 Timer Write Register C Upper Digit (TWCU)

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 54 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

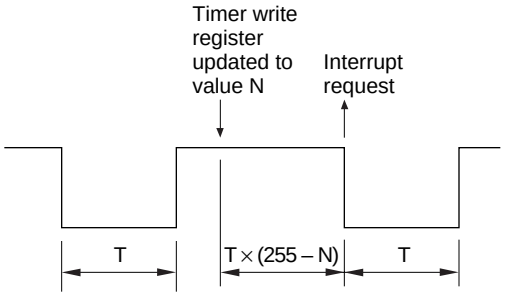
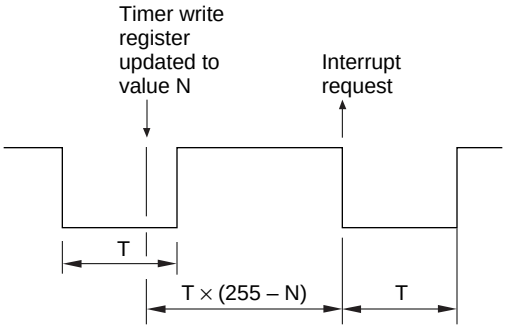
Figure 55 Timer Read Register C Upper Digit (TRCU)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 26. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

In this case, the lower digit (TWCL) must be written to first, bit writing only to the lower digit does not change the timer C value. Timer C is changed to the value in timer write register B at the same time the upper digit (TWCU) is written to.

Table 26 PWM Output Following Update of Timer Write Register

Mode	PWM Output: Timer Write Register is Updated during High PWM Output	PWM Output: Timer Write Register is Updated during Low PWM Output
Reload		

Alarm Output Function

The MCU has a built-in pulse output function called BUZZ. The pulse frequency can be selected from the prescaler S's outputs, and the output frequency depends on the state of port mode register C (PMRC: $025). The duty cycle of the pulse output is fixed at 50%.

Port Mode Register C (PMRC: $025): Four-bit write-only register that selects the alarm frequencies as shown in figure 57. It is reset to $0 by MCU reset.

Port Mode Register A (PMRA: $004): Four-bit write-only register that selects D_3/BUZZ pin function as shown in figure 51. It is reset to $0 by MCU reset.

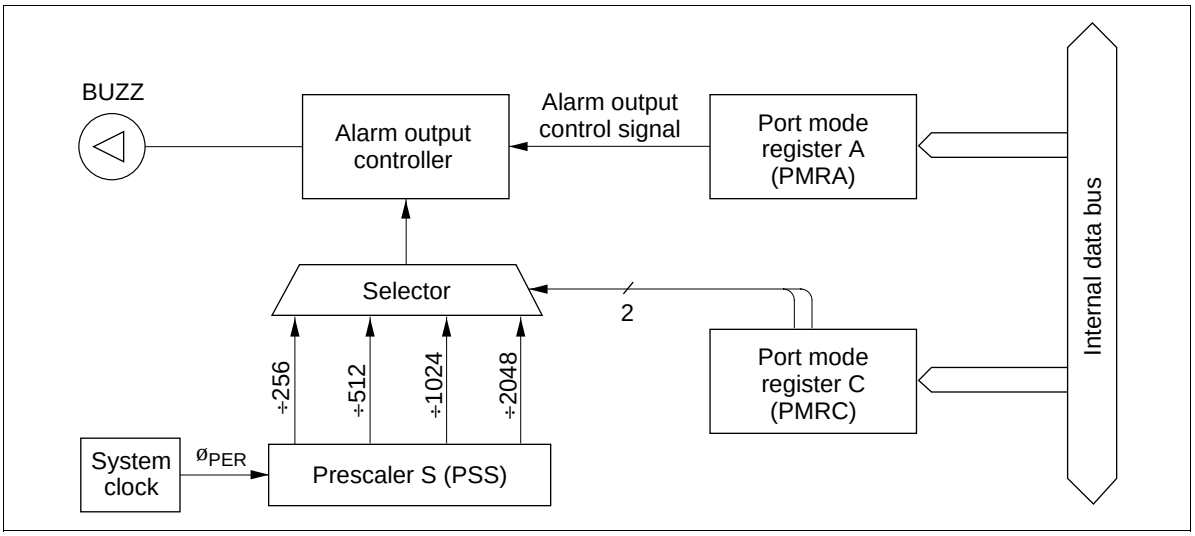


Figure 56 Alarm Output Function Block Diagram

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	Undefined	0
Read/Write	W	W	W	W
Bit name	PMRC3	PMRC2	PMRC1	PMRC0

PMRC3	PMRC2	System Clock Divisor
0	0	÷2048
	1	÷1024
1	0	÷512
	1	÷256

PMRC0	Serial Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 57 Port Mode Register C (PMRC)

Serial Interface

The serial interface serially transfers and receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Four registers, an octal counter, and a selector are also configured for the serial interface as follows.

- Serial data register (SRL: $006, SRU: $007)
- Serial mode register (SMR: $005)
- Port mode register A (PMRA: $004)
- Port mode register C (PMRC: $025)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

The block diagram of the serial interface is shown in figure 58.

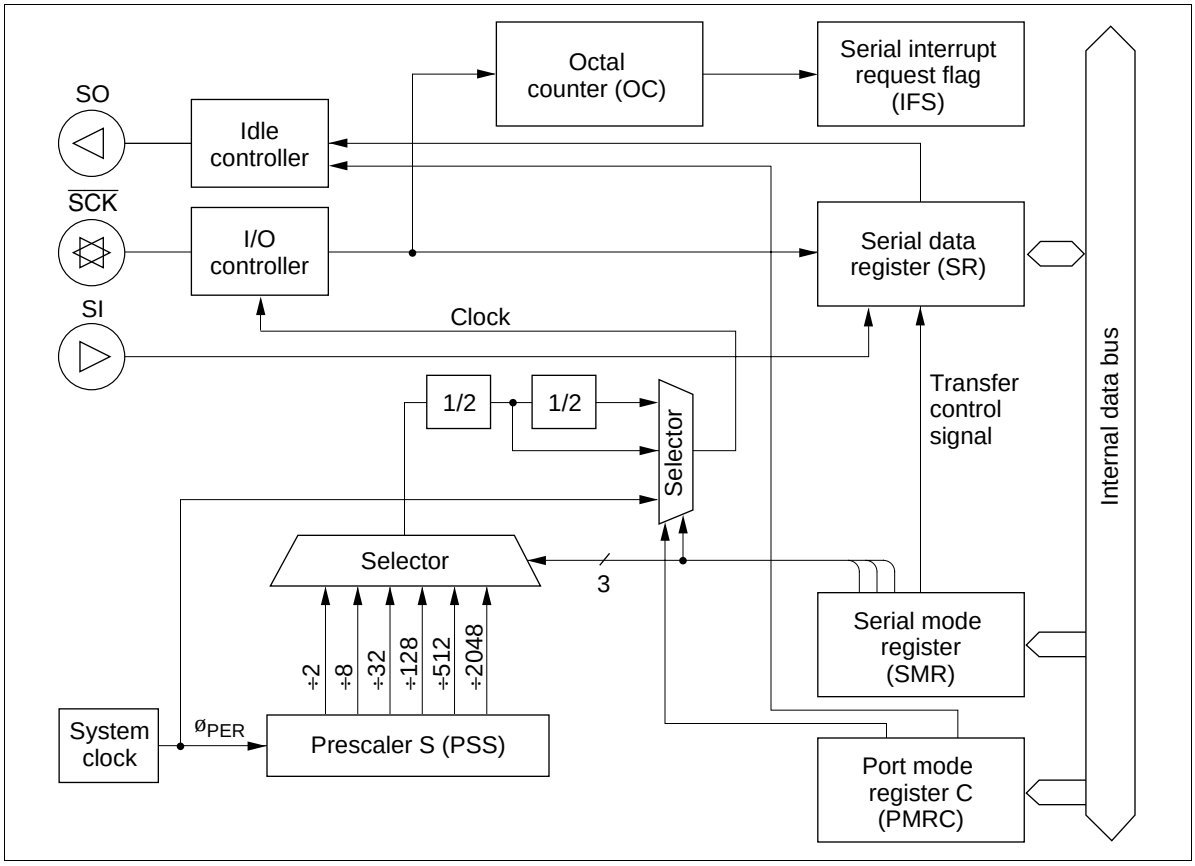


Figure 58 Serial Interface Block Diagram

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 27 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004) and the serial mode register (SMR: $005) settings; to change the operating mode, always initialize the serial interface internally by writing data to the serial mode register. Note that the serial interface is initialized by writing data to the serial mode register. Refer to the following Serial Mode Register section for details.

Pin Setting: The $R0_0/\overline{SCK}$ pin is controlled by writing data to the serial mode register (SMR: $005). The $R0_1$/SI and $R0_2$/SO pins are controlled by writing data to port mode register A (PMRA: $004). Refer to the following Registers for Serial Interface section for details.

Transmit Clock Source Setting: The transmit clock source is set by writing data to the serial mode register (SMR: $005) and port mode register C (PMRC: $025). Refer to the following Registers for Serial Interface section for details.

Data Setting: Transmit data is set by writing data to the serial data register (SRL: $006, SRU, $007). Receive data is obtained by reading the contents of the serial data register. The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO pin is invalid until the first data is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, and it increments at the rising edge of the transmit clock. When the eighth transmit clock signal is input or when serial transmission/receive is discontinued, the octal counter is reset to 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and the transfer stops.

When the prescaler output is selected as the transmit clock, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SMR0– SMR2) of serial mode register (SMR: $005) and bit 0 (PMRC0) of port mode register C (PMRC: $025) as listed in table 28.

Operating States: The serial interface has the following operating states; transitions between them are shown in figure 59.

- STS wait state
- Transmit clock wait state
- Transfer state
- Continuous clock output state (only in internal clock mode)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 59). In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), the serial interface enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is the period between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts the serial data register, and puts the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to the serial mode register (SMR: $005) (04, 14) in transmit clock wait state.

- Transfer state: Transfer state is the period between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

  In transfer state, writing data to the serial mode register (SMR: $005) (06, 16) initializes the serial interface, and STS wait state is entered.

  If the state changes from transfer to another state, the serial interrupt request flag (IFS: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{SCK}$ pin.

When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If the serial mode register (SMR: $005) is written to in continuous clock output mode (18), STS wait state is entered.

Output Level Control in Idle States: In idle states, that is, STS wait state and transmit clock wait state, the output level of the SO pin can be controlled by setting bit 1 (PMRC1) of port mode register C (PMRC: $025) to 0 or 1. The output level control example is shown in figure 60. Note that the output level cannot be controlled in transfer state.

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 61.

Table 27 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

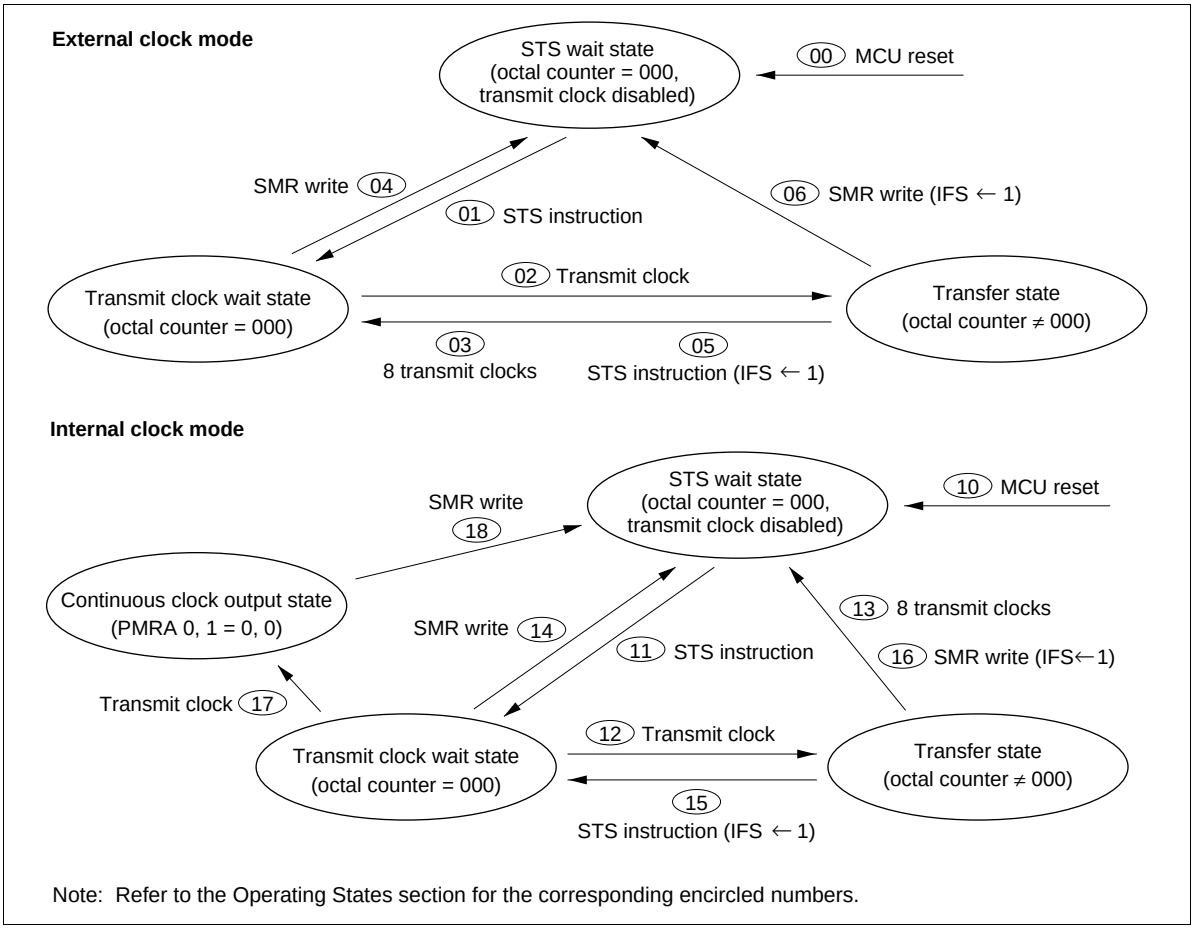
Table 28 Serial Transmit Clock (Prescaler Output)

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer completion processing is performed and IFS is reset, writing to the serial mode register (SMR: $005) changes the state from transfer to STS wait. At this time IFS is set again, and therefore the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to the serial mode register (SMR: $005) again.
- Serial interrupt request flag (IFS: $003, bit 2) set: If the state is changed from transfer to another by writing to the serial mode register (SMR: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag is not set. To set the serial interrupt request flag, serial mode register write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}$ pin is at 1, that is, after executing the input instruction to port R0.



Note: Refer to the Operating States section for the corresponding encircled numbers.

Figure 59 Serial Interface State Transitions

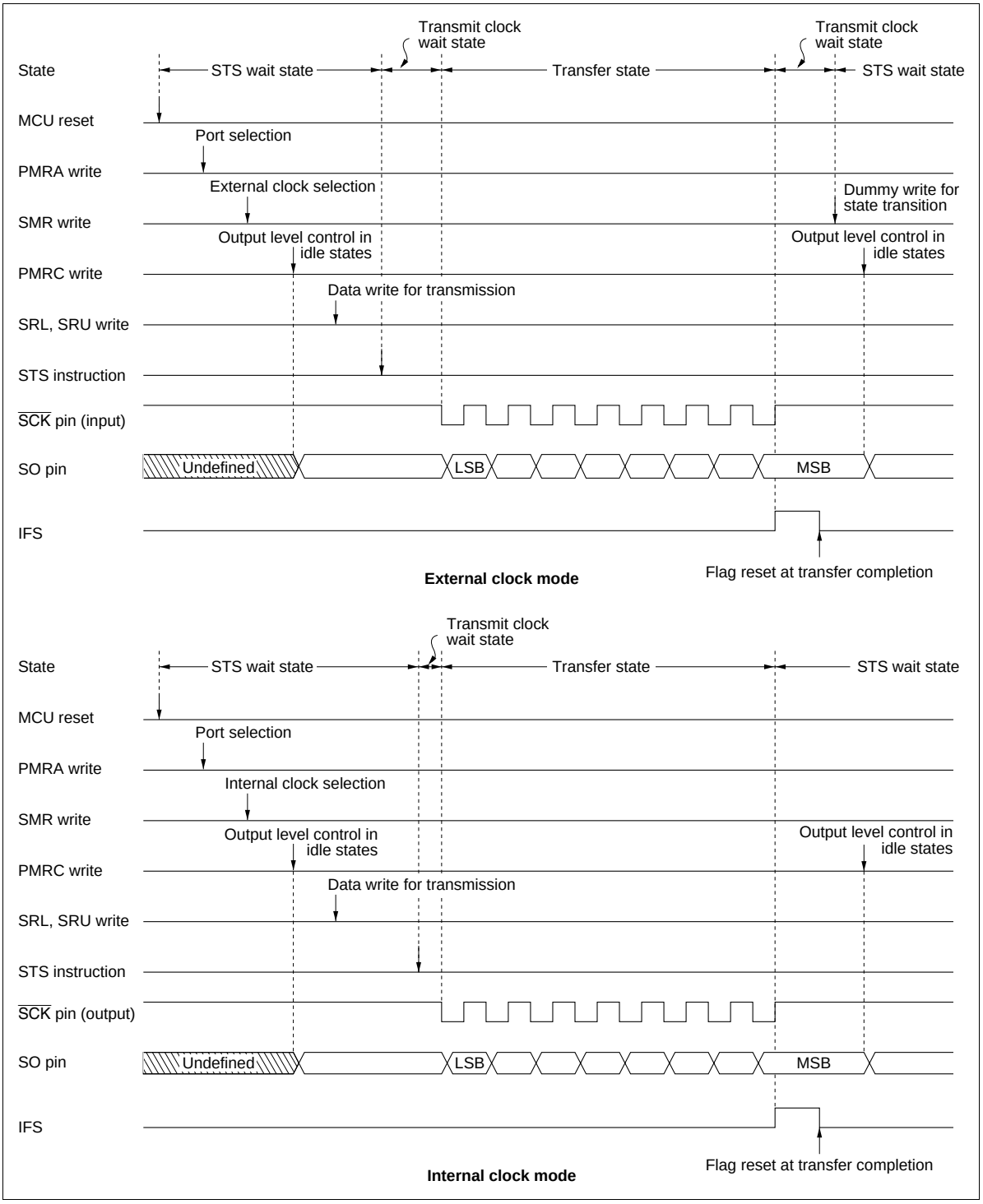
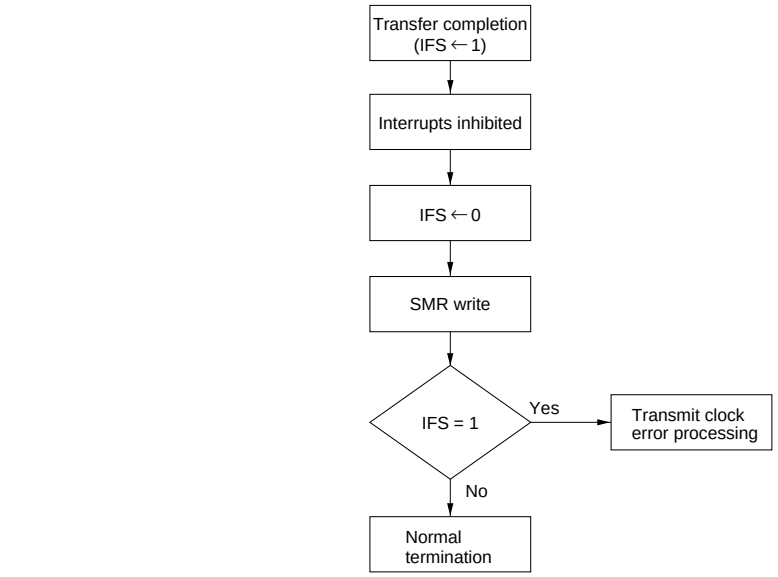
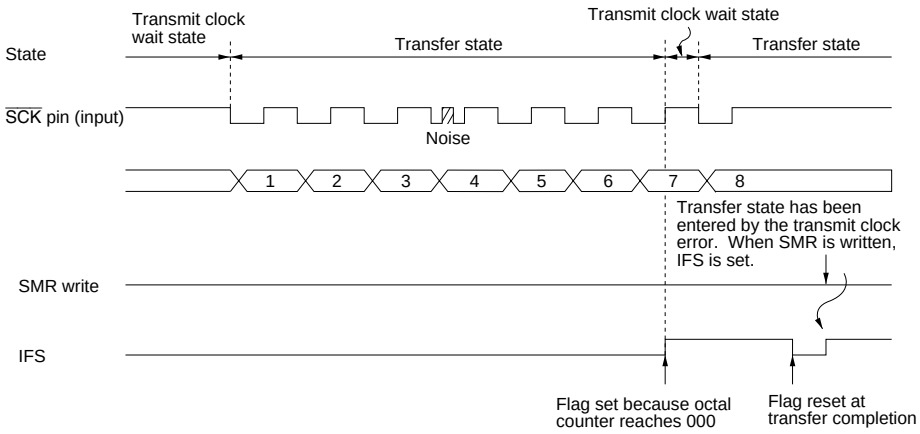


Figure 60 Example of Serial Interface Operation Sequence



Transmit clock error detection flowchart



Transmit clock error detection procedure

Figure 61 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

- Serial Mode Register (SMR: $005)
- Serial Data Register (SRL: $006, SRU: $007)
- Port Mode Register A (PMRA: $004)
- Port Mode Register C (PMRC: $025)
- Miscellaneous Register (MIS: $00C)

Serial Mode Register (SMR: $005): This register has the following functions (figure 62).

- $R0_0/\overline{SCK}$ pin function selection
- Transmit clock selection
- Prescaler division ratio selection
- Serial interface initialization

Serial mode register (SMR: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register (SMR: $005) discontinues the input of the transmit clock to the serial data register and octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial interrupt request flag (IFS: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	Refer to table 28
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 62 Serial Mode Register (SMR)

Port Mode Register C (PMRC: $025): This register has the following functions (figure 63).

- Prescaler division ratio selection
- Output level control in idle states

Port mode register C (PMRC: $025) is a 4-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (PMRC0) of this register, the prescaler division ratio is selected. Bit 0 (PMRC0) can be reset to 0 by MCU reset. By setting bit 1 (PMRC1), the output level of the SO pin is controlled in idle states. The output level changes at the same time that PMRC1 is written to.

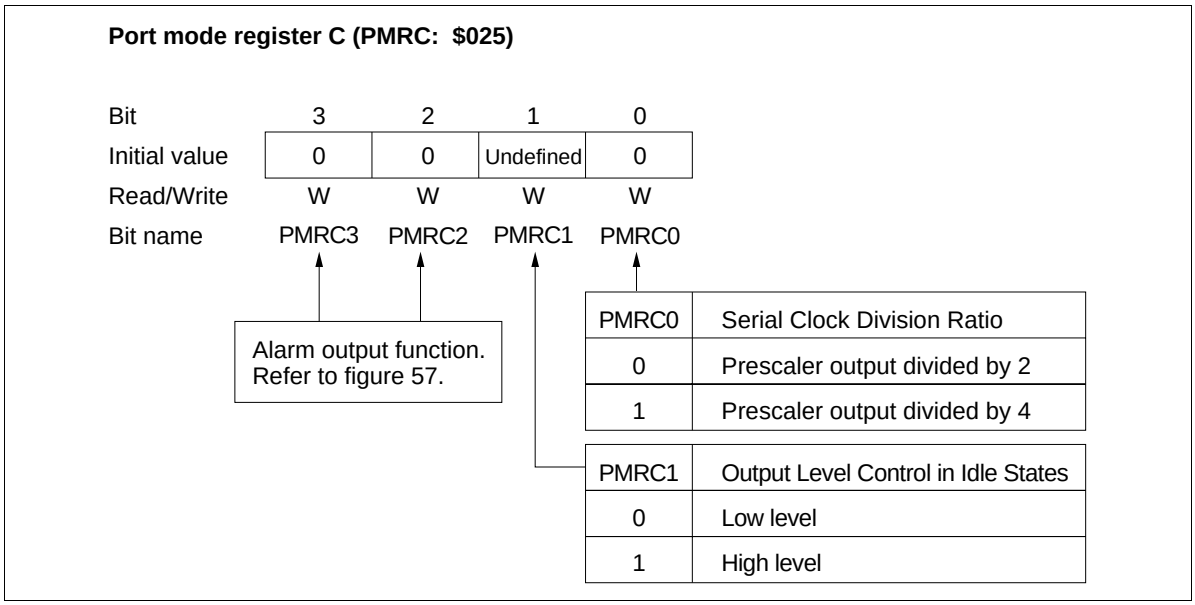


Figure 63 Port Mode Register C (PMRC)

Serial Data Register (SRL: $006, SRU: $007): This register has the following functions (figures 64 and 65).

- Transmission data write and shift
- Receive data shift and read

Writing data in this register is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 66.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register (lower digit) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 64 Serial Data Register (SRL)

Serial data register (upper digit) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 65 Serial Data Register (SRU)

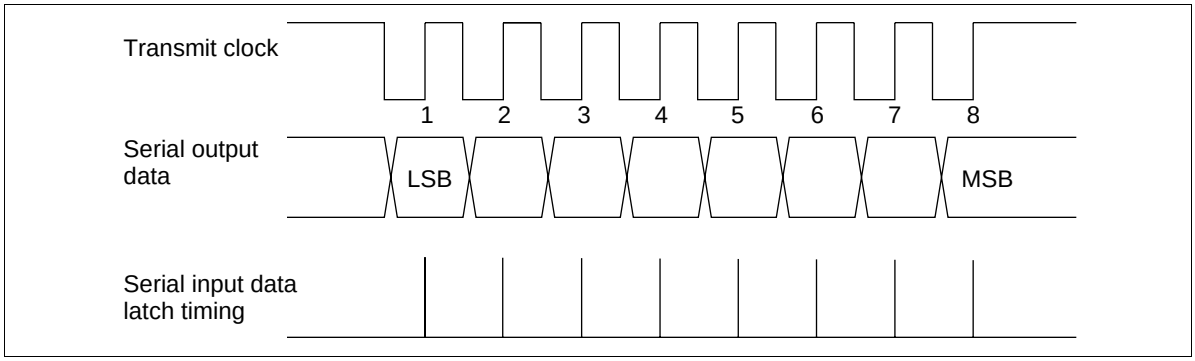


Figure 66 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 67).

- $R0_1$/SI pin function selection
- $R0_2$/SO pin function selection

Port mode register A (PMRA: $004) is a 4-bit write-only register, and is reset to $0 by MCU reset.

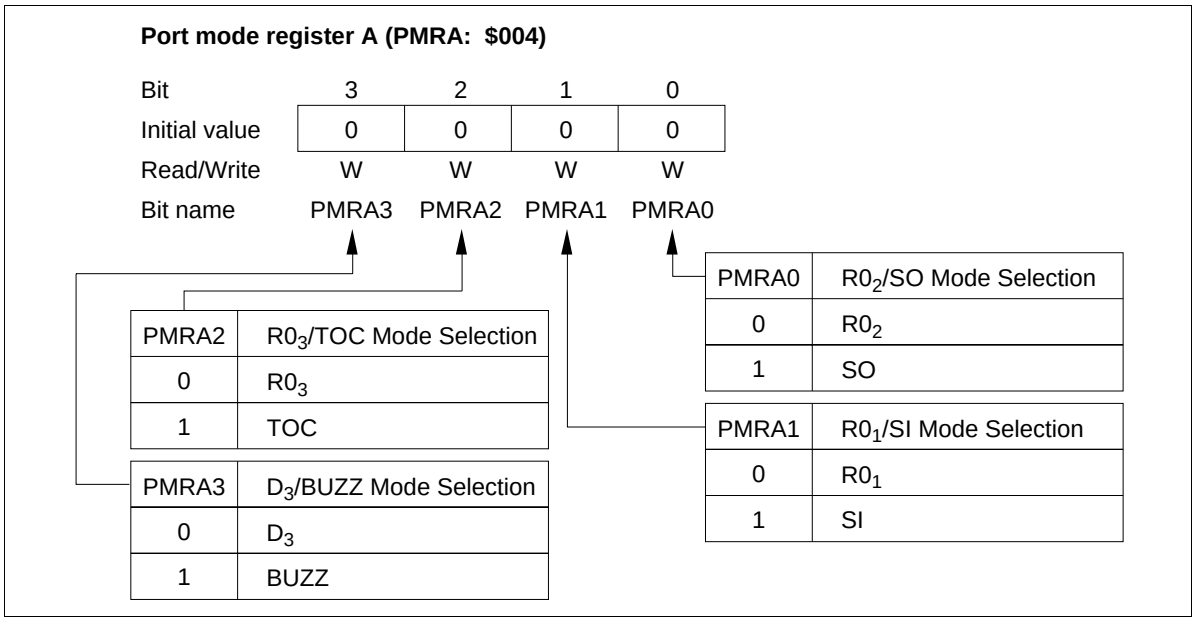


Figure 67 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 68).

- $R0_2$/SO pin PMOS control

Miscellaneous register (MIS: $00C) is a 4-bit write-only register and is reset to $0 by MCU reset.

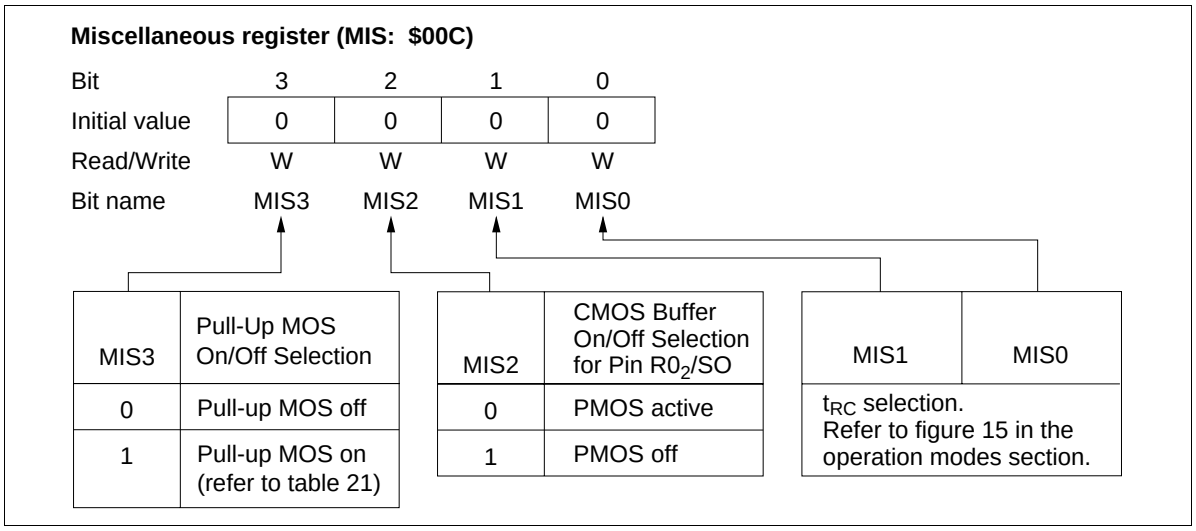


Figure 68 Miscellaneous Register (MIS)

A/D Converter

The MCU has a built-in A/D converter that uses a sequential comparison method with a resistor ladder. It can measure twelve analog inputs with 8-bit resolution. The block diagram of the A/D converter is shown in figure 69.

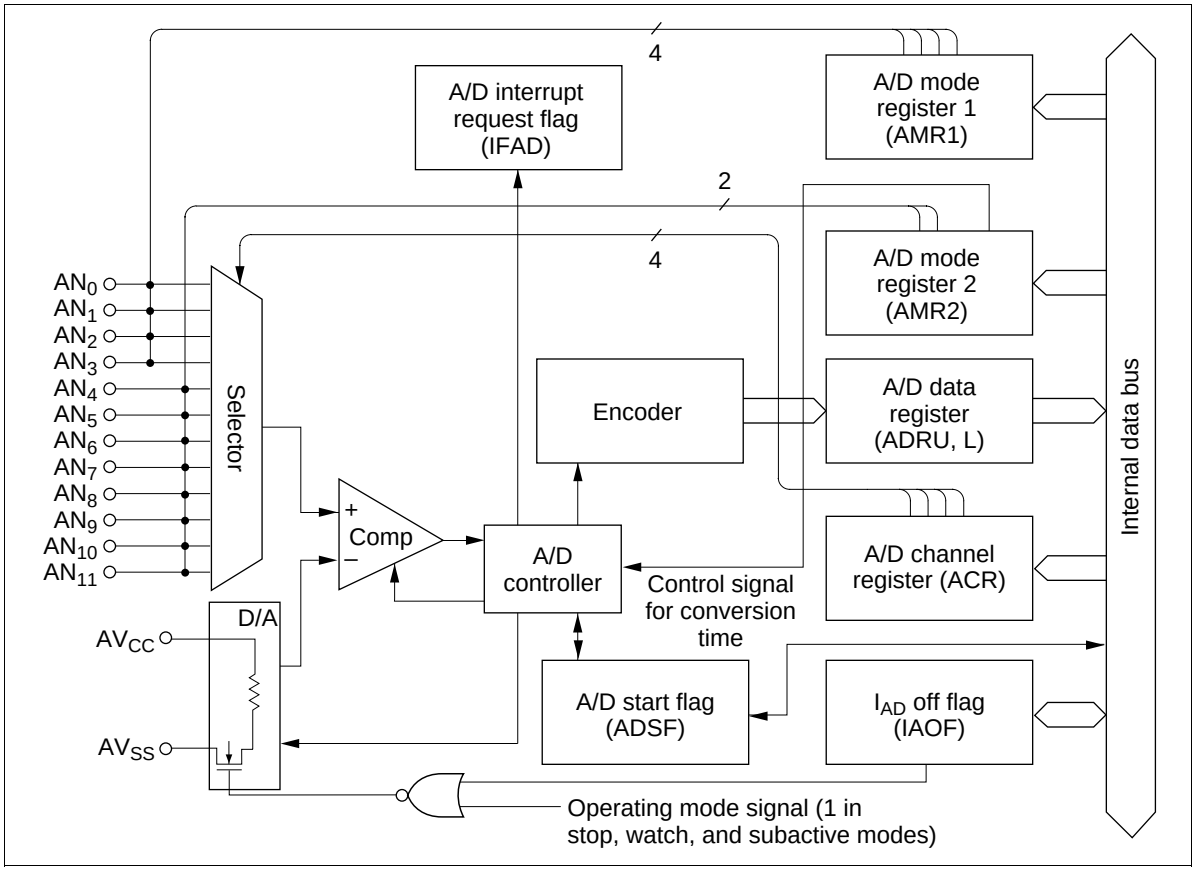


Figure 69 A/D Converter Block Diagram

Registers for A/D Converter Operation

A/D Mode Register 1 (AMR1: $019): Four-bit write-only register which selects digital or analog ports, as shown in figure 70.

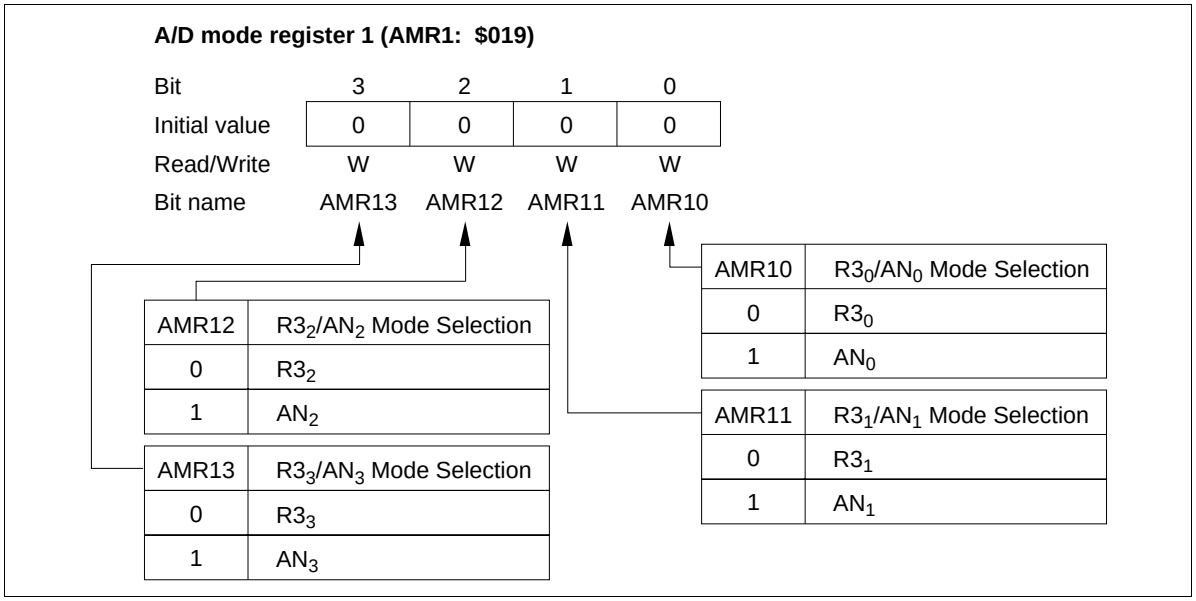


Figure 70 A/D Mode Register 1 (AMR1)

A/D Mode register 2 (AMR2: $01A): Three-bit write-only register which is used to set the A/D conversion period and to select digital or analog ports. Bit 0 of the A/D mode register selects the A/D conversion period, and bits 1 and 2 select ports R4–R5 as pins AN_4–AN_{11} in 4-pin units (figure 71).

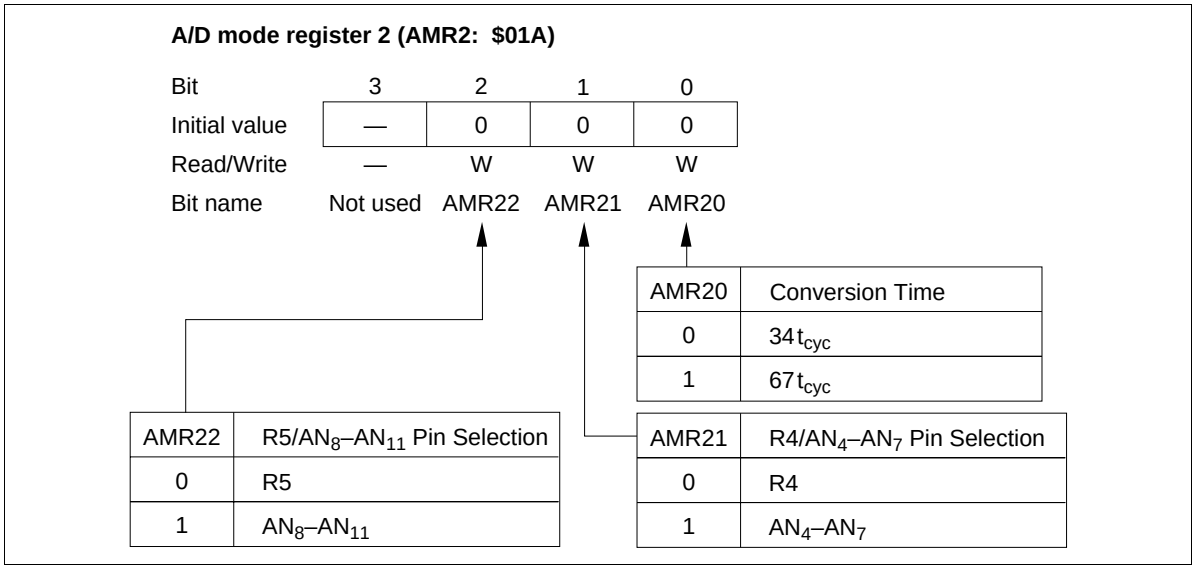


Figure 71 A/D Mode Register 2 (AMR2)

A/D Channel Register (ACR: $016): Four-bit write-only register which indicates analog input pin information, as shown in figure 72.

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ACR3	ACR2	ACR1	ACR0

ACR3	ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	0	AN_0
			1	AN_1
		1	0	AN_2
			1	AN_3
	1	0	0	AN_4
			1	AN_5
		1	0	AN_6
			1	AN_7
1	0	0	0	AN_8
			1	AN_9
		1	0	AN_{10}
			1	AN_{11}
	1	Don't care.	Don't care.	Not used

Figure 72 A/D Channel Register (ACR)

A/D Start Flag (ADSF: $02C, Bit 2): One-bit flag that initiates A/D conversion when set to 1. At the completion of A/D conversion, the converted data is stored in the A/D data register and the A/D start flag is cleared. Refer to figure 73.

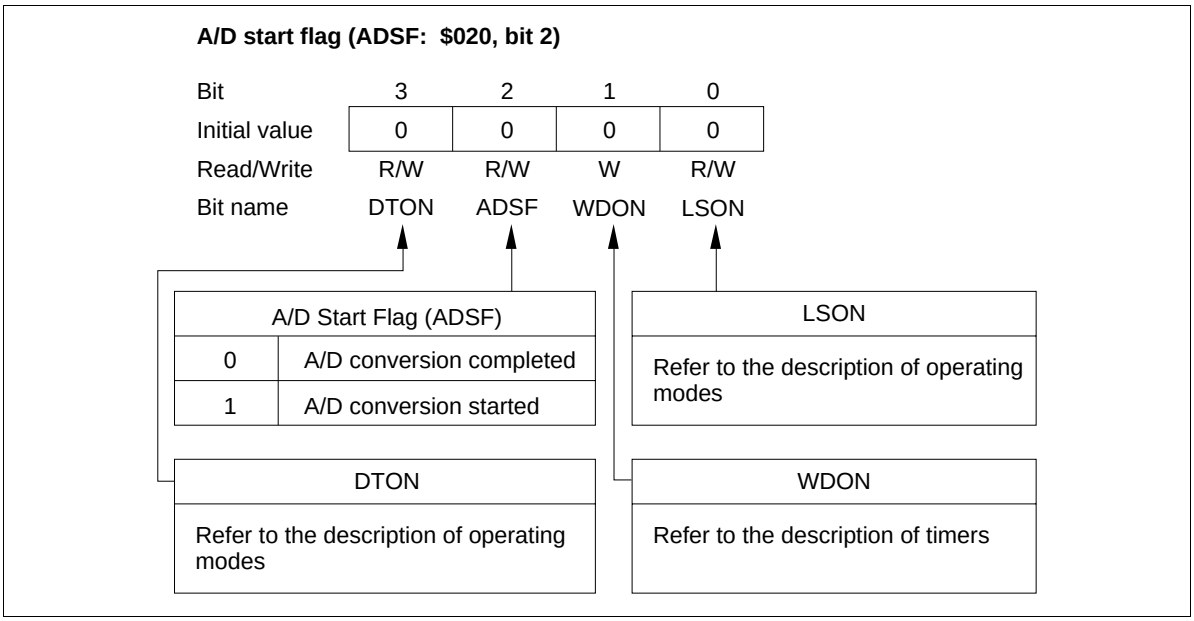


Figure 73 A/D Start Flag (ADSF)

I_{AD} Off Flag (IAOF: $021, Bit 2): By setting the I_{AD} off flag to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode, as shown in figure 74.

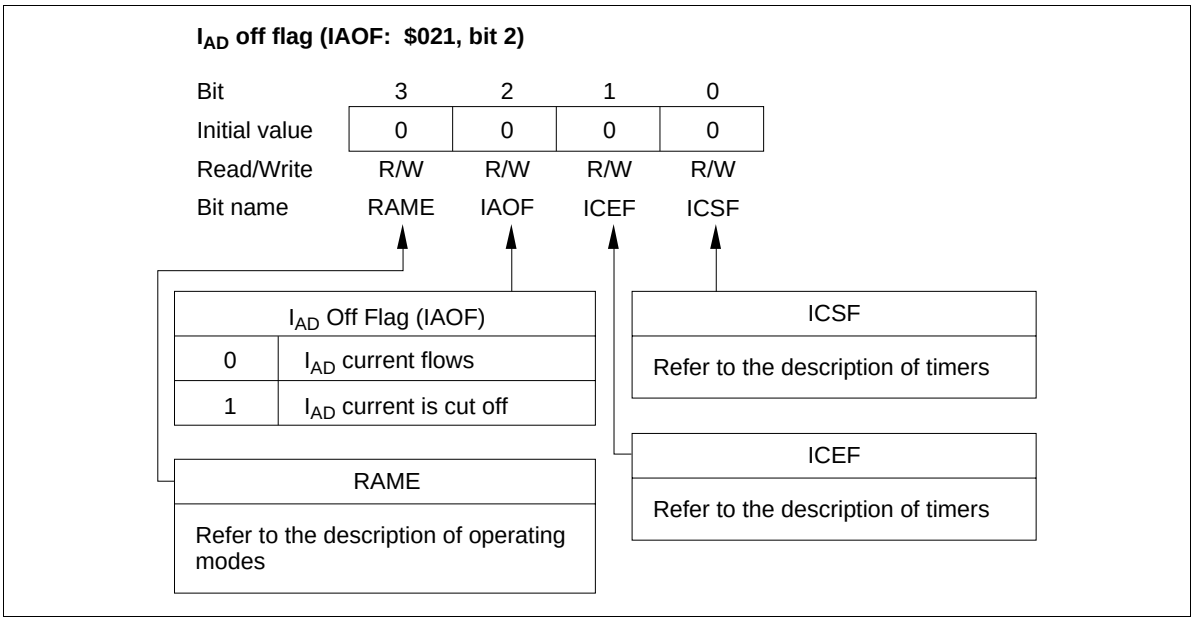


Figure 74 I_{AD} Off Flag (IAOF)

A/D Data Register (ADRL: $017, ADRU: $018): Eight-bit read-only register consisting of a 4-bit lower digit and 4-bit upper digit. This register is not cleared by reset. After the completion of A/D conversion, the resultant eight-bit data is held in this register until the start of the next conversion (figures 75, 76, and 77).

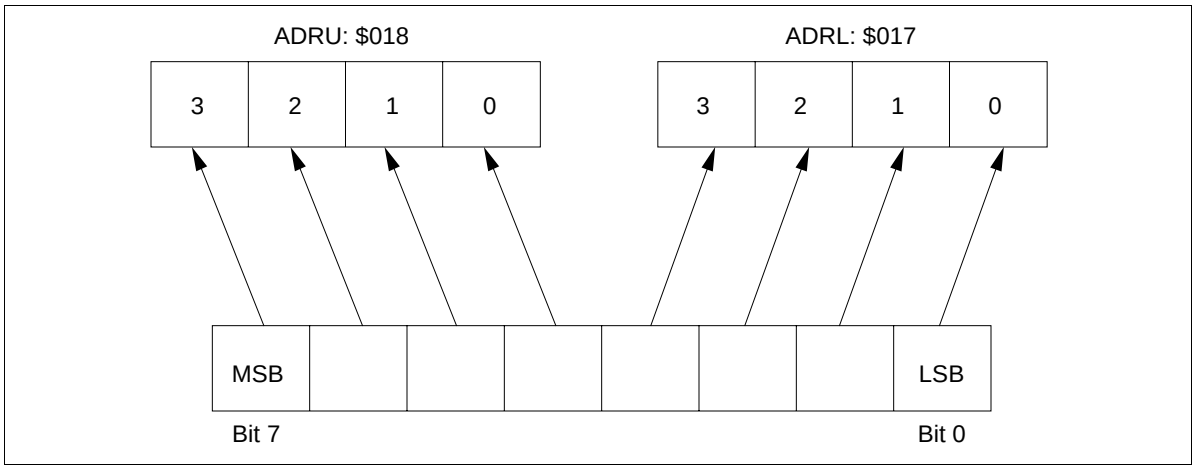


Figure 75 A/D Data Registers (ADRU, ADRL)

A/D data register (lower digit) (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 76 A/D Data Register Lower Digit (ADRL)

A/D data register (upper digit) (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 77 A/D Data Register Upper Digit (ADRU)

Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop, watch, or subactive mode. In addition, to save power while in these modes, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from V_{CC}, connect a 0.1-µF bypass capacitor between the AV_{CC} and AV_{SS} pins. (However, this is not necessary when the AV_{CC} pin is directly connected to the V_{CC} pin.)
- The contents of the A/D data register are not guaranteed during A/D conversion. To ensure that the A/D converter operates stably, do not execute port output instructions during A/D conversion.
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by A/D mode register 1 or 2 (AMR1 or AMR2) as an analog pin will remain pulled up (figure 78).

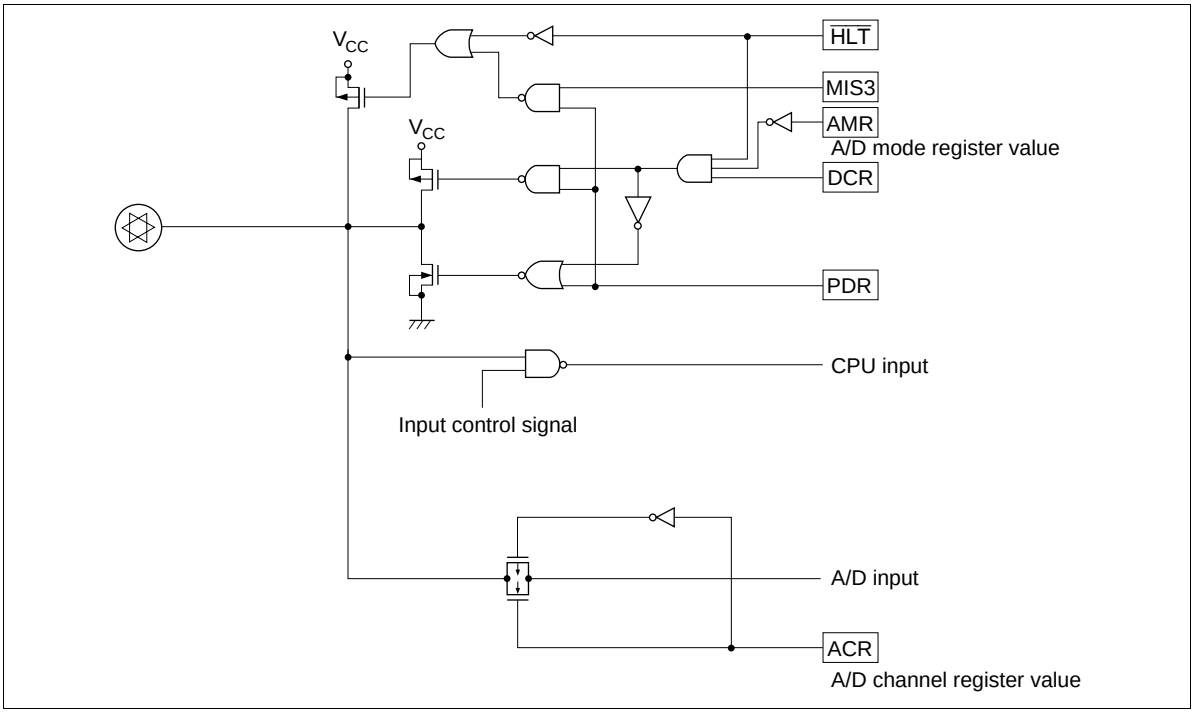


Figure 78 R Port/Analog Multiplexed Pin Circuit

Pin Description in PROM Mode

The HD407A4369 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number			MCU Mode		PROM Mode	
DP-64S	FP-64B	FP-64A	Pin	I/O	Pin	I/O
1	59	57	$R6_0$	I/O		
2	60	58	$R6_1$	I/O		
3	61	59	$R6_2$	I/O		
4	62	60	$R6_3$	I/O		
5	63	61	$R7_0$	I/O		
6	64	62	$R7_1$	I/O		
7	1	63	$R7_2$	I/O		
8	2	64	$R0_0/\overline{SCK}$	I/O	V_{CC}	
9	3	1	$R0_1$/SI	I/O	V_{CC}	
10	4	2	$R0_2$/SO	I/O	O_1	I/O
11	5	3	$R0_3$/TOC	I/O	O_2	I/O
12	6	4	TEST	I	V_{PP}	
13	7	5	$\overline{RESET}$	I	$\overline{RESET}$	I
14	8	6	OSC_1	I	V_{CC}	
15	9	7	OSC_2	O		
16	10	8	GND	—	GND	
17	11	9	X1	I	GND	
18	12	10	X2	O		
19	13	11	AV_{SS}	—	GND	
20	14	12	$R3_0/AN_0$	I/O	O_0	I/O
21	15	13	$R3_1/AN_1$	I/O	O_1	I/O
22	16	14	$R3_2/AN_2$	I/O	O_2	I/O
23	17	15	$R3_3/AN_3$	I/O	O_3	I/O
24	18	16	$R4_0/AN_4$	I/O	O_4	I/O
25	19	17	$R4_1/AN_5$	I/O	$\overline{M}_0$	I
26	20	18	$R4_2/AN_6$	I/O	$\overline{M}_1$	I
27	21	19	$R4_3/AN_7$	I/O		
28	22	20	$R5_0/AN_8$	I/O		
29	23	21	$R5_1/AN_9$	I/O		
30	24	22	$R5_2/AN_{10}$	I/O		

Pin Number			MCU Mode		PROM Mode	
DP-64S	FP-64B	FP-64A	Pin	I/O	Pin	I/O
31	25	23	$R5_3/AN_{11}$	I/O		
32	26	24	AV_{CC}	—	V_{CC}	
33	27	25	V_{CC}	—	V_{CC}	
34	28	26	$D_0/\overline{INT}_0$	I/O	O_3	I/O
35	29	27	$D_1/\overline{INT}_1$	I/O	O_4	I/O
36	30	28	D_2/EVNB	I/O	A_1	I
37	31	29	D_3/BUZZ	I/O	A_2	I
38	32	30	$D_4/\overline{STOPC}$	I/O		
39	33	31	D_5	I/O	A_3	I
40	34	32	D_6	I/O	A_4	I
41	35	33	D_7	I/O	A_9	I
42	36	34	D_8	I/O	V_{CC}	
43	37	35	D_9	I/O		
44	38	36	D_{10}	I/O		
45	39	37	D_{11}	I/O		
46	40	38	D_{12}	I/O		
47	41	39	D_{13}	I/O		
48	42	40	$R8_0$	I/O	$\overline{CE}$	I
49	43	41	$R8_1$	I/O	$\overline{OE}$	I
50	44	42	$R8_2$	I/O	A_{13}	I
51	45	43	$R8_3$	I/O	A_{14}	I
52	46	44	$R9_0$	I/O		
53	47	45	$R9_1$	I/O		
54	48	46	$R9_2$	I/O		
55	49	47	$R9_3$	I/O		
56	50	48	$R1_0$	I/O	A_5	I
57	51	49	$R1_1$	I/O	A_6	I
58	52	50	$R1_2$	I/O	A_7	I
59	53	51	$R1_3$	I/O	A_8	I
60	54	52	$R2_0$	I/O	A_0	I
61	55	53	$R2_1$	I/O	A_{10}	I
62	56	54	$R2_2$	I/O	A_{11}	I
63	57	55	$R2_3$	I/O	A_{12}	I
64	58	56	RA_1	I	O_0	I/O

Notes: 1. I/O: Input/output pin; I: Input pin; O: Output pin

2. O_0 to O_4 consist of two pins each. Tie each pair together before using them.

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{\text{RESET}}$, $\overline{\text{M}}_0$, and $\overline{\text{M}}_1$ low, as shown in figure 79. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and a 100-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 29.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 16 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

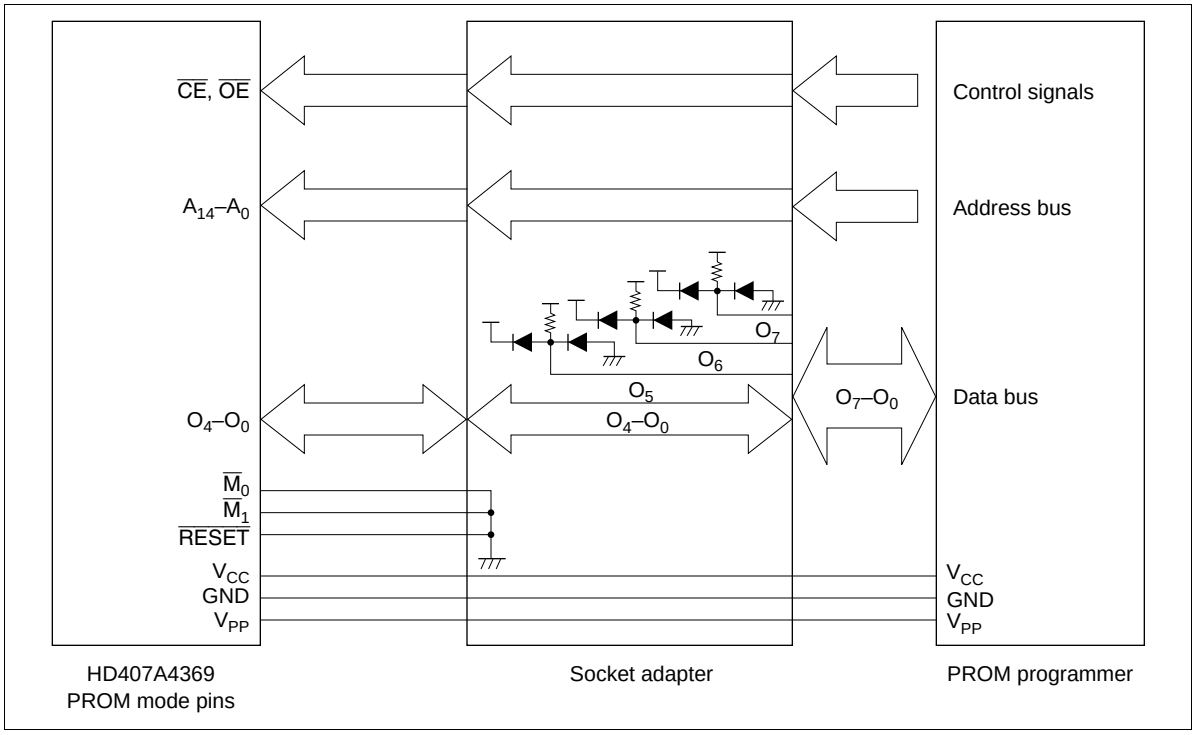


Figure 79 PROM Mode Connections

Table 29 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	**Model Name**	**Package**	**Manufacture**	**Model Name**
DATA I/O corp	121 B	DP-64S	Hitachi	HS4369ESS01H
		FP-64B		HS4369ESF01H
		FP-64A		HS4369ESH01H
AVAL corp	PKW-1000	DP-64S	Hitachi	HS4369ESS01H
		FP-64B		HS4369ESF01H
		FP-64A		HS4369ESH01H

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 30.

For details of PROM programming, refer to the following Notes on PROM Programming section.

Table 30 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_4**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 80 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

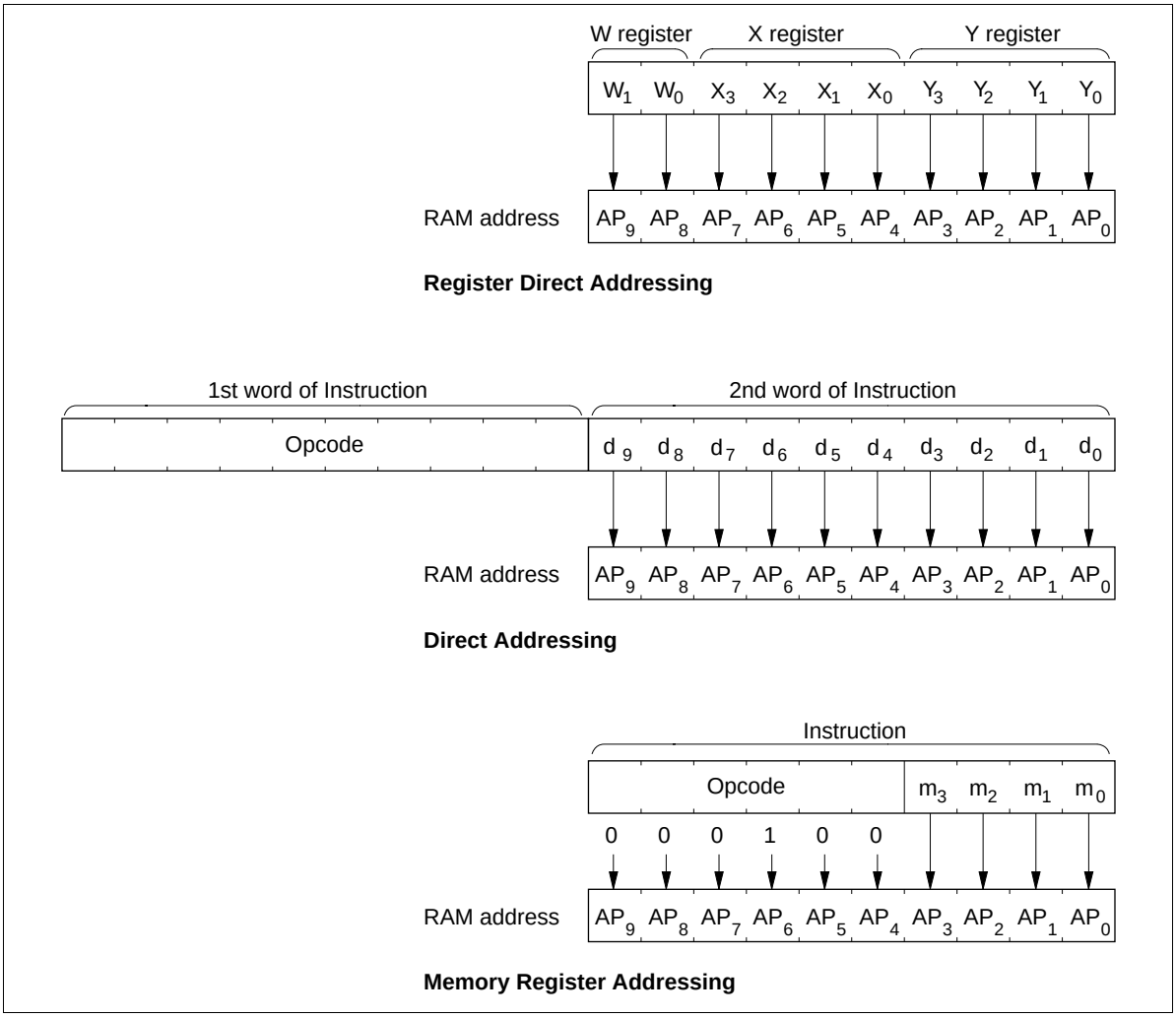


Figure 80 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 81 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 83. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $0000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 82. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

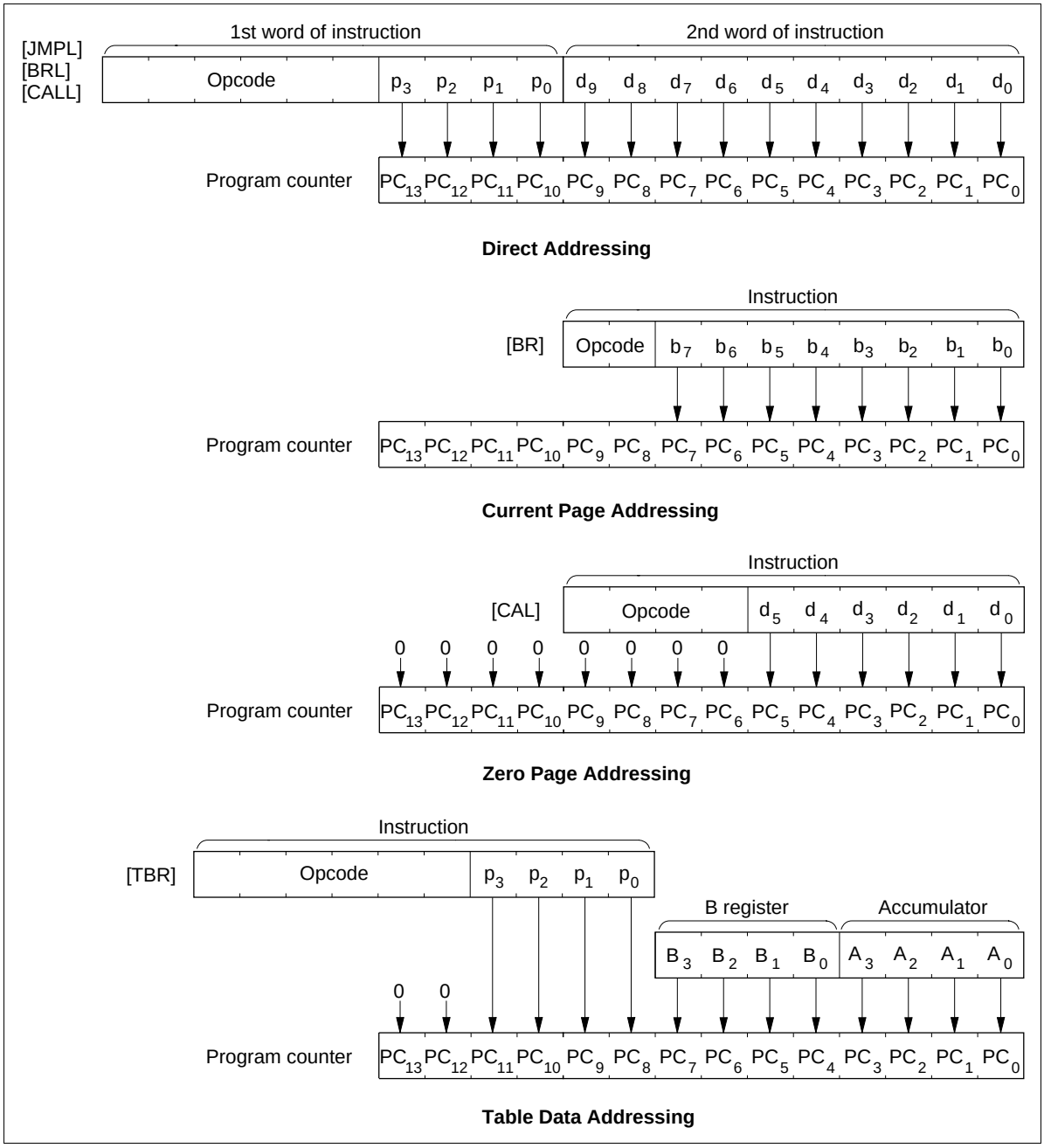


Figure 81 ROM Addressing Modes

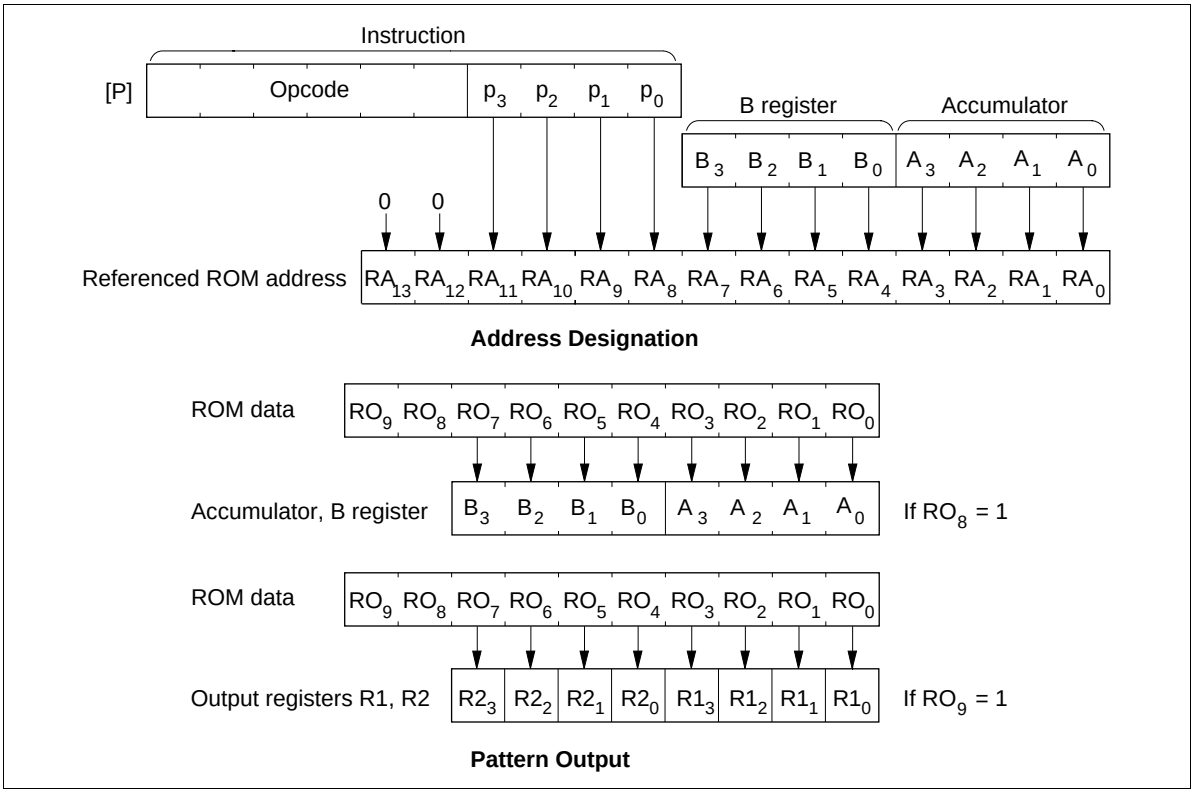


Figure 82 P Instruction

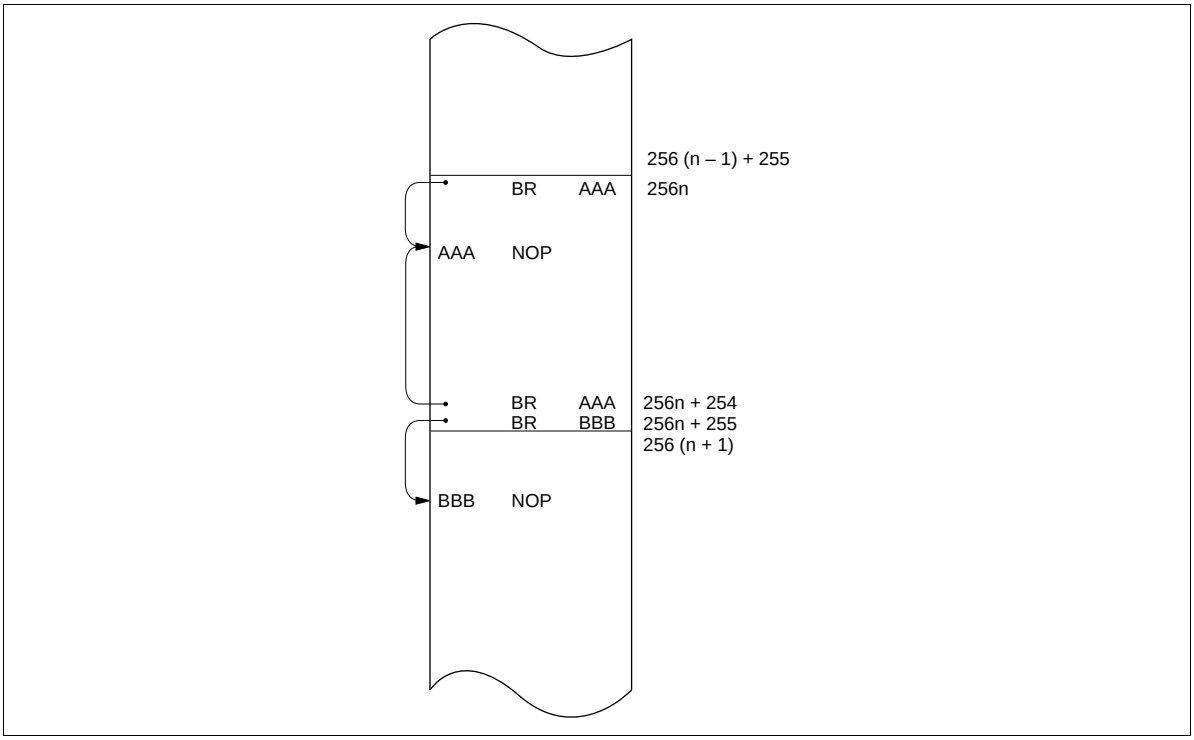


Figure 83 Branching when the Branch Destination is on a Page Boundary

Instruction Set

The HD404369 Series has 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM address instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM address instructions
- Input/output instructions
- Control instructions

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Total permissible input current	$\sum I_O$	105	mA	4
Total permissible output current	$-\sum I_O$	50	mA	5
Maximum input current	I_O	4	mA	6, 7
		30	mA	6, 8
Maximum output current	$-I_O$	4	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of HD407A4369.
2. Applies to all standard voltage pins.
3. Applies to intermediate-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports D_0 to D_{13}, R0, R3 to R9.
8. Applies to ports R1 and R2.
9. The maximum output current is the maximum current flowing from V_{CC} to each I/O pin

Electrical Characteristics

DC Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	$0.8V_{CC}$	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	–0.3	—	$0.2V_{CC}$	V		
		SI	–0.3	—	$0.3V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	100	µA	V_{CC} = 5 V, 32 kHz oscillator	4
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	—	20	µA	V_{CC} = 5 V, 32 kHz oscillator	4

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5V, X1 = GND, X2 = Open	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_{13}, R0–R9, RA_1 at V_{CC}

4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_{13}, R0–R9, RA_1 at V_{CC}

I/O Characteristics for Standard Pins (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_{13}, R0, R3–R9, RA_1	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{13}, R0, R3–R9, RA_1	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{13}, R0, R3–R9	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	D_0–D_{13}, R0, R3–R9	—	—	0.4	V	I_{OL} = 1.6 mA	
Input leakage current	$\|I_{IL}\|$	D_0–D_{13}, R0, R3–R9, RA_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$–I_{PU}$	D_0–D_{13}, R0, R3–R9	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: 1. Output buffer current is excluded.

I/O Characteristics for Intermediate-Voltage Pins (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R1, R2	$0.7V_{CC}$	—	12	V		
Input low voltage	V_{IL}	R1, R2	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R1, R2	11.5	—	—	V	500 kΩ at 12 V	
Output low voltage	V_{OL}	R1, R2	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	R1, R2	—	—	20	µA	V_{in} = 0 V to 12 V	1

Note: 1. Excludes output buffer current.

A/D Converter Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C;HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0–AN_{11}	AV_{SS}	—	AV_{CC}	V		
Current flowing between AV_{CC} and AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0–AN_{11}	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	12	Channel		
Absolute accuracy			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_{11}	1	—	—	MΩ		

Note: 1. Connect this to V_{CC} if the A/D converter is not used.

Standard f_{OSC} = 5 MHz Version AC Characteristics (HD404364/HD404368/HD4043612/HD404369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	1
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
	t_{subcyc}		—	244.14	—	µs	32-kHz oscillator, 1/8 system clock division ratio	
			—	122.07	—	µs	32-kHz oscillator, 1/4 system clock division ratio	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		2
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		2
		X1, X2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		3
$\overline{INT}_0$, $\overline{INT}_1$, EVNB high widths	t_{IH}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{INT}_0$, $\overline{INT}_1$, EVNB low widths	t_{IL}	$\overline{INT}_0$, $\overline{INT}_1$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		5
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		6
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		6
Input capacitance	C_{in}	All input pins except R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		R1, R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 5.0 MHz

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

2. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

3. Refer to figure 84.
4. Refer to figure 85.
5. Refer to figure 86.
6. Refer to figure 87.

High-Speed f_{OSC} = 8.5 MHz Version AC Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	1/4 system clock division ratio	1
			0.4	4	8.5	MHz		2, 3
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
			0.47	1	10	µs		2, 3
	t_{subcyc}		—	244.14	—	µs	32-kHz oscillator, 1/8 system clock division ratio	
			—	122.07	—	µs	32-kHz oscillator, 1/4 system clock division ratio	
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		4
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		4
		X1, X2	—	—	2	s		4
External clock high width	t_{CPH}	OSC_1	80	—	—	ns		5
			47	—	—	ns		3, 5
External clock low width	t_{CPL}	OSC_1	80	—	—	ns		5
			47	—	—	ns		3, 5
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		5
			—	—	15	ns		3, 5
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		5
			—	—	15	ns		3, 5
$\overline{INT_0}$, $\overline{INT_1}$, EVNB high widths	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		6
$\overline{INT_0}$, $\overline{INT_1}$, EVNB low widths	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		6

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
$\overline{\text{RESET}}$ low width	t_{RSTL}	$\overline{\text{RESET}}$	2	—	—	t_{cyc}		7
$\overline{\text{STOPC}}$ low width	t_{STPL}	$\overline{\text{STOPC}}$	1	—	—	t_{RC}		8
$\overline{\text{RESET}}$ rise time	t_{RSTr}	$\overline{\text{RESET}}$	—	—	20	ms		7
$\overline{\text{STOPC}}$ rise time	t_{STPr}	$\overline{\text{STOPC}}$	—	—	20	ms		8
Input capacitance	C_{in}	All input pins except TEST, R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	9
		TEST	—	—	180	pF	f = 1 MHz, V_{in} = 0 V	10
		R1, R2	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 5.0 MHz

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

2. When using the subsystem oscillator (32.768 kHz), one of the following relationships for f_{OSC} must be applied.

0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or 1.6 MHz ≤ f_{OSC} ≤ 8.5 MHz

The operating range for f_{OSC} can be set with bit 1 of system clock selection register 1 (SSR1: $027).

3. V_{CC} = 4.5 to 5.5V
4. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches 2.7 V at power-on.

b. After $\overline{\text{RESET}}$ input goes low when stop mode is cancelled.

c. After $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least a duration of t_{RC}.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

5. Refer to figure 84.
6. Refer to figure 85.
7. Refer to figure 86.
8. Refer to figure 87.
9. Applies to the HD40A4364, HD40A4368, HD40A43612, and HD40A4369.
10. Applies to the HD407A4369.

Serial Interface Timing Characteristics (HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C; HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/HD40A43612/HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	Load shown in figure 89	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 89	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	Load shown in figure 89	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 89	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	Load shown in figure 89	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 89	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

During Transmit Clock Input

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	Load shown in figure 89	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. Refer to figure 88.

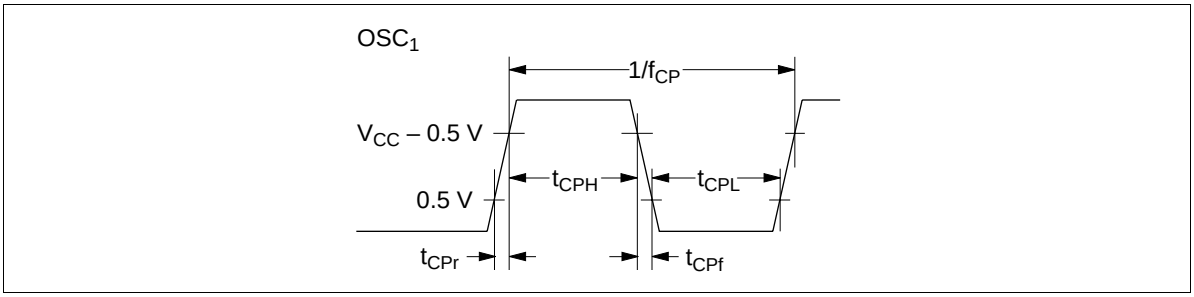


Figure 84 External Clock Timing

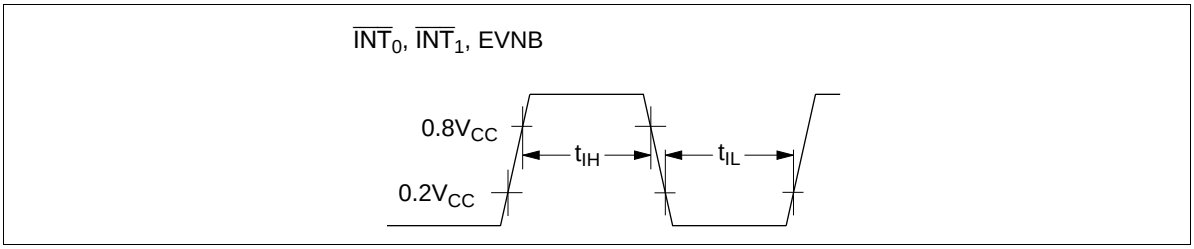


Figure 85 Interrupt Timing

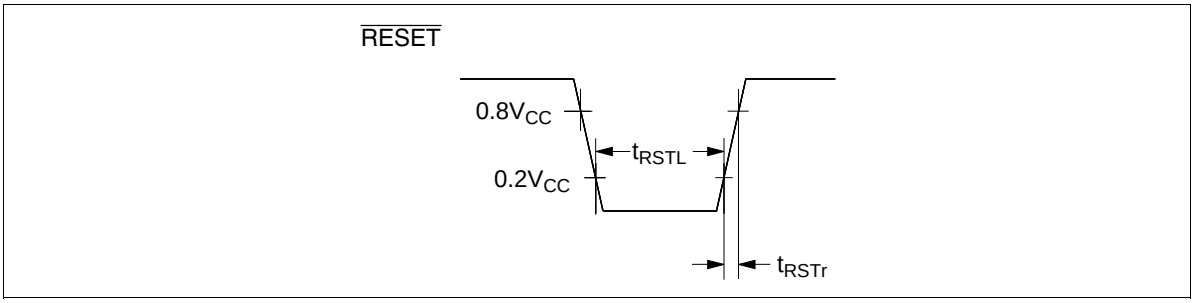


Figure 86 $\overline{\text{RESET}}$ Timing

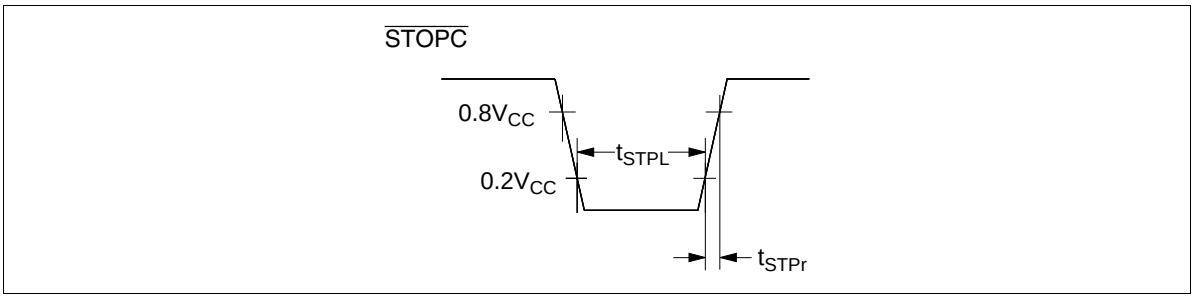
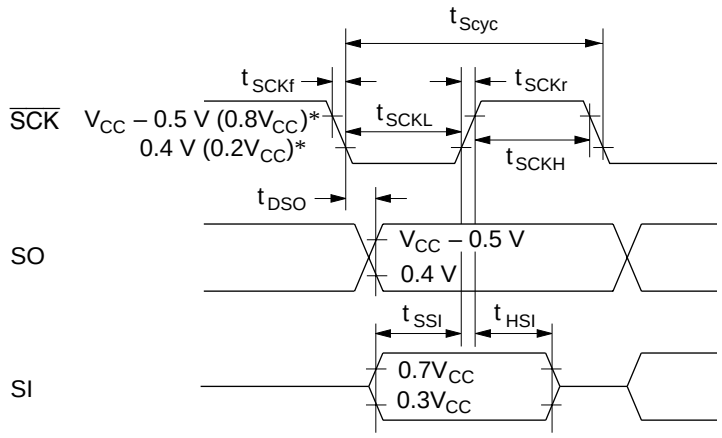


Figure 87 $\overline{\text{STOPC}}$ Timing



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 88 Serial Interface Timing

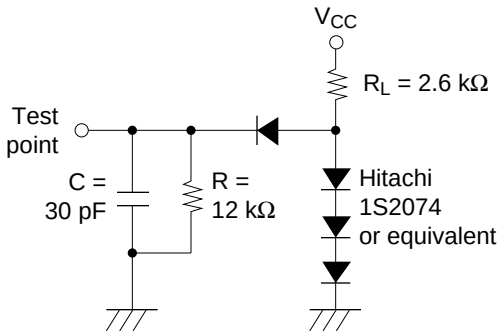


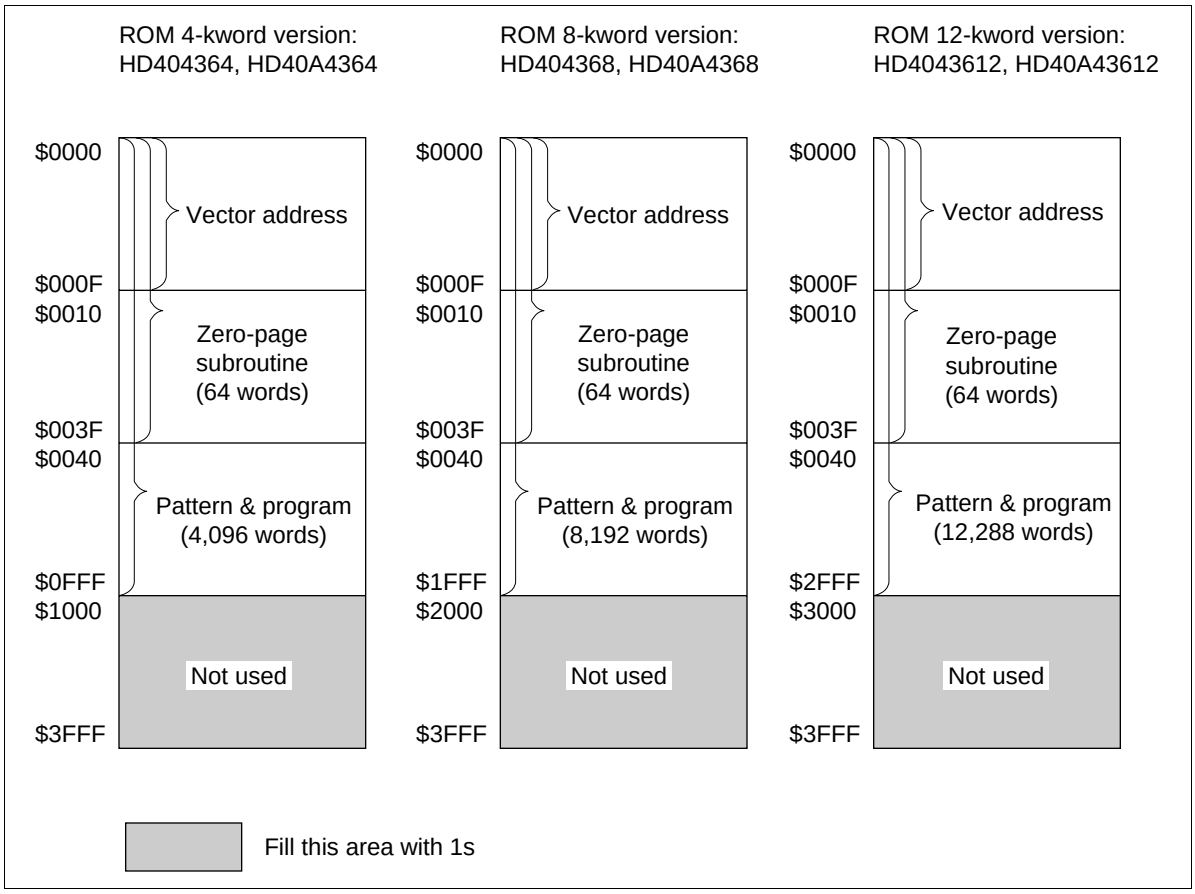
Figure 89 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404364, HD40A4364, HD404368, HD40A4368, HD4043612 and HD40A43612 as a 16-kword version (HD404369, HD40A4369). The 16-kword data sizes are required to change ROM data to mask manufacturing data since the program used is for a 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404364/HD404368/HD4043612/HD404369/HD40A4364/HD40A4368/ HD40A43612/HD40A4369 Option List

Please check off the appropriate applications and enter the necessary information.

1. ROM size

☐ 5 MHz operation	HD404364	4-kword
☐ 8.5 MHz operation	HD40A4364	
☐ 5 MHz operation	HD404368	8-kword
☐ 8.5 MHz operation	HD40A4368	
☐ 5 MHz operation	HD4043612	12-kword
☐ 8.5 MHz operation	HD40A43612	
☐ 5 MHz operation	HD404369	16-kword
☐ 8.5 MHz operation	HD40A4369	

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

2. Optional Functions

*☐ With 32-kHz CPU operation, with time base for clock
*☐ Without 32-kHz CPU operation, with time base for clock
☐ Without 32-kHz CPU operation, without time base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

4. System Oscillator (OSC1, OSC2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

5. Stop mode

☐ Used
☐ Not used

6. Package

☐ DP-64S
☐ FP-64B
☐ FP-64A

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