National Semiconductor

August 1996

Not Intended For New Designs

Comlinear CLC200
Fast Settling, Wideband Operational Amplifiers

General Description

The CLC200 operational amplifier achieves performance far superior to that of other high performance op amps. A proprietary Comlinear design provides a **bandwidth of DC-95MHz and an unprecedented settling time of 18nsec to 0.1%.** And since thermal tail has been eliminated, the CLC200 can be depended upon to settle fast and solidly maintain its level. Drive capability is also impressive at $24V_{pp}$ and 100mA.

Using the CLC200 is as easy as adding power supplies and a gain-setting resistor. The result is reliable, consistent performance because such characteristics as bandwidth and settling time are virtually independent of gain setting. Unlike conventional op amp designs where the optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of –1, maximum slew rate at a gain of +1, et cetera, the CLC200 offers predictable response at gain settings from ±1 to ±50. This, coupled with consistent performance from unit to unit with **no external compensation**, makes the CLC200 a real time and cost-saver in design and production situations alike.

Minimizing settling time was a design goal of the CLC200. Settling time is one of the most demanding of all op amp requirements since it is affected by the op amp's bandwidth, gain flatness, and harmonic distortion. The result of this effort is an amplifier fast enough for the most demanding high speed D to A converters and "flash" A to D converters.

The superior slew rate and rise and fall times of the CLC200 make it an ideal amplifier for a broad range of pulse, analog, and digital applications. Flat gain and phase response from DC to beyond 50MHz ensure distortion levels well below those of other op amps. A **full power bandwidth of 20MHz** eliminates the need for power buffers in many applications.

The CLC200 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

CLC200AI	-25°C to +85°C	12-pin TO-8 can
CLC200A8C	-55°C to +125°C	12-pin TO-8 can, MIL-STD-883, Level B
CLC200AK	-55°C to +125°C	12-pin TO-8 can, features burn-in and hermetic testing
CLC200AM	-55°C to +125°C	12-pin TO-8 can, screened to Comlinear's M std. for high reliability

DESC SMD number: 5962-89910

Typical Performance

parameter	gain setting +2	+20	+50	−2	−20	−50	units
−3dB bandwidth	150	95	75	100	95	90	MHz
rise time (20V)	—	4	5	4	4	4	ns
slew rate	4	4	4	4	4	4	V/ns
settling time (0.1%)	—	18	23	18	18	23	ns

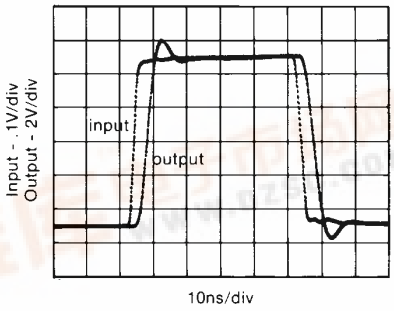
Features

- -3dB bandwidth of 95MHz
- 0.1% settling in 18ns
- 4000V/µs slew rate
- Low distortion, linear phase
- 3.6ns rise and fall times

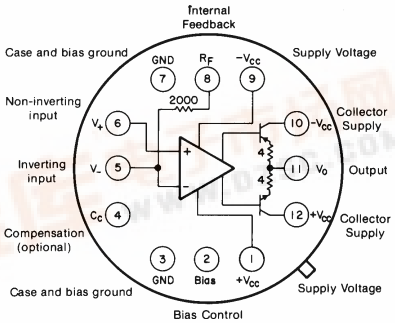
Applications

- Fast, precision A to D, D to A conversion
- Baseband and video communications
- Radar, sonar, IF processors
- Laser drivers, photodiode preamps
- High-density buffering
- Graphic CRT composite video drive amp

Large Signal Pulse Response

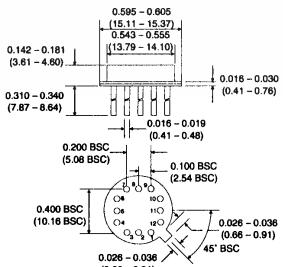


Bottom View



Pin 8 provides access to a 2000 ohm feedback resistor. Pin 2 allows the user to reduce the amplifier supply current or to turn the amplifier off completely.

Package Dimensions



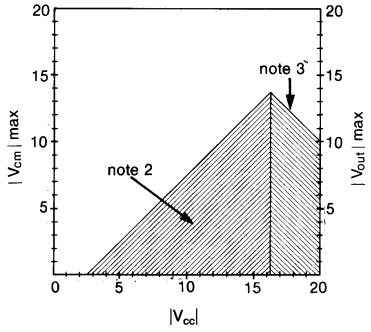
CLC200 Electrical Characteristics (A_V = +20, V_{cc} = ±5V, R_L = 200Ω, R_f = 2000Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	CLC200AI[1]	+25°C	–25°C	+25°C	+85°C		
Ambient Temperature	CLC200A8[1]	+25°C	–55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
* –3dB bandwidth	V_{out}<2V_{pp}	95	> 85	> 85	> 80	MHz	SSBW
gain flatness at	V_{out}<2V_{pp}						
* peaking	0.1 to 25MHz	0	< 0.4	< 0.3	< 0.4	dB	GFPL
* peaking	>25MHz	0.2	< 0.8	< 0.6	< 1.0	dB	GFPH
* rolloff	at 50MHz	—	< 0.6	< 0.4	< 0.6	dB	GFR
group delay	to 50MHz	4.2 ± 0.5	—	—	—	ns	GD
linear phase deviation	to 50MHz	1	< 2	< 2	< 2	°	LPD
reverse isolation	to 50MHz						
non-inverting		60	> 50	> 50	> 50	dB	RINI
inverting		45	> 35	> 35	> 35	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	3.6	< 4.1	< 4.1	< 4.4	ns	TRS
	20V step	4	< 5	< 5	< 6	ns	TRL
settling time to .02%	10V step[4]	25	—	—	—	ns	TSP
to .1%	10V step[4]	18	< 25	< 25	< 25	ns	TS
overshoot	10V step	5	< 12	< 10	< 10	%	OS
slew rate (overdriven input)		4	> 3	> 3	> 3	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
*2nd harmonic distortion	2V_{pp}, 20MHz	–52	< –45	< –45	< –45	dBc	HD2
*3rd harmonic distortion	2V_{pp}, 20MHz	–58	< –50	< –50	< –50	dBc	HD3
equivalent noise input							
noise floor	>100kHz	–156	< –150	< –150	< –150	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	35	< 70	< 70	< 70	µV	INV
noise floor	>5MHz	–156	< –150	< –150	< –150	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	35	< 70	< 70	< 70	µV	INV
STATIC DC PERFORMANCE							
*input offset voltage		10	< 25	< 25	< 25	mV	VIO
average temperature coefficient[1]		35	< 120	< 120	< 120	µV/°C	DVIO
*input bias current	non-inverting	10	< 40	< 30	< 40	µA	IBN
average temperature coefficient[1]		20	< 125	< 125	< 125	nA/°C	DIBN
*input bias current	inverting	20	< 70	< 50	< 70	µA	IBI
average temperature coefficient[1]		70	< 250	< 250	< 250	nA°/C	DIBI
*power supply rejection ratio		55	> 45	> 45	> 45	dB	PSRR
common mode rejection ratio		46	> 40	> 40	> 40	dB	CMRR
*supply current	no load	29	< 36	< 34	< 36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	> 100	> 100	> 100	kΩ	RIN
	capacitance	2.4	< 3	< 3	< 3	pF	CIN
ouput impedance	at DC	—	< 0.1	< 0.1	< 0.1	Ω	RO
	at 50MHz	1, 35	—	—	—	Ω, nH	ZO
output voltage range	no load	±12	> ±11	> ±11	> ±11	V	VO
internal feedback resistor	absolute tolerance	< 0.4	—	—	—	%	RFA

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

Common Mode and Output Voltage Limits



supply voltage (V_{cc})	±20V
output current	±100mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	A8: −55°C to + 125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

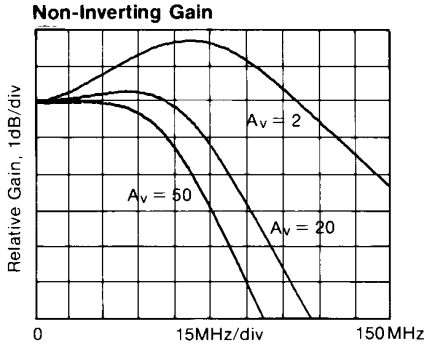
note 1: Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8 units are tested at –55°C, +25°C, and +125°C. AI units are tested only at +25°C although performance at –25°C and +85°C is guaranteed to be better than or equal to the performance specified for A8 devices in the –55°C and +125°C ranges. Maximum temperature coefficient parameters apply only to A8 devices.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1µs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed V_{cc}. (V_{cm} is the voltage at the non-inverting input, pin 6.)

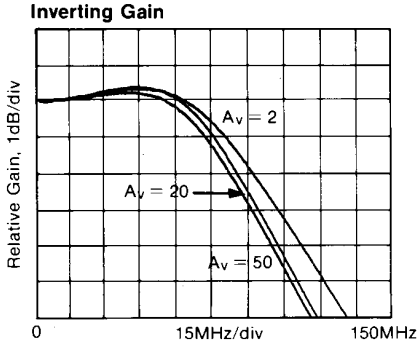
note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{cc} is ± 15V.

CLC200 Typical Performance Characteristics (T_A = +25°, A_V = +20, V_{CC} = ±5V, R_L = 200Ω; unless specified)

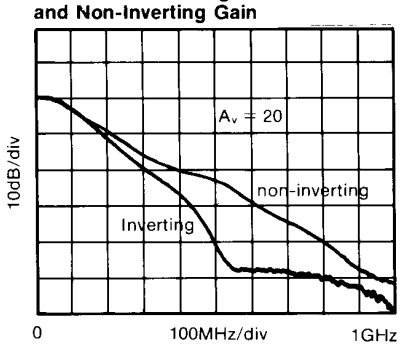
Non-Inverting Gain



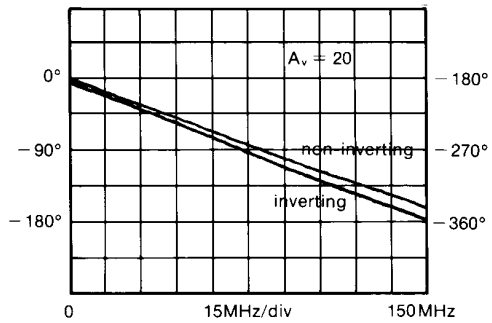
Inverting Gain



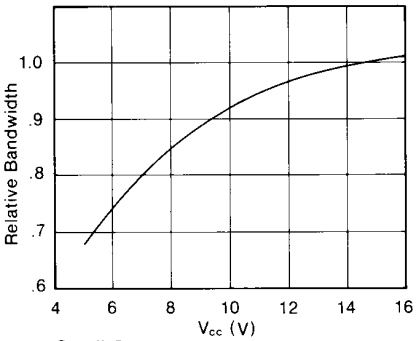
Broadband Inverting and Non-Inverting Gain



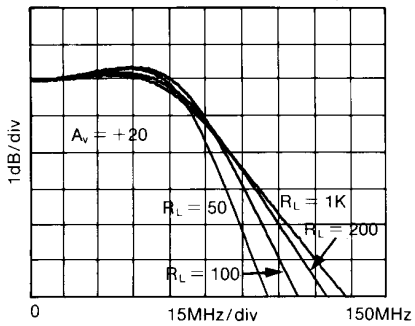
Inverting and Non-Inverting Phase



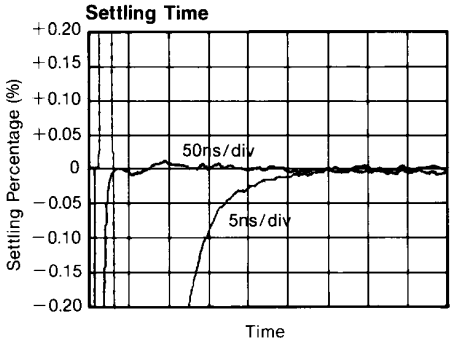
Relative Bandwidth vs. V_{cc}



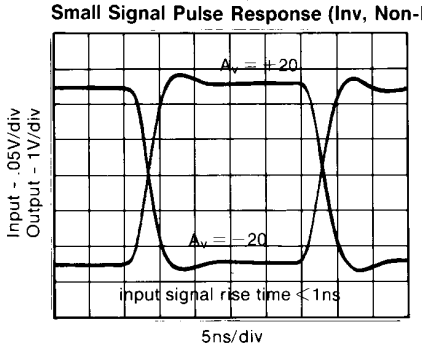
Gain vs. Frequency for Various R_Ls



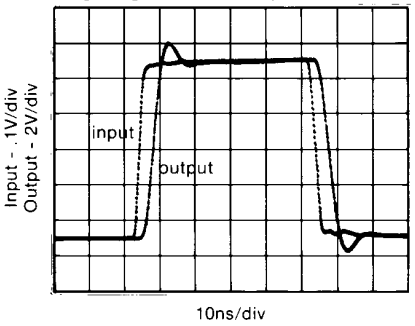
Settling Time



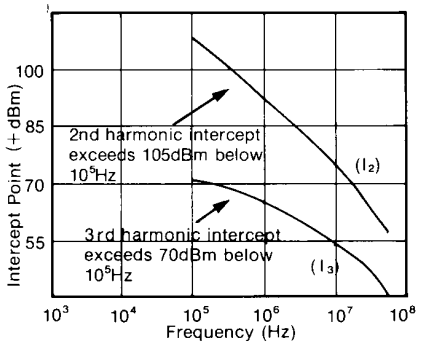
Small Signal Pulse Response (Inv, Non-Inv)



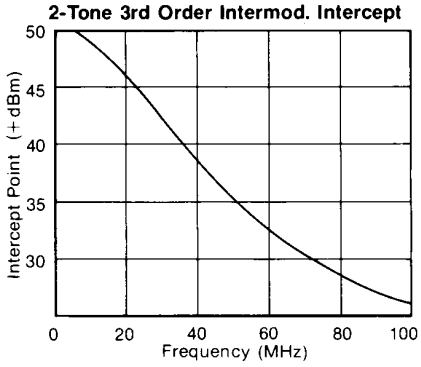
Large Signal Pulse Response



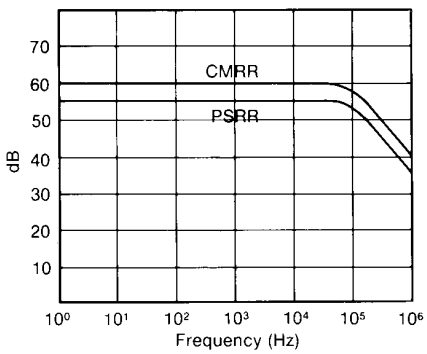
2nd and 3rd Harmonic Distortion Intercept



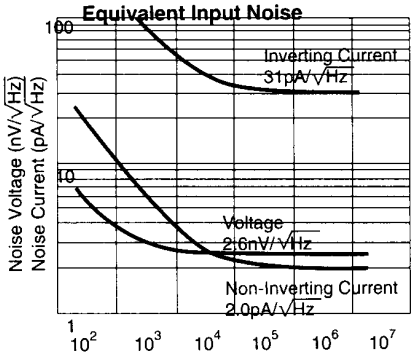
2-Tone 3rd Order Intermod. Intercept

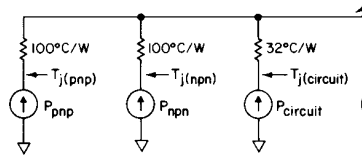


CMRR and PSRR



Equivalent Input Noise





θ_{ca} = 65°C/W in still air without a heatsink
38°C/W in still air with a Thermalloy 2268
15°C/W in 300ft/min air with a Thermalloy 2268

$P_{circuit} = I_{cc}\,[(+V_{cc}) - (-V_{cc})]$ where I_{cc} = 23mA at ±15V

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})\,(R_{col} + 4)]\,(I_{col})$ (% duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

I_{col} = V_{out}/R_{load} or 4mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{cc}$.

$T_{j\,(pnp)} = P_{pnp}\,(100 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}\,(32 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

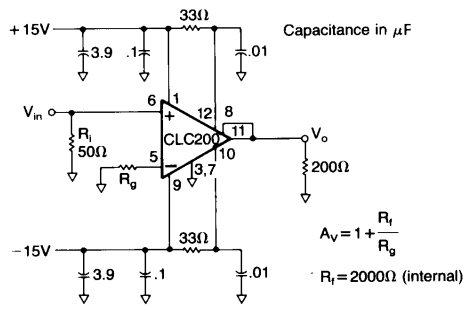


Figure 1: suggested non-inverting gain circuit

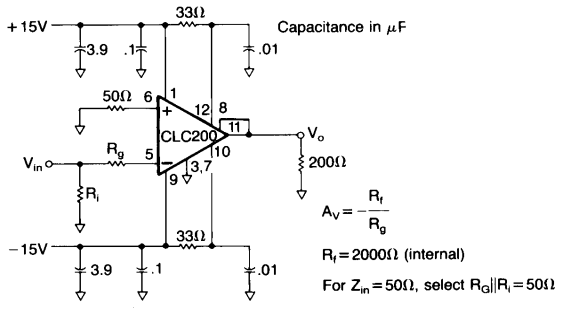


Figure 2: suggested inverting gain circuit

Test fixture schematics are available upon request.

Controlling Bandwidth and Passband Response

As with any op amp, the ratio of the two feedback resistors R_f and R_g determines the gain of the CLC200. Unlike conventional op amps, however, the closed loop pole-zero response of the CLC200 is affected very little by the value of R_g. R_g scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology. R_f does influence the feedback and so the CLC200 has been internally compensated for optimum performance with $R_f = 2000\Omega$, but any value of $R_f > 1k\Omega$ may be used with a single capacitor placed between pins 4 and 5 for compensation. See Table 1. As R_f decreases, C_c must increase to maintain flat gain. Slew rate will decrease slightly with increasing C_c, but other parameters such as bandwidth, settling time, and phase linearity will improve. Large values of R_f and C_c can be used together or separately to reduce the bandwidth. This may be desirable for reducing the bandwidth in applications not requiring the full frequency response available although this may cause the output noise to increase at low gains.

Table 1: Bandwidth versus R_f and C_c

R_f (kΩ)	C_c (pF)	$f \pm 0.3$dB (MHz)	$f - 3.0$dB (MHz)
10.0	0	5	15
5.0	0	10	30
3.0	0	20	60
2.0	0	50	100
1.5	0.25	70	130
1.0	0.50	120	170

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip of coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available from Comlinear at minimal cost.

Distortion and Amplification Fidelity

The graphs of intercept point versus frequency on the preceding page output voltage of the CLC200. First, convert the output voltage (V_O) to $V_{RMS} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{RMS}^2))$ to get output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC200 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

For linear operation of the CLC200 at large output voltage swings (DC component not included) and at high frequencies, observe the (AC output voltage) × (frequency) product specification of 400V · MHz. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

Operation with Reduced Bias Current

Placing a resistor between pins 1 and 2 will cause the CLC200 bias current to be reduced. A value of 20K will cause only a slight reduction, 3K will almost halve the current, while less than 1K will reduce bias to about 5mA and the amplifier will be off. In this condition, the input signal will be greatly attenuated. In the reduced bias, on condition, bandwidth will be roughly proportional to the reduction in bias current. A mechanical or semiconductor switch can be used to turn the amplifier off. Any connection which would cause current to flow out of pin 2 will result in increased bias current and may lead to device destruction from overheating and excessive current.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly qualified applications engineers to provide technical and design assistance.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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