MAXIM

Microprocessor Programmable Universal Active Filters

General Description

The MAX260/261/262 CMOS dual second-order universal switched-capacitor active filters allow microprocessor control of precise filter functions. No external components are required for a variety of bandpass, lowpass, highpass, notch and allpass configurations. Each device contains two second-order filter sections which place center frequency, Q, and filter operating mode under programmed control.

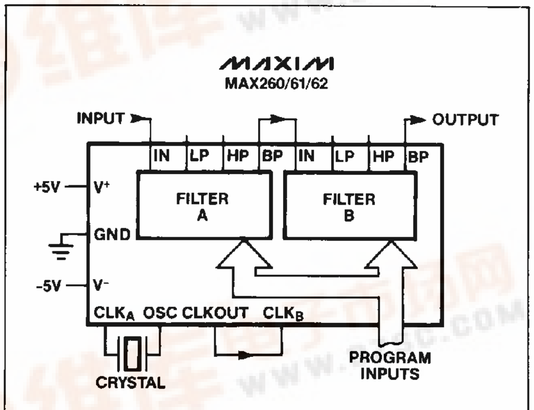
An input clock, along with a 6-bit f_0 program input, determine the filter's center or corner frequency without affecting other filter parameters. The filter Q is also programmed independently. Separate clock inputs for each filter section operate with either a crystal, RC network, or external clock generator.

The MAX260 has superior offset and DC specifications than the MAX261 and MAX262 and a center frequency (f_0) range of 7.5kHz. The MAX261 handles center frequencies to 57kHz while the MAX262 extends the center frequency range to 140kHz by employing lower clock-to-f_0 ratios. All devices are available in 24-pin DIP and small outline packages in commercial, extended, and military temperature ranges.

Applications

- μP Tuned Filters
- Anti-Aliasing Filters
- Digital Signal Processing
- Adaptive Filters
- Signal Analysis
- Phase-Locked Loops

Functional Diagram



Fourth-Order Bandpass Filter

Features

- ◆ **Filter Design Software Available**
- ◆ **Microprocessor Interface**
- ◆ **64-Step Center Frequency Control**
- ◆ **128-Step Q Control**
- ◆ **Independent Q and f_0 Programming**
- ◆ **Guaranteed Clock to f_0 Ratio—1% (A grade)**
- ◆ **75kHz f_0 Range (MAX262)**
- ◆ **Single +5V and ±5V Operation**

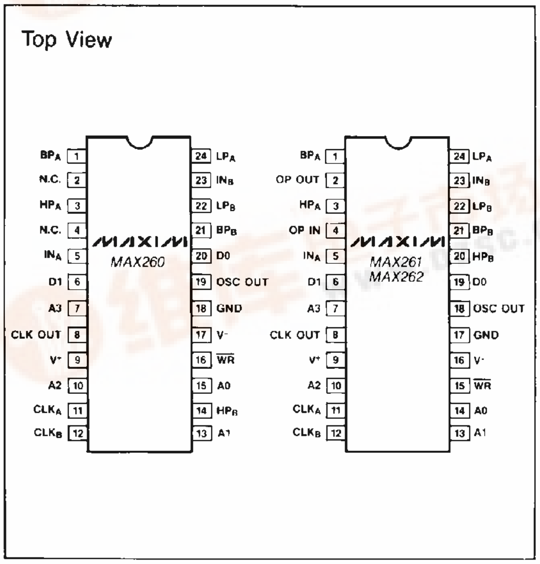
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX260ACNG	0°C to +70°C	Plastic DIP	1%
MAX260BCNG	0°C to +70°C	Plastic DIP	2%
MAX260AENG	-40°C to +85°C	Plastic DIP	1%
MAX260BENG	-40°C to +85°C	Plastic DIP	2%
MAX260ACWG	0°C to +70°C	Wide SO	1%
MAX260BCWG	0°C to +70°C	Wide SO	2%
MAX260AMRG	-55°C to +125°C	CERDIP	1%
MAX260BMRG	-55°C to +125°C	CERDIP	2%
MAX261ACNG	0°C to +70°C	Plastic DIP	1%

** All devices—24-pin packages 0.3" wide packages*

Ordering Information Continued on Last Page

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage, any pin .... V^--0.3V to V^++0.3V
Input Current, any pin .... ±50mA
Power Dissipation
  Plastic DIP (derate 8.33mW/°C above 70°C) ... 660mW
  CERDIP (derate 12.5mW/°C above 70°C) 1000mW
  Wide SO (derate 11.8mW/°C above 70°C) 944mW

Operating Temperature
  MAX260/261/262XCXG .... 0°C to +70°C
  MAX260/261/262XEXG .... -40°C to +85°C
  MAX260/261/262XMXG .... -55°C to +125°C
Storage Temperature .... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				See Table 1		
Maximum Clock Frequency				See Table 1		
f_{CLK}/f_0 Ratio Error (Note 1)	T_A = T_{MIN} to T_{MAX}	MAX260A		±0.2	±1.0	%
		MAX260B		±0.2	±2.0	
		MAX261/62A		±0.2	±1.0	
		MAX261/62B		±0.2	±2.0	
f_0 Temperature Coefficient				-5		ppm/°C
Q Accuracy (deviation from ideal continuous filter) (Note 2)	T_A = T_{MIN} to T_{MAX}					%
	Q = 0.5 to 16	MAX260A		±1	±5	
	Q = 0.5 to 16	MAX260B		±1	±10	
	Q = 32	MAX260A		±2	±10	
	Q = 32	MAX260B		±2	±15	
	Q = 64	MAX260A		±4	±15	
	Q = 64	MAX260B		±4	±22	
	Q = 0.5 to 16	MAX261/62A		±1	±5	
	Q = 0.5 to 16	MAX261/62B		±1	±10	
	Q = 32	MAX261/62A		±2	±10	
	Q = 32	MAX261/62B		±2	±15	
	Q = 64	MAX261/62A		±4	±15	
	Q = 64	MAX261/62B		±4	±22	
Q Temperature Coefficient				±20		ppm/°C
DC Lowpass Gain Accuracy		MAX260A		±0.1	±0.2	dB
		MAX260B		±0.1	±0.3	
		MAX261/62A		±0.1	±0.25	
		MAX261/62B		±0.1	±0.5	
Gain Temperature Coefficient	Lowpass (at D.C.)	MAX260		-5		ppm/°C
		MAX261/62		-5		
	Bandpass (at f_0)	MAX260/61/62		+20		
Offset Voltage At Filter Outputs—LP, BP, HP (Note 3)	T_A = T_{MIN} to T_{MAX}, Q = 4 Mode 1	MAX260A		±0.05	±0.25	V
		MAX260B		±0.15	±0.45	
		MAX261A		±0.40	±0.90	
		MAX261B		±0.80	±1.60	
		MAX262A		±0.40	±0.90	
		MAX262B		±0.80	±1.60	
	Mode 3	MAX260A		±0.075	±0.30	
		MAX260B		±0.075	±0.50	
		MAX261A		±0.50	±1.00	
		MAX261B		±0.90	±1.60	
		MAX262A		±0.50	±1.00	
		MAX262B		±0.90	±1.60	
Offset Voltage Temperature Coefficient	f_{CLK}/f_0 = 100.53, Q = 4 T_A = T_{MIN} to T_{MAX}			±0.75		mV/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V^+ = +5V, V^- = -5V, CLK_A = CLK_B = ± 5V 350kHz for the MAX260 and 1.5MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Feedthrough				±4		mV
Crosstalk				-70		dB
Wideband Noise (Note 4)	Q = 1, 2nd-Order, LP/BP			See Typ. Oper. Char.		μV_{RMS}
	4th-Order LP (Fig. 26)			90		
	4th-Order BP (Fig. 24)			100		
Harmonic Distortion at f_0	Q = 4, V_{IN} = $1.5V_{PP}$			-57		dB
Supply Voltage Range	T_A = T_{MIN} to T_{MAX}		±2.37	±5	±6.3	V
Power Supply Current (Note 5)	T_A = T_{MIN} to T_{MAX} CMOS Level Logic Inputs	MAX260		15	20	mA
		MAX261		16	20	
		MAX262		16	20	
Shutdown Supply Current	$Q0_A$-$Q6_A$ = all 0, CMOS Level Logic Inputs (Note 5)			1.5		mA
INTERNAL AMPLIFIERS						
Output Signal Swing (Note 6)	T_A = T_{MIN} to T_{MAX}, 10kΩ load			±4.75		V
Output Short Circuit Current	Source			50		mA
	Sink			2		
Power Supply Rejection Ratio	0Hz to 10kHz			-70		dB
Gain Bandwidth Product				2.5		MHz
Slew Rate				6		V/μs

ELECTRICAL CHARACTERISTICS (for V± = ±2.5V ±5%)

V^+ = +2.37V, V^- = -2.37V, CLK_A = CLK_B = ±2.5V 250kHz for the MAX260 and 1MHz for the MAX261/62, f_{CLK}/f_0 = 199.49 for MAX260/61 and 139.80 for MAX262, Filter Mode 1, T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Center Frequency Range				(Note 7)		
Maximum Clock Frequency				(Note 7)		
f_{CLK}/f_0 Ratio Error (Notes 1, 8)	Q = 8	MAX26XA		±0.1	1	%
		MAX26XB		±0.1	2	
Q Accuracy (deviation from ideal continuous filter) (Notes 2, 8)	Q = 8 f_{CLK}/f_0 = 199.49	MAX260A		±2	±5	%
		MAX260B		±2	±10	
	f_{CLK}/f_0 = 199.49	MAX261A		±2	±5	
		MAX261B		±2	±10	
	f_{CLK}/f_0 = 139.80	MAX262A		±2	±5	
		MAX262B		±2	±10	
Output Signal Swing	All Outputs (Note 6)			±2		V
Power Supply Current	CMOS Level Logic Inputs (Note 5)			7		mA
Shutdown Current	CMOS Level Logic Inputs (Note 5)			0.35		mA

Note 1: f_{CLK}/f_0 accuracy is tested at 100.53, 103.67, 106.81, 113.1, 125.66, 150.8, and 199.49 on the MAX260/61, and at 40.84, 43.98, 47.12, 53.41, 65.97, 91.11, and 139.8 on the MAX262.

Note 2: Q accuracy tested at Q = 0.5, 1, 2, 4, 8, 16, 32, and 64. Q of 32 and 64 tested at 1/2 stated clock frequency.

Note 3: The Offset Voltage is specified for the entire filter. Offset is virtually independent of Q and f_{CLK}/f_0 ratio setting. The test clock frequency for Mode 3 is 175kHz for the MAX260 and 750kHz for the MAX261/262.

Note 4: Output noise is measured with an RC output smoothing filter at 4 × f_0 to remove clock feedthrough.

Note 5: TTL logic levels are: HIGH = 2.4V, LOW = 0.8V. CMOS logic levels are: HIGH = 5V, LOW = 0V. Power supply current is typically 4mA higher with TTL logic and clock input levels.

Note 6: On the MAX260 only, the HP output signal swing is typically 0.75V less than the LP or BP outputs.

Note 7: At ±2.5V supplies, the f_0 range and maximum clock frequency are typically 75% of values listed in Table 1.

Note 8: f_{CLK}/f_0 and Q accuracy are a function of the accuracy of internal capacitor ratios. No increase in error is expected at ±2.5V as compared to ±5V however these parameters are only tested to the extent indicated by the MIN or MAX limits.

INTERFACE SPECIFICATIONS (Note 9)

(V^+ = +5V, V^+ = -5V, T_A = +25°C unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$ Pulse Width	t_{WR}		250	150		ns
Address Setup	t_{AS}		25			ns
Address Hold	t_{AH}		0			ns
Data Setup	t_{DS}		100	50		ns
Data Hold	t_{DH}		10	0		ns
Logic Input High	V_{IH}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}	2.4			V
Logic Input Low	V_{IL}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B $T_A = T_{MIN}$ to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_B CLK_A $T_A = T_{MIN}$ to T_{MAX}		6	10 60	μA
Input Capacitance	C_{IN}	$\overline{WR}$, D0-D1, A0-A3, CLK_A, CLK_B			15	pF

Note 9: Interface timing specifications are guaranteed by design and are not subject to test.

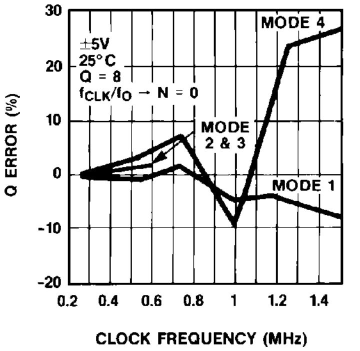
Pin Description

MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
9	9	V^+	Positive supply voltage
17	16	V^-	Negative supply voltage
18	17	GND	Analog Ground. Connect to the system ground for dual supply operation or mid-supply for single supply operation. GND should be well bypassed in single supply applications.
11	11	CLK_A	Input to the oscillator and clock input to section A. This clock is internally divided by 2.
12	12	CLK_B	Clock input to filter B. This clock is internally divided by 2.
8	8	CLK OUT	Clock Output for crystal and R-C oscillator operation
19	18	OSC OUT	Connects to crystal or R-C for self clocked operation

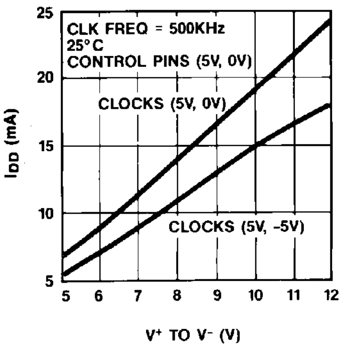
MAX260 PIN #	MAX261/2 PIN #	NAME	FUNCTION
5,23	5,23	IN_A,IN_B	Filter inputs
1,21	1,21	BP_A,BP_B	Bandpass outputs
24,22	24,22	LP_A,LP_B	Lowpass outputs
3,14	3,20	HP_A,HP_B	Highpass/Notch/Allpass outputs
16	15	$\overline{WR}$	Write Enable input
15,13, 10,7	14,13, 10,7	A0,A1 A2,A3	Address inputs for f_0 and Q input data locations
20,6	19,6	D0,D1	Data inputs for f_0 and Q programming
	2	OP OUT	Output of uncommitted op-amp on MAX261/62 only. Pin 2 is a no-connect on the MAX260
	4	OP IN	Inverting input of uncommitted op-amp on MAX261/62 only (Non-inverting input is internally connected to ground). Pin 4 is a no-connect on the MAX260.

Typical Operating Characteristics

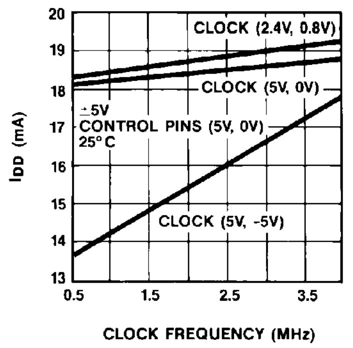
Q ERROR vs CLOCK FREQUENCY MAX260



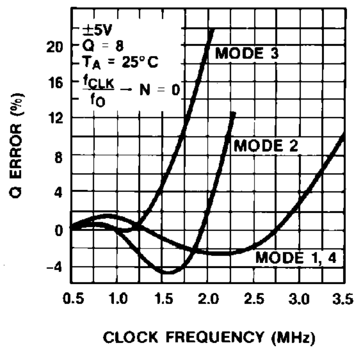
I_{DD} vs POWER SUPPLY VOLTAGE



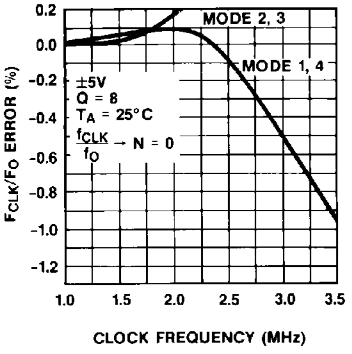
I_{DD} vs CLOCK FREQUENCY



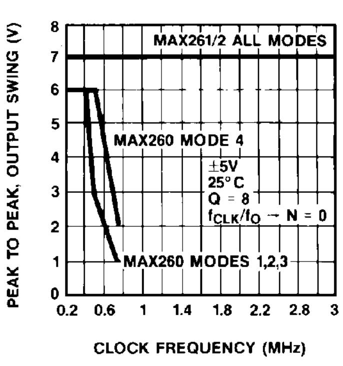
Q ERROR vs CLOCK FREQUENCY MAX261/2



F_{CLK}/F_O ERROR vs CLOCK FREQUENCY MAX261/2



OUTPUT SIGNAL SWING vs CLOCK FREQUENCY



Wideband RMS Noise (db ref. to 2.47V_{RMS}, 7V_{p-p}) **±5V Supplies**

	Mode	Q = 1			Q = 8			Q = 64		
		LP	BP	HP/AP/N	LP	BP	HP/AP/N	LP	BP	HP/AP/N
MAX261/2	1	-84	-90	-84	-80	-82	-85	-72	-73	-85
	2	-88	-90	-88	-84	-82	-84	-77	-73	-76
	3	-84	-90	-88	-80	-82	-82	-73	-73	-74
	4	-83	-89	-84	-79	-81	-85	-71	-73	-85
MAX260	1	-87	-89	-86	-81	-81	-86	-73	-73	-86
	2	-89	-88	-85	-83	-80	-82	-75	-72	-74
	3	-87	-88	-85	-80	-82	-80	-71	-72	-72
	4	-87	-88	-86	-81	-80	-86	-71	-72	-86

Notes:

1. f_{CLK} = 1 MHz for MAX261/2, f_{CLK} = 350kHz for MAX260
2. f_{CLK}/f_0 ratio programmed at N = 63 (see Table 2)
3. Clock feedthrough is removed with an RC lowpass at $4f_0$, i.e. R = 3.9kΩ, C = 2000pF for MAX261.

Noise Spectral Distribution (MAX261, f_{CLK} = 1 MHz, dB ref. to 2.47V_{RMS}, 7V_{p-p})

Measurement Bandwidth	Q=1	Q=8	Q=64
Wideband	-84	-80	-72
3 KHz	-87	-87	-86
C Message Weighted	-93	-93	-93

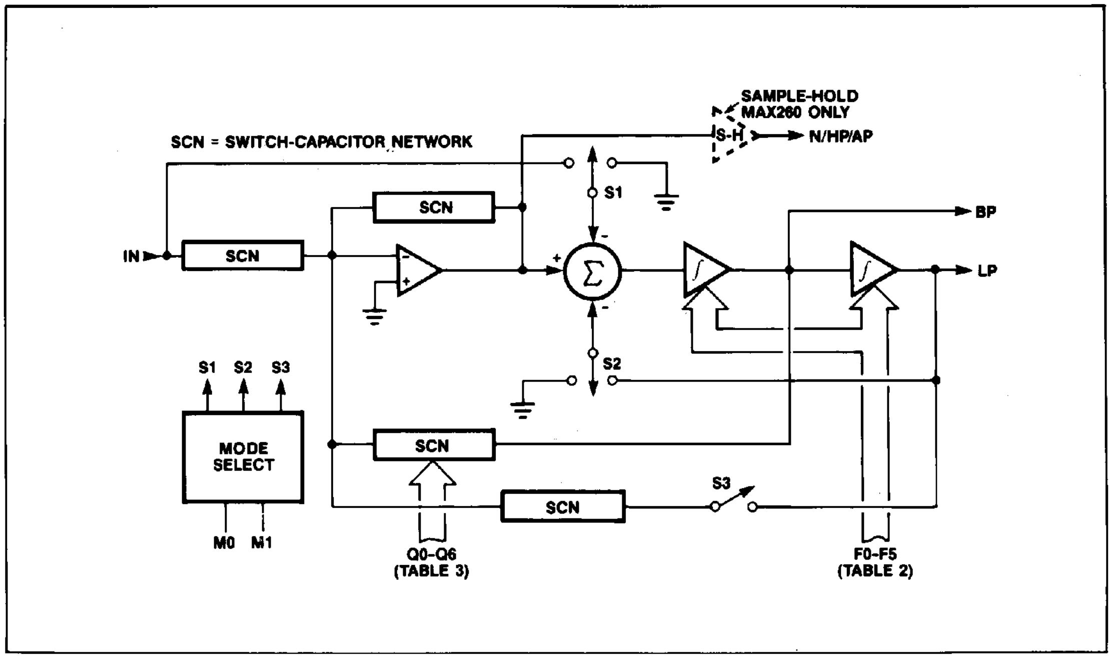


Figure 1. Filter Block Diagram (One Second-Order Section)

Introduction

Each MAX260/61/62 contains two second-order switched-capacitor active filters. Figure 1 shows the filter's state variable topology, employed with two cascaded integrators and one summing amplifier. The MAX261 and MAX262 also contain an uncommitted amplifier. On-chip switches and capacitors provide feedback to control each filter section's f_0 and Q. Internal capacitor ratios are primarily responsible for the accuracy of these parameters. Although these switched-capacitor networks (SCN) are in fact sampled systems, their behavior very closely matches that of continuous filters, such as RC active filters. The ratio of the clock frequency to the filter center frequency (f_{CLK}/f_0) is kept large so that ideal second-order state-variable response is maintained.

The MAX262 uses a lower range of sampling (f_{CLK}/f_0) ratios than the MAX260 or MAX261 to allow higher operating f_0 frequencies and signal bandwidths. These reduced sample rates result in somewhat more deviation from ideal continuous filter parameters than with the MAX260/61. However, these differences can be compensated using Figure 20 (See "Applications Hints") or Maxim's filter design software.

The MAX260 employs auto-zero circuitry not included in the MAX261 or 262. This provides improved DC characteristics, and improved low frequency performance at the expense of high end f_0 and signal bandwidth. The N/HP/AP outputs of the MAX260 are internally sample-and-held, as a result of its auto-zero operation. Signal swing at this output is somewhat reduced as a result (MAX260 only). See Table 1 for bandwidth comparisons of the three filters.

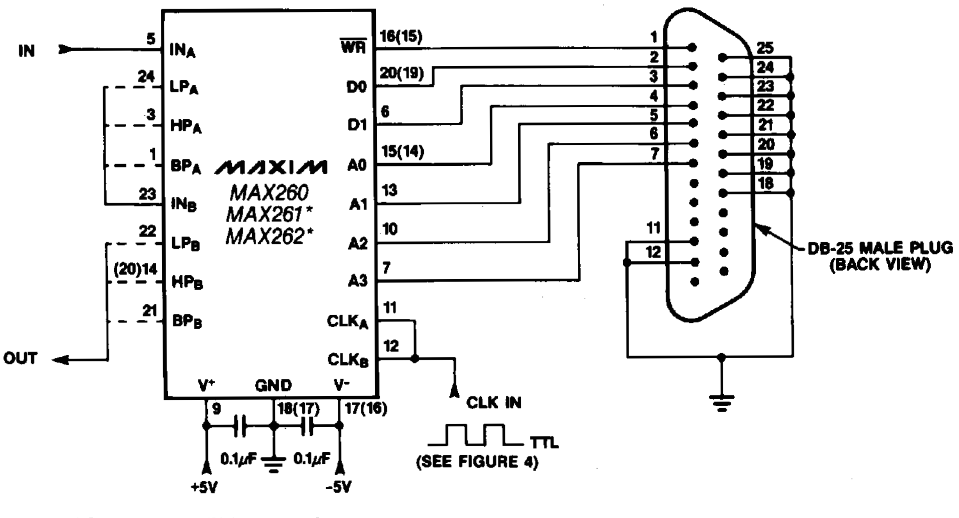
Maxim also provides design programs which aid in converting filter response specifications into the f_0 and Q program codes used by the MAX260 series devices. This software also precompensates f_0 and Q when low sample rates are used.

It is important to note that in all MAX260 series filters, the filter's internal sample rate is one half the input clock rate (CLK_A or CLK_B) due to an internal division by two. All clock related data, tables, and other discussions in this data sheet refer to the frequency at the CLK_A or CLK_B input, i.e. twice the internal sample rate, unless specifically stated otherwise.

Quick Look Design Procedure

The MAX260, MAX261 and MAX262, with Maxim's filter design software, greatly simplifies the design procedures for many active filters. Most designs can be realized using a three step process described in this section. If the design software is not used, or if the filter complexity is beyond the scope of this section, refer to the remainder of this data sheet for more detailed applications and design information.

```
100  AB$="FILTER A " : GOSUB 150 : REM GET DATA FOR SECTION A
110  ADD = 0 : GOSUB 220 : REM WRITE DATA TO THE PRINTER PORT
120  AB$="FILTER B " : GOSUB 150 : REM GET DATA FOR B
130  ADD = 32 : GOSUB 220 : REM WRITE DATA TO PRINTER PORT
140  GOTO 100
150  PRINT "MODE (1 to 4, see Table 5) "; AB$; : INPUT M
160  IF M<1 OR M>4 THEN GOTO 150
170  PRINT "CLOCK RATIO (0 to 63, N of Table 2) "; AB$; : INPUT F
180  IF F<0 OR F>63 THEN GOTO 170
190  PRINT "Q (0 to 127, N of Table 3) "; AB$; : INPUT Q
200  IF Q<0 OR Q>127 THEN GOTO 190 ELSE : PRINT
210  RETURN
220  LPRINT CHR$(ADD+M-1); : ADD = ADD+4
230  FOR I = 1 TO 3
240  X=(ADD + (F - 4*INT(F/4))) : LPRINT CHR$(X);
250  F=INT(F/4) : ADD = ADD + 4
260  NEXT I
270  FOR I = 1 TO 4
280  X=(ADD + (Q - 4*INT(Q/4))) : LPRINT CHR$(X);
290  Q=INT(Q/4) :: ADD = ADD + 4
300  NEXT I
310  RETURN
```



* PIN NUMBERS IN ( ) ARE FOR MAX261/262

Figure 2. Basic Program and Hardware Connections to Parallel Printer Port for "Quick Look" Using a Personal Computer.

Step 1—Filter Design

Start with the program "PZ" to determine what type of filter is needed. This helps determine the type (Butterworth, Chebyshev, etc.) and the number of poles for the optimum choice. The program also plots the frequency response and calculates the pole/zero (f_0) and Q values for each second-order section. Each MAX260/61/62 contains two second-order sections and devices may be cascaded for higher order filters.

Step 2—Generate Programming Coefficients

Starting with the f_0 and Q values obtained in Step 1, use the program "MPP" to generate the digital coefficients which program each second-order section's f_0 and Q. The program displays values for "N" ("N = __ for f_0" and "N = __ for Q"). N is the decimal equivalent of the binary code that sets the filter section's f_0 or Q. These are the same "N"s that are listed in Tables 2 and 3.

An input clock frequency and filter "Mode" must also be selected in this step, however if a specific clock rate is not selected, "GEN" will pick one. With regard to mode selection, Mode 1 is the most convenient choice for most bandpass and lowpass filters. Exceptions are elliptic bandpass and lowpass filters which require Mode 3. Highpass filters also use Mode 3, while allpass filters use Mode 4. For further information regarding these filter modes see "Filter Operating Modes" in this data sheet.

Step 3—Loading the Filter

When the N values for the f_0 and Q of each second-order filter section are determined, the filter can then be programmed and operated. What follows is a convenient method of programming the filter and evaluating a design if a personal computer is available.

A short Basic program loads data into the MAX260/261/262 via the personal computer's parallel printer port. The program asks for the filter Mode as well as the N values for the f_0 and Q of each section. These coefficients are then loaded into the filter in the form of ASCII characters. This program may be used with or without Maxim's other filter design software. The program and the appropriate hardware connections for a Centronics type printer port are shown in Figure 2.

Filter Design Software

Maxim provides software programs to help speed the transition from frequency response design requirements to working hardware. A series of programs are available, including:

Program PZ. Given the requirements, such as center frequency, Q, passband ripple, and stopband attenuation, PZ will calculate the pole frequencies, Q's, zeros, and the number of stages needed.

Program MPP. For programmed filters, MPP computes the input codes to use and describes the expected performance of the design.

Program FR. When a design of one or more stages is completed, FR checks the final cascaded assembly. The output frequency response can be compared with that expected from PZ.

Program PR.BAS Allows a MAX260/61/62 to be programmed via a personal computer. The Mode, f_0, and Q of each section are typed in, and the proper codes are sent to the filter via the computer's parallel printer port. This program is also provided in Figure 2.

Other design programs are also included for use with other Maxim filter products.

Other Filter Products

Maxim has developed a number of other filter products in addition to the MAX260, MAX261 and MAX262:

PIN PROGRAMMABLE ACTIVE FILTERS—A dual second-order universal filter that needs no external components. A Microprocessor interface is not required.

MAX263	0.4Hz to 30kHz f_0 range
MAX264	1Hz to 75kHz f_0 range

RESISTOR AND PIN PROGRAMMABLE FILTERS—A dual second-order universal filter where f_0 adjustment beyond pin-programmable resolution employs external resistors.

MAX265	0.4Hz to 30kHz f_0 range. Includes two uncommitted op-amps.
MAX266	1Hz to 75kHz f_0 range. Includes two uncommitted op-amps.
MF10	Industry Standard. Resistor Programmed Only

PIN PROGRAMMABLE BANDPASS FILTERS—A dual second-order bandpass that needs no external components. A Microprocessor interface is not required.

MAX267	0.4Hz to 30kHz f_0 range
MAX268	1Hz to 75kHz f_0 range

PROGRAMMABLE ANTI-ALIAS FILTER—A programmable dual second-order continuous (not switched) lowpass filter. No clock noise is generated. Designed for use as an anti-alias filter in front of, or as a smoothing filter following, any sampled filter or system.

MAX270	1kHz to 25kHz Cutoff Frequency Range

5th ORDER LOW PASS FILTER—Features zero offset and drift errors for designs requiring high DC accuracy.

MAX280, LT1062	0.1Hz to 20kHz Cutoff Frequency Range

Detailed Description

f_0 and Q Programming

Figure 3 shows a block diagram of the MAX260. Each 2nd-order filter section has its own clock input and independent f_0 and Q control. The actual center frequency is a function of the filter's clock rate, 6-bit f_0 control word (see Table 2), and operating Mode. The Q of each section is also set by a separate programmed input (see Table 3). This way each half of a MAX260/61/62 is tuned independently so that complex filter polynomials can be realized. Equations which convert program code numbers to f_{CLK}/f_0 and Q values are listed in the notes beneath Tables 2 and 3.

Table 1. Typical Clock and Center Frequency Limits

PART	Q	MODE	f_{CLK}	f_0
MAX260	1	1	1Hz-400kHz	0.01Hz-4.0kHz
	1	2	1Hz-425kHz	0.01Hz-6.0kHz
	1	3	1Hz-500kHz	0.01Hz-5.0kHz
	1	4	1Hz-400kHz	0.01Hz-4.0kHz
	8	1	1Hz-500kHz	0.01Hz-5.0kHz
	8	2	1Hz-700kHz	0.01Hz-10.0kHz
	8	3	1Hz-700kHz	0.01Hz-5.0kHz
	8	4	1Hz-600kHz	0.01Hz-4.0kHz
	64	1	1Hz-750kHz	0.01Hz-7.5kHz
	90	2	1Hz-500kHz	0.01Hz-7.0kHz
	64	3	1Hz-400kHz	0.01Hz-4.0kHz
	64	4	1Hz-750kHz	0.01Hz-7.5kHz
MAX261	1	1	40Hz-4.0MHz	0.4Hz-40kHz
	1	2	40Hz-4.0MHz	0.5Hz-57kHz
	1	3	40Hz-4.0MHz	0.4Hz-40kHz
	1	4	40Hz-4.0MHz	0.4Hz-40kHz
	8	1	40Hz-2.7MHz	0.4Hz-27kHz
	8	2	40Hz-2.1MHz	0.5Hz-30kHz
MAX261	8	3	40Hz-1.7MHz	0.4Hz-17kHz
	8	4	40Hz-2.7MHz	0.4Hz-27kHz
	64	1	40Hz-2.0MHz	0.4Hz-20kHz
	90	2	40Hz-1.2MHz	0.4Hz-18kHz
	64	3	40Hz-1.2MHz	0.4Hz-12kHz
	64	4	40Hz-2.0MHz	0.4Hz-20kHz
MAX262	1	1	40Hz-4.0MHz	1.0Hz-100kHz
	1	2	40Hz-4.0MHz	1.4Hz-140kHz
	1	3	40Hz-4.0MHz	1.0Hz-100kHz
	1	4	40Hz-4.0MHz	1.0Hz-100kHz
	8	1	40Hz-2.5MHz	1.0Hz-60kHz
	8	2	40Hz-1.4MHz	1.4Hz-50kHz
	8	3	40Hz-1.4MHz	1.0Hz-35kHz
	8	4	40Hz-2.5MHz	1.0Hz-60kHz
	64	1	40Hz-1.5MHz	1.0Hz-37kHz
	90	2	40Hz-0.9MHz	1.4Hz-32kHz
	64	3	40Hz-0.9MHz	1.0Hz-22kHz
	64	4	40Hz-1.5MHz	1.0Hz-37kHz

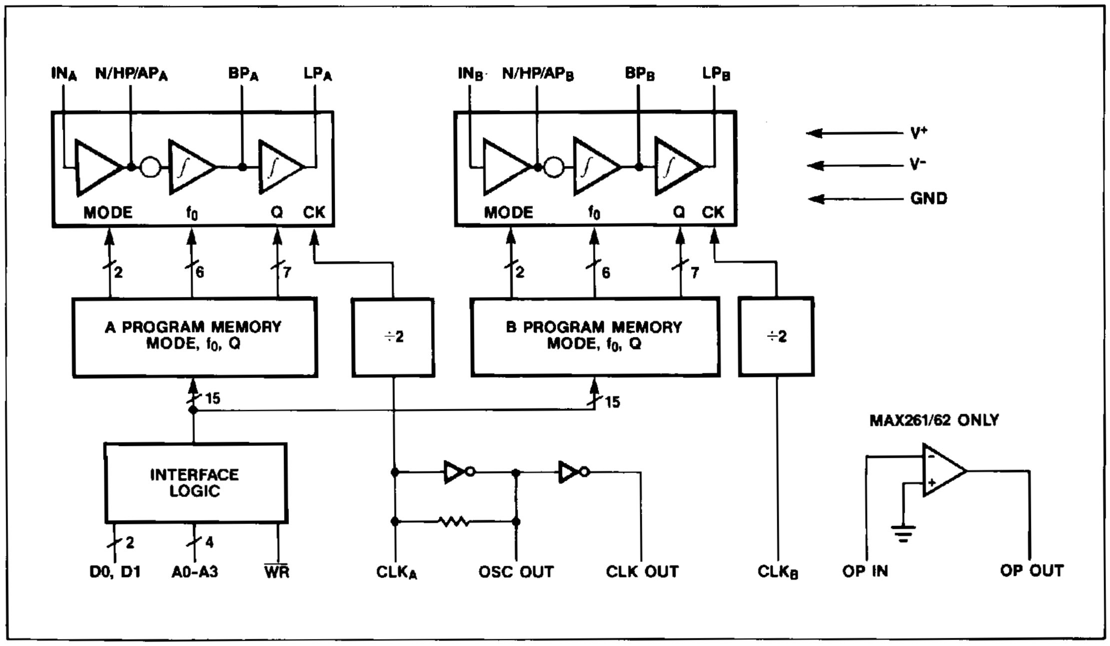


Figure 3. MAX260/61/62 Block Diagram

Microprocessor Programmable Universal Active Filters

Table 2. f_{CLK}/f_0 Program Selection Table

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
100.53	71.09	40.84	28.88	0	0	0	0	0	0	0
102.10	72.20	42.41	29.99	1	0	0	0	0	0	1
103.67	73.31	43.98	31.10	2	0	0	0	0	1	0
105.24	74.42	45.55	32.21	3	0	0	0	0	1	1
106.81	75.53	47.12	33.32	4	0	0	0	1	0	0
108.38	76.64	48.69	34.43	5	0	0	0	1	0	1
109.96	77.75	50.27	35.54	6	0	0	0	1	1	0
111.53	78.86	51.84	36.65	7	0	0	0	1	1	1
113.10	79.97	53.41	37.76	8	0	0	1	0	0	0
114.67	81.08	54.98	38.87	9	0	0	1	0	0	1
116.24	82.19	56.55	39.99	10	0	0	1	0	1	0
117.81	83.30	58.12	41.10	11	0	0	1	0	1	1
119.38	84.42	59.69	42.21	12	0	0	1	1	0	0
120.95	85.53	61.26	43.32	13	0	0	1	1	0	1
122.52	86.64	62.83	44.43	14	0	0	1	1	1	0
124.09	87.75	64.40	45.54	15	0	0	1	1	1	1
125.66	88.86	65.97	46.65	16	0	1	0	0	0	0
127.23	89.97	67.54	47.76	17	0	1	0	0	0	1
128.81	91.80	69.12	48.87	18	0	1	0	0	1	0
130.38	92.19	70.69	49.98	19	0	1	0	0	1	1
131.95	93.30	72.26	51.10	20	0	1	0	1	0	0
133.52	94.41	73.83	52.20	21	0	1	0	1	0	1
135.08	95.52	75.40	53.31	22	0	1	0	1	1	0
136.66	96.63	76.97	54.43	23	0	1	0	1	1	1
138.23	97.74	78.53	55.54	24	0	1	1	0	0	0
139.80	98.86	80.11	56.65	25	0	1	1	0	0	1
141.37	99.97	81.68	57.76	26	0	1	1	0	1	0
142.94	101.08	83.25	58.87	27	0	1	1	0	1	1
144.51	102.89	84.82	59.98	28	0	1	1	1	0	0
146.08	103.30	86.39	61.09	29	0	1	1	1	0	1
147.65	104.41	87.96	62.20	30	0	1	1	1	1	0
149.23	105.52	89.54	63.31	31	0	1	1	1	1	1
150.80	106.63	91.11	64.42	32	1	0	0	0	0	0
152.37	107.74	92.68	65.53	33	1	0	0	0	0	1
153.98	108.85	94.25	66.64	34	1	0	0	0	1	0
155.51	109.96	95.82	67.75	35	1	0	0	0	1	1
157.08	111.07	97.39	68.86	36	1	0	0	1	0	0
158.65	112.18	98.96	69.98	37	1	0	0	1	0	1
160.22	113.29	100.53	71.09	38	1	0	0	1	1	0
161.79	114.41	102.10	72.20	39	1	0	0	1	1	1
163.36	115.52	102.67	73.31	40	1	0	1	0	0	0
164.93	116.63	105.24	74.42	41	1	0	1	0	0	1
166.50	117.74	106.81	75.53	42	1	0	1	0	1	0
168.08	118.85	108.38	76.64	43	1	0	1	0	1	1
169.65	119.96	109.96	77.75	44	1	0	1	1	0	0
171.22	121.07	111.53	78.86	45	1	0	1	1	0	1
172.79	122.18	113.10	79.97	46	1	0	1	1	1	0
174.36	123.29	114.66	81.08	47	1	0	1	1	1	1

Table 2. f_{CLK}/f_0 Program Selection Table (Continued)

f_{CLK}/f_0 RATIO				PROGRAM CODE						
MAX260/61		MAX262								
MODE 1,3,4	MODE 2	MODE 1,3,4	MODE 2	N	F5	F4	F3	F2	F1	F0
175.93	124.40	116.24	82.19	48	1	1	0	0	0	0
177.50	125.51	117.81	83.30	49	1	1	0	0	0	1
179.07	126.62	119.38	84.41	50	1	1	0	0	1	0
180.64	127.73	120.95	85.53	51	1	1	0	0	1	1
182.21	128.84	122.52	86.64	52	1	1	0	1	0	0
183.78	129.96	124.09	87.75	53	1	1	0	1	0	1
185.35	131.07	125.66	88.86	54	1	1	0	1	1	0
186.92	132.18	127.23	89.97	55	1	1	0	1	1	1
188.49	133.29	128.81	91.08	56	1	1	1	0	0	0
190.07	134.40	130.38	92.19	57	1	1	1	0	0	1
191.64	135.51	131.95	93.30	58	1	1	1	0	1	0
193.21	136.62	133.52	94.41	59	1	1	1	0	1	1
194.78	137.73	135.09	95.52	60	1	1	1	1	0	0
196.35	138.84	136.66	96.63	61	1	1	1	1	0	1
197.92	139.95	138.23	97.74	62	1	1	1	1	1	0
199.49	141.06	139.80	98.85	63	1	1	1	1	1	1

Notes: 1) For the MAX260/61, $f_{CLK}/f_0 = (64 + N)\pi/2$ in Mode 1, 3, and 4, where N varies from 0 to 63.
2) For the MAX262, $f_{CLK}/f_0 = (26 + N)\pi/2$ in Mode 1, 3, and 4, where N varies 0 to 63.
3) In Mode 2, all f_{CLK}/f_0 ratios are divided by $\sqrt{2}$. The functions are then:
MAX260/61 $f_{CLK}/f_0 = 1.11072\ (64 + N)$, MAX262 $f_{CLK}/f_0 = 1.11072\ (26 + N)$

Table 3. Q Program Selection Table

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.500*	0.707*	0*	0	0	0	0	0	0	0
0.504	0.713	1	0	0	0	0	0	0	1
0.508	0.718	2	0	0	0	0	0	1	0
0.512	0.724	3	0	0	0	0	0	1	1
0.516	0.730	4	0	0	0	0	1	0	0
0.520	0.736	5	0	0	0	0	1	0	1
0.525	0.742	6	0	0	0	0	1	1	0
0.529	0.748	7	0	0	0	0	1	1	1
0.533	0.754	8	0	0	0	1	0	0	0
0.538	0.761	9	0	0	0	1	0	0	1
0.542	0.767	10	0	0	0	1	0	1	0
0.547	0.774	11	0	0	0	1	0	1	1
0.552	0.780	12	0	0	0	1	1	0	0
0.556	0.787	13	0	0	0	1	1	0	1
0.561	0.794	14	0	0	0	1	1	1	0
0.566	0.801	15	0	0	0	1	1	1	1
0.571	0.808	16	0	0	1	0	0	0	0
0.577	0.815	17	0	0	1	0	0	0	1
0.582	0.823	18	0	0	1	0	0	1	0
0.587	0.830	19	0	0	1	0	0	1	1
0.593	0.838	20	0	0	1	0	1	0	0
0.598	0.846	21	0	0	1	0	1	0	1
0.604	0.854	22	0	0	1	0	1	1	0
0.609	0.862	23	0	0	1	0	1	1	1
0.615	0.870	24	0	0	1	1	0	0	0
0.621	0.879	25	0	0	1	1	0	0	1
0.627	0.887	26	0	0	1	1	0	1	0
0.634	0.896	27	0	0	1	1	0	1	1
0.640	0.905	28	0	0	1	1	1	0	0
0.646	0.914	29	0	0	1	1	1	0	1
0.653	0.924	30	0	0	1	1	1	1	0
0.660	0.933	31	0	0	1	1	1	1	1
0.667	0.943	32	0	1	0	0	0	0	0
0.674	0.953	33	0	1	0	0	0	0	1
0.681	0.963	34	0	1	0	0	0	1	0
0.688	0.973	35	0	1	0	0	0	1	1
0.696	0.984	36	0	1	0	0	1	0	0
0.703	0.995	37	0	1	0	0	1	0	1
0.711	1.01	38	0	1	0	0	1	1	0
0.719	1.02	39	0	1	0	0	1	1	1
0.727	1.03	40	0	1	0	1	0	0	0
0.736	1.04	41	0	1	0	1	0	0	1
0.744	1.05	42	0	1	0	1	0	1	0
0.753	1.06	43	0	1	0	1	0	1	1
0.762	1.08	44	0	1	0	1	1	0	0
0.771	1.09	45	0	1	0	1	1	0	1
0.780	1.10	46	0	1	0	1	1	1	0
0.790	1.12	47	0	1	0	1	1	1	1

Notes: 4) * Writing all 0s into Q0A-Q6A on Filter A activates a low power shutdown mode. BOTH filter sections are deactivated. Therefore this Q value is only achievable in filter B.

Table 3. Q Program Selection Table (Continued)

PROGRAMMED Q		PROGRAM CODE							
MODE 1,3,4	MODE 2	N	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0.800	1.13	48	0	1	1	0	0	0	0
0.810	1.15	49	0	1	1	0	0	0	1
0.821	1.16	50	0	1	1	0	0	1	0
0.831	1.18	51	0	1	1	0	0	1	1
0.842	1.19	52	0	1	1	0	1	0	0
0.853	1.21	53	0	1	1	0	1	0	1
0.865	1.22	54	0	1	1	0	1	1	0
0.877	1.24	55	0	1	1	0	1	1	1
0.889	1.26	56	0	1	1	1	0	0	0
0.901	1.27	57	0	1	1	1	0	0	1
0.914	1.29	58	0	1	1	1	0	1	0
0.928	1.31	59	0	1	1	1	0	1	1
0.941	1.33	60	0	1	1	1	1	0	0
0.955	1.35	61	0	1	1	1	1	0	1
0.969	1.37	62	0	1	1	1	1	1	0
0.985	1.39	63	0	1	1	1	1	1	1
1.00	1.41	64	1	0	0	0	0	0	0
1.02	1.44	65	1	0	0	0	0	0	1
1.03	1.46	66	1	0	0	0	0	1	0
1.05	1.48	67	1	0	0	0	0	1	1
1.07	1.51	68	1	0	0	0	1	0	0
1.08	1.53	69	1	0	0	0	1	0	1
1.10	1.56	70	1	0	0	0	1	1	0
1.12	1.59	71	1	0	0	0	1	1	1
1.14	1.62	72	1	0	0	1	0	0	0
1.16	1.65	73	1	0	0	1	0	0	1
1.19	1.68	74	1	0	0	1	0	1	0
1.21	1.71	75	1	0	0	1	0	1	1
1.23	1.74	76	1	0	0	1	1	0	0
1.25	1.77	77	1	0	0	1	1	0	1
1.28	1.81	78	1	0	0	1	1	1	0
1.31	1.85	79	1	0	0	1	1	1	1
1.33	1.89	80	1	0	1	0	0	0	0
1.36	1.93	81	1	0	1	0	0	0	1
1.39	1.97	82	1	0	1	0	0	1	0
1.42	2.01	83	1	0	1	0	0	1	1
1.45	2.06	84	1	0	1	0	1	0	0
1.49	2.10	85	1	0	1	0	1	0	1
1.52	2.16	86	1	0	1	0	1	1	0
1.56	2.21	87	1	0	1	0	1	1	1
1.60	2.26	88	1	0	1	1	0	0	0
1.64	2.32	89	1	0	1	1	0	0	1
1.68	2.40	90	1	0	1	1	0	1	0
1.73	2.45	91	1	0	1	1	0	1	1
1.78	2.51	92	1	0	1	1	1	0	0
1.83	2.59	93	1	0	1	1	1	0	1
1.88	2.66	94	1	0	1	1	1	1	0
1.94	2.74	95	1	0	1	1	1	1	1
2.00	2.83	96	1	1	0	0	0	0	0
2.06	2.92	97	1	1	0	0	0	0	1
2.13	3.02	98	1	1	0	0	0	1	0
2.21	3.12	99	1	1	0	0	0	1	1
2.29	3.23	100	1	1	0	0	1	0	0
2.37	3.35	101	1	1	0	0	1	0	1
2.46	3.48	102	1	1	0	0	1	1	0
2.56	3.62	103	1	1	0	0	1	1	1
2.67	3.77	104	1	1	0	1	0	0	0
2.78	3.96	105	1	1	0	1	0	0	1
2.91	4.11	106	1	1	0	1	0	1	0
3.05	4.31	107	1	1	0	1	0	1	1
3.20	4.53	108	1	1	0	1	1	0	0
3.37	4.76	109	1	1	0	1	1	0	1
3.56	5.03	110	1	1	0	1	1	1	0
3.76	5.32	111	1	1	0	1	1	1	1
4.00	5.66	112	1	1	1	0	0	0	0
4.27	6.03	113	1	1	1	0	0	0	1
4.57	6.46	114	1	1	1	0	0	1	0
4.92	6.96	115	1	1	1	0	0	1	1
5.33	7.54	116	1	1	1	0	1	0	0
5.82	8.23	117	1	1	1	0	1	0	1
6.40	9.05	118	1	1	1	0	1	1	0
7.11	10.1	119	1	1	1	0	1	1	1
8.00	11.3	120	1	1	1	1	0	0	0
9.14	12.9	121	1	1	1	1	0	0	1
10.7	15.1	122	1	1	1	1	0	1	0
12.8	18.1	123	1	1	1	1	0	1	1
16.0	22.6	124	1	1	1	1	1	0	0
21.3	30.2	125	1	1	1	1	1	0	1
32.0	45.3	126	1	1	1	1	1	1	0
64.0	90.5	127	1	1	1	1	1	1	1

Notes: 5) In Modes 1, 3, and 4: Q = 64/(128-N)

6) In Mode 2, the listed Q values are those of Mode 1 multiplied by $\sqrt{2}$. Then Q = 90.51/(128-N)

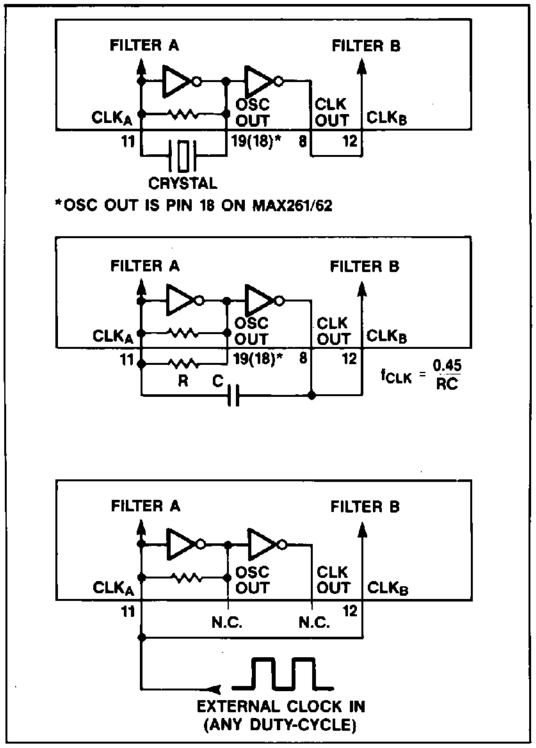


Figure 4. Clock Input Connections

Oscillator and Clock Inputs

The clock circuitry of the MAX260/61/62 can operate with a crystal, resistor-capacitor (RC) network, or an external clock generator as shown in Figure 4. If an RC oscillator is used, the clock rate, f_{CLK}, nominally equals 0.45/RC.

The duty cycle of the clock at CLK$_A$ and CLK$_B$ is unimportant because the input is internally divided by two to generate the sampling clock for each filter section. It is important to note that this internal division also halves the sample rate when considering aliasing and other sampled system phenomenon.

Microprocessor Interface

f_0, Q, and Mode selection data is stored in an internal program memory. The memory contents are updated by writing to addresses selected by A0-A3. D0 and D1 are the data inputs. A map of the memory locations is shown in Table 4. Data is stored in the selected address on the rising edge of $\overline{WR}$. Address and data inputs are TTL and CMOS compatible when the filter is powered from ±5 volts. With other power supply voltages, CMOS logic levels should be used. Interface timing is shown in Figure 5. Note: Clock inputs CLK$_A$ and CLK$_B$ have no relation to the digital interface. They control the switched-capacitor filter sample rate only.

Table 4. Program Address Locations

DATA BIT		ADDRESS				LOCATION
D0	**D1**	**A3**	**A2**	**A1**	**A0**	
FILTER A						
M0$_A$	M1$_A$	0	0	0	0	0
F0$_A$	F1$_A$	0	0	0	1	1
F2$_A$	F3$_A$	0	0	1	0	2
F4$_A$	F5$_A$	0	0	1	1	3
Q0$_A$	Q1$_A$	0	1	0	0	4
Q2$_A$	Q3$_A$	0	1	0	1	5
Q4$_A$	Q5$_A$	0	1	1	0	6
Q6$_A$		0	1	1	1	7
FILTER B						
M0$_B$	M1$_B$	1	0	0	0	8
F0$_B$	F1$_B$	1	0	0	1	9
F2$_B$	F3$_B$	1	0	1	0	10
F4$_B$	F5$_B$	1	0	1	1	11
Q0$_B$	Q1$_B$	1	1	0	0	12
Q2$_B$	Q3$_B$	1	1	0	1	13
Q4$_B$	Q5$_B$	1	1	1	0	14
Q6$_B$		1	1	1	1	15

Note: Writing 0 into Q0$_A$-Q6$_A$ (address locations 4-7) on Filter A activates shutdown mode. BOTH filter sections deactivate.

Some noise may be generated on the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

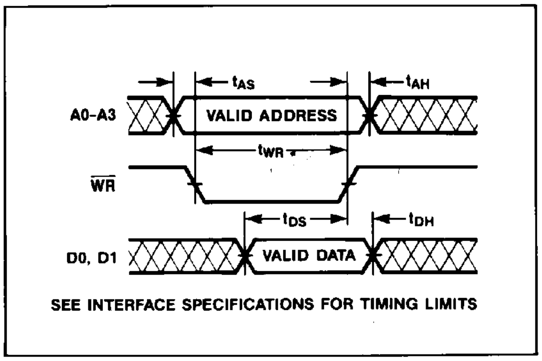


Figure 5. Interface Timing

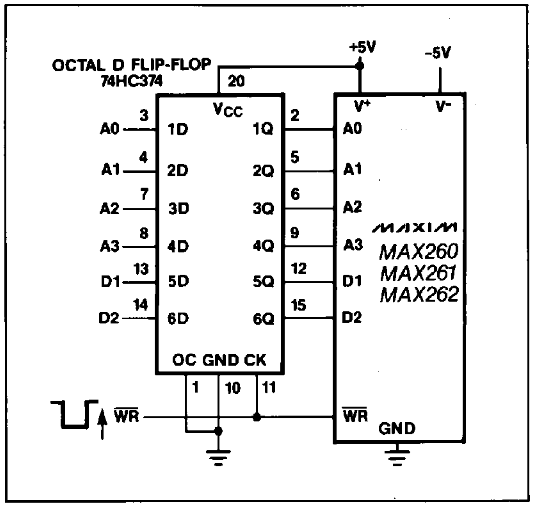


Figure 6. Buffering/Latching Logic Inputs

Shutdown Mode

The MAX260/61/62 enters a shutdown/standby mode when all zeroes are written to the Q addresses of filter A ($Q0_A$-$Q6_A$). When shut down, power consumption with ±5V supplies typically drops to 10mW. When reactivating the filter after shutdown, allow 2ms to return to full operation.

Filter Operating Modes

There are several ways in which the summing amplifier and integrators in each MAX260/61/62 filter section can be configured. The four most versatile interconnections (modes) are selected by writing to inputs M0 and M1 (See Tables 4 and 5). These modes use no external components. A fifth mode, 3A, makes use of an additional op-amp (included in the MAX261 and 262) and external resistors but uses the same internal configuration, and is selected with the same programming code, as Mode 3.

Figures 7 through 11 show symbolic representations of the MAX260 filter modes. Only one second-order section is shown in each case. The A and B sections of one MAX260/61/62 can be programmed for different modes if desired. The f_0, f_N (notch), Q, and various output gains in each case are shown in Table 5.

Filter Mode Selection

MODE 1 (Figure 7) is useful when implementing all-pole lowpass and bandpass filters such as Butterworth, Chebyshev, Bessel, etc.. It can also be used for notch filters, but only second-order notches because the relative pole and zero locations are fixed. Higher order notch filters require more latitude in f_0 and f_N, which is why they are more easily implemented with Mode 3A.

Mode 1, along with Mode 4, supports the highest clock frequencies (See Table 1) because the input summing amplifier is outside the filter's resonant loop (Figure 7). The gain of the lowpass and notch outputs

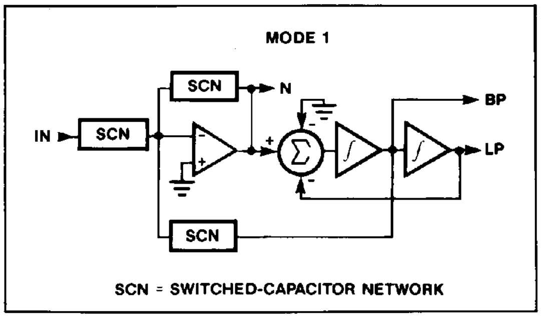


Figure 7. Filter Mode 1: Second-Order Bandpass, Lowpass and Notch

Table 5. Filter Modes for Second-Order Functions

MODE	M1, M0	FILTER FUNCTIONS	f_0	Q	f_N	H_{OLP}	H_{OBP}	H_{ON1} ($f \to 0$)	H_{ON2} ($f \to f_{CLK}/4$)	OTHER
1	0, 0	LP, BP, N	SEE TABLE 2	SEE TABLE 3	f_0	-1	-Q	-1	-1	
2	0, 1	LP, BP, N			$f_0\sqrt{2}$	-0.5	$-Q/\sqrt{2}$	-0.5	-1	
3	1, 0	LP, BP, HP				-1	-Q			$H_{OHP} = -1$
3A	1, 0	LP, BP, HP, N			$f_0\sqrt{\frac{R_H}{R_L}}$	-1	-Q	$+\frac{R_G}{R_L}$	$+\frac{R_G}{R_H}$	$H_{OHP} = -1$
4	1, 1	LP, BP, AP				-2	-2Q			$H_{OAP} = -1$ $f_Z = f_0$, $Q_Z = Q$

Notes:
f_0 = Center Frequency
f_N = Notch Frequency
H_{OLP} = Lowpass Gain at DC
H_{OBP} = Bandpass Gain at f_0
H_{OHP} = Highpass Gain as f approaches $f_{CLK}/4$
H_{ON1} = Notch Gain as f approaches DC
H_{ON2} = Notch Gain as f approaches $f_{CLK}/4$
H_{OAP} = Allpass Gain
f_Z, Q_Z = f and Q of Complex Pole Pair

is 1, while the bandpass gain at the center frequency is Q. For bandpass gains other than Q, the filter input or output can be scaled by a resistive divider or op-amp.

MODE 2 (Figure 8) is used for all-pole lowpass and bandpass filters. Key advantages compared to Mode 1 are higher available Qs (See Table 3) and lower output noise. Mode 2's available f_{CLK}/f_0 ratios are $\sqrt{2}$ less than with Mode 1 (See Table 2) so a wider overall range of f_0s can be selected from a single clock when both modes are used together. This is demonstrated in the Wide Passband Chebyshev Bandpass design example.

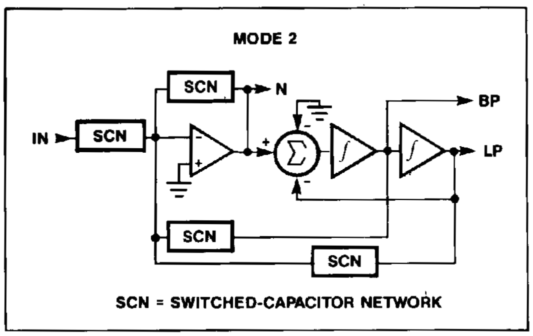


Figure 8. Filter Mode 2: Second-Order Bandpass, Lowpass and Notch

MODE 3 (Figure 9) is the only mode which produces high-pass filters. The maximum clock frequency is somewhat less than with MODE 1 (See Table 1).

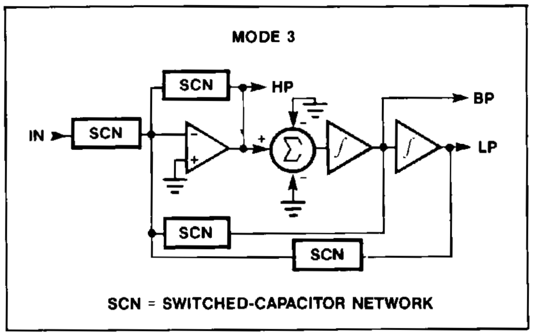


Figure 9. Filter Mode 3: Second-Order Bandpass, Lowpass and Highpass

MODE 3A (Figure 10) uses a separate op-amp to sum the highpass and lowpass outputs of Mode 3, creating a separate notch output. This output allows the notch to be set independently of f_0 by adjusting the op-amp's feedback resistor ratio (R_H, R_L). R_H, R_L, and R_G are external resistors. Because the notch can be independently set, Mode 3A is also useful when designing pole-zero filters such as elliptics.

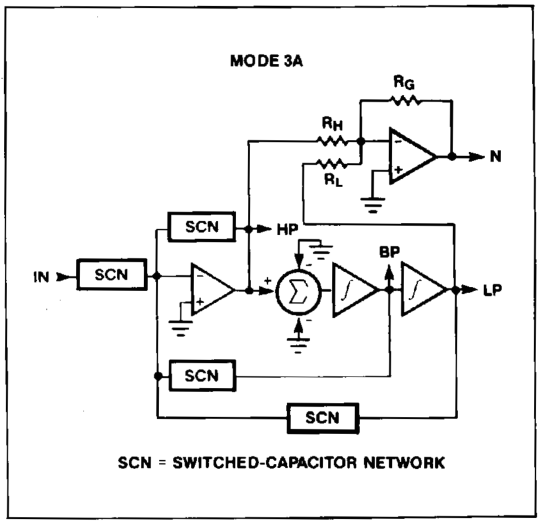


Figure 10. Filter Mode 3A: Second-Order Bandpass, Lowpass, Highpass and Notch. For elliptic LP, BP, HP and Notch, the N output is used

MODE 4 (Figure 11) is the only mode that provides an allpass output. This is useful when implementing group delay equalization. In addition to this, Mode 4 can also be used in all pole lowpass and bandpass filters. Along with Mode 1, it is the fastest operating mode for the filter, although the gains are different than in Mode 1. When the allpass function is used, note that some amplitude peaking occurs (approximately 0.3dB when Q = 8) at f_0. Also note that f_0 and Q sampling errors are highest in Mode 4 (See Figure 20).

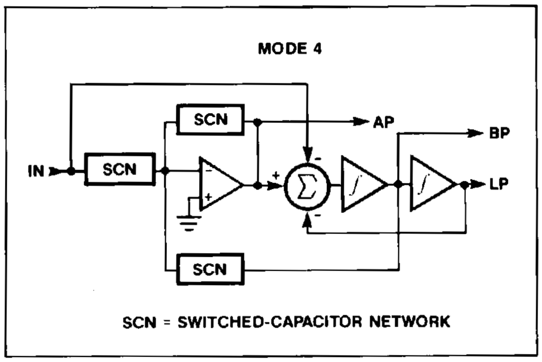


Figure 11. Filter Mode 4: Second-Order Bandpass, Lowpass and Allpass

Description of Filter Functions

BANDPASS (Figure 12)

For all pole bandpass and lowpass filters (Butterworth, Bessel, Chebyshev) use Mode 1 if possible. If appropriate f_{CLK}/f_0 or Q values are not available in Mode 1, Mode 2 may provide a selection that is closer to the required values. Mode 1 however has the highest bandwidth (See Table 1). For pole-zero filters such as elliptics see Mode 3A.

$$G(s) = H_{OBP}\frac{s(\omega_0/Q)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OBP} = Bandpass output gain at $\omega = \omega_0$

f_0 = $\omega_0/2\pi$ = The center frequency of the complex pole pair. Input-output phase shift is -180° at f_0.

Q = The quality factor of the complex pole pair. Also the ratio of f_0 to -3dB bandwidth of the second-order bandpass response.

LOWPASS See Bandpass text. (Figure 13)

$$G(s) = H_{OLP}\frac{\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OLP} = Lowpass output gain at DC

f_0 = $\omega_0/2\pi$

HIGHPASS (Figure 14)

Mode 3 is the only mode with a highpass output. It will work for all pole filter types such as Butterworth, Bessel and Chebyshev. Use mode 3A for filters employing both poles and zeros such as elliptics.

$$G(s) = H_{OHP}\frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OHP} = Highpass output gain as f approaches $f_{CLK}/4$

f_0 = $\omega_0/2\pi$

NOTCH (Figure 15)

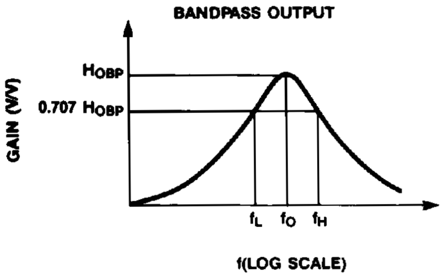
Mode 3A is recommended for multi-pole notch filters. In 2nd order filters, Mode 1 can also be used. The advantages of Mode 1 are higher bandwidth compared to mode 3 (Higher f_N can be implemented) and no need for external components as required in Mode 3A.

$$G(s) = H_{ON2}\frac{s^2 + \omega_n^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{ON2} = Notch output gain as f approaches $f_{CLK}/4$

H_{ON1} = Notch output gain as f approaches DC

f_n = $\omega_n/2\pi$

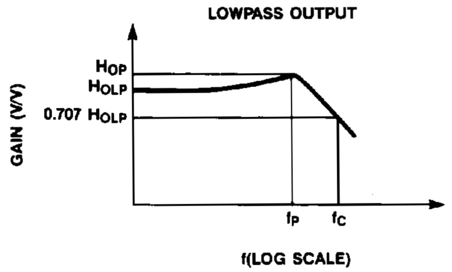


$$Q = \frac{f_O}{f_H - f_L},\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O\left[\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right]$$

$$f_H = f_O\left[\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right]$$

Figure 12. Second-Order Bandpass Characteristics

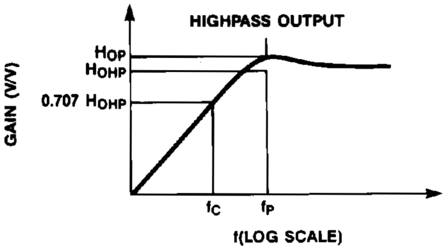


$$f_C = f_O \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_O\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 13. Second-Order Lowpass Characteristics



$$f_C = f_O \times \left[\sqrt{\left(1-\frac{1}{2Q^2}\right)+\sqrt{\left(1-\frac{1}{2Q^2}\right)^2+1}}\right]^{-1}$$

$$f_P = f_O \times \left[\sqrt{1-\frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1-\frac{1}{4Q^2}}}$$

Figure 14. Second-Order Highpass Characteristics

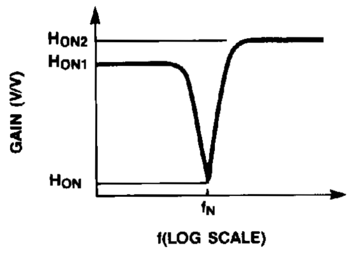


Figure 15. Second-Order Notch Characteristics

ALL PASS

Mode 4 is the only configuration in which an allpass function can be realized.

$$G(s) = H_{OAP}\,\frac{s^2 - s(\omega_o/Q) + \omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

H_{OAP} = All pass output gain for DC $< f < f_{CLK}/4$

$f_0 = \omega_0/2\pi$

Filter Design Procedure

The procedure for most filter designs is to first convert the required frequency response specifications to f_0s and Qs for the appropriate number of second-order sections that implement the filter. This can be done by using design equations or tables in available literature, or can be conveniently calculated using Maxim's filter design software. Once the f_0 and Qs have been found, the next step is to turn them into the digital program coefficients required by the MAX260/61/62. An operating Mode and clock frequency (or clock/center frequency ratio) must also be selected.

Next, if the sample rate ($f_{CLK}/2$) is low enough to cause significant errors, the selected f_0s and Qs should be corrected to account for sampling effects by using Figure 20 or Maxim's design software. In most cases, the sampling errors are small enough to require no correction, i.e. less than 1%. In any case, with or without correction, the required f_0s and Qs can then be selected from Tables 2 and 3. Maxim's filter design software can also perform this last step. The desired f_0s and Qs are stated, and the appropriate digital coefficients are supplied.

Cascading Filters

In some designs, such as very narrow band filters, several second-order sections with identical center frequency may be cascaded. The total Q of the resultant filter is:

$$\text{Total } Q_T = \frac{Q}{\sqrt{(2^{1/N} - 1)}}$$

Q is the Q of each individual filter section, and N is the number of sections. In Table 6, the total Q and bandwidth are listed for up to five identical second-order sections. B is the bandwidth of each section.

Table 6. Cascading Identical Bandpass Filter Sections

Total Sections	Total B.W.	Total Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Note: B = individual stage bandwidth, Q = individual stage Q.

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In high order bandpass filters, stages with different f_0s and Qs are also often cascaded. When this happens the overall filter gain at the bandpass center frequency is not simply the product of the individual gains because f_0, the frequency where each section's gain is specified, is different for each second-order section. The gain of each section at the cascaded filter's center frequency must be determined to obtain the total gain.

For all-pole filters the gain, $H(f_0)$, at each second-order section's f_0 is divided by an adjustment factor, G, to obtain that section's gain, $H(f_{0BP})$, at the overall center frequency:

$H_1(f_{0BP}) = H(f_{01})/G_1$ = Section 1's Gain at f_{0BP}

$$G_1 = \frac{Q_1[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1}$$

where $F_1 = f_{01}/f_{0BP}$

G_1, Q_1, and f_{01} are the gain adjustment factor, Q, and f_0 for the first of the cascaded second-order sections. The gain of the other sections (2, 3 etc.) at f_{0BP} is determined the same way. The overall gain is:

$H(f_{0BP}) = H_1(f_{0BP}) \times H_2(f_{0BP}) \times$ etc.

For cascaded filters with zeros (f_Z) such as elliptics, the gain adjustment factor for each stage is:

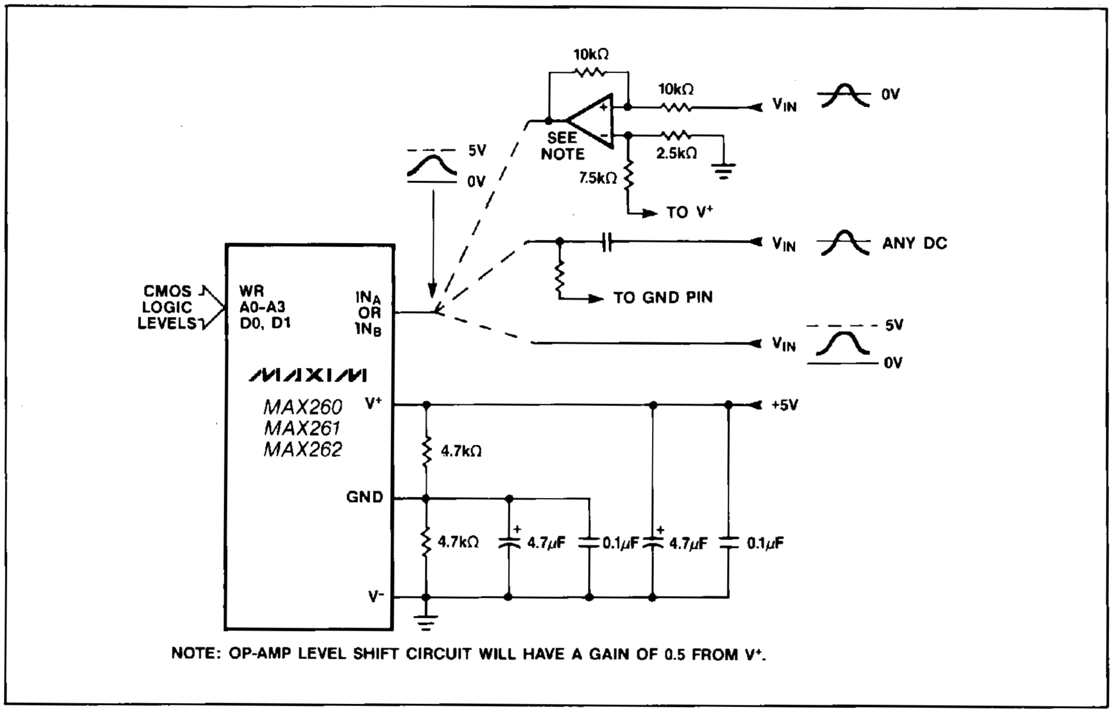
$$G_1 = \frac{Q_1[F_{Z1}^2 - F_1^2]\,[(F_1^2 - 1)^2 + (F_1/Q_1)^2]^{1/2}}{F_1^2(F_{Z1}^2 - 1)}$$

where $F_{1Z} = f_{Z1}/f_{0BP}$, and F_1 is the same as above.

Application Hints

Power Supplies

The MAX260/61/62 can be operated with a variety of power supply configurations including +5V to +12V single supply, or ±2.5V to ±5V dual supplies. When a single supply is used, V⁻ is connected to system ground and the filter's GND pin should be biased at V⁺/2. The input signal is then either capacitively coupled to the filter input or biased to V⁺/2. Figure 16 shows circuit connections for single supply operation.



NOTE: OP-AMP LEVEL SHIFT CIRCUIT WILL HAVE A GAIN OF 0.5 FROM V⁺.

Figure 16. Power Supply and Input Connections for Single Supply Operation

When power supplies other than ±5V are used, CMOS input logic levels (HIGH = V^+, LOW = GND or V^-) are required for $\overline{WR}$, D0-D1, A0-A3, CLK_A and CLK_B . With ±5V supplies, either TTL or CMOS levels can be used. Note however that power consumption at ±5V is reduced if CLK_A and CLK_B are driven with ±5V, rather than TTL or 0 to 5V levels. Operation with +5V or ±2.5V power lowers power consumption but also reduces bandwidth by approximately 25% compared to +12V or ±5V supplies.

Best performance is achieved if V^+ and V^- are bypassed to ground with 4.7μF electrolytic (Tantalum is preferred.) and 0.1μF ceramic capacitors. These should be located as close to the supply pins as possible. The lead length of the bypass capacitors should be shortest at the V^+ and V^- pins. When using a single supply V^+ and GND should be bypassed to V^- as shown in Figure 16.

Output Swing and Clipping

MAX260/61/62 outputs are designed to drive 10kΩ loads. For the MAX261 and MAX262, all filter outputs swing to within 0.15V of each supply rail with a 10kΩ load. In the MAX260 only, an internal sample-hold circuit reduces voltage swing at the N/HP/AP output compared to LP and BP. N/HP/AP therefore swings to within 1V (10kΩ load) of either rail on the MAX260.

To ensure that the outputs are not driven beyond their maximum range (output clipping), the peak amplitude response, individual section gains (H_{OBP}, H_{OLP}, H_{OHP}), input signal level, and filter offset voltages must be carefully considered. It is especially important to check UNUSED outputs for clipping (i.e. the lowpass output in a bandpass hookup) because overload at ANY filter stage severely distorts the overall response. The maximum signal swing with ±4.75V supplies and a 1.0V filter offset is approximately ±3.5V.

For example lets assume a fourth-order lowpass filter is being implemented with a Q of 2 using Mode 1. With a single 5V supply (i.e. ±2.5V with respect to chip GND) the maximum output signal is ±2V (w.r.t. GND). Since in Mode 1 the maximum signal is Q times the input signal, the input should not exceed ±(2/Q)V, or ±1V in this case.

Clock Feedthrough and Noise

Typical wideband noise for MAX260 series devices is 0.5mV_{pp} from DC to 100kHz. The noise is virtually independent of clock frequency. In multistage filters, the section with the highest Q should be placed first for lower output noise.

The output waveform of the MAX260 series and other switched capacitor filters appears as a sampled signal with stepping or "staircasing" of the output waveform occurring at the internal sample rate ($f_{CLK}/2$). This stepping, if objectionable, can be removed by adding a single pole RC filter. With no input signal, clock related feedthrough is approximately 8mV_{pp}. This can also be attenuated with an RC smoothing filter as shown with the MAX261 in Figure 17.

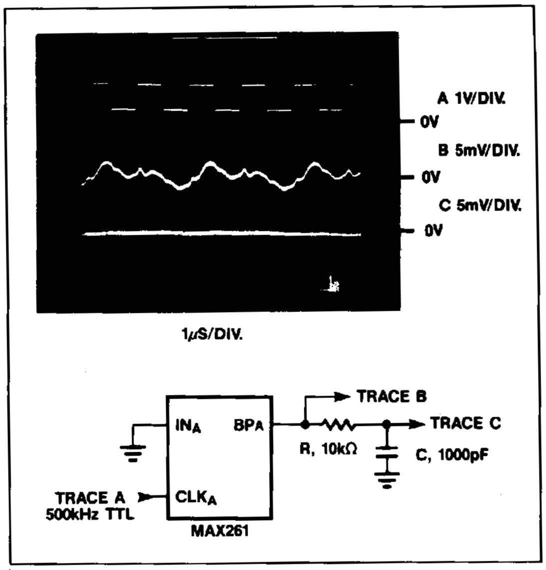


Figure 17. MAX261 Bandpass Output Clock Noise

Some noise also may be generated at the filter outputs by transitions at the logic inputs. If this is objectionable, the digital lines should be buffered from the device by logic gates as shown in Figure 6.

Input Impedance

The input to each filter is the switched capacitor circuit shown in Figure 18. In the MAX260, the input capacitor charges to the input voltage V_{IN} during the first half clock cycle. During the second half-cycle its charge is transferred to the feedback capacitor. The resultant input impedance can be approximated by:

$$R_{IN} = 1/(C_{IN}f_{CLK}/2) = 2/(C_{IN}f_{CLK}).$$

C_{IN} is around 12pF, hence for a clock frequency of 500kHz, R_{IN} = 333kΩ. The input also has about 5pF of fixed capacitance to ground.

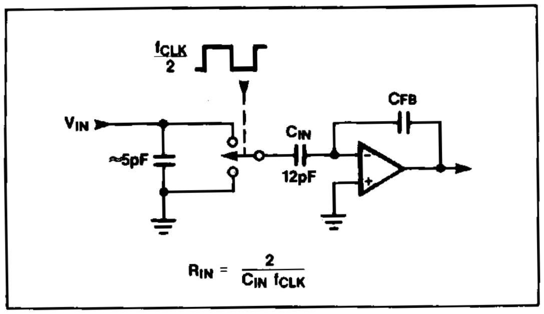


Figure 18. MAX260 Input Model

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The MAX261/262 input structure is shown in Figure 19. Here C_A = 12pF and C_B = 0.016pF and only C_B is switched, so the input resistance is 750 times larger compared to the MAX260 (R_{IN} = 250MΩ). The MAX261/62 has a fixed capacitance of approximately 5pF to ground.

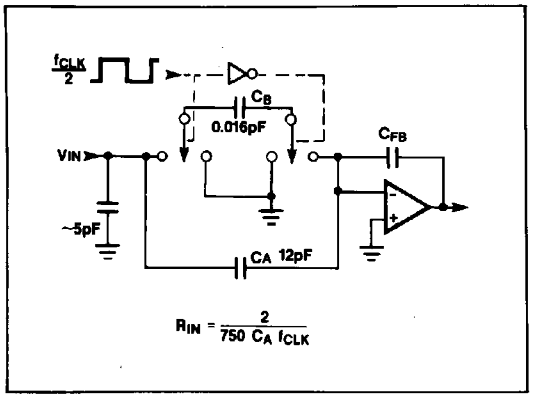


Figure 19. MAX261/262 Input Model

f_0 and Q at Low Sample Rates

When low f_{CLK}/f_0 ratios and low Q settings are selected, deviation from ideal continuous filter response may be noticeable in some designs. This is due to interaction between Q, and f_0 at low f_{CLK}/f_0 ratios and Qs. The data in Figure 20 quantifies these differences. Since the errors are predictable, the graphs can be used to correct the selected f_0 and Q so that the actual realized parameters are on target. These predicted errors are not unique to MAX260 series devices and in fact occur with all types of sampled filters. Consequently, these corrections can be applied to other switched-capacitor filters. In the majority of cases, the errors are not significant, i.e. less than 1%, and correction is not needed. However, the MAX262 does employ a lower range of f_{CLK}/f_0 ratios than the MAX260 or MAX261 and is more prone to sampling errors as the tables show.

Maxim's filter design software applies the previous corrections automatically as a function of desired f_{CLK}/f_0, and Q. Therefore, Figure 20 should NOT be used when Maxim's software determines f_0 and Q. This results in overcompensation of the sampling errors since the correction factors are then counted twice.

The data plotted in Figure 20 applies for Modes 1 and 3. When using Figure 20 for Mode 4, the f_0 error obtained from the graph should be multiplied by 1.5 and the Q error should be multiplied by 3.0. In Mode 2 the value of f_{CLK}/f_0 should be multiplied by $\sqrt{2}$ and the programmed Q should be divided by $\sqrt{2}$ before using the graphs.

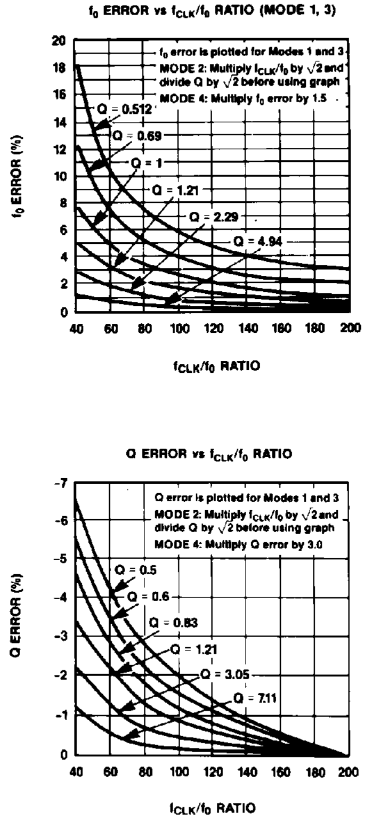


Figure 20. Sampling Errors in f_{CLK}/f_0 and Q at Low f_{CLK}/f_0 and Q Settings

Aliasing

As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. In particular, input signal components near the sampling rate generate difference frequencies that often fall within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, (f_{CLK} = 200kHz) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Remember that with the MAX260 series filters, the nyquist rate (one half the sample rate) is in fact $f_{CLK}/4$ because f_{CLK} is internally divided by two.

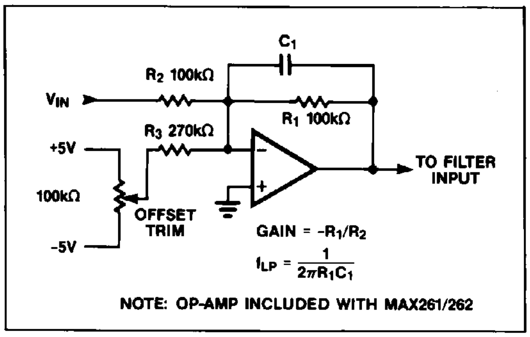
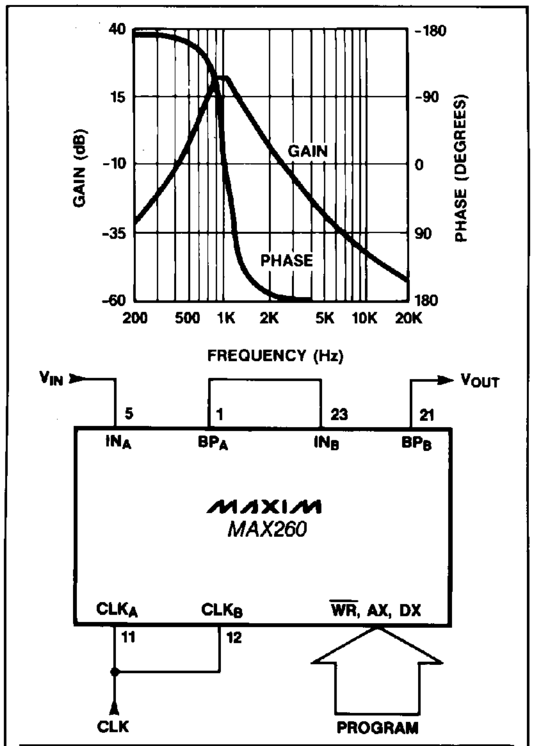


Figure 21. Circuit for DC Offset Adjustment

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can cause aliasing. In many cases the input signal itself may be band limited and require no special anti-alias filtering. The wideband MAX262 uses lower f_{CLK}/f_0 ratios than the MAX260/61 and for this reason is more likely to require input filtering than the MAX260 or MAX261.



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
150kHz	1	N = 42	N = 23	N = 119	N = 119

Figure 22. Fourth-Order Chebyshev Bandpass Filter

Trimming DC Offset

The DC offset voltage at the LP or Notch output can be adjusted with the circuit in Figure 21. This circuit also uses the input op-amp to implement a single pole anti-alias filter. Note that the total offset will generally be less in multistage filters than when only one section is used since each offset is typically negative and each section inverts. When the HP or BP outputs are used, the offset can be removed with capacitor coupling.

Design Examples

Fourth-Order Chebyshev Bandpass Filter

Figure 22 shows both halves of a MAX260 cascaded to form a fourth-order Chebyshev bandpass filter. The desired parameters are:

Center frequency (f_0) = 1 kHz
Pass bandwidth = 200 Hz
Stop Bandwidth = 600 Hz
Max. passband ripple = 0.5 dB
Min. stopband Attenuation = 15 dB

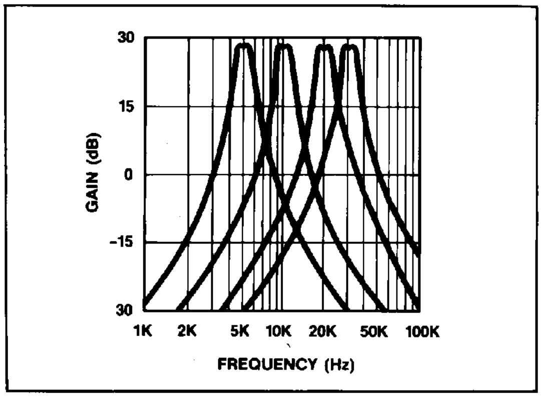


Figure 23. MAX261 Fourth-Order Chebyshev Bandpass Using Coefficients of Figure 22.)

From the above parameters, the order (number of poles), and the f_0 and Q of each section can be determined. Such a derivation is beyond the scope of this data sheet, however there are a number of sources which provide design data for this procedure. These include look-up tables, design texts and computer programs. Design software is available from Maxim to provide comprehensive solutions for most popular filter configurations. The A and B section parameters for the above filter are:

f_{0A} = 904 Hz
Q_A = 7.05
f_{0B} = 1106 Hz
Q_B = 7.05

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To implement this filter, both halves operate in Mode 1 and use the same clock. See selection Tables 2 and 3. The programmed parameters are:

$CLK_A = CLK_B = 150$ kHz
$f_{CLK}/f_{0A} = 166.50$ (Mode 1, N=42), actual $f_{0A} = 902.4$Hz
$f_{CLK}/f_{0B} = 136.66$ (Mode 1, N=23), actual $f_{0B} = 1099.7$Hz
$Q_A = Q_B = 7.11$ (Mode 1, N=119)

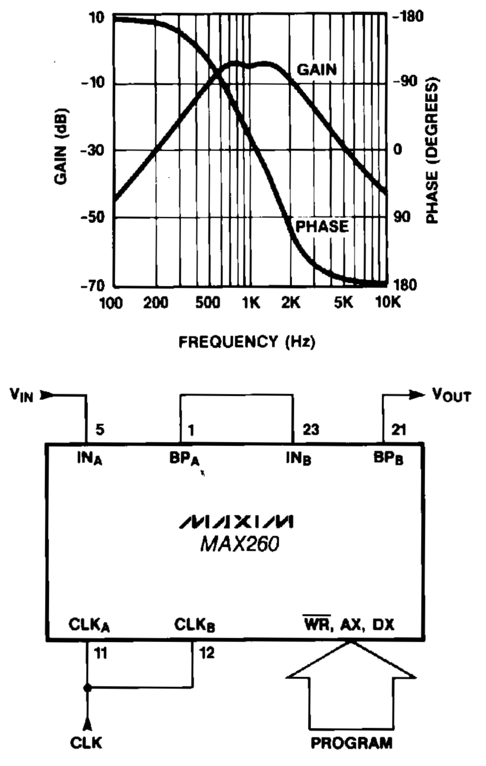
Sampling errors are very small at this f_{CLK}/f_0 ratio so the actual realized Q is very close to 7.05 (See Figure 20 or Filter Program MPP). Often the realized Q will not be exactly the target value at high Qs because programming resolution lowers as Q increases. This doesn't affect most filter designs, since 3-digit Q accuracy is practically never required, and a Q resolution of 1 is provided up to Qs of 10. The overall filter gain at f_0 is 16.4V/V or 24.3dB (See Cascading Filters section). If another gain is required, amplification or attenuation must be added at the input, output, or between stages.

In Figure 23, a series of response curves are shown for the above configuration using a MAX261 with clock frequencies ranging from 750kHz to 4MHz (f_0 from 500Hz to 30kHz). Note that the rightmost curve shows about 2dB of gain peaking compared to the lower frequency curves, indicating the upper limit of usable filter accuracy at this Q (See Table 1)

Wide Passband Chebyshev Bandpass

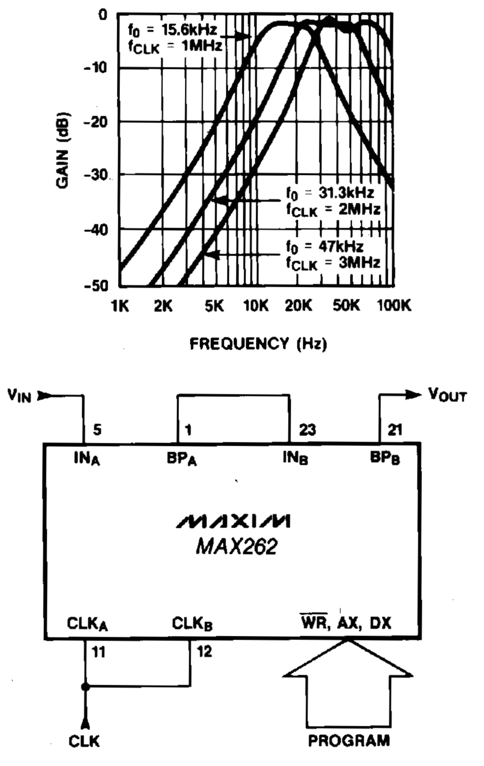
In this example (Figure 24) the desired parameters are:

Center frequency (f_0) = 1 kHz
Pass bandwidth = 1 kHz
Stop bandwidth = 3 kHz
Max passband ripple = 1 dB
Min stopband Attenuation = 20 dB



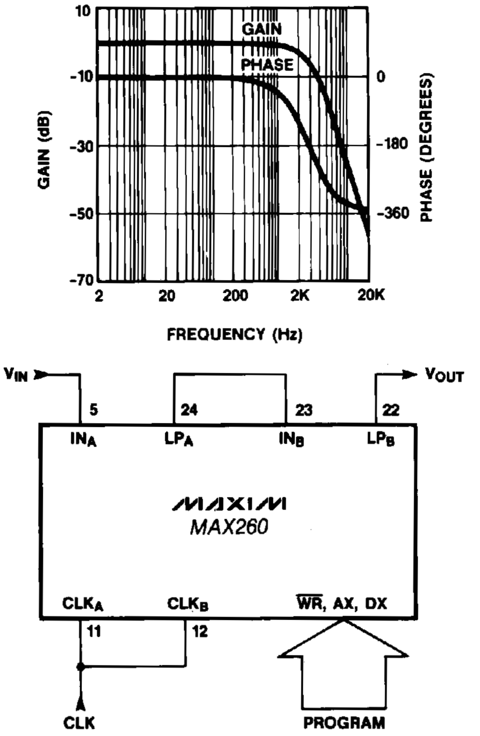
$CLK_{A,B}$	$MODE_A$	$MODE_B$	f_{0A}	f_{0B}	Q_A	Q_B
120kHz	1	2	N=56	N=5	N=96	N=83

Figure 24. Wide Passband Chebyshev Bandpass Filter



$CLK_{A,B}$	MODE	f_{0A}	f_{0B}	Q_A	Q_B
1 to 3MHz	1	N=38	N=0	N=96	N=96

Figure 25. High Frequency Chebyshev Bandpass Filter



$CLK_{A,B}$	MODE	f_{OA}	f_{OB}	Q_A	Q_B
400KHz	1	N = 22	N = 25	N = 79	N = 11

Figure 26. Fourth-Order Butterworth Lowpass

From the above parameters, we use either lookup tables, design texts or Maxim's filter design programs to generate the order (number of poles), and the f_0 and Q of each second-order section. The A and B parameters are:

f_{0A} = 639 Hz	f_{0B} = 1564 Hz
Q_A = 2.01	Q_B = 2.01

To implement this filter, section A operates in Mode 1 and section B uses Mode 2 to provide a wider overall range of f_{CLK}/f_0 ratios. This way one clock frequency can drive both sections A and B. See selection Tables 2 and 3.

CLK_A = CLK_B = 120 kHz

f_{CLK}/f_{0A} = 188.49 (Mode 1, N=56), actual f_{0A} = 636.6 Hz

f_{CLK}/f_{0B} = 76.64 (Mode 2, N=5), actual f_{0B} = 156.5 Hz

Q_A = 2.000 (Mode 1, N=96), Q_B = 2.01 (Mode 2, N=83)

The overall passband gain at f_0 will be 0.64V/V or -3.9dB.

High Frequency Chebyshev Bandpass

The same Chebyshev response shape shown in Figure 24 is implemented at higher frequencies with a MAX262 in Figure 25. The curves show plots for center frequencies of 15.6kHz, 31.3kHz, and 47kHz. Not only is this faster than the MAX260 implementation but Mode 1 can be used in both halves of the MAX262 for this filter because the range of available f_{CLK}/f_0 ratios is wider with the MAX262 than the MAX260.

Fourth-Order Butterworth Lowpass

Figure 26 shows a fourth-order Butterworth lowpass with a cutoff frequency of 3kHz. Section A and B of a MAX260 are cascaded. The f_0 and Q parameters for each section are:

f_{0A} = 3kHz	f_{0B} = 3kHz
Q_A = 1.307	Q_B = 0.541

Mode 1 and a 400kHz clock are used. Because of low Q values, the sampling errors of Figure 20 begin to look significant in this case. From the graphs, using f_{CLK}/f_0 ratio near 133, f_0A will be about 4% high, f_0B will be 1.5% high. Q_A will be -1.2% low, and Q_B will be -0.5% low. If these errors are not a problem, the corrections can be ignored. They are included here for best possible accuracy:

CLK_A = CLK_B = 400 kHz

f_{CLK}/f_{0A} = 135.08 (N=22), f_{0B} = 2961 Hz
(-1.3% correction)

f_{CLK}/f_{0B} = 139.80 (N=25), f_{0A} = 2861 Hz
(-4.6% correction)

Q_A = 1.306 (N=79, Q resolution prevents +0.5% correction)

Q_B = 0.547 (N=11, +1.1% correction)

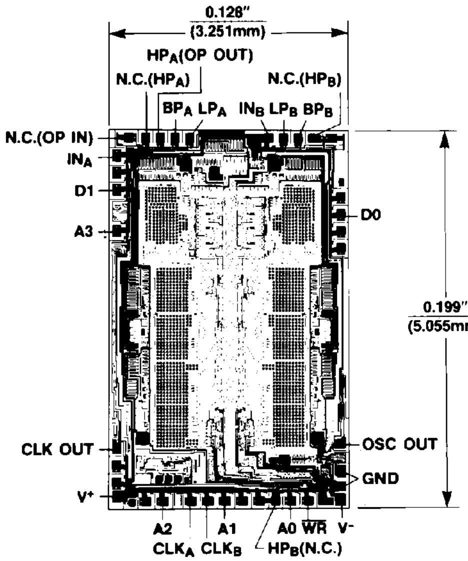
Measured wideband noise for this filter is 123µV RMS. If Mode 2 were used, the noise would be 87µV RMS. For lower noise with either Mode the first section should have the highest Q (Section A in this example).

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ACCURACY
MAX261BCNG	0°C to +70°C	Plastic DIP	2%
MAX261AENG	-40°C to +85°C	Plastic DIP	1%
MAX261BENG	-40°C to +85°C	Plastic DIP	2%
MAX261ACWG	0°C to +70°C	Wide SO	1%
MAX261BCWG	0°C to +70°C	Wide SO	2%
MAX261AMRG	-55°C to +125°C	CERDIP	1%
MAX261BMRG	-55°C to +125°C	CERDIP	2%
MAX262ACNG	0°C to +70°C	Plastic DIP	1%
MAX262BCNG	0°C to +70°C	Plastic DIP	2%
MAX262AENG	-40°C to +85°C	Plastic DIP	1%
MAX262BENG	-40°C to +85°C	Plastic DIP	2%
MAX262ACWG	0°C to +70°C	Wide SO	1%
MAX262BCWG	0°C to +70°C	Wide SO	2%
MAX262AMRG	-55°C to +125°C	CERDIP	1%
MAX262BMRG	-55°C to +125°C	CERDIP	2%

** All devices—24-pin 0.3" wide packages*

Chip Topography



NOTE: LABELS IN PARENTHESES ( ) ARE FOR MAX261/62 ONLY