

**2700 PIXELS  $\times$  3 COLOR CCD LINEAR IMAGE SENSOR**

The  $\mu$ PD3720A is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The  $\mu$ PD3720A has 3 rows of 2700 pixels and 3 pairs of 2 rows of 1350-bit charge transferred registers, reset feed-through level clamp circuits, clamp pulse generation circuit and voltage amplifiers. It is suitable for color image scanners, color facsimiles and so on.

**FEATURES**

- Valid photocell : 2700 pixels  $\times$  3
- Photocell's pitch : 10.5  $\mu$ m
- Line spacing : 42  $\mu$ m (4 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance  $10^7$  lx $\cdot$ hour)
- Resolution : 12 dot/mm A4 (210  $\times$  297 mm) size (shorter side)  
300 dpi US letter (8.5"  $\times$  11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 3 MHz MAX.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits  
Clamp pulse generation circuit  
Voltage amplifiers
- Pin assign : Compatible with the  $\mu$ PD3720

**ORDERING INFORMATION**

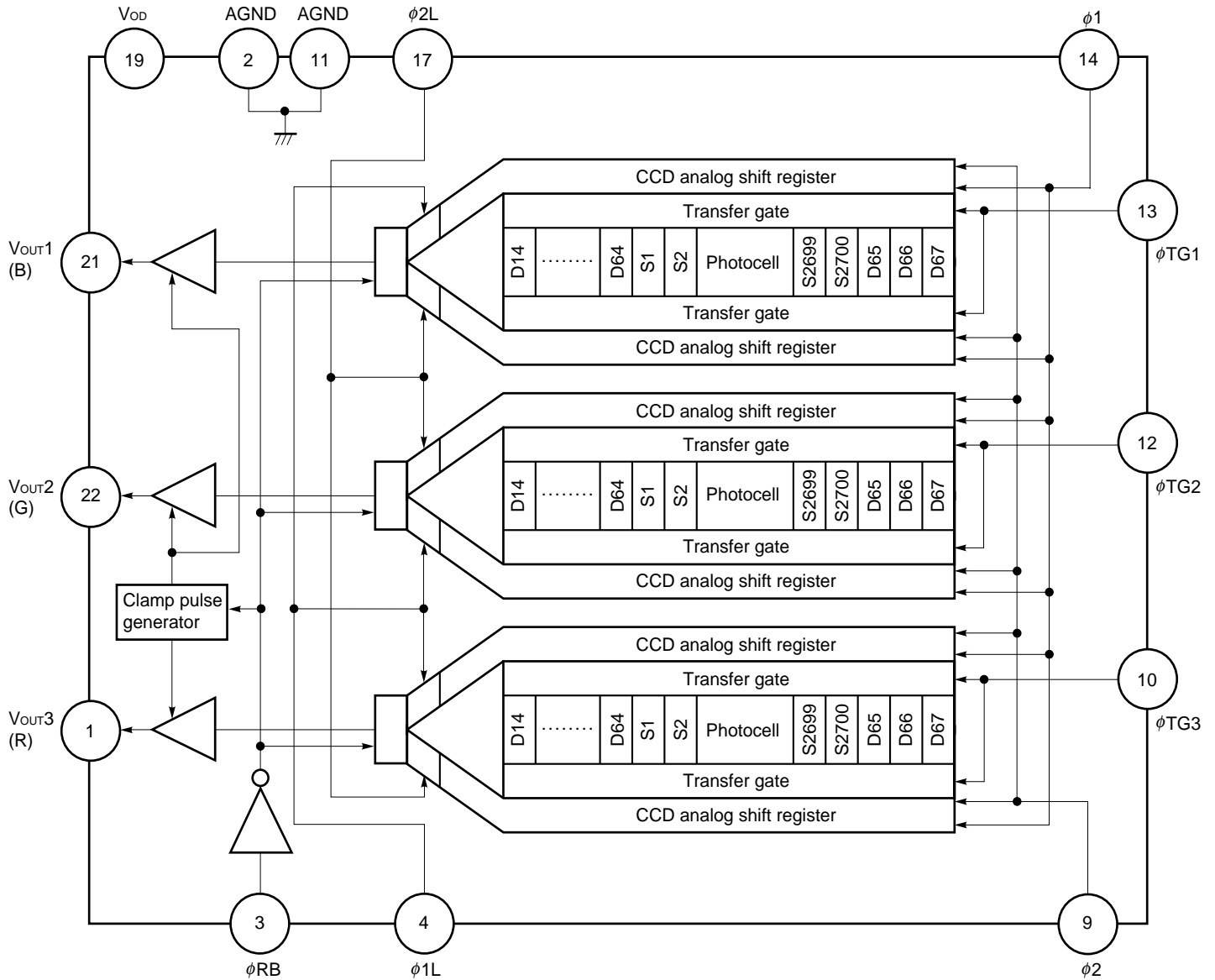
Part Number	Package
$\mu$ PD3720ACY	CCD linear image sensor 22-pin plastic DIP (400 mil)

The information in this document is subject to change without notice.

COMPARISON CHART

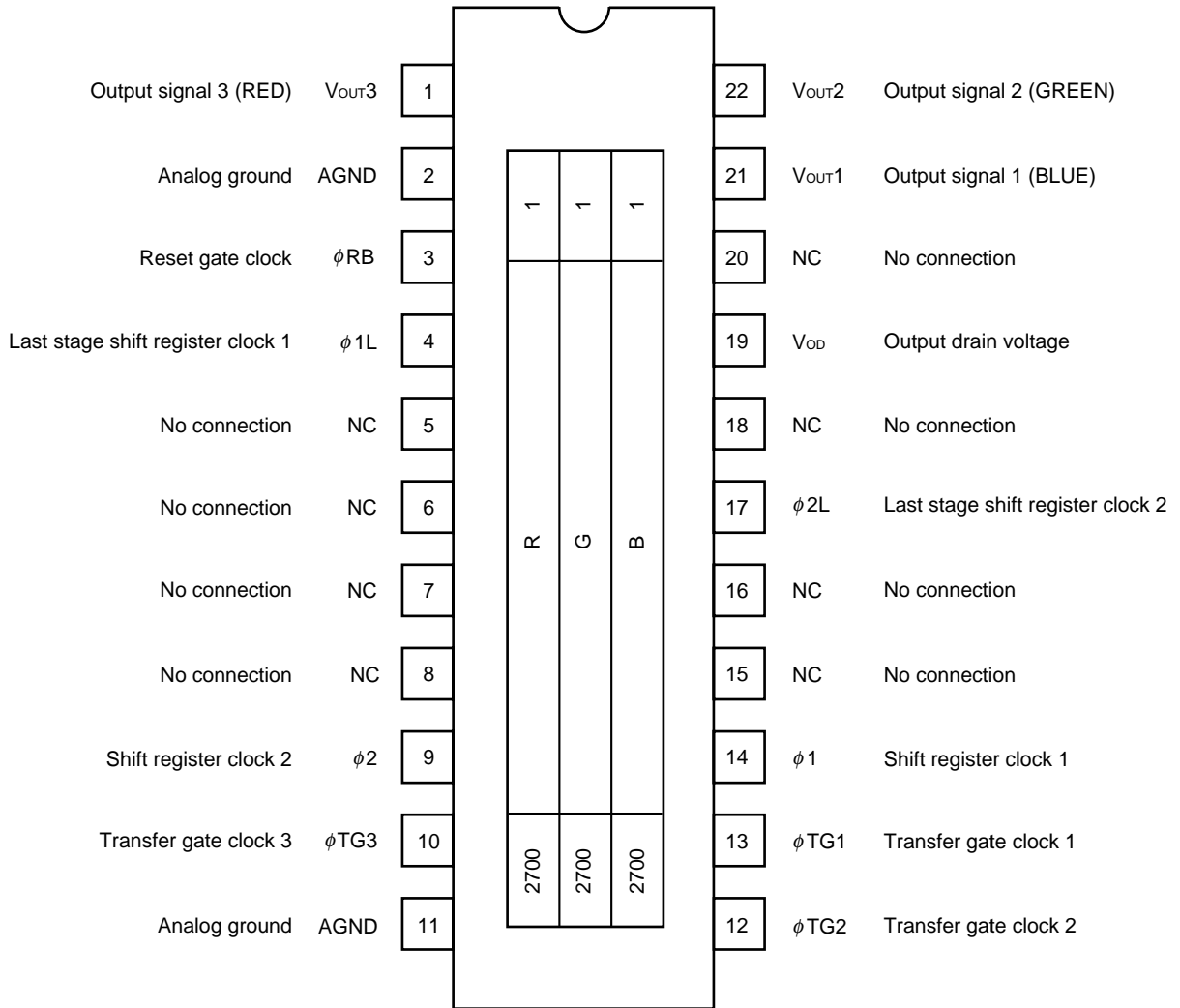
Item		μPD3720A	μPD3720
PIN CONFIGURATION	Pin 11	Analog ground	Digital ground
ELECTRICAL CHARACTERISTICS	Output fall delay time TYP. (ns)	70	80
TIMING CHART	Output signal waveform	Spike noise reduced	-

BLOCK DIAGRAM

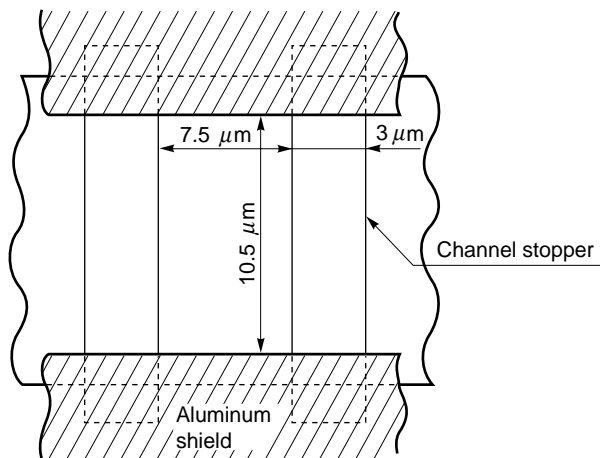


**PIN CONFIGURATION (Top View)**

CCD linear image sensor 22-pin plastic DIP(400 mil)



**PHOTOCELL STRUCTURE DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	Ratings	Unit
Output drain voltage	V <sub>OD</sub>	-0.3 to +15	V
Shift register clock voltage	V <sub>φ1</sub> , V <sub>φ2</sub> , V <sub>φ1L</sub> , V <sub>φ2L</sub>	-0.3 to +15	V
Reset gate clock voltage	V <sub>φRB</sub>	-0.3 to +15	V
Transfer gate clock voltage	V <sub>φTG1</sub> – V <sub>φTG3</sub>	-0.3 to +15	V
Operating ambient temperature	T <sub>A</sub>	-25 to +60	°C
Storage temperature	T <sub>stg</sub>	-40 to +70	°C

**Caution** Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V <sub>OD</sub>	11.4	12.0	12.6	V
Shift register clock signal high level	V <sub>φ1H</sub> , V <sub>φ2H</sub> , V <sub>φ1LH</sub> , V <sub>φ2LH</sub>	4.5	5.0	5.5	V
Shift register clock signal low level	V <sub>φ1L</sub> , V <sub>φ2L</sub> , V <sub>φ1LL</sub> , V <sub>φ2LL</sub>	-0.3	0	+0.5	V
Reset gate clock high level	V <sub>φRBH</sub>	4.5	5.0	5.5	V
Reset gate clock low level	V <sub>φRBL</sub>	-0.3	0	+0.5	V
Transfer gate clock high level	V <sub>φTG1H</sub> – V <sub>φTG3H</sub>	4.5	5.0	5.5	V
Transfer gate clock low level	V <sub>φTG1L</sub> – V <sub>φTG3L</sub>	-0.3	0	+0.5	V
Data rate	f <sub>φRB</sub>	–	1	3	MHz

**ELECTRICAL CHARACTERISTICS**

( $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi RB} = 1\text{ MHz}$ , data rate = 1 MHz, storage time = 5 ms,  
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1mm), input signal clock = 5  $V_{p-p}$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	$V_{sat}$		2.0	3.0	–	V
Saturation exposure	Red	SER		0.15		$\text{lx}\cdot\text{s}$
	Green	SEG		0.16		$\text{lx}\cdot\text{s}$
	Blue	SEB		0.27		$\text{lx}\cdot\text{s}$
Photo response non-uniformity	PRNU	$V_{OUT} = 1\text{ V}$		6	20	%
Average dark signal	ADS	Light shielding		0.5	2.5	mV
Dark signal non-uniformity	DSNU	Light shielding		1.5	8.0	mV
Power consumption	$P_W$			400	600	mW
Output impedance	$Z_o$			0.5	1	$\text{k}\Omega$
Response	Red	$R_R$	14.14	20.20	26.26	$\text{V}/\text{lx}\cdot\text{s}$
	Green	$R_G$	12.95	18.50	24.05	$\text{V}/\text{lx}\cdot\text{s}$
	Blue	$R_B$	7.77	11.10	14.43	$\text{V}/\text{lx}\cdot\text{s}$
Image lag	IL	$V_{OUT} = 1\text{ V}$		2	10	%
Offset level <b>Note1</b>	$V_{OS}$		3	4.5	6.6	V
Output fall delay time <b>Note2</b>	$t_d$	$V_{OUT} = 1\text{ V}$		70		ns
Total transfer efficiency	TTE	$V_{OUT} = 1\text{ V}$ , data rate = 3 MHz	92	98		%
Register imbalance	RI	$V_{OUT} = 1\text{ V}$	0	1.0	4.0	%
Response peak	Red			630		nm
	Green			540		nm
	Blue			460		nm
Dynamic range	DR1	$V_{sat} / \text{DSNU}$		2000		times
	DR2	$V_{sat} / \sigma$		3000		times
Reset feed-through noise <b>Note1</b>	RFTN	Light shielding	–1000	–300	+300	mV
Random noise	$\sigma$	Light shielding	–	1.0	–	mV

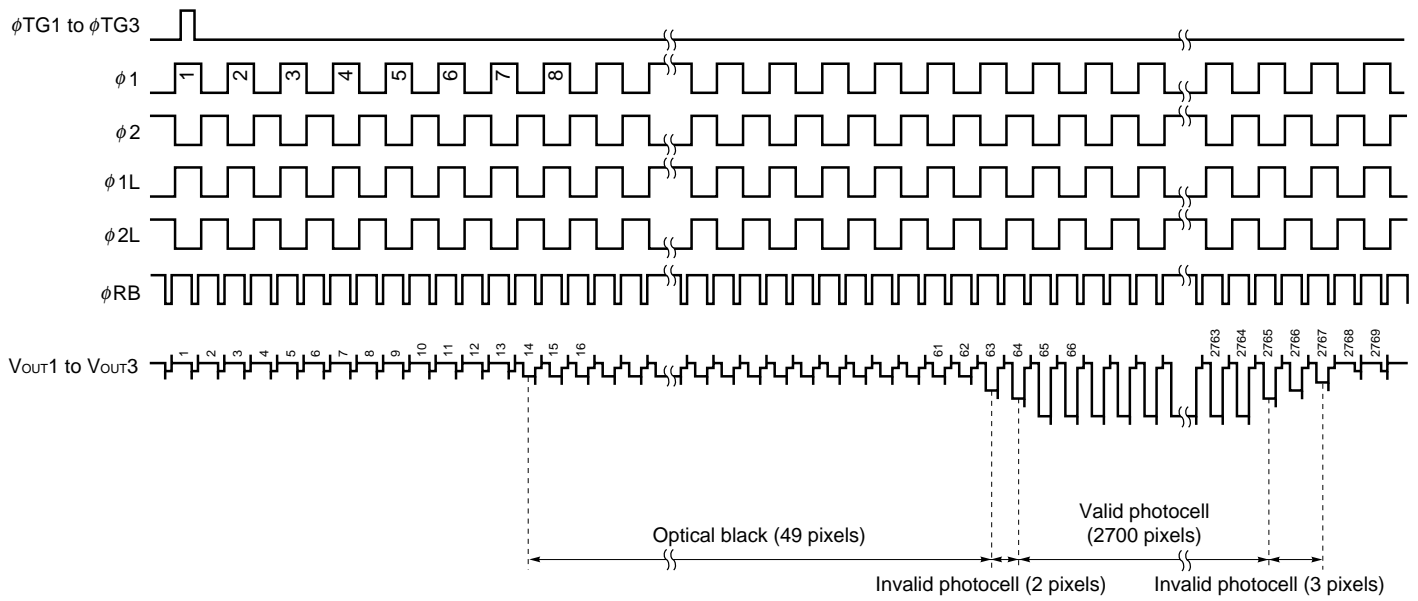
**Notes 1.** Refer to **TIMING CHART2**.

**2.** When each fall delay time of  $\phi 1L$  and  $\phi 2L$  ( $t_2'$ ,  $t_1'$ ) is the TYP. value (refer to **TIMING CHART 2**).

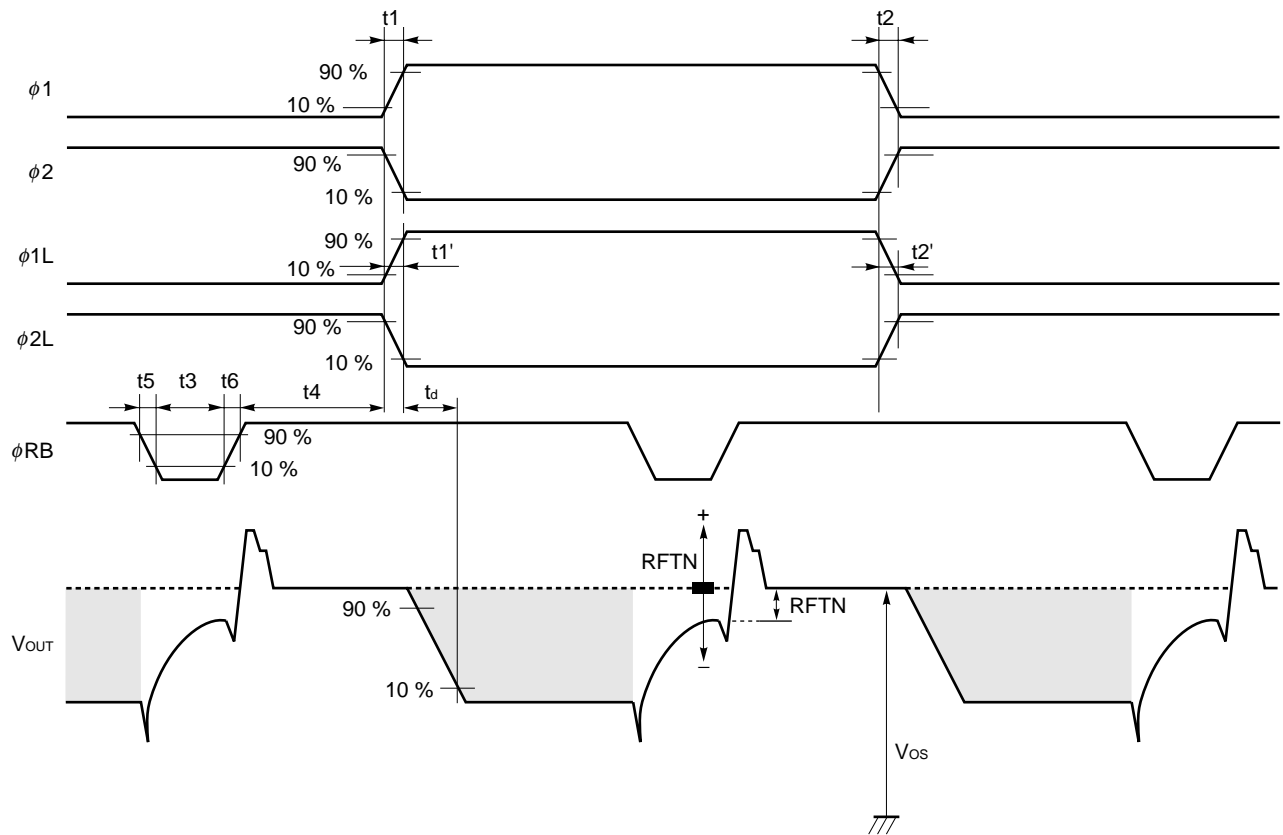
## INPUT PIN CAPACITANCE

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Transfer gate clock pin capacitance	$C_{\phi TG}$	$\phi TG1$	13		200		pF
		$\phi TG2$	12		200		pF
		$\phi TG3$	10		200		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	$\phi RB$	3		50		pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	$\phi 1L$	4		30		pF
		$\phi 2L$	17		30		pF
Shift register clock pin capacitance 1	$C_{\phi 1}$	$\phi 1$	14		700		pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	$\phi 2$	9		700		pF

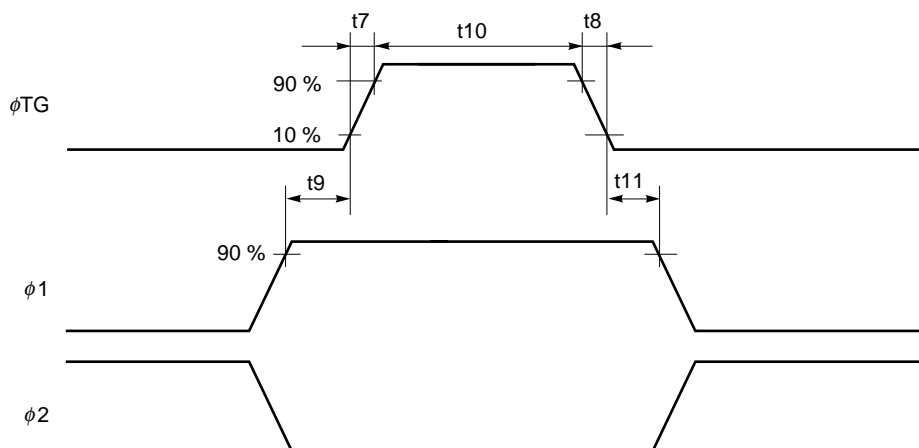
**TIMING CHART 1 (for each color)**



**TIMING CHART 2 (for each color)**

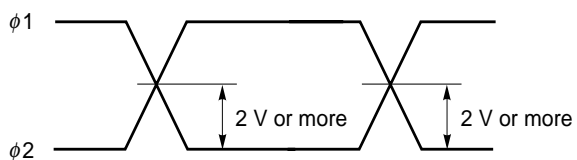


φTG1 to φTG3, φ1, φ2 TIMING CHART

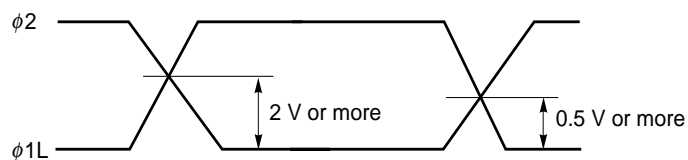


Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t4	130	300	–	ns
t3	20	150	–	ns
t5, t6	0	50	–	ns
t7, t8	0	50	–	ns
t9, t11	900	1000	–	ns
t10	3000	10000	–	ns

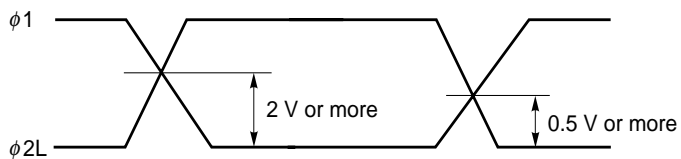
φ1, φ2 cross points



φ1L, φ2 cross points



φ1, φ2L cross points



**Remark** Adjust cross points (φ1, φ2), (φ1L, φ2) and (φ1, φ2L) with input resistance of each pin.



**DEFINITIONS OF CHARACTERISTIC ITEMS**

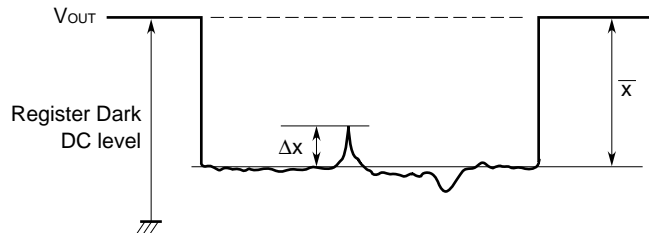
1. Saturation voltage:  $V_{sat}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

$\Delta x$  : maximum of  $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{2700} x_j}{2700}$$

$x_j$  : Output voltage of valid pixel number j



4. Average dark signal: ADS  
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{2700} d_j}{2700}$$

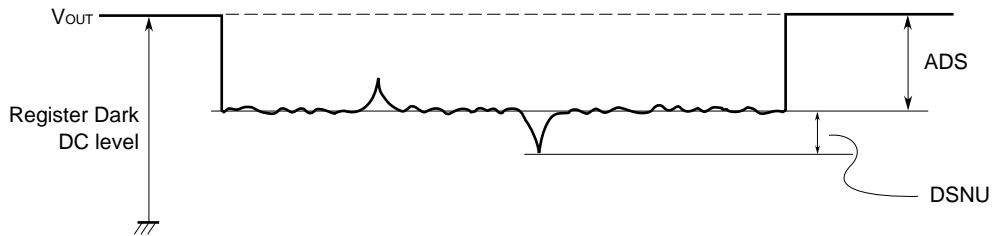
$d_j$  : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV): maximum of } |d_j - \text{ADS}| \text{ } _{j=1 \text{ to } 2700}$$

$d_j$ : Dark signal of valid pixel number  $j$



6. Output impedance:  $Z_o$

Impedance of the output pins viewed from outside.

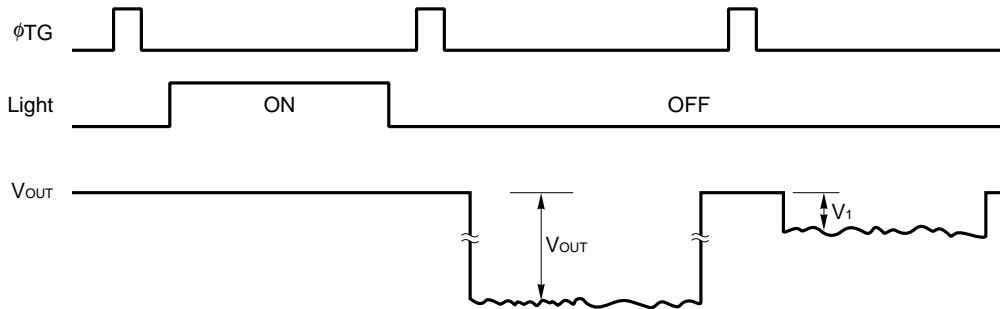
7. Response: R

Output voltage divided by exposure ( $\text{lx}\cdot\text{s}$ ).

Note that the response varies with a light source (spectral characteristic).

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{\text{OUT}}} \times 100$$

9. Register Imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels

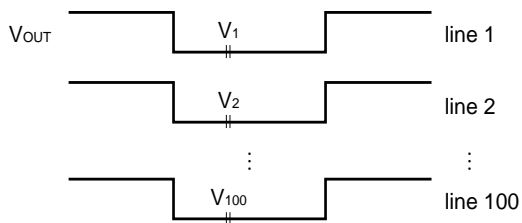
V<sub>j</sub> : Output voltage of each pixel

10. Random noise: σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

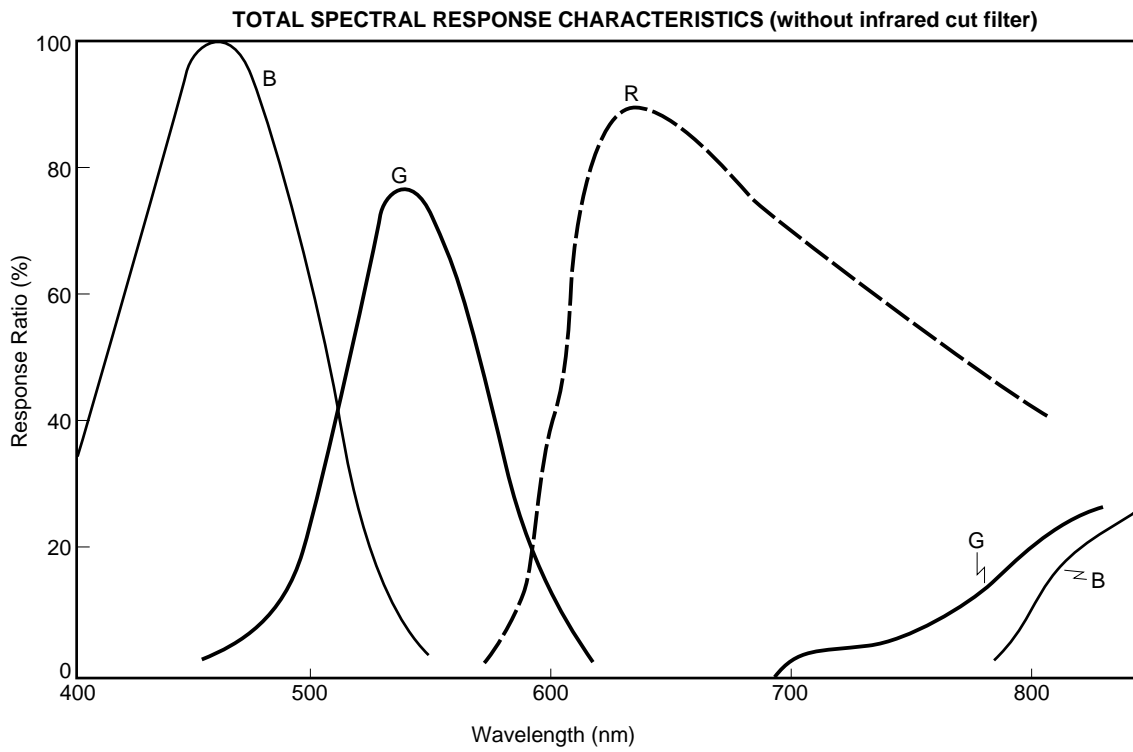
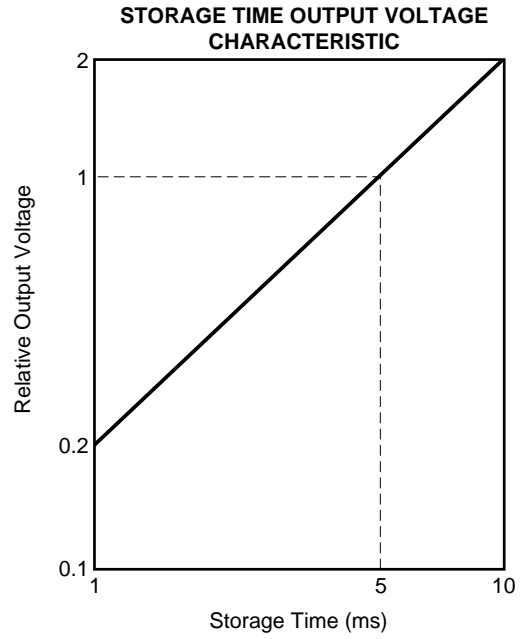
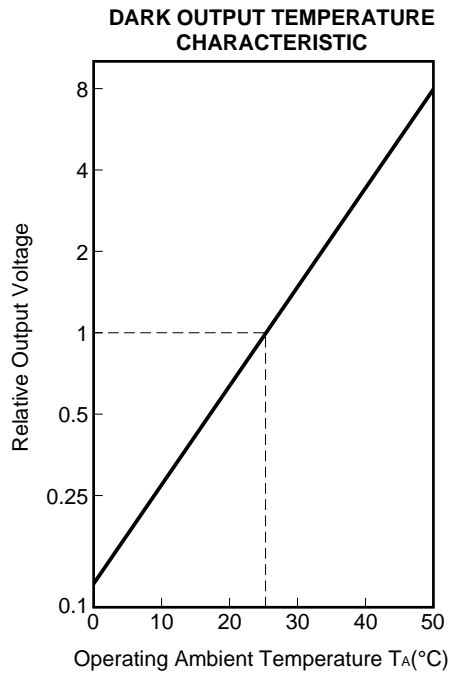
$$\sigma = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V<sub>i</sub> : A valid pixel output signal among all of the valid pixels for each color

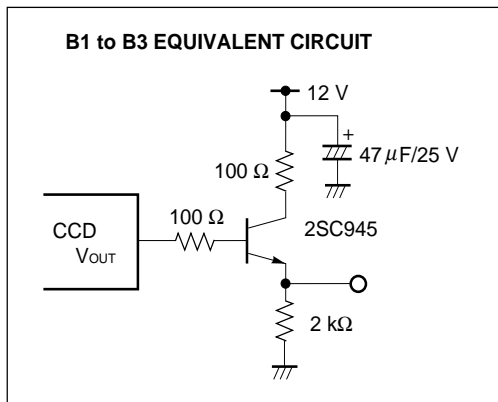
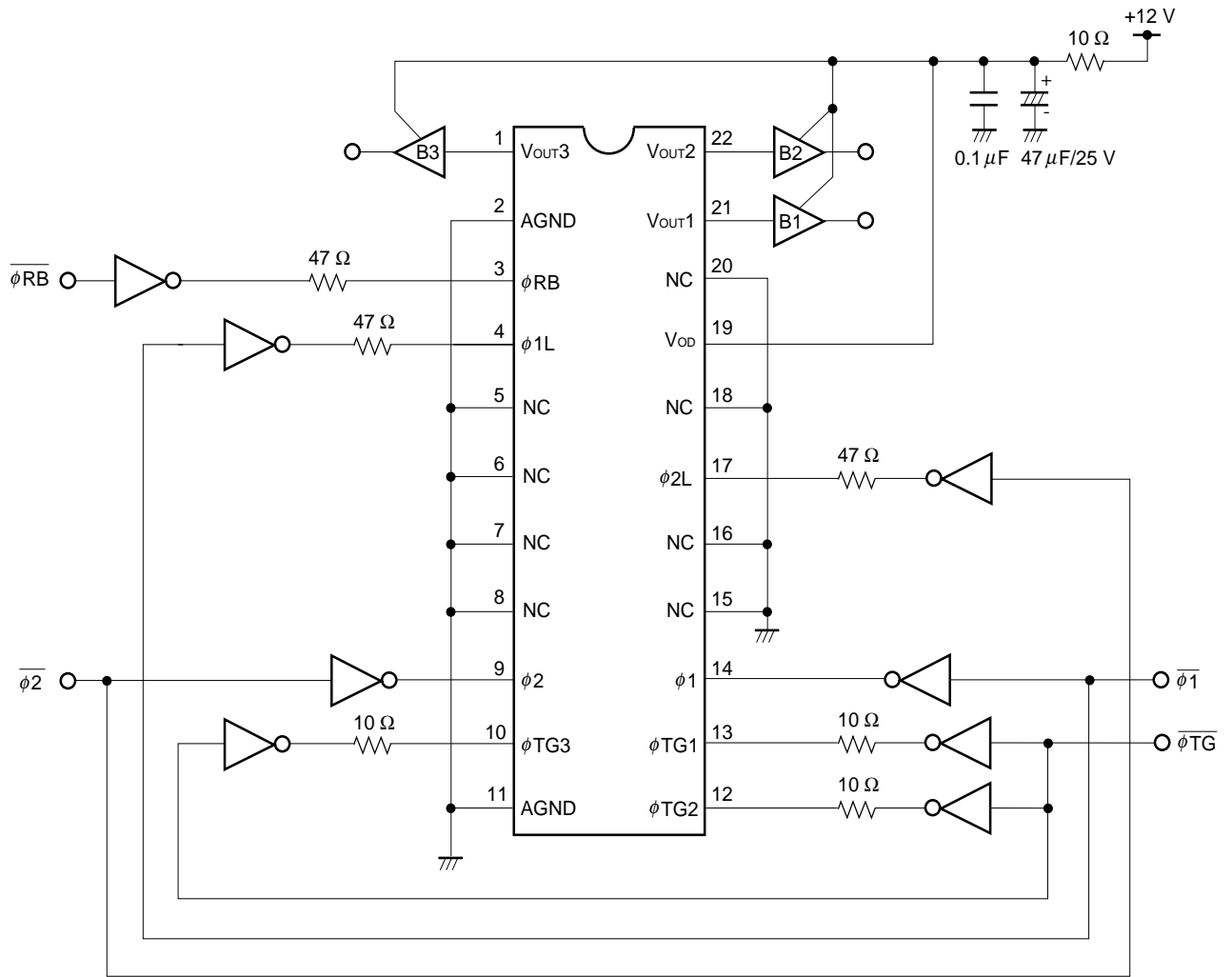


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES ( $T_A = +25\text{ }^\circ\text{C}$ )



APPLICATION CIRCUIT EXAMPLE

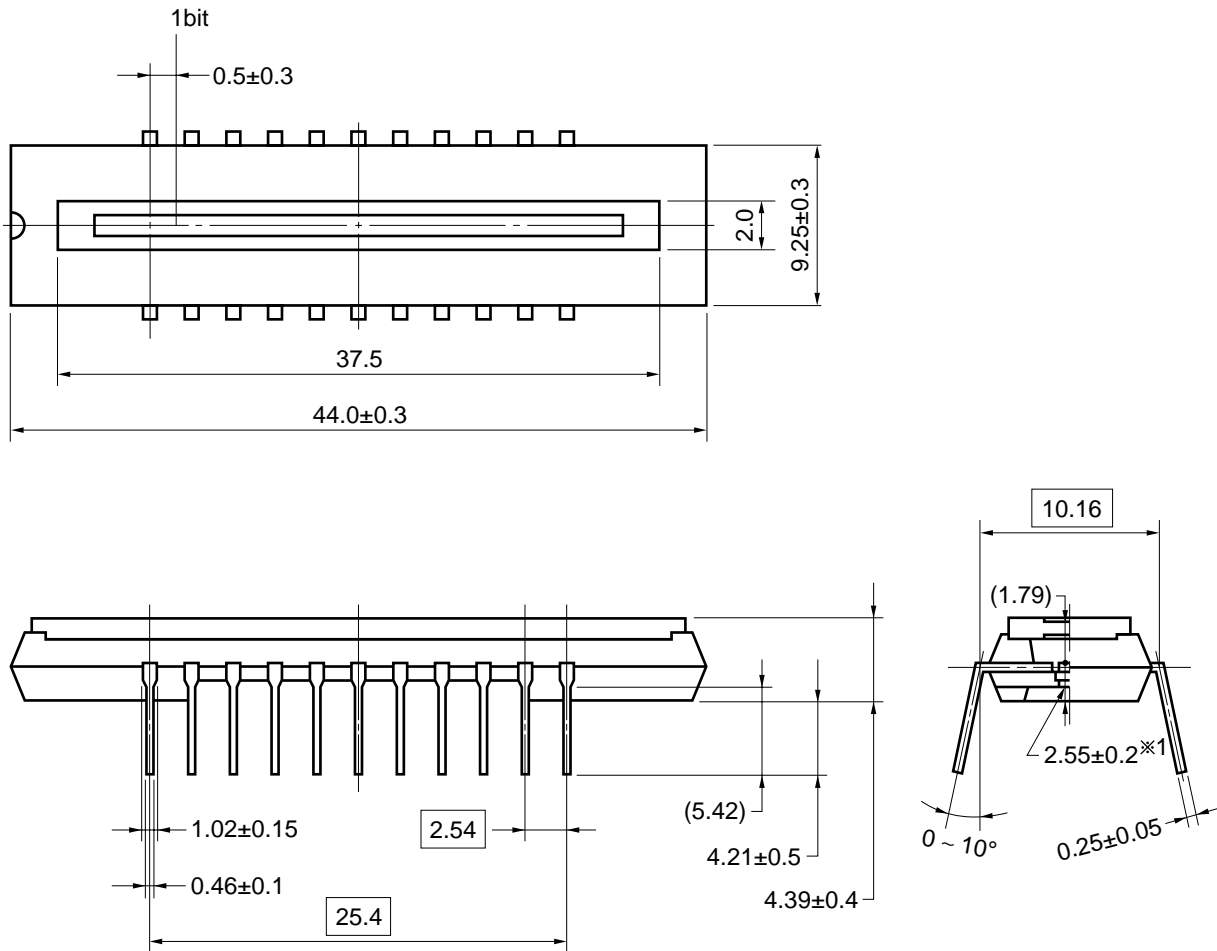


Remark Inverters :  $\mu$ PD74HC04

PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22PIN PLASTIC DIP (400 mil)

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9 × 8.35 × 0.7 <sup>※2</sup>	1.5

※1 The bottom of the package ↔ The surface of the chip

※2 The thickness of the cap over the chip

22C-1CCD-PKG6

**RECOMMENDED SOLDERING CONDITIONS**

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "**Semiconductor Device Mounting Technology Manual**"(C10535E).

**Type of Through-hole Device**

μPD3720ACY: CCD linear image sensor 22-pin plastic DIP (400 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 260 °C or below, Heat time: 10 seconds or less (per each lead).

**Caution** For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body dose not get jet soldered.

During assembly care should be taken to prevent solder or flux from contacting the plastic cap.

The optical characteristics could be degraded by such contact.

**NOTES ON CLEANING THE PLASTIC CAP**

**① CLEANING THE PLASTIC CAP**

Care should be taken when cleaning the surface to prevent scratches. The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

**② RECOMMENDED SOLVENTS**

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP



[MEMO]

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## [MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.