

# SN74CBT6800A 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS005L – MARCH 1993 – REVISED JULY 1999

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

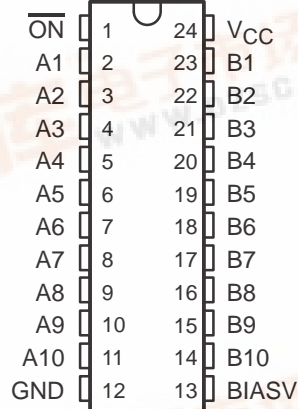
## description

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ( $\overline{ON}$ ) input. When  $\overline{ON}$  is low, the switch is on and port A is connected to port B. When  $\overline{ON}$  is high, the switch between port A and port B is open. When  $\overline{ON}$  is high or  $V_{CC}$  is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

The SN74CBT6800A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

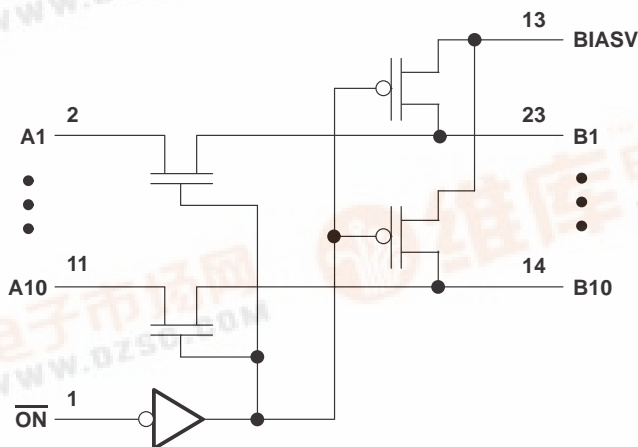
DB, DBQ, DW, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUT $\overline{ON}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

## logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74CBT6800A

## 10-BIT FET BUS SWITCH

### WITH PRECHARGED OUTPUTS

SCDS005L – MARCH 1993 – REVISED JULY 1999

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Bias voltage range, BIASV	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	104°C/W
DBQ package	103°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
BIASV Supply voltage	1.3	$V_{CC}$	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA				−1.2	V
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V or GND				±5	μA
I <sub>O</sub>		V <sub>CC</sub> = 4.5 V, BIASV = 2.4 V, V <sub>O</sub> = 0		0.25			mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND				50	μA
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				2.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0			3.5		pF
C <sub>O</sub> (OFF)		V <sub>O</sub> = 3 V or 0, Switch off			4.5		pF
r <sub>on</sub> ¶		V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V	V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA		11	20	Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA	3	7	
				I <sub>I</sub> = 30 mA	3	7	
			V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA		6	15	

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

<sup>¶</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

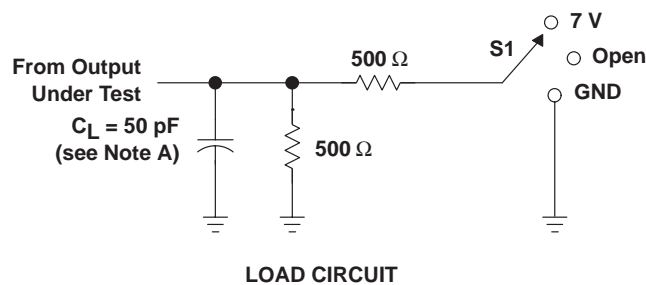
**SN74CBT6800A**  
**10-BIT FET BUS SWITCH**  
**WITH PRECHARGED OUTPUTS**  
 SCDS005L – MARCH 1993 – REVISED JULY 1999

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

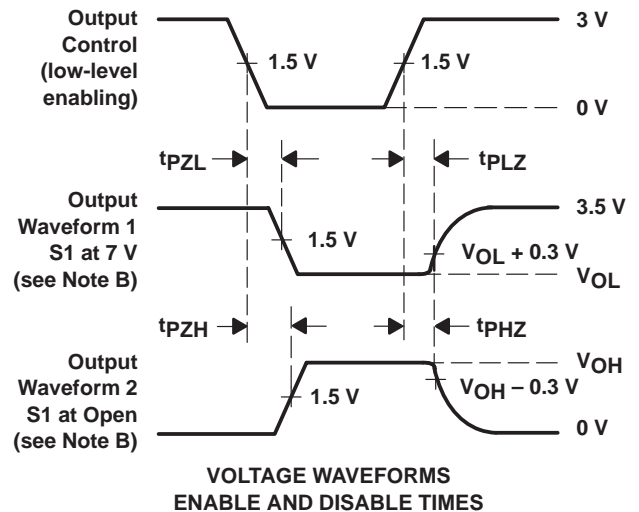
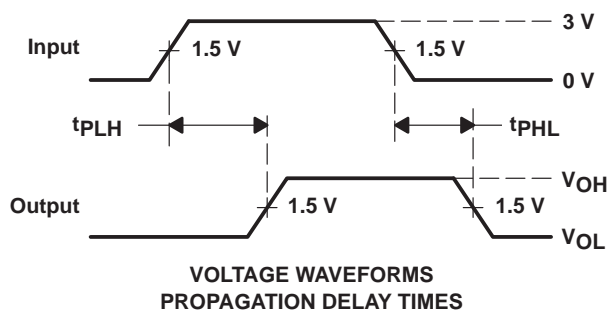
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}^\dagger$		A or B	B or A		0.35		0.25	ns
$t_{PZH}$	BIASV = GND	$\overline{ON}$	A or B		6	2	5.1	ns
$t_{PZL}$	BIASV = 3 V				6	2	5.6	
$t_{PHZ}$	BIASV = GND	$\overline{ON}$	A or B		5.5	1	5	ns
$t_{PLZ}$	BIASV = 3 V				5.5	2	5.9	

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PHZ}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.