19-2392; Rev 0; 4/02

MAXIM

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

General Description

The MAX9160 125MHz, 14-port LVTTL/LVCMOS clock driver repeats the selected LVDS or LVTTL/LVCMOS input on two output banks. Each bank consists of seven LVTTL/LVCMOS series terminated outputs and a bank enable. The LVDS input has a fail-safe function. The MAX9160 has a propagation delay that can be adjusted using an external resistor to set the bias current for an internal delay cell. The LVTTL/LVCMOS outputs feature 200ps maximum output-to-output skew and ±100ps maximum added peak-to-peak jitter.

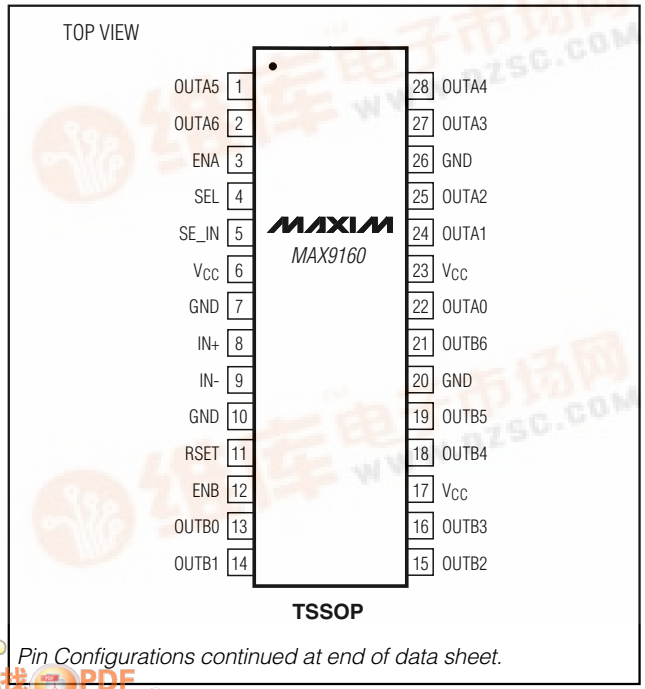
The MAX9160 is designed to operate with a 3.3V supply voltage over the extended temperature range of -40°C to +85°C. This device is available in 28-pin exposed- and nonexposed-pad TSSOP and 32-lead 5mm x 5mm QFN packages.

Applications

Cellular Base Stations	Digital Cross-Connects
Servers	DSLAMs
Add/Drop Multiplexers	Networking Equipment

Typical Application Circuit and Functional Diagram appear at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

Features

- **LVDS or LVTTL/LVCMOS Input Selection**
- **LVDS Input Fail-Safe Sets Outputs High for Open, Undriven Short, or Undriven Parallel Termination**
- **Two Output Banks with Separate Bank Enables**
- **Integrated Output Series Termination for 60Ω Lines**
- **200ps (max) Output-to-Output Skew**
- **±100ps (max) Peak-to-Peak Added Output Jitter**
- **42% to 58% Output Duty Cycle at 125MHz**
- **Guaranteed 125MHz Operating Frequency**
- **LVDS Input Is High Impedance with V_{CC} = 0V or Open (Hot Swappable)**
- **28-Pin Exposed- and Nonexposed-Pad TSSOP or 32-Lead QFN Packages**
- **-40°C to +85°C Operating Temperature**
- **3.0V to 3.6V Supply Voltage**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9160EUI	-40°C to +85°C	28 TSSOP
MAX9160AEUI	-40°C to +85°C	28 TSSOP-EP**
MAX9160EGJ*	-40°C to +85°C	32 QFN-EP

**Future product—contact factory for availability.*
***Exposed pad.*

Function Table

EN_	SEL	SE_IN	V_{ID}	OUT_
H	H	H	X	H
H	H	L or open	X	L
H	L or open	X	≥ +50mV	H
H	L or open	X	≤ -50mV	L
H	L or open	X	Open, undriven short, or undriven parallel termination	H
L or Open	X	X	X	L

V_{ID} = V_{IN+} - V_{IN-}
H = high logic level
L = low logic level
X = don't care

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4V
IN+, IN- to GND.....-0.3V to +4V
SE_IN, EN_, SEL, RSET, OUT_ to GND .....-0.3V to V_{CC} + 0.3V
Output Short-Circuit Duration (OUT_) (Note 1) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1024mW
28-Pin TSSOP-EP (derate 23.8mW/°C above +70°C) ..1904mW
32-Pin QFN (derate 21.2mW/°C above +70°C) 1704mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
ESD Protection
Human Body Model (IN+, IN-) .....±16kV
Human Body Model (SE_IN) .....±8kV
Soldering Temperature (10s).....+300°C

Note 1: Short one output at a time. Do not exceed the absolute maximum junction temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, ENA = ENB = high, RSET = 12kΩ ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (SE_IN, ENA, ENB, SEL)							
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			GND		0.8	V
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA		-1.5	-0.85		V
Input Current	I_{IN}	V_{IN} = high or low		-20		+20	µA
SE_IN Capacitance (Note 4)	C_{IN}	SE_IN to GND				6.1	pF
LVDS INPUT (IN+, IN-)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V		-15		+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V		-20		+20	
Power-Off Input Current	$I_{IN+(off)}$ $I_{IN-(off)}$	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0V or open		-15		+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, V_{CC} = 0V or open		-20		+20	
Input Resistor 1	R_{IN1}	V_{CC} = 3.6V or 0V, Figure 1		51		100	kΩ
Input Resistor 2	R_{IN2}	V_{CC} = 3.6V or 0 V, Figure 1		200		341	kΩ
Input Capacitance (Note 4)	C_{IN}	IN+ or IN- to GND				6.0	pF
OUTPUTS (OUT_)							
Output Short-Circuit Current (Note 1)	I_{OS}	SEL = high, SE_IN = high, V_{OUT} = 0V		-115		-30	mA
		SEL = low, V_{ID} = 100mV, V_{OUT} = 0V					
Output Capacitance (Note 4)	C_O	OUT_ to GND				9	pF
Output High Voltage	V_{OH}	I_{OH} = -100µA		V_{CC} - 0.2			V
		I_{OH} = -4mA		2.4			
		I_{OH} = -8mA		2.1			
Fail-Safe Output High Voltage	V_{OHFS}	SEL = low, inputs open, undriven short, or undriven parallel terminated	I_{OH} = -100µA	V_{CC} - 0.2			V
			I_{OH} = -4mA	2.4			
			I_{OH} = -8mA	2.1			

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, ENA = ENB = high, RSET = 12kΩ ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage	V_{OL}	I_{OL} = 100µA			0.2	V
		I_{OL} = 4mA			0.4	
		I_{OL} = 8mA			0.8	
Supply Current	I_{CC}	SEL = high, SE_IN = high or low, no load			15	µA
		SEL = low, V_{ID} = -100mV or 100mV, no load		7.0	10	mA
Output Series Resistance (Note 5)	R_S	Output switched high, V_{OUT} = 1.65V		72		Ω
		Output switched low, V_{OUT} = 1.65V		61		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, C_L = 20pF, ENA = ENB = high, SEL = high or low, RSET = 12kΩ ±1%, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 6, 7, 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise Time	t_R	Figures 2 and 3		1.4		2.95	ns
Fall Time	t_F			1.4		2.95	ns
Low-to-High Propagation Delay IN+, IN- to OUT_	t_{PLH1}	SEL = low	RSET = 12kΩ	5.3	6.5	8.0	ns
			RSET = open	4.9		9.0	
High-to-Low Propagation Delay IN+, IN- to OUT_	t_{PHL1}	SEL = low	RSET = 12kΩ	5.3	6.4	8.0	ns
			RSET = open	4.9		9.0	
Low-to-High Propagation Delay SE_IN to OUT_	t_{PLH2}	SEL = high		2.2	2.9	3.8	ns
High-to-Low Propagation Delay SE_IN to OUT_	t_{PHL2}	SEL = high		2.2	3.1	3.8	ns
Added Peak-to-Peak Output Jitter	t_J	100mV peak-to-peak supply noise at 200kHz, 3.3V supply				100	ps
Output Duty Cycle	ODC	f_{IN} = 125MHz		42		58	%
		f_{IN} = 35MHz		48.75		51.25	
Output-to-Output Skew (Note 9)	t_{SKOO}					200	ps
Part-to-Part Skew (Note 10)	t_{SKPP1}	SE_IN to OUT_, SEL = high				0.9	ns
		IN+, IN- to OUT_, SEL = low				2.2	
Part-to-Part Skew (Note 11)	t_{SKPP2}	SE_IN to OUT_, SEL = high				1.6	ns
		IN+, IN- to OUT_, SEL = low				2.7	
Maximum Switching Frequency (Note 12)	f_{MAX}			125			MHz

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, and V_{ID}.

Note 3: Parameter limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, C_L = 20pF, ENA = ENB = high, SEL = high or low, RSET = 12kΩ ±1%, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 6, 7, 8)

Note 4: Guaranteed by design and characterization.

Note 5: Total of driver output resistance and integrated series resistor.

Note 6: AC parameters are guaranteed by design and characterization and are not production tested. Limits are set at ±6 sigma.

Note 7: C_L includes scope probe and test jig capacitance.

Note 8: Pulse generator conditions for SE_IN input: frequency = 125MHz, 50% duty cycle, Z_O = 50Ω, t_R = 1.2ns, and t_F = 1.2ns (20% to 80%), V_{OH} = V_{CC}, V_{OL} = 0V. Pulse generator conditions for IN+, IN- input: frequency = 125MHz, 50% duty cycle, Z_O = 50Ω, t_R = 1ns, and t_F = 1ns (20% to 80%). V_{ID}, V_{CM} as specified in *AC Electrical Characteristics* general conditions.

Note 9: Measured between outputs with identical loads at $V_{CC}/2$ for a same-edge transition.

Note 10: t_{SKPP1} is the greatest difference in propagation delay between different parts operating under identical conditions within rated conditions.

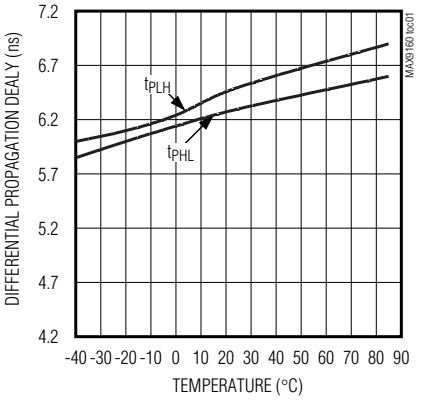
Note 11: t_{SKPP2} is the greatest difference in propagation delay between different parts operating within rated conditions.

Note 12: All AC specifications met at f_{MAX}.

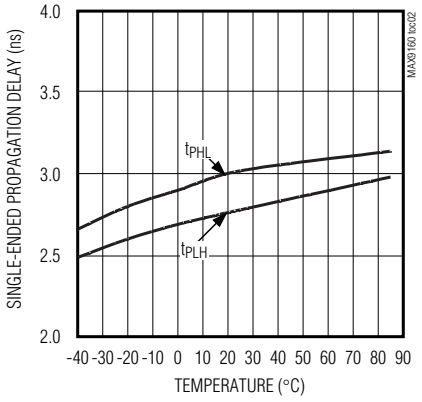
Typical Operating Characteristics

(MAX9160 with RSET = 12kΩ ±1%, V_{CC} = 3.3V, C_L = 20pF, ENA = ENB = high, $|V_{ID}|$ = 0.2, V_{CM} = 1.2V, f_{IN} = 125MHz, T_A = +25°C, unless otherwise noted.)

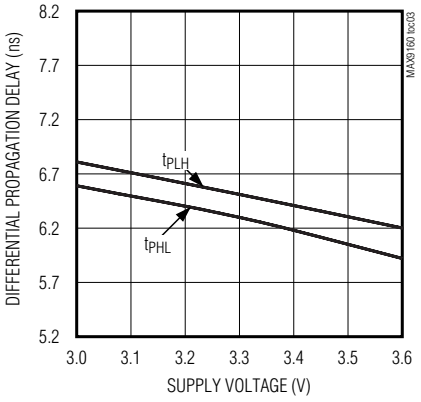
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



SINGLE-ENDED PROPAGATION DELAY vs. TEMPERATURE



DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE

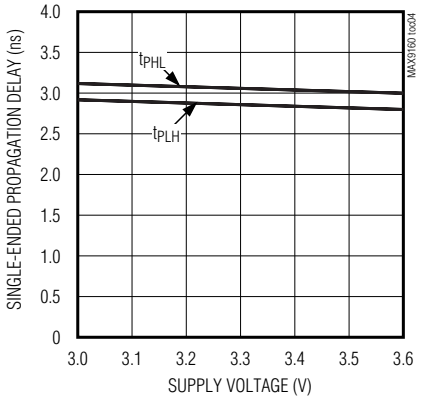


LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

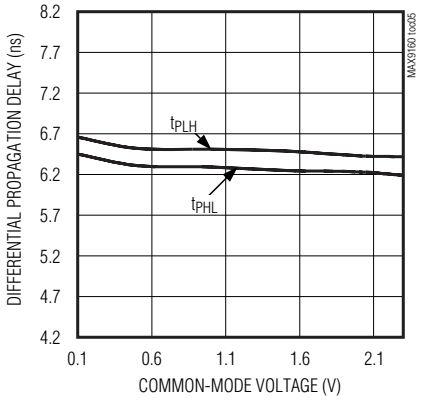
Typical Operating Characteristics (continued)

(MAX9160 with RSET = 12kΩ ±1%, V_{CC} = 3.3V, C_L = 20pF, ENA = ENB = high, $|V_{ID}|$ = 0.2, V_{CM} = 1.2V, f_{IN} = 125MHz, T_A = +25°C, unless otherwise noted.)

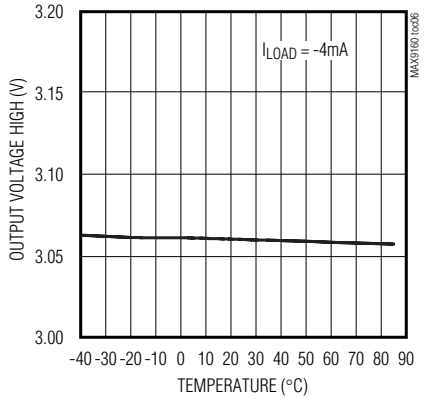
SINGLE-ENDED PROPAGATION DELAY vs. SUPPLY VOLTAGE



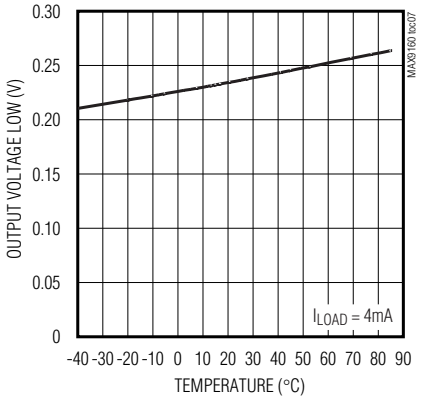
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



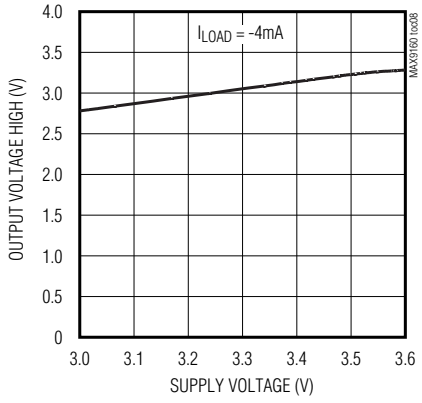
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



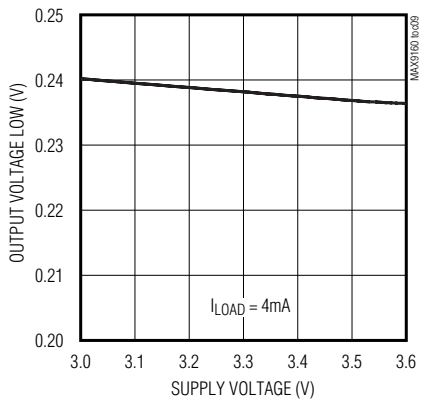
OUTPUT VOLTAGE LOW vs. TEMPERATURE



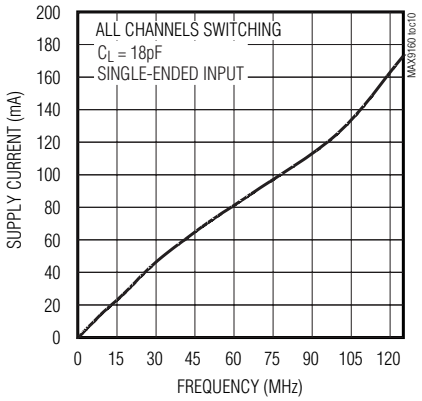
OUTPUT VOLTAGE HIGH vs. SUPPLY VOLTAGE



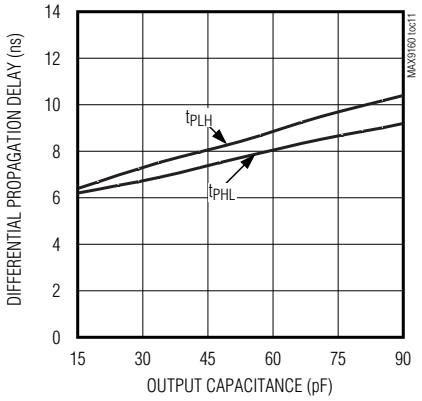
OUTPUT VOLTAGE LOW vs. SUPPLY VOLTAGE



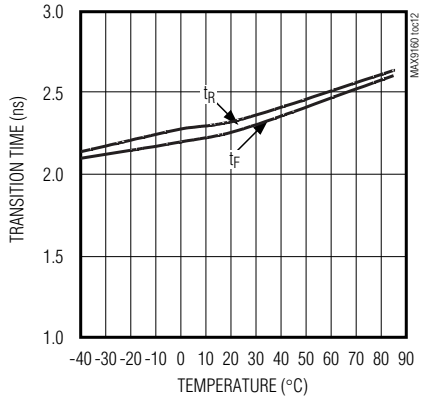
SUPPLY CURRENT vs. FREQUENCY



DIFFERENTIAL PROPAGATION DELAY vs. OUTPUT CAPACITANCE



TRANSITION TIME vs. TEMPERATURE

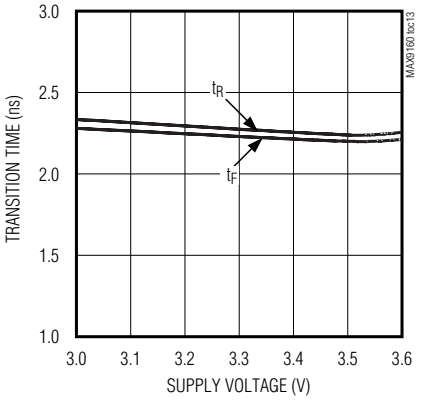


LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

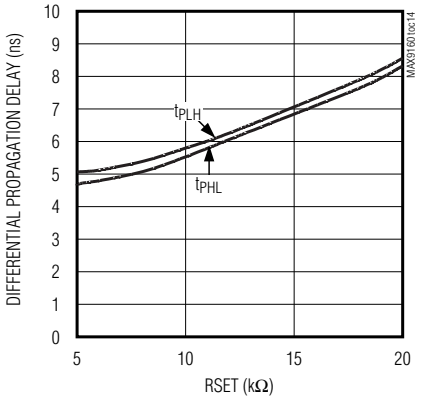
Typical Operating Characteristics (continued)

(MAX9160 with RSET = 12kΩ ±1%, V_{CC} = 3.3V, C_L = 20pF, ENA = ENB = high, $|V_{ID}|$ = 0.2, V_{CM} = 1.2V, f_{IN} = 125MHz, T_A = +25°C, unless otherwise noted.)

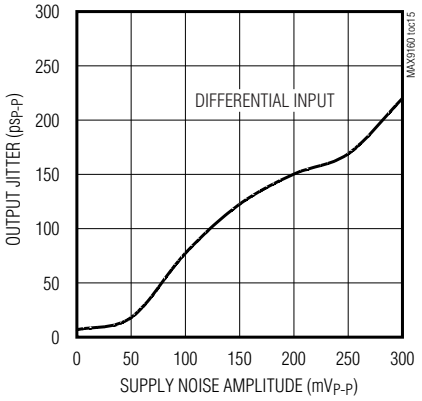
TRANSITION TIME vs. SUPPLY VOLTAGE



DIFFERENTIAL PROPAGATION DELAY vs. RSET



OUTPUT JITTER vs. 200kHz SUPPLY NOISE AMPLITUDE



Pin Description

PIN		NAME	FUNCTION
QFN	TSSOP		
1	4	SEL	LVCMOS/LVTTL Level Logic Input. SEL = high selects SE_IN. SEL = low or open selects IN+, IN-. SEL is pulled to GND by an internal resistor.
2	5	SE_IN	LVCMOS/LVTTL Level Input. SE_IN is pulled to GND by an internal resistor.
3, 12, 16, 22, 29	6, 17, 23	V_{CC}	Positive Supply Voltage. Bypass with 0.1µF and 0.001µF capacitors to ground.
4, 7, 13, 19, 25, 28	7, 10, 20, 26	GND	Ground
5	8	IN+	Noninverting Input of Differential Input
6	9	IN-	Inverting Input of Differential Input
8	11	RSET	Connect a 12kΩ ±1% resistor to ground to decrease the minimum to maximum IN+, IN- to OUT_ propagation delay.
9	12	ENB	LVCMOS/LVTTL Level Logic Input. When ENB = high, outputs OUTB_ are enabled and follow the selected input. When ENB = low or open, outputs OUTB_ are driven low. ENB is pulled to GND by an internal resistor.
10, 11, 14, 15, 17, 18, 20	13–16, 18, 19, 21	OUTB_	Bank B LVCMOS/LVTTL Outputs

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Pin Description (continued)

PIN		NAME	FUNCTION
QFN	TSSOP		
21, 23, 24, 26, 27, 30, 31	1, 2, 22, 24, 25, 27, 28	OUTA_	Bank A LVCMOS/LVTTL Outputs
32	3	ENA	LVCMOS/LVTTL Level Logic Input. When ENA = high, outputs OUTA_ are enabled and follow the selected input. When ENA = low or open, outputs OUTA_ are driven low. ENA is pulled to GND by an internal resistor.
EP*		Exposed Pad	Solder to PC board

**MAX9160EGJ and MAX9160AEUI.*

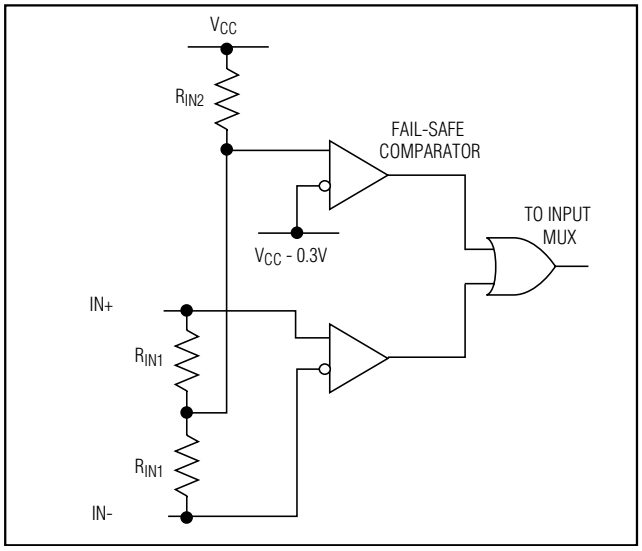


Figure 1. Fail-Safe Input Circuit

Detailed Description

The MAX9160 125MHz, 14-port LVTTL/LVCMOS clock driver repeats the selected LVDS or LVTTL/LVCMOS input on two output banks. Each bank consists of seven LVTTL/LVCMOS series terminated outputs and a bank enable. The LVDS input has a fail-safe function. The MAX9160 has a propagation delay that can be adjusted using an external resistor to set the bias current for an internal delay cell. The LVTTL/LVCMOS outputs feature 200ps maximum output-to-output skew and ±100ps maximum added peak-to-peak jitter.

The MAX9160 is designed to operate with a 3.3V supply voltage over the extended temperature range of -40°C to +85°C. This device is available in 28-pin exposed and nonexposed pad TSSOP and 32-lead 5mm x 5mm QFN packages.

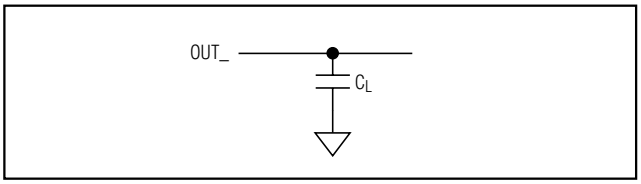


Figure 2. Output Load

Fail-Safe

A fail-safe circuit on the MAX9160 sets enabled outputs high when the LVDS input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the LVDS input is selected and undriven, noise may cause the enabled outputs to switch. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when a driver output is in high impedance. A shorted input can occur because of a cable failure.

When the MAX9160 LVDS input is driven with a differential signal with a common-mode voltage between $|V_{ID}/2|$ and 2.4V - $|V_{ID}/2|$, the fail-safe circuit is not activated. If the input is open, undriven and shorted, or undriven and parallel terminated, an internal resistor in the fail-safe circuit pulls both of the LVDS inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high (Figure 1).

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

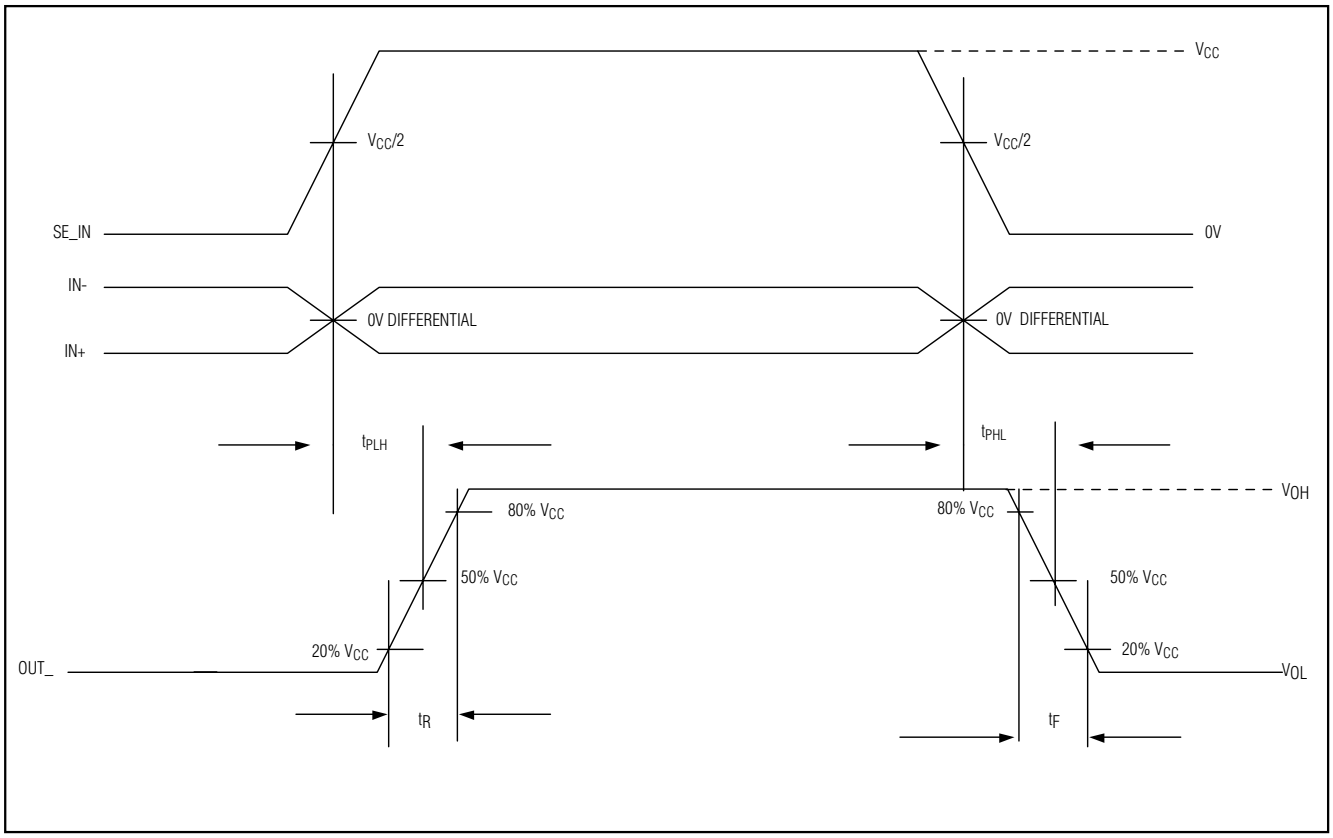


Figure 3. Transition Time and Propagation Delay Timing Diagram

Propagation Delay and RSET

The MAX9160 delay can be adjusted by connecting a resistor from RSET to ground. See *Typical Operating Characteristics* for a graph of delay vs. RSET.

Output Enables

Each bank of seven LVTTL/LVCMOS drivers is controlled by an output enable. Outputs follow the selected input when EN_ is high. Outputs are low (not high impedance) when EN_ = low.

Power Dissipation and Package Type

Power dissipation at high switching frequencies may exceed the power dissipation capacity of the standard TSSOP package (see the Supply Current vs. Frequency graph in the *Typical Operating Characteristics*). An EP version of the TSSOP package is available that dissipates higher power. Also, a space-saving QFN package with EP is available. The EP must be soldered to the PC board.

Supply Bypassing

Bypass each supply pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the device.

Board Layout

A four-layer PC board that provides separate power, ground, input, and output signals is recommended. Keep input and output signals separated to prevent coupling.

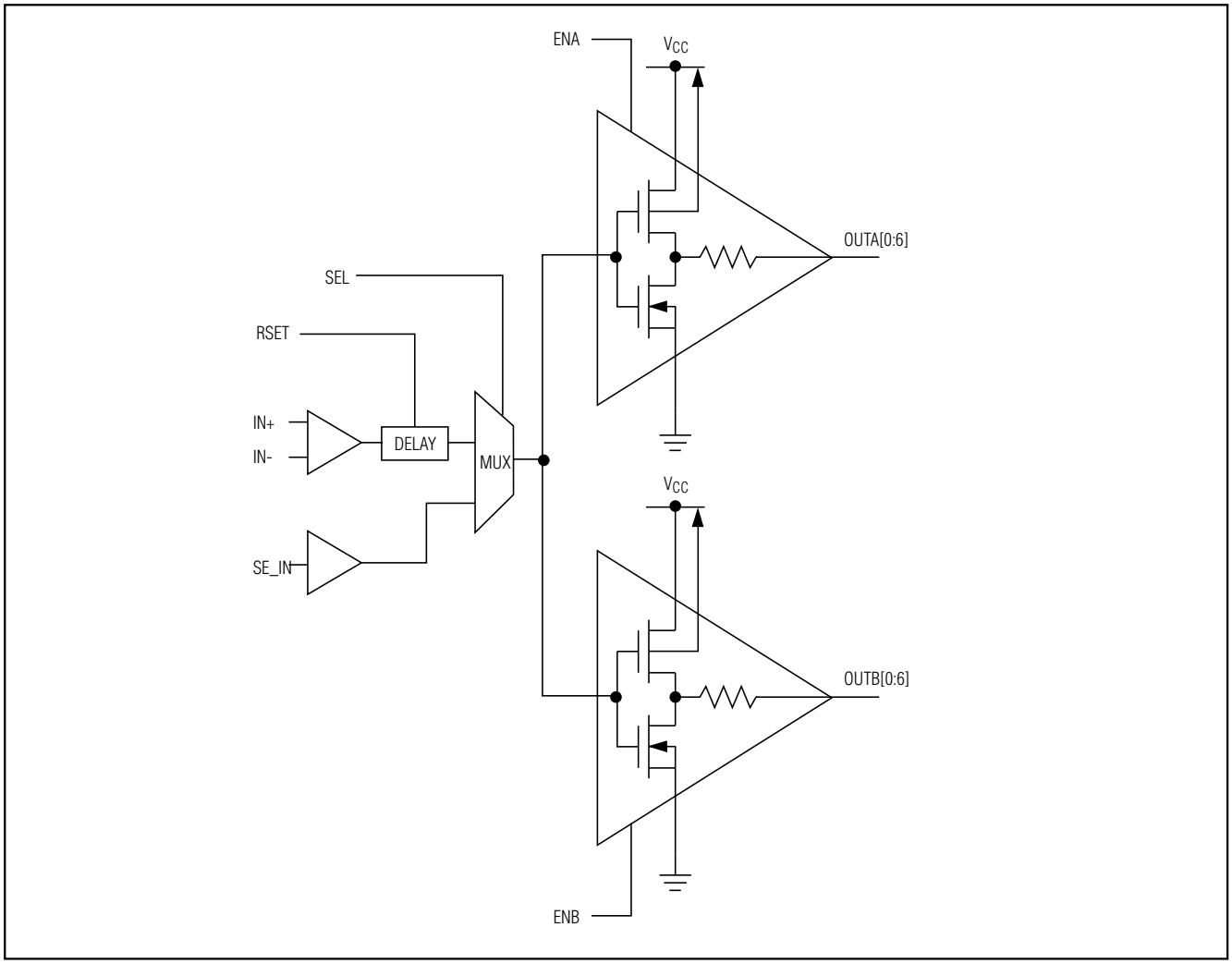
Chip Information

TRANSISTOR COUNT: 756

PROCESS: CMOS

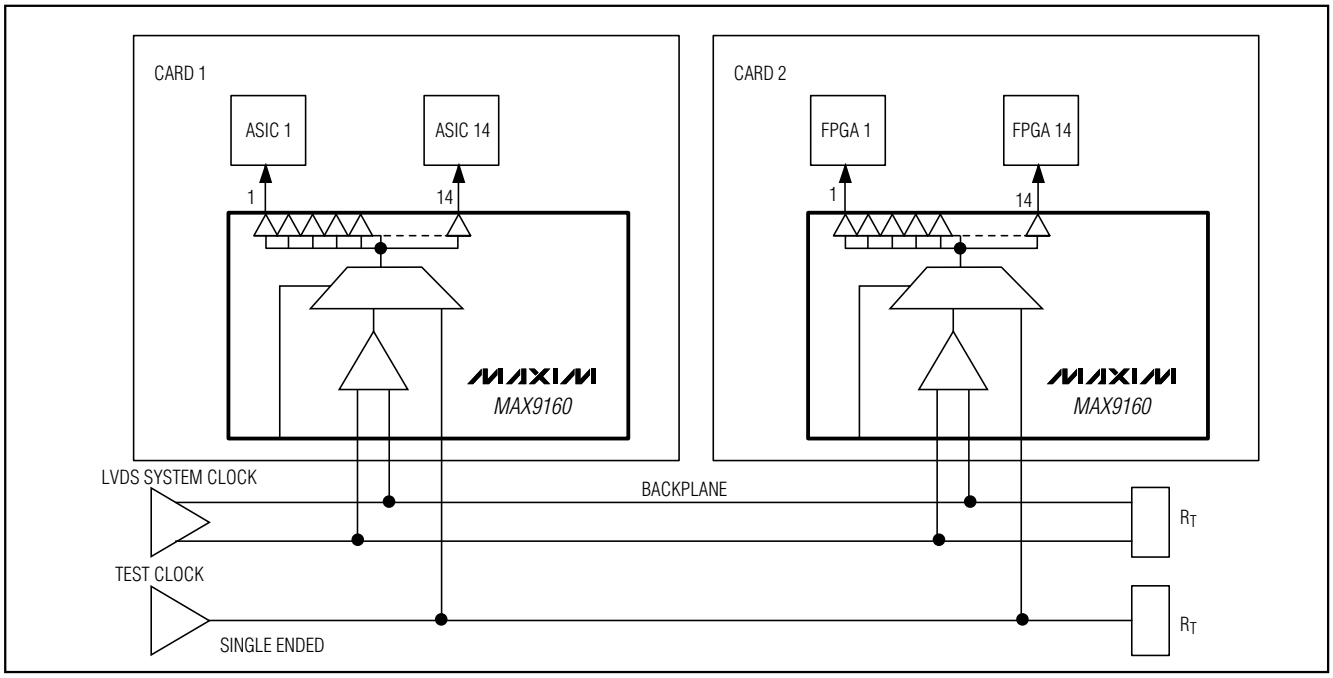
LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Functional Diagram

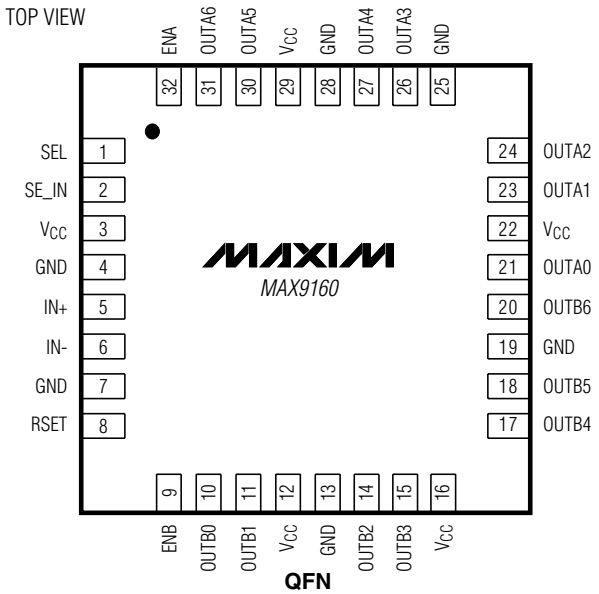


LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Typical Application Circuit



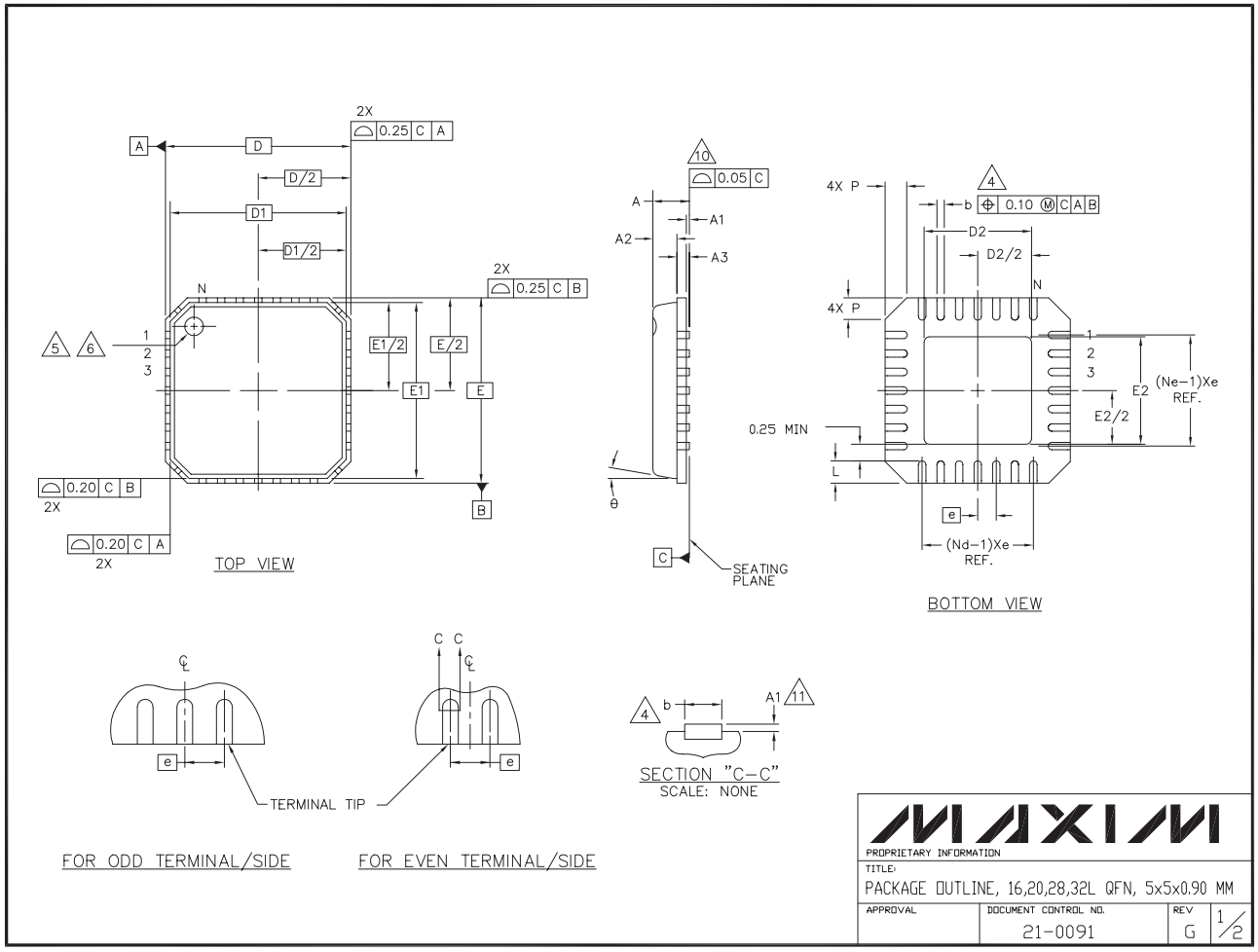
Pin Configurations (continued)



LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

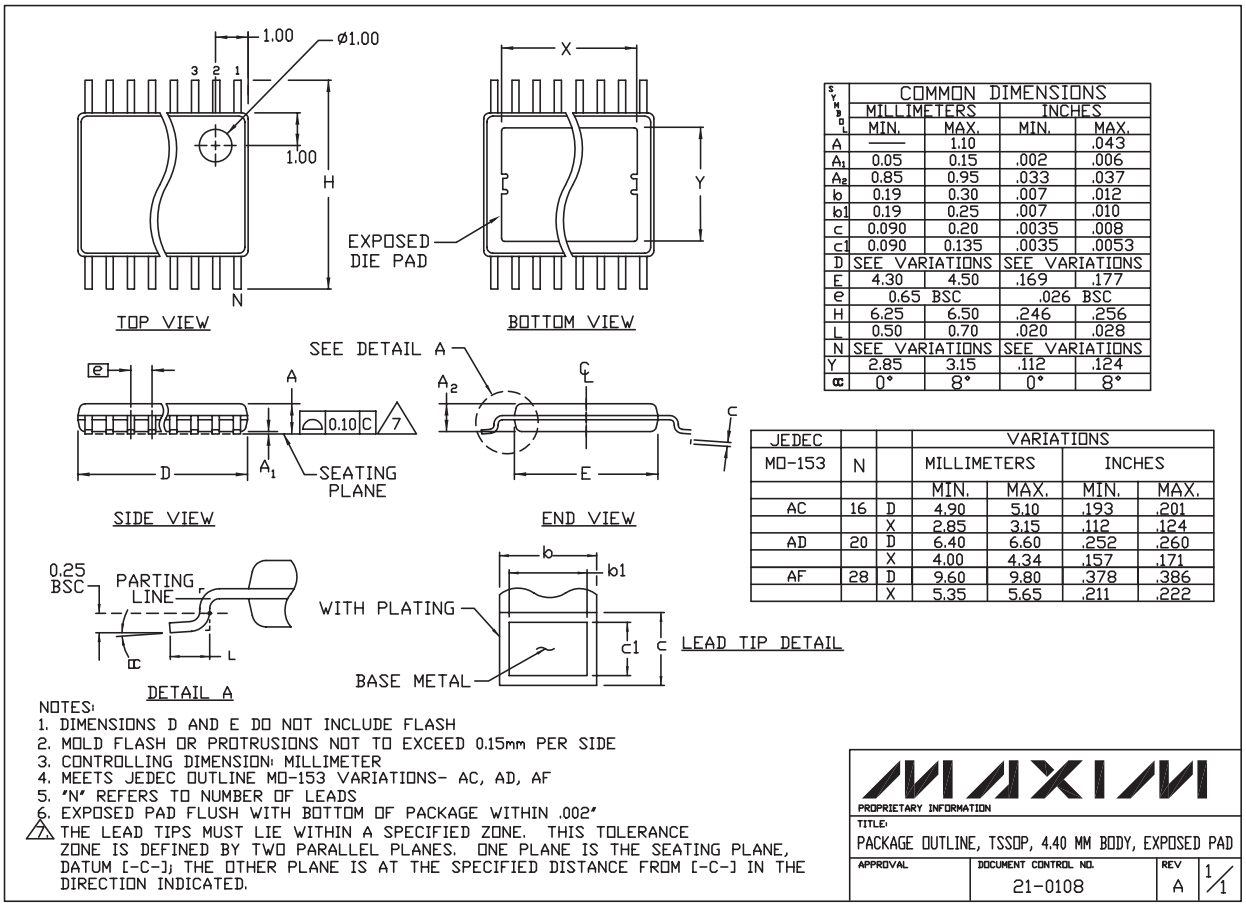
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2

LVDS or LVTTL/LVCMOS Input to 14 LVTTL/LVCMOS Output Clock Driver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP, 4.0.EXP PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AC	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AF	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS- AC, AD, AF
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	A	1/1