LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES

SCES628A – APRIL 2005 – REVISED APRIL 2005

- **Member of the Texas Instruments Widebus+™ Family**
- **Designed to Optimize Power Savings in Portable Applications**
- **1.65-V to 5.5-V Level Translation Using Dual Supplies**
- **Matched Pinout With CompactFlash™ (CF) Connector Pin Configurations to Optimize PCB Layout**
- **Input-Disable Feature Allows Floating Input Conditions**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD**
  - **15-kV Human-Body Model**
  - **±4-kV IEC61000-4-2, Contact Discharge (Latch-Up Immune)**

description/ordering information

This CompactFlash™ (CF) interface chip is designed to provide a single-chip solution for CF card interfaces. Separate V_{CC} rails for the system bus side and the CF connector bus side allow voltage-level shifting. This is helpful for interfacing between a core chipset, which may operate from 3.3 V down to 1.65 V, and CF cards, which operate from 3.3-V or 5-V supply voltages. All the input buffers feature the input-disable function, which allows conditional floating input signals. The input, output, and I/O buffers on the CF connector side have been defined to comply with CF+ and CompactFlash specification revisions 1.4 and 2.0.

This device has 16-bit data lines and 24-bit address/command lines. $\overline{CD1}$ and $\overline{CD2}$ have internal pullup resistors to pull them to a high logic state if there is no card in the CF slot. The presence of a CF card in the CF card slot generates a low logic signal at $\overline{SCD}$. A separate power-supply pin, V_{CC_SD}, controls the $\overline{SCD}$ output buffer. The $\overline{SCD}$ signal can be used to control a voltage regulator, which may power the CF slot and the CF side of this device. V_{CC_SD} is particularly helpful when the core processor operates at a low V_{CC}, but the regulator needs a higher control signal voltage.

The $\overline{MASTER\_EN}$ signal controls all the buffers and transceivers except $\overline{CD1}$ and $\overline{CD2}$. If $\overline{MASTER\_EN}$ is high, the SN74LV4320A is in a power-down mode. The $\overline{BUF\_EN}$ signal, in conjunction with $\overline{MASTER\_EN}$, controls the 11-bit address lines and 13-bit control/command lines.

The 16-bit data lines use two separate enable signals. $\overline{ENL}$, in conjunction with $\overline{MASTER\_EN}$, controls the lower 8-bit data lines (D07–D00). $\overline{ENH}$, in conjunction with $\overline{MASTER\_EN}$, controls the upper 8-bit data lines (D15–D08). A DIR($\overline{S}$/CF) input controls the data direction between the system bus and the CF card. An additional DIR_OUT pin generates the DIR($\overline{S}$/CF) signal using the $\overline{SOE}$ and $\overline{SIORD}$ signals. With either $\overline{SOE}$ or $\overline{SIORD}$ being low, the data direction is from the CF card side to the system side (DIR_OUT = L). DIR($\overline{S}$/CF) and DIR_OUT are placed adjacent to each other, which is convenient for connecting DIR($\overline{S}$/CF) and DIR_OUT, if DIR_OUT is used. This saves an additional signal from the system controller to control the data direction.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKF	Tape and reel	SN74LV4320AGKFR	LM320A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

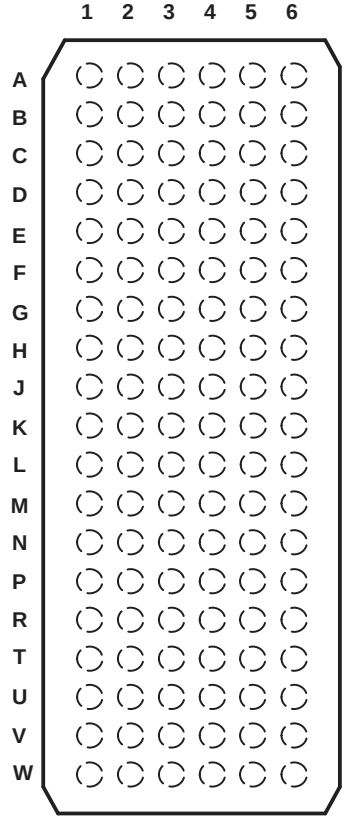
description/ordering information (continued)

BVD1, BVD2, $\overline{\text{INPACK}}$, READY, $\overline{\text{WAIT}}$, and WP have 100-kΩ internal pullup resistors, eliminating the need for external pullups. The resistors are within the tolerance of CF+ and CompactFlash specification revisions 1.4 and 2.0.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

board-optimized pin configuration

GKF PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	D12	D04	D03	SD14	SD12	SD11
B	D13	D05	D11	SD13	SD10	SD09
C	D14	D06	SD15	$\overline{\text{SINPACK}}$	SD08	SD07
D	D15	D07	V_{CC_CF}	V_{CC_S}	SD06	SD05
E	$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	GND	GND	SD04	SD03
F	$\overline{\text{OE}}$	A10	V_{CC_CF}	V_{CC_S}	SD02	SD01
G	A09	$\overline{\text{IORD}}$	GND	GND	SD00	$\overline{\text{SCE1}}$
H	A08	$\overline{\text{IOWR}}$	V_{CC_CF}	V_{CC_S}	$\overline{\text{EN\_L}}$	$\overline{\text{EN\_H}}$
J	A07	$\overline{\text{WE}}$	GND	GND	$\overline{\text{MASTER\_EN}}$	$\overline{\text{BUF\_EN}}$
K	A06	READY	A05	$\overline{\text{SCE2}}$	$\overline{\text{SOE}}$	$\overline{\text{SIORD}}$
L	A04	RESET	GND	GND	$\overline{\text{SWE}}$	$\overline{\text{SIOWR}}$
M	A03	$\overline{\text{WAIT}}$	V_{CC_CF}	V_{CC_S}	SREADY	SRESET
N	A02	$\overline{\text{INPACK}}$	GND	GND	$\overline{\text{SWAIT}}$	$\overline{\text{SREG}}$
P	A01	$\overline{\text{REG}}$	V_{CC_CF}	GND	SBVD2	SBVD1
R	A00	BVD2	V_{CC_CF}	V_{CC_S}	SA10	SWP
T	D00	BVD1	V_{CC_SD}	DIR($\overline{\text{S}}$/CF)	SA08	SA09
U	D01	D08	$\overline{\text{CD1}}$	DIR_OUT	SA06	SA07
V	D02	D09	$\overline{\text{CD2}}$	SA00	SA04	SA05
W	WP	D10	$\overline{\text{SCD}}$	SA01	SA02	SA03

FUNCTION TABLES

Lower 8-Bit Data Bus Transceivers (D07–D00, SD07–SD00)

INPUTS			OPERATION
$\overline{\text{MASTER\_EN}}$	$\overline{\text{ENL}}$	DIR ($\overline{\text{S}}$/CF)	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D07–D00 and SD07–SD00 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

Upper 8-Bit Data Bus Transceivers (D15–D08, SD15–SD08)

INPUTS			OPERATION
$\overline{\text{MASTER\_EN}}$	$\overline{\text{ENH}}$	DIR ($\overline{\text{S}}$/CF)	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D15–D08 and SD15–SD08 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

Address Bus Buffers

INPUTS			OUTPUT
$\overline{\text{MASTER\_EN}}$	$\overline{\text{BUF\_EN}}$	SA	A
L	L	H	H
L	L	L	L
L	H	X	Z. SA inputs can float.
H	X	X	Z, low power mode

X = H or L

Command Line Buffers
($\overline{\text{BVD1}}$, $\overline{\text{BVD2}}$, $\overline{\text{INPACK}}$, $\overline{\text{OE}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{READY}}$, $\overline{\text{REG}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{WAIT}}$, $\overline{\text{WE}}$, WP,)

INPUTS			OUTPUT
$\overline{\text{MASTER\_EN}}$	$\overline{\text{BUF\_EN}}$	INPUT	
L	L	H	H
L	L	L	L
L	H	X	Z. Command line buffer inputs can float.
H	X	X	Z, low power mode

X = H or L

Reset

INPUTS		OUTPUT
$\overline{\text{MASTER\_EN}}$	SRESET	RESET
L	H	H
L	L	L
H	X	Z, low power mode

X = H or L

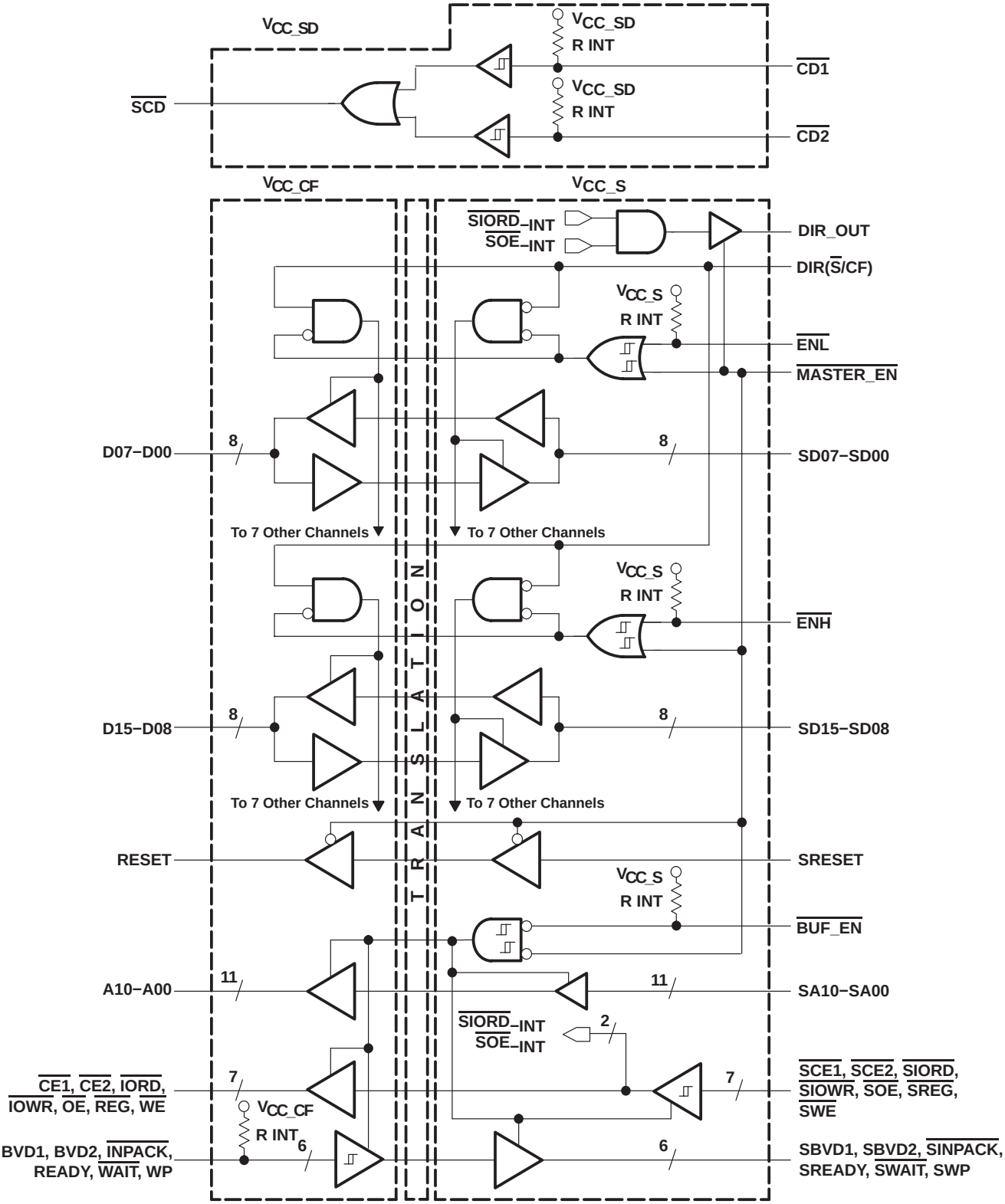
FUNCTION TABLES (Continued)

DIR_OUT

INPUTS				OUTPUT DIR_OUT
$\overline{\text{BUF\_EN}}$	$\overline{\text{MASTER\_EN}}$	$\overline{\text{SOE}}$	$\overline{\text{SIORD}}$	
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	H
H	L	X	X	L
X	H	X	X	Z, low power mode

X = H or L

logic diagram



NOTE: R INT ≥ 100 kΩ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC_S}	−0.5 V to 4.6 V
V_{CC_CF}, V_{CC_SD}	−0.5 V to 6.5 V
Input voltage range, V_I: I/O ports (SD, SA) (see Note 1)	−0.5 V to 4.6 V
I/O ports (D, A)	−0.5 V to 6.5 V
Input ports ($\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, $\overline{SREG}$, $\overline{SWE}$)	−0.5 V to 4.6 V
Input ports (BVD1, BVD2, $\overline{READY}$, $\overline{INPACK}$, $\overline{WAIT}$, WP)	−0.5 V to 6.5 V
Control ports (DIR($\overline{S}$/CF), $\overline{MASTER\_EN}$, $\overline{ENL}$, $\overline{ENH}$)	−0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): System port	−0.5 V to 4.6 V
CF port	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): System port	−0.5 V to V_{CC_S} + 0.5 V
CF port	−0.5 V to V_{CC_CF} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC_S}, V_{CC_CF}, V_{CC_SD}, or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	36°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output-current ratings are observed.
2. This value is limited to 6.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 6)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CC_SD}	Card-detect supply voltage				1.65	5.5	V
V_{CC_S}	System-side supply voltage				1.65	V_{CC_CF}	V
V_{CC_CF}	CF-side supply voltage				3	5.5	V
V_{IH}	High-level input voltage	Card-detect inputs ($\overline{CD1}$, $\overline{CD2}$,)	1.65 V to 5.5 V		$V_{CC\_SD} \times 0.65$		V
V_{IL}	Low-level input voltage	Card-detect inputs ($\overline{CD1}$, $\overline{CD2}$,)	1.65 V to 5.5 V			$V_{CC\_SD} \times 0.35$	V
V_{IH}	High-level input voltage	System port (SD, SA, SRESET)	1.65 V to 1.95 V		$V_{CC\_S} \times 0.65$		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	System port (SD, SA, SRESET)	1.65 V to 1.95 V			$V_{CC\_S} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	Control inputs ($\overline{DIR}$, $\overline{MASTER\_EN}$, $\overline{ENL}$, $\overline{ENH}$, $\overline{BUF\_EN}$)	1.65 V to 1.95 V		$V_{CC\_S} \times 0.65$		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Control inputs ($\overline{DIR}$, $\overline{MASTER\_EN}$, $\overline{ENL}$, $\overline{ENH}$, $\overline{BUF\_EN}$)	1.65 V to 1.95 V			$V_{CC\_S} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	CF port (D, A)	3 V to 3.6 V		2		V
			4.5 V to 5.5 V		$V_{CC\_CF} \times 0.7$		
V_{IL}	Low-level input voltage	CF port (D, A)	3 V to 3.6 V			0.8	V
			4.5 V to 5.5 V			$V_{CC\_CF} \times 0.3$	
V_O	Output voltage	Card-detect output voltage			0	V_{CC_SD}	V
		System-side output voltage			0	V_{CC_S}	
		CF-side output voltage			0	V_{CC_CF}	
I_{OH}	High-level output current	Card detect		1.65 V to 1.95 V		−2	mA
				1.95 V to 2.7 V		−4	
				2.7 V to 3.6 V		−8	
				4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current	Card detect		1.65 V to 1.95 V		2	mA
				1.95 V to 2.7 V		4	
				2.7 V to 3.6 V		8	
				4.5 V to 5.5 V		12	

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Notes 4 through 6) (continued)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
I_{OH}	High-level output current	System port		1.65 V to 1.95 V		2	mA
				1.95 V to 2.7 V		6	
				2.7 V to 3.6 V		12	
I_{OL}	Low-level output current	System port		1.65 V to 1.95 V		2	mA
				1.95 V to 2.7 V		6	
				2.7 V to 3.6 V		12	
I_{OH}	High-level output current	CF port		3 V to 3.6 V		12	mA
				4.5 V to 5.5 V		16	
I_{OL}	Low-level output current	CF port		3 V to 3.6 V		12	mA
				4.5 V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		1.65 V to 2.7 V			>20	ns/V
			2.7 V to 3.6 V			>20	
			4.5 V to 5.5 V			>20	
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (CF card-detect logic) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC_SD}	T_A = 25°C			−40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.65 V to 5.5 V	V_{CC_SD}−0.1			V_{CC_SD}−0.2		V
		I_{OH} = −2 mA		1.65 V	1.2			1.2		
		I_{OH} = −4 mA		2.3 V	2			2		
		I_{OH} = −6 mA		2.7 V	2.3			2.3		
		I_{OH} = −8 mA		3 V	2.4			2.4		
		I_{OH} = −12 mA		4.5 V	3.8			3.8		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.65 V to 5.5 V			0.1		0.2	V
		I_{OL} = 2 mA		1.65 V			0.2		0.2	
		I_{OL} = 4 mA		2.3 V			0.2		0.2	
		I_{OL} = 6 mA		2.7 V			0.3		0.3	
		I_{OL} = 8 mA		3 V			0.4		0.4	
		I_{OL} = 12 mA		4.5 V			0.5		0.5	
I_I		$V_I = V_{CC\_SD}$		1.65 V to 5.5 V			±0.5		±1	µA
		V_I = 0 V					−55		−60	
I_{off}		V_I or V_O = 0 to 5.5 V		0 V			55		60	µA
R_{INT}		$\overline{CD1}$ = GND, $\overline{CD2}$ = GND		1.65 V to 5.5 V		150	300	100	300	kΩ
I_{CC_SD}		$\overline{CD1}$ and $\overline{CD2}$ = V_{CC_SD}	I_{O_SD} = 0	5.5 V			0.5		1	µA
		$\overline{CD1}$ or $\overline{CD2}$ = GND, $\overline{CD2}$ or $\overline{CD1}$ = V_{CC_SD}					10		10	
C_i	$\overline{CD1}$ or $\overline{CD2}$	$V_I = V_{CC\_SD}$ or GND		5.5 V		9				pF

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{T+}	$\overline{SOE}$, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SWE}$, $\overline{SREG}$			1.65 V	3 V to 5.5 V		0.95		0.6	1.4	V
				2.3 V			1.32		0.9	1.8	
				2.7 V			1.49		1	2	
				3 V			1.67		1.2	2.2	
V_{T-}	$\overline{SOE}$, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SWE}$, $\overline{SREG}$			1.65 V	3 V to 5.5 V		0.66		0.19	0.8	V
				2.3 V			0.87		0.39	1.15	
				2.7 V			0.98		0.49	1.32	
				3 V			1.08		0.59	1.5	
ΔV_T	$\overline{SOE}$, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SWE}$, $\overline{SREG}$			1.65 V	3 V to 5.5 V		0.31		0.1	0.7	V
				2.3 V			0.46		0.25	0.7	
				2.7 V			0.52		0.3	0.9	
				3 V			0.61		0.4	0.9	
V_{T+}	BVD1, BVD2, $\overline{READY}$, $\overline{INPACT}$, $\overline{WAIT}$			1.65 V to 3.6 V	3 V		1.67		1.3	2.2	V
					4.5 V		2.44		1.9	3.1	
V_{T-}	BVD1, BVD2, $\overline{READY}$, INPACK, $\overline{WAIT}$, WP			1.65 V to 3.6 V	3 V		1.11		0.6	1.5	V
					4.5 V		1.43		1	2	
ΔV_T	BVD1, BVD2, $\overline{READY}$, $\overline{INPACT}$, $\overline{WAIT}$			1.65 V to 3.6 V	3 V		0.58		0.35	1	V
					4.5 V		1.02		0.6	1.5	
V_{T+}	$\overline{BUF\_EN}$, $\overline{ENH}$, ENL, MASTER_EN			1.65 V	3 V to 5.5 V		1		0.6	1.4	V
				2.3 V			1.37		1.1	1.8	
				2.7 V			1.54		1.1	2	
				3 V			1.72		1.3	2.2	
V_{T-}	$\overline{BUF\_EN}$, $\overline{ENH}$, ENL, MASTER_EN			1.65 V	3 V to 5.5 V		0.34		0.15	1	V
				2.3 V			0.63		0.15	1.2	
				2.7 V			0.75		0.2	1.32	
				3 V			0.88		0.4	1.5	
ΔV_T	$\overline{BUF\_EN}$, $\overline{ENH}$, ENL, MASTER_EN			1.65 V	3 V to 5.5 V		0.67		0.08	1.1	V
				2.3 V			0.76		0.2	1.2	
				2.7 V			0.8		0.26	1.3	
				3 V			0.86		0.3	1.4	
V_{OH_S}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.65 V to 3.6 V	3 V to 5.5 V	V_{CC_S} −0.1 V			V_{CC_S} −0.2 V		V
		I_{OH} = −2 mA		1.65 V		1.2			1.2		
		I_{OH} = −4 mA		2.3 V		2			2		
		I_{OH} = −6 mA		2.7 V		2.3			2.3		
		I_{OH} = −12 mA		3 V		2.4			2.4		
V_{OL_S}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.65 V to 3.6 V	3 V to 5.5 V			0.1		0.2	V
		I_{OL} = 2 mA		1.65 V				0.2		0.2	
		I_{OL} = 4 mA		2.3 V				0.2		0.2	
		I_{OL} = 6 mA		2.7 V				0.3		0.3	
		I_{OL} = 12 mA		3 V				0.5		0.5	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)(see Notes 4 and 5) (continued)

PARAMETER		TEST CONDITIONS		V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH_CF}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.65 V to 3.6 V	3 V to 5.5 V	V_{CC_CF} −0.1 V			V_{CC_CF} −0.2 V		V
		I_{OH} = 12 mA			3 V	2.4			2.4		
		I_{OH} = 16 mA			5.5 V	3.8			3.8		
V_{OL_CF}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.65 V to 3.6 V	3 V to 5.5 V			0.1		0.2	V
		I_{OL} = 12 mA			3 V			0.5		0.5	
		I_{OL} = 16 mA			5.5 V			0.5		0.5	
I_I	Inputs without pullup resistor	V_I = GND to V_{CCI} (see Note 7)		1.65 V to 3.6 V	3.6 V to 5.5 V			±0.5		±1	µA
	Inputs with pullup resistor	$V_I = V_{CCI}$ (see Note 7)			3 V to 5.5 V			±0.5		±1	
		V_I = 0 V						55		60	
I_{off}	S port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V			±0.5		±1	µA
	CF port			0 to 3.6 V	0 V			±0.5		±1	
I_{OZ}†	S or CF output ports	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{MASTER\_EN}$ = V_{IH}	3.6 V	5.5 V			±0.5		±1	µA
	CF outputs		$\overline{MASTER\_EN}$ = don't care		0 V			±0.5		±1	
I_{CC_S}	Inputs SD15-SD00, SA10-SA00, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, SREG, SWE)	$V_I = V_{CC\_S}$ or GND	I_O = 0, $\overline{ENL}$ = V_{CC_S}, $\overline{ENH}$ = V_{CC_S}, $\overline{BUF\_EN}$ = V_{CC_S}, DIR($\overline{S}$/CF) = V_{CC_S}	1.65 V to 3.6 V	3.6 V to 5.5 V			1.5		3	µA
	Control inputs ($\overline{ENL}$, $\overline{ENH}$, $\overline{BUF\_EN}$)	$\overline{ENL}$ = $\overline{ENH}$ = $\overline{BUF\_EN}$ = V_{CC_S}	I_O = 0, DIR($\overline{S}$/CF) = V_{CC_S}, All other inputs = V_{CC_S} or GND					1.5		3	
		One of $\overline{ENL}$, $\overline{ENH}$, $\overline{BUF\_EN}$ = GND, Others = V_{CC_S}						36		36	

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
7. $V_{CCI} = V_{CC\_S}$ for DIR($\overline{S}$/CF), $\overline{ENL}$, $\overline{ENH}$, SD15–SD00, SA10–SA00, $\overline{MASTER\_EN}$, SRESET, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, SREG, SWE, $\overline{BUF\_EN}$
$V_{CCI} = V_{CC\_CF}$ for D15–D00, BVD1, BVD2, $\overline{INPACK}$, READY, $\overline{WAIT}$, WP

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
I_{CC_CF}	Input (D15–D00)	$V_I = V_{CC\_CF}$ or GND	I_O = 0, DIR(S/CF) = GND, BVD1, BVD2, INPACK, READY, WAIT, WP = V_{CC_CF}	1.65 V to 3.6 V	3 V to 5.5 V			1.5		3	µA
	Inputs (BVD1, BVD2, INPACK, READY, WAIT, WP)	BVD1 = BVD2 = INPACK = READY WAIT = WP = V_{CC_CF}	I_O = 0, DIR(S/CF) = GND, D15–D00 = V_{CC_CF} or GND	1.65 V to 3.6 V	3 V to 5.5 V			1.5		3	
		One of BVD1, DVD2, INPACK, READY, WAIT, WP = GND. All others= V_{CC_CF}	I_O = 0, DIR(S/CF) = GND, D15–D00 = V_{CC_CF} or GND	1.65 V to 3.6 V	3 V to 5.5 V			60		60	
R_{INT}				1.65 V to 3.6 V	3 V to 5.5 V		150	300		300	kΩ
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3				pF
	SAxx, SOE, SCE1, SCE2, SIORD, SIOWR, SREG, SWE						3				
	Axx, BVD1, BVD2, READY, INPACK, WAIT, WP						9				
C_{io}	S I/O ports	V_O = 3.3 V or GND		3.3 V	3.3 V		7				pF
	CF I/O ports						12				

switching characteristics over recommended operating free-air temperature range ($\overline{CD1}$, $\overline{CD2}$) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_SD}	T_A = 25°C			−40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	$\overline{CD1}$ or $\overline{CD2}$	$\overline{SCD}$		1.8 V ± 0.15 V	3.1	7.1	13.5	1.8	15.5	ns
				2.5 V ± 0.2 V	2.7	4.6	7.1	1.6	9.1	
				2.7 V	2.4	4	5.7	1.6	9.1	
				3.3 V ± 0.3 V	2	3.4	5.1	1.2	6.8	
				5 V ± 0.5 V	1.7	2.6	3.6	1	5.5	

switching characteristics over recommended operating free-air temperature range (BVD1, BVD2, $\overline{INPACK}$, READY, $\overline{WAIT}$, WP) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	CF input	S output	$\overline{MASTER\_EN}$ = $\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	3.1	6	10.2	2.4	12.9	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	2.9	5.6	9.6	2.2	13.9	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	2.7	4.6	6.5	1.9	10	
				2.5 V ± 0.2 V	5 V ± 0.5 V	2.5	4.2	5.8	1.7	8.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	2.5	4	5.6	1.6	8.8	
				3.3 V ± 0.3 V	5 V ± 0.5 V	2.3	3.6	4.9	1.5	7	
t_{en}	$\overline{MASTER\_EN}$	S output	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	11.1	18.9	30.7	9.2	35.5	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	11.1	19.3	30.9	8	35.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	9.9	12.9	17.4	6.9	22.6	
				2.5 V ± 0.2 V	5 V ± 0.5 V	9.9	13.1	17.4	7	22.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	9.5	11.2	13.4	6.3	18.3	
				3.3 V ± 0.3 V	5 V ± 0.5 V	9.5	11.3	13.5	6.3	18.2	
t_{dis}	$\overline{MASTER\_EN}$	S output	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	6.8	13.7	23.9	6	25.1	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	6.1	13.4	22	5.4	23.3	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	4.9	8.6	13.3	4	14.5	
				2.5 V ± 0.2 V	5 V ± 0.5 V	4.6	8.5	13.6	3.9	14.5	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	5	8.1	12.2	4.2	13.2	
				3.3 V ± 0.3 V	5 V ± 0.5 V	4.5	8	12.2	3.6	18.2	
t_{en}	$\overline{BUF\_EN}$	S output	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.7	17.7	33.2	7.6	35.5	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	10.7	18.3	29.3	8.7	35.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	9.6	12.4	16.6	6.6	22.6	
				2.5 V ± 0.2 V	5 V ± 0.5 V	9.6	12.6	16.7	6.6	22.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	9.2	10.9	13	6.1	18.3	
				3.3 V ± 0.3 V	5 V ± 0.5 V	9.2	10.9	13	6.1	18.2	
t_{dis}	$\overline{BUF\_EN}$	S output	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	6.9	12.9	22.3	5.9	24.2	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	5.4	12.4	20.5	4.8	22.8	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	4.4	8	12.7	3.6	14.5	
				2.5 V ± 0.2 V	5 V ± 0.5 V	4.2	7.9	12.8	3.6	14.2	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	4.6	7.7	11.7	3.8	12.3	
				3.3 V ± 0.3 V	5 V ± 0.5 V	4.1	7.6	11.7	3.3	12.4	

switching characteristics over recommended operating free-air temperature range (data bus I/Os) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	SD	$\overline{MASTER\_EN}$ = $\overline{ENL}$ = $\overline{ENH}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	4.2	7.2	11.8	3	13.7	ns
					5 V ± 0.5 V	3.7	6.4	10.7	2.7	13.9	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	3.8	5.7	8	2.4	10	
					5 V ± 0.5 V	3.3	4.9	6.8	2.1	12.4	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	3.5	5.1	6.9	2.2	8.8	
					5 V ± 0.5 V	3	4.3	5.7	1.8	7	
	SD	D		1.8 V ± 0.15 V	3.3 V ± 0.3 V	3.4	5.7	9.8	2.6	11.1	
					5 V ± 0.5 V	3.1	5.4	9.6	2.4	9.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	2.8	4.3	6.2	1.9	8.2	
					5 V ± 0.5 V	2.6	3.8	5.4	1.7	7	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	2.5	3.7	5.2	1.5	7.2	
					5 V ± 0.5 V	2.2	3.3	4.5	1.4	6	
t_{en}	$\overline{MASTER\_EN}$	D	$\overline{ENL}$ = $\overline{ENH}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	13.7	18.2	24.4	9.4	27.9	ns
					5.5 V ± 0.5 V	13.7	17.9	29.9	8	31	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	12.3	15.1	18.8	7.9	23	
					5.5 V ± 0.5 V	12.3	14.8	17.6	8	21.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	11.6	14	17.1	7.3	21.4	
					5.5 V ± 0.5 V	11.6	13.7	15.9	7.4	20.3	
		SD		1.8 V ± 0.15 V	3.3 V ± 0.3 V	11.6	19.6	31.8	9.4	36.3	
					5.5 V ± 0.5 V	11.7	20.1	32	9.5	36.2	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	10.3	13.4	18	7.2	22.6	
					5.5 V ± 0.5 V	10.3	13.6	18.1	7.1	22.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	9.8	11.6	14	6.4	18.3	
					5.5 V ± 0.5 V	9.8	11.7	14	6.4	18.2	
t_{dis}	$\overline{MASTER\_EN}$	D	$\overline{ENL}$ = $\overline{ENH}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.6	12.8	18.1	7.3	20.2	ns
					5.5 V ± 0.5 V	7.6	11.5	16.4	6.3	17.8	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	7.8	10.8	14.7	6.4	16.4	
					5.5 V ± 0.5 V	6.7	9.4	12.6	5.4	13.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	7.2	9.9	13.4	5.9	15	
					5.5 V ± 0.5 V	6.1	8.6	11.4	4.8	12.5	
		SD		1.8 V ± 0.15 V	3.3 V ± 0.3 V	6.9	12.9	21.7	6	24.2	
					5.5 V ± 0.5 V	6.1	12.6	20.8	5.3	22.8	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	4.9	7.9	11.8	4.1	14.5	
					5.5 V ± 0.5 V	4.7	7.8	11.7	3.9	14.2	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	5	7.1	9.8	4	12	
					5.5 V ± 0.5 V	4.7	7	9.8	3.8	18.2	

switching characteristics over recommended operating free-air temperature range (data bus I/Os) (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{en}	$\overline{ENL}$ or $\overline{ENH}$	D	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	9.4	17.6	23.4	8.3	27.2	ns
					5.5 V ± 0.5 V	13.5	17.4	22.6	7.7	27.8	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	12.3	15	18.5	7.9	22.8	
					5.5 V ± 0.5 V	12.3	14.7	17.4	8	21.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	11.7	14.1	17	7.3	21.4	
					5.5 V ± 0.5 V	11.6	13.7	16	7.4	20.3	
		SD		1.8 V ± 0.15 V	3.3 V ± 0.3 V	9.5	18.7	30.5	9.1	35.5	
					5.5 V ± 0.5 V	9.6	19.1	30.5	9.1	35.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	10	13	17.4	6.8	22.6	
					5.5 V ± 0.5 V	10	13.2	17.4	6.8	22.6	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	9.6	11.3	13.6	6.2	18.3	
					5.5 V ± 0.5 V	9.6	11.4	13.6	6.3	18.2	
t_{dis}	$\overline{ENL}$ or $\overline{ENH}$	D	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.5	12.1	16.8	7.2	20.2	ns
					5.5 V ± 0.5 V	7.7	10.8	15	6.3	16.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	7.6	10.4	13.8	6.2	16.4	
					5.5 V ± 0.5 V	6.9	9.1	11.9	5.4	13.1	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	7.3	9.7	12.9	5.9	15	
					5.5 V ± 0.5 V	6.5	8.4	11	5.2	12	
		SD		1.8 V ± 0.15 V	3.3 V ± 0.3 V	6.5	12	20	5.7	24.2	
					5.5 V ± 0.5 V	5.7	11.8	19	5	22.8	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	4.6	7.4	11.1	3.8	14.5	
					5.5 V ± 0.5 V	4.4	7.3	11.1	3.7	14.2	
				3.3 V± 0.3 V	3.3 V ± 0.3 V	4.9	6.8	9.3	4	12	
					5.5 V ± 0.5 V	4.3	6.7	9.2	3.5	18.2	

switching characteristics over recommended operating free-air temperature range (SA10–SA00, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, $\overline{SREG}$, $\overline{SWE}$) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	S input	CF output (control)	$\overline{MASTER\_EN}$ = $\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	3.4	6.1	9.8	2.5	10.4	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	3	5.8	9.7	2.4	10.2	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	2.6	4.5	6.7	1.8	8.4	
				2.5 V ± 0.2 V	5 V ± 0.5 V	2.4	4.1	6	1.7	6.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	2.2	3.9	5.8	1.4	7	
				3.3 V ± 0.3 V	5 V ± 0.5 V	2	3.5	5	1.3	5.8	
		CF output (A pins)	$\overline{MASTER\_EN}$ = $\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	3.4	5.7	8.7	2.8	10.3	
				1.8 V ± 0.15 V	5 V ± 0.5 V	3.3	5.4	8.2	2.8	9.7	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	2.9	4.3	6.2	1.9	8.4	
				2.5 V ± 0.2 V	5 V ± 0.5 V	2.7	3.9	5.4	1.9	6.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	2.6	3.7	5.2	1.7	7	
				3.3 V ± 0.3 V	5 V ± 0.5 V	2.3	3.3	4.4	1.5	5.8	
t_{en}	$\overline{MASTER\_EN}$	CF output (control)	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	10.8	17.9	24.8	7.9	29.7	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	10.8	17.5	26.2	8.1	30.2	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	9.4	14.2	19.4	6.4	23.3	
				2.5 V ± 0.2 V	5 V ± 0.5 V	9.4	14.1	19.3	6.6	23.1	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	8.7	13.1	17.8	5.8	21.4	
				3.3 V ± 0.3 V	5 V ± 0.5 V	8.7	13	17.5	6	21.2	
t_{dis}	$\overline{MASTER\_EN}$	CF output (control)	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	7.3	13.8	22.5	6.2	25.8	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	6.8	12.1	19.7	5.9	26.3	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	6.1	11.8	19.2	4.9	20.2	
				2.5 V ± 0.2 V	5 V ± 0.5 V	5.9	10	16.3	4.6	19.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	5.6	11	18.3	4.6	19.1	
				3.3 V ± 0.3 V	5 V ± 0.5 V	5.4	9.2	15.5	3.9	18	
t_{en}	$\overline{BUF\_EN}$	CF output (A pins)	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	12.9	17.5	23.7	7.7	29.7	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	13.3	17.8	24.4	9.4	30.2	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	11.7	14.4	17.9	7.5	23.3	
				2.5 V ± 0.2 V	5 V ± 0.5 V	11.8	14.3	17.1	7.7	23.1	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	11	13.3	16.2	6.9	21.4	
				3.3 V ± 0.3 V	5 V ± 0.5 V	11.1	13.2	15.3	6.5	21.2	
t_{dis}	$\overline{BUF\_EN}$	CF output (A pins)	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.9	13.6	19.7	7.5	25.8	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	7.6	11.8	17.1	6.6	26.3	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	8	11.6	16	6.6	20.1	
				2.5 V ± 0.2 V	5 V ± 0.5 V	6.7	9.7	13.2	5	19.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	7.7	10.6	14.7	6	18.2	
				3.3 V ± 0.3 V	5 V ± 0.5 V	6.1	8.9	11.9	4.9	18	

switching characteristics over recommended operating free-air temperature range (SA10–SA00, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, $\overline{SREG}$, $\overline{SWE}$) (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{en}	$\overline{BUF\_EN}$	CF output (A pins)	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	12.3	16.4	21.9	7.7	27.2	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	12.6	16.7	22.6	8.6	29.1	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	11.2	13.8	17	7.1	21.7	
				2.5 V ± 0.2 V	5 V ± 0.5 V	11.4	13.7	16.3	7.3	21.5	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	10.7	12.9	15.6	6.7	19.5	
				3.3 V ± 0.3 V	5 V ± 0.5 V	10.8	12.8	14.8	6.5	19.6	
t_{dis}	$\overline{BUF\_EN}$	CF output (A pins)	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.4	13.9	21.2	7.2	23.2	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	7.6	12.3	18.5	6.6	23.7	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	7.7	12.3	18.2	6.4	19.8	
				2.5 V ± 0.2 V	5 V ± 0.5 V	6.7	10.6	15.3	5	18.4	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	7.2	11.5	16.4	5.9	18	
				3.3 V ± 0.3 V	5 V ± 0.5 V	6.4	10	14.3	4.9	17	
t_{en}	$\overline{BUF\_EN}$	CF output	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	12.5	16.6	22.3	8.7	27.2	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	12.8	17	23.1	8.8	29.1	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	11.4	14.1	17.5	7.3	21.7	
				2.5 V ± 0.2 V	5 V ± 0.5 V	11.6	14	16.9	7.4	21.5	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	10.9	13.2	16	6.8	20	
				3.3 V ± 0.3 V	5 V ± 0.5 V	11	13.1	15.3	6.5	19.6	
t_{dis}	$\overline{BUF\_EN}$	CF output	$\overline{MASTER\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.6	13.9	21.5	7.4	23.2	ns
				1.8 V ± 0.15 V	5 V ± 0.5 V	7.7	12.1	19.8	6.6	23.7	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	7.9	12.3	18.5	6.5	19.8	
				2.5 V ± 0.2 V	5 V ± 0.5 V	6.6	10.4	17.1	5	18.4	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	7.4	11.7	17.5	6.1	18.9	
				3.3 V ± 0.3 V	5 V ± 0.5 V	6.1	9.7	16.2	4.9	17	
t_{en}	$\overline{MASTER\_EN}$	DIR_OUT	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	6.1	14.2	29.6	4.9	32.8	ns
					5 V ± 0.5 V	6	14.2	30	4.9	33.2	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	4.8	8.8	15.4	3.4	19.3	
					5 V ± 0.5 V	4.8	8.8	15.5	3.4	19.3	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	4.2	6.9	11.1	2.7	14.4	
					5 V ± 0.5 V	4.2	6.9	11.1	2.6	14.4	
t_{dis}	$\overline{MASTER\_EN}$	DIR_OUT	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	5.4	10	16.6	4.2	32.6	ns
					5 V ± 0.5 V	5.4	9.9	16.1	4.8	32.6	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	3.9	6.5	10.5	1.5	19.3	
					5 V ± 0.5 V	3.9	6.6	10.4	1.7	19.3	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	4.4	6.7	10.3	1.4	14.4	
					5 V ± 0.5 V	4.3	6.7	10.1	1.5	14.4	
t_{pd}	$\overline{SIORD}$ or $\overline{SOE}$	DIR_OUT	$\overline{BUF\_EN}$ = V_{IL}	1.8 V ± 0.15 V	3.3 V ± 0.3 V	5	9.3	15.7	4	17.9	ns
					5 V ± 0.5 V	5	9.3	15.7	4	17.9	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	3.9	6	8.5	2.8	11	
					5 V ± 0.5 V	3.9	6	8.5	2.8	11	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	3.3	4.7	6.2	2.2	8.2	
					5 V ± 0.5 V	3.3	4.7	6.2	2.2	8.2	

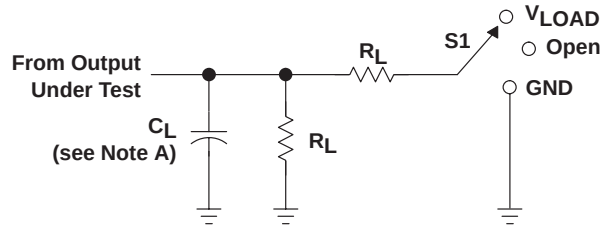
switching characteristics over recommended operating free-air temperature range (SA10–SA00, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$, $\overline{SIOWR}$, $\overline{SOE}$, $\overline{SREG}$, $\overline{SWE}$) (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC_S}	V_{CC_CF}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	$\overline{BUF\_EN}$	DIR_OUT	$\overline{BUF\_EN} = V_{IL}$	1.8 V ± 0.15 V	3.3 V ± 0.3 V	8.9	19.5	35.9	7.1	39.2	ns
					5 V ± 0.5 V	8.9	19.5	35.8	7	39.3	
				2.5 V ± 0.2 V	3.3 V ± 0.3 V	6.8	11.9	19.1	5	22.8	
					5 V ± 0.5 V	6.8	11.9	19.2	4.9	22.8	
				3.3 V ± 0.3 V	3.3 V ± 0.3 V	5.8	9	13.3	4	15.8	
					5 V ± 0.5 V	5.8	9	13.3	3.9	15.9	

operating characteristics, V_{CCS} and V_{CC_CF} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdS}	Power dissipation capacitance per transceiver, system-port input, CF-port output	Outputs enabled	C_L = 0, f = 10 MHz	1.93	pF
		Outputs disabled		0.04	
	Power dissipation capacitance per transceiver, CF-port input, system-port output	Outputs enabled		14.35	
		Outputs disabled		0.04	
C_{pdCF}	Power dissipation capacitance per transceiver, system-port input, CF-port output	Outputs enabled	C_L = 0, f = 10 MHz	22.85	pF
		Outputs disabled		0.04	
	Power dissipation capacitance per transceiver, CF-port input, system-port output	Outputs enabled		4.66	
		Outputs disabled		3.65	

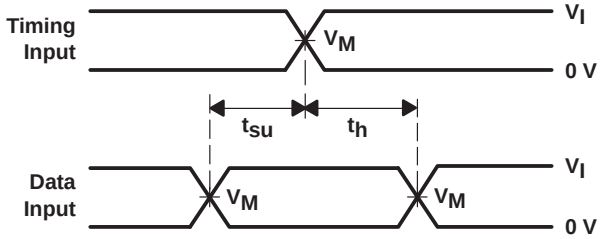
PARAMETER MEASUREMENT INFORMATION



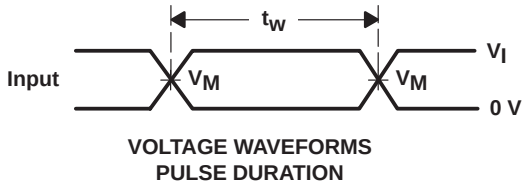
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

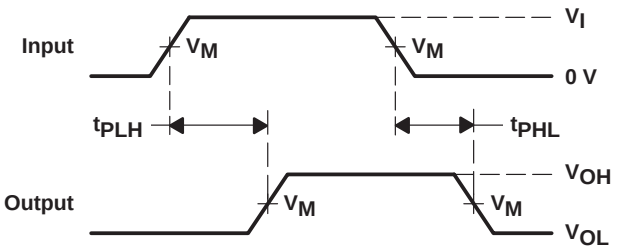
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.5 ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	15 pF	2 kΩ	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	15 pF	2 kΩ	0.3 V
5.5 V ± 0.5 V	2.7 V	≤2.5 ns	1.5 V	6 V	15 pF	2 kΩ	0.5 V



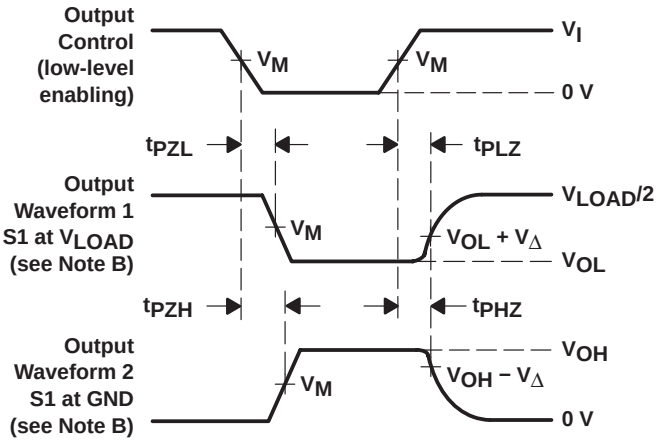
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

23-Apr-2005

PACKAGING INFORMATION

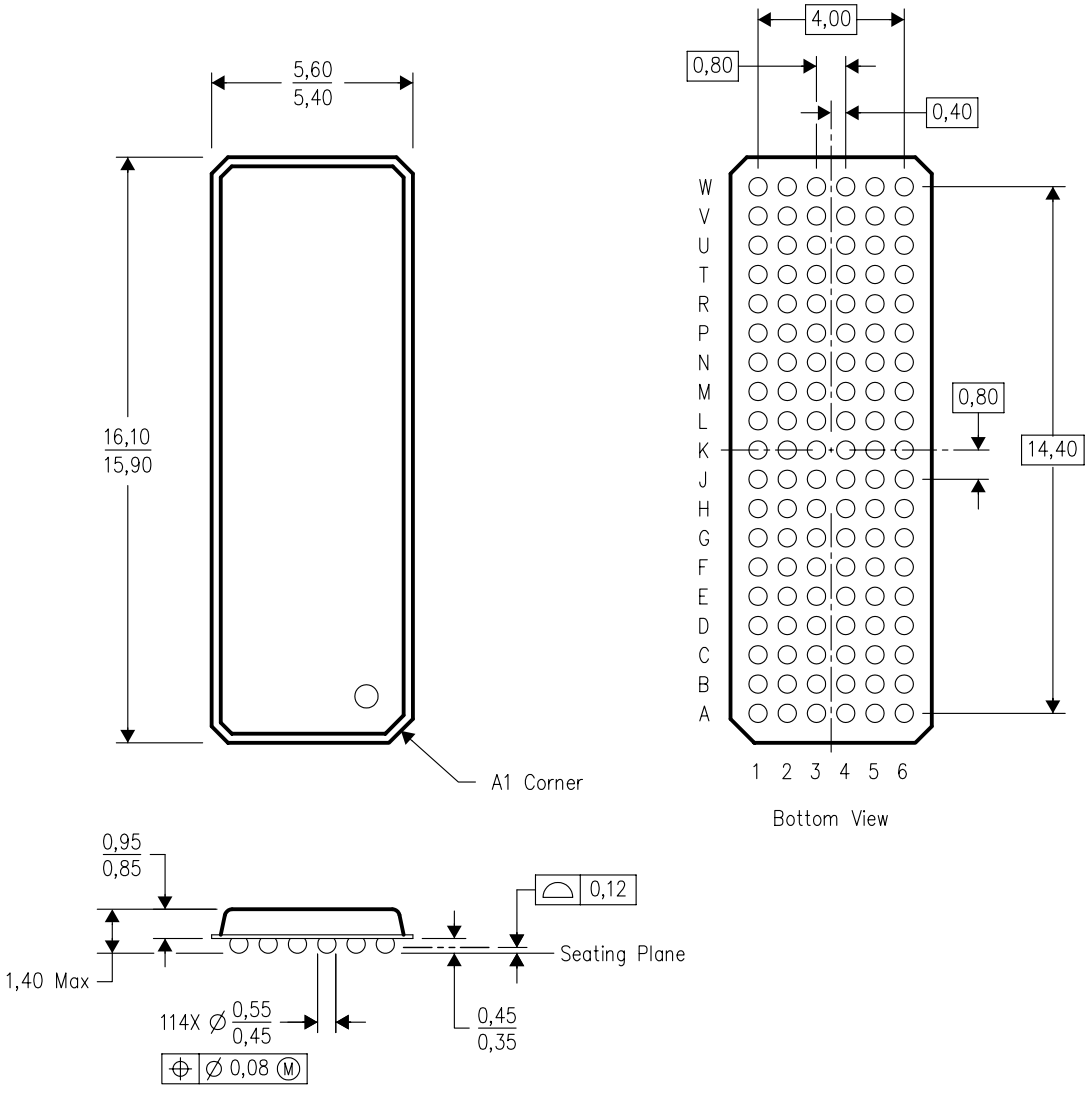
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LV4320AGKFR	ACTIVE	LFBGA	GKF	114	1000	TBD	SNPB	Level-3-220C-168 HR
SN74LV4320AZKFR	ACTIVE	LFBGA	ZKF	114	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-250C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

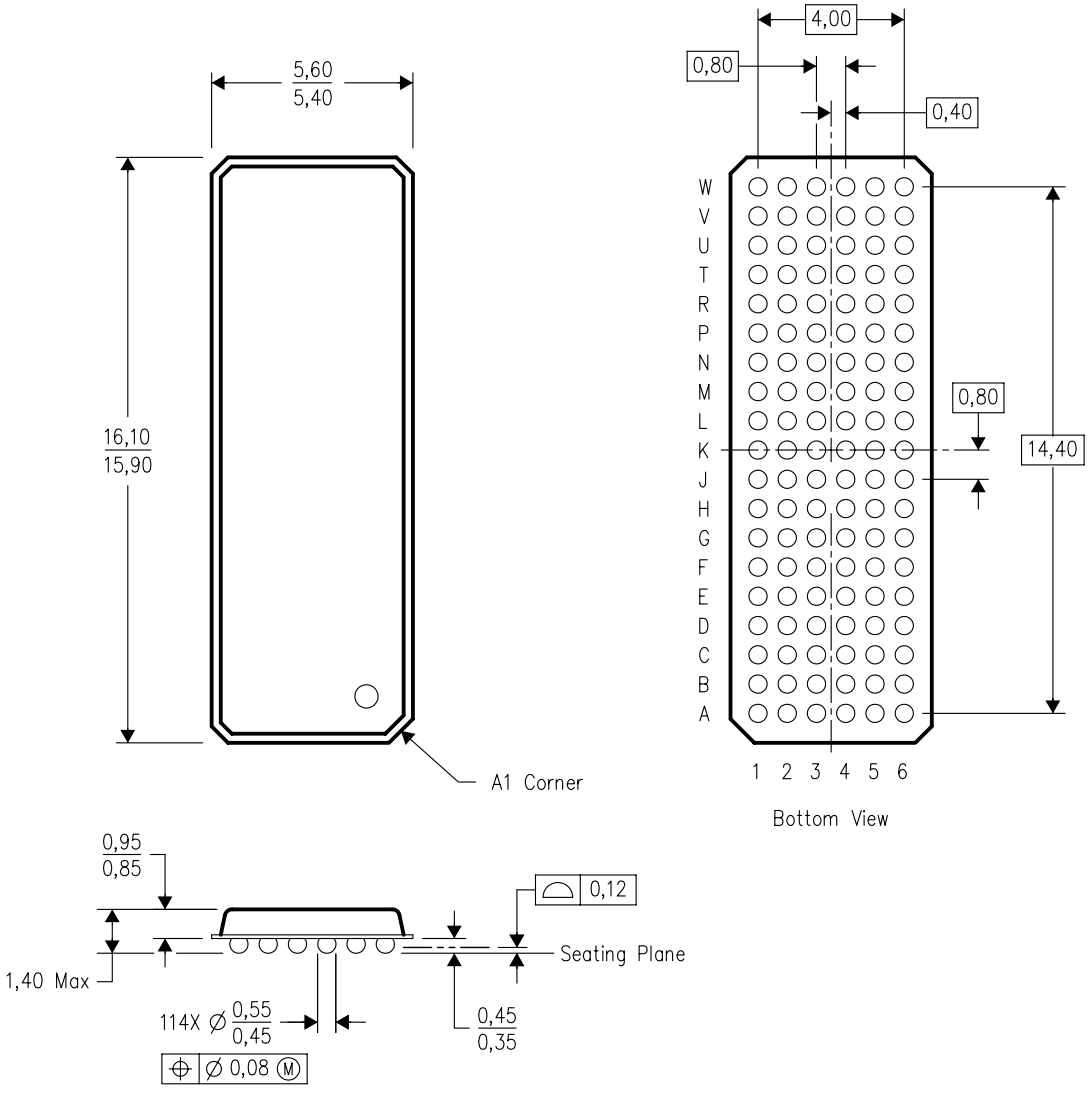
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

GKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation DC.
D. This package is tin–lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead–free.

ZKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation DC.
D. This package is lead–free. Refer to the 114 GKF package (drawing 4188954) for tin–lead (SnPb).

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