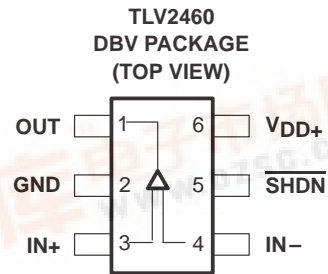


查询TLV2460AID供应商 TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN
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- **Input Common-Mode Range Exceeds Both Supply Rails . . . $-0.2V$ to $V_{DD+} + 0.2V$**
- **Gain Bandwidth Product . . . 6.4MHz**
- **Supply Current . . . 500 μ A/channel**
- **Input Offset Voltage . . . 100 μ V**
- **Input Noise Voltage . . . 11nV/ \sqrt Hz**
- **Rail-to-Rail Output Swing**
- **Slew Rate . . . 1.6 V/ μ s**
- **\pm 90mA Output Drive Capability**
- **Micropower Shutdown Mode (TLV2460/3/5) . . . 0.3 μ A/channel**
- **Available in 5- or 6-pin SOT23 and 8- or 10-Pin MSOP**
- **Characterized From $T_A = -40^{\circ}C$ to $125^{\circ}C$**
- **Universal Op Amp EVM**



description

The TLV246x is a family of low-power rail-to-rail input/output operational amplifiers specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

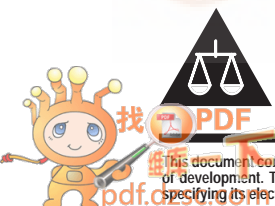
The operational amplifier has 6.4 MHz of bandwidth and 1.6 V/ μ s of slew rate with only 500 μ A of supply current, providing good ac performance with low power consumption. Three members of the family offer a shutdown terminal, which places the amplifier in an ultra-low supply current mode ($I_{DD} = 0.3 \mu$ A/ch). While in shutdown, the operational-amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/ \sqrt Hz and input offset voltage of 100 μ V.

This family is available in the low-profile SOT23, MSOP, and TSSOP packages. The TLV2460 is the first rail-to-rail input/output operational amplifier with shutdown available in the 6-pin SOT23, making it perfect for high-density circuits. The family is specified over an expanded temperature range ($T_A = -40^{\circ}C$ to $125^{\circ}C$) for use in industrial control and automotive systems.

FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2460	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2461	1	8	8	5	—	—	—	
TLV2462	2	8	8	—	—	8	—	
TLV2463	2	14	14	—	—	10	Yes	
TLV2464	4	14	14	—	14	—	—	
TLV2465	4	16	16	—	16	—	Yes	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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TLV2460 and TLV2461 AVAILABLE OPTIONS

T _A	V _{IOMax} AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	SOT-23† (DBV)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2460CD TLV2461CD	TLV2460CDBV TLV2461CDBV	TLV2460CP TLV2461CP	TLV2460Y TLV2461Y
-40°C to 125°C	2000 µV	TLV2460ID TLV2461ID	TLV2460IDBV TLV2461IDBV	TLV2460IP TLV2461IP	— —
	1500 µV	TLV2460AID TLV2461AID	— —	TLV2460AIP TLV2461AIP	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460CDR).

‡ Chip forms are tested at T_A = 25°C only.

TLV2462 and TLV2463 AVAILABLE OPTIONS

T _A	V _{IOMax} AT 25°C	PACKAGED DEVICES					CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	MSOP (DGK)	MSOP† (DGS)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2462CD TLV2463CD	TLV2462CDGK —	— TLV2463CDGS	— TLV2463CN	TLV2462CP —	TLV2462Y TLV2463Y
-40°C to 125°C	2000 µV	TLV2462ID TLV2463ID	TLV2462IDGK —	— TLV2463IDGS	— TLV2463IN	TLV2462IP —	— —
	1500 µV	TLV2462AID TLV2463AID	— —	— —	— TLV2463AIN	TLV2462AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462CDR).

‡ Chip forms are tested at T_A = 25°C only.

TLV2464 and TLV2465 AVAILABLE OPTIONS

T _A	V _{IOMax} AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	2000 µV	TLV2464CD TLV2465CD	TLV2464CN TLV2465CN	TLV2464CPW TLV2465CPW	TLV2464Y TLV2465Y
-40°C to 125°C	2000 µV	TLV2464ID TLV2465ID	TLV2464IN TLV2465IN	TLV2464IPW TLV2465IPW	— —
-40°C to 125°C	1500 µV	TLV2464AID TLV2465AID	TLV2464AIN TLV2465AIN	TLV2464AIPW TLV2465AIPW	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2464CDR).

‡ Chip forms are tested at T_A = 25°C only.

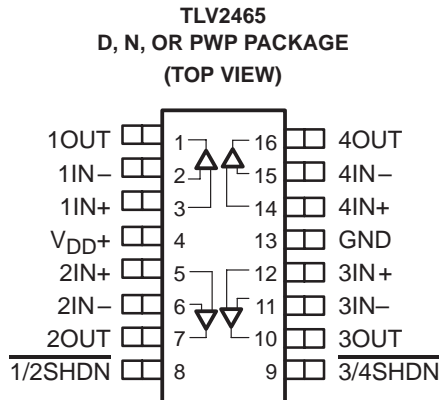
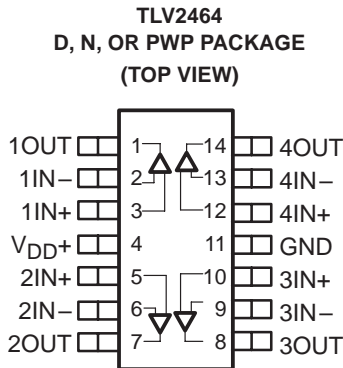
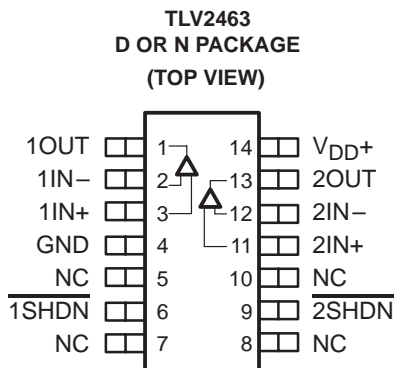
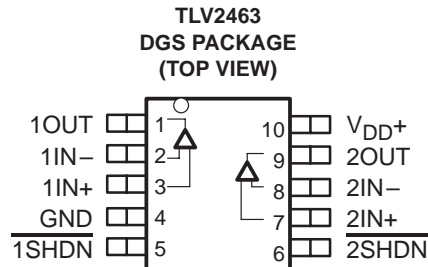
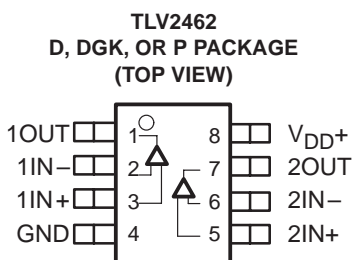
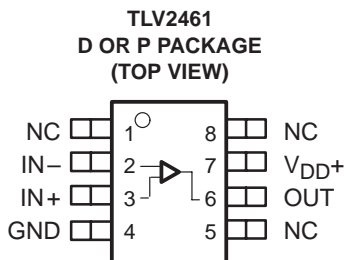
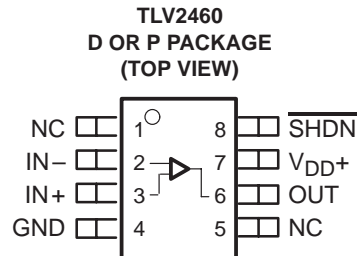
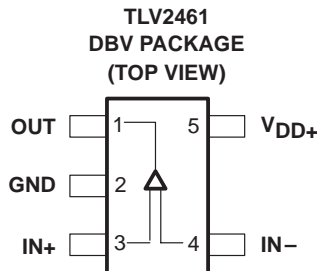
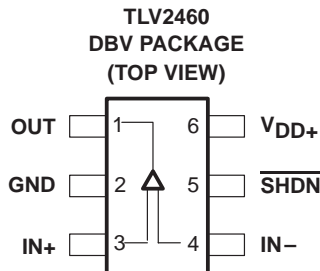
SOT-23 AND MSOP DEVICE SYMBOLS

DEVICE TYPE	NO. OF TERMINALS	PACKAGE NAME	SYMBOL
SOT-23	6 Pin	TLV2460CDBV	VAOC
		TLV2460IDBV	VAOI
	5 Pin	TLV2461CDBV	VAPC
		TLV2461IDBV	VAPI
MSOP	8 Pin	TLV2462CDGK	xxTIAAI
		TLV2462IDGK	xxTIAAJ
	10 Pin	TLV2463CDGS	xxTIAAK
		TLV2463IDGS	xxTIAAL

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TLV246x PACKAGE PINOUTS



NC – No internal connection

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	6 V
Differential input voltage, V_{ID}	$V_{DD} - 0.2 \text{ V}$ to $V_{DD} + 0.2 \text{ V}$
Input current, I_I (any input)	$\pm 200 \text{ mA}$
Output current, I_O	$\pm 175 \text{ mA}$
Total input current, I_I (into V_{DD+})	175 mA
Total output current, I_O (out of GND)	175 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	-40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	725 mW
D (14)	26.9	122.6	725 mW
D (16)	25.7	114.7	725 mW
DBV (5)	55	324.1	437 mW
DBV (6)	55	294.3	437 mW
DGK	54.23	259.96	424 mW
DGS	54.1	257.71	424 mW
N (14)	32	78	1150 mW
N (16)	32	78	1150 mW
P	41	104	1000 mW
PW (14)	29.3	173.6	700 mW
PW (16)	28.7	161.4	700 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	± 1.35	± 3	
Common-mode input voltage range, V_{ICR}		GND	V_{DD+}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	-40	125	

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage (TLV246x)	$V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	100	2000	μV	
		Full range	2200			
V_{IO} Input offset voltage (TLV246xA)		25°C	150	1500	μV	
		Full range	1700			
α_{VIO} Temperature coefficient of input offset voltage				2	$\mu\text{V}/^\circ\text{C}$	
I_{IO} Input offset current		$V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	2.8	7	nA
	TLV246xC		Full range			
	TLV246xI		Full range			
I_{IB} Input bias current	25°C		4.4	14	nA	
	TLV246xC		Full range			
	TLV246xI		Full range			
V_{ICR} Common-mode input voltage range	CMRR > 66 dB $R_S = 50\ \Omega$	25°C	-0.2 to 3.2		V	
	CMRR > 60 dB $R_S = 50\ \Omega$	Full range	-0.2 to 3.2			
V_{OH} High-level output voltage	$I_{OH} = -2.5\text{ mA}$	25°C	2.9		V	
		Full range	2.8			
	$I_{OH} = -10\text{ mA}$	25°C	2.7			
		Full range	2.5			
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 2.5\text{ mA}$	25°C	0.1		V	
		Full range	0.2			
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 10\text{ mA}$	25°C	0.3			
		Full range	0.5			
I_{OS} Short-circuit output current	Sourcing	25°C	50		mA	
		Full range	20			
	Sinking	25°C	40			
		Full range	20			
I_O Output current		25°C	± 30		mA	
A_{VD} Large-signal differential voltage amplification	$R_L = 10\text{ k}\Omega$	25°C	90	105	dB	
		Full range	89			
$r_{i(d)}$ Differential input resistance		25°C	10^9		Ω	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	7		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C	33		Ω	
CMRR Common-mode rejection ratio	$V_{ICR} = -0.2\text{ V to } 3.2\text{ V}$, $R_S = 50\ \Omega$	25°C	66	80	dB	
		TLV246xC	Full range			
		TLV246xI	Full range			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 6\text{ V}$, No load	$V_{IC} = V_{DD}/2$,	25°C	80	85	dB
			Full range	75		
	$V_{DD} = 3\text{ V to } 5\text{ V}$, No load	$V_{IC} = V_{DD}/2$,	25°C	85	95	
			Full range	80		

† Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
I_{DD} Supply current (per channels)	$V_O = 1.5\text{ V}$, SHDN > 1.02 V	No load,	25°C	0.5	0.575	mA
			Full range	0.9		
$V_{(ON)}$ Turnon voltage level	$A_V = 1$	Channel 1	25°C	1.021		V
		Channel 2		1.02		
$V_{(OFF)}$ Turnoff voltage level	$A_V = 1$	Channel 1	25°C	0.822		V
		Channel 2		0.817		
$I_{DD(SHDN)}$ Supply current in shutdown (TLV2460, TLV2463, TLV2465)	SHDN < 0.8 V, Per channel in shutdown	25°C	0.3			μA
		Full range	2.5			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 160\text{ pF}$,	25°C	1	1.6	$\text{V}/\mu\text{s}$
			Full range	0.8		
V_n Equivalent input noise voltage	$f = 100\text{ Hz}$	25°C	16			$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C	11			
I_n Equivalent input noise current	$f = 1\text{ kHz}$	25°C	0.13			$\text{pA}/\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$	$A_V = 1$	25°C	0.006%		
		$A_V = 10$		0.02%		
		$A_V = 100$		0.08%		
$t_{(on)}$ Amplifier turnon time	$A_V = 1$, $R_L = 10\text{ k}\Omega$	Both channels	25°C	7.6		μs
		Channel 1 only, Channel 2 on		7.65		
		Channel 2 only, Channel 1 on		7.25		
$t_{(off)}$ Amplifier turnoff time	$A_V = 1$, $R_L = 10\text{ k}\Omega$	Both channels	25°C	333		ns
		Channel 1 only, Channel 2 on		328		
		Channel 2 only, Channel 1 on		329		
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 160\text{ pF}$	$R_L = 10\text{ k}\Omega$,	25°C	5.2		MHz
t_s Settling time	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%	25°C	1.47		μs
		0.01%		1.78		
	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 56\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%		1.77		
		0.01%		1.98		
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 160\text{ pF}$	25°C	44°			
Gain margin		25°C	7		dB	

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage (TLV246x)	$V_{DD} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	150	2000	μV	
		Full range	2200			
V_{IO} Input offset voltage (TLV246xA)		25°C	150	1500	μV	
		Full range	1700			
α_{VIO} Temperature coefficient of input offset voltage		25°C	2		$\mu\text{V}/^\circ\text{C}$	
I_{IO} Input offset current		$V_{DD} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	0.3	7	nA
	TLV246xC		Full range			
	TLV246xI		Full range			
I_{IB} Input bias current	25°C		1.3	14	nA	
	TLV246xC		Full range			
	TLV246xI		Full range			
V_{ICR} Common-mode input voltage range	CMRR > 71 dB, $R_S = 50\ \Omega$	25°C	-0.2 to 5.2		V	
	CMRR > 60 dB, $R_S = 50\ \Omega$	Full range	0 to 5			
V_{OH} High-level output voltage	$I_{OH} = -2.5\text{ mA}$	25°C	4.9		V	
		Full range	4.8			
	$I_{OH} = -10\text{ mA}$	25°C	4.8			
		Full range	4.7			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 2.5\text{ mA}$	25°C	0.1		V	
		Full range	0.2			
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 10\text{ mA}$	25°C	0.2			
		Full range	0.3			
I_{OS} Short-circuit output current	Sourcing	25°C	145		mA	
		Full range	60			
	Sinking	25°C	100			
		Full range	60			
I_O Output current		25°C	± 90		mA	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	92	109	dB
			Full range	90		
$r_{i(d)}$ Differential input resistance		25°C	10^9		Ω	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	7		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C	29		Ω	
CMRR Common-mode rejection ratio	$V_{ICR} = -0.2\text{ V to }5.2\text{ V}$, $R_S = 50\ \Omega$	25°C	71	85	dB	
		TLV246xC	Full range			
		TLV246xI	Full range			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }6\text{ V}$, No load	$V_{IC} = V_{DD}/2$	25°C	80	85	dB
			Full range	75		
	$V_{DD} = 3\text{ V to }5\text{ V}$, No load	$V_{IC} = V_{DD}/2$	25°C	85	95	dB
			Full range	80		

† Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
I_{DD} Supply current (per channel)	$V_O = 2.5\text{ V}$, SHDN > 1.38 V	No load,	25°C	0.55	0.65	mA
			Full range	1		
$V_{(ON)}$ Turnon voltage level	$A_V = 1$	Channel 1	25°C	1.372		V
		Channel 2		1.368		
$V_{(OFF)}$ Turnoff voltage level	$A_V = 1$	Channel 1	25°C	1.315		V
		Channel 2		1.309		
$I_{DD}(SHDN)$ Supply current in shutdown (TLV2460, TLV2463, TLV2465)	SHDN < 1.3 V, Per channels in shutdown	25°C	1			μA
		Full range	3			

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV246x			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O(PP) = 2\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 160\text{ pF}$,	25°C	1	1.6	$\text{V}/\mu\text{s}$
			Full range	0.8		
V_n Equivalent input noise voltage	$f = 100\text{ Hz}$	25°C	14			$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C	11			
I_n Equivalent input noise current	$f = 100\text{ Hz}$	25°C	0.13			$\text{pA}/\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O(PP) = 4\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 10\text{ kHz}$	$A_V = 1$	25°C	0.004%		
		$A_V = 10$		0.01%		
		$A_V = 100$		0.04%		
$t_{(on)}$ Amplifier turnon time	$A_V = 1$, $R_L = 10\text{ k}\Omega$	Both channels	25°C	7.6		μs
		Channel 1 only, Channel 2 on		7.65		
		Channel 2 only, Channel 1 on		7.25		
$t_{(off)}$ Amplifier turnoff time	$A_V = 1$, $R_L = 10\text{ k}\Omega$	Both channels	25°C	333		ns
		Channel 1 only, Channel 2 on		328		
		Channel 2 only, Channel 1 on		329		
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 160\text{ pF}$	$R_L = 10\text{ k}\Omega$,	25°C	6.4		MHz
t_s Settling time	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%	25°C	1.53		μs
		0.01%		1.83		
	$V_{(STEP)PP} = 2\text{ V}$, $A_V = -1$, $C_L = 56\text{ pF}$, $R_L = 10\text{ k}\Omega$	0.1%		3.13		
		0.01%		3.33		
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 160\text{ pF}$	25°C	45°			
Gain margin		25°C	7		dB	

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

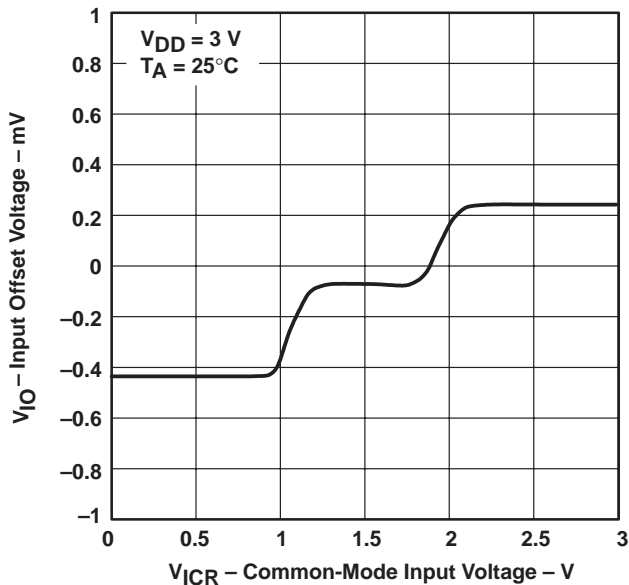


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

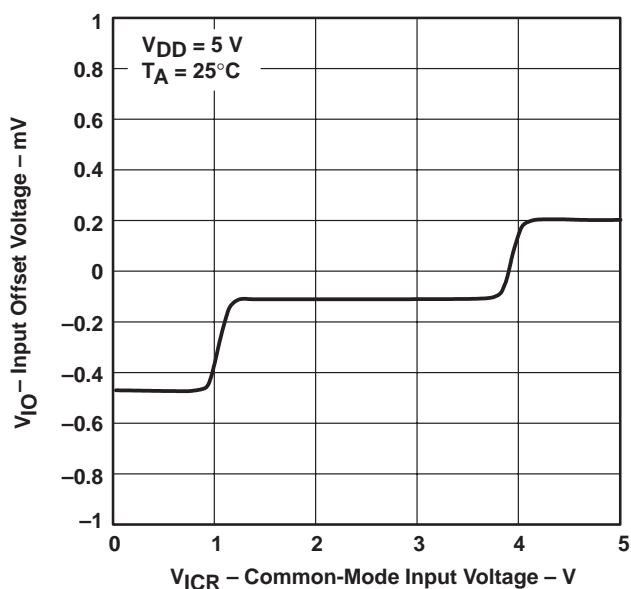


Figure 2

INPUT BIAS AND INPUT OFFSET CURRENT
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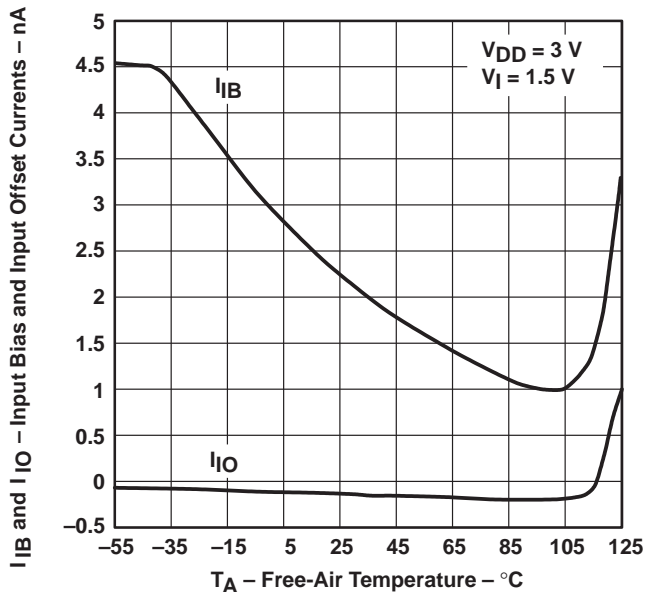


Figure 3

INPUT BIAS AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

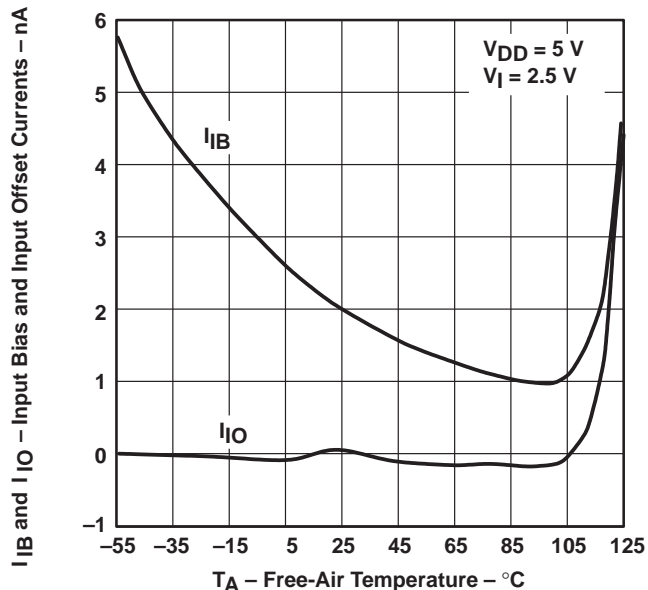


Figure 4

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

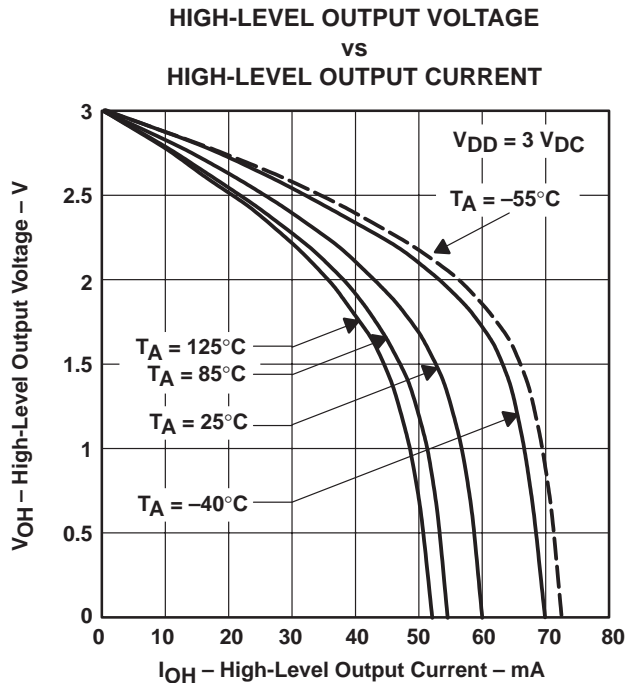


Figure 5

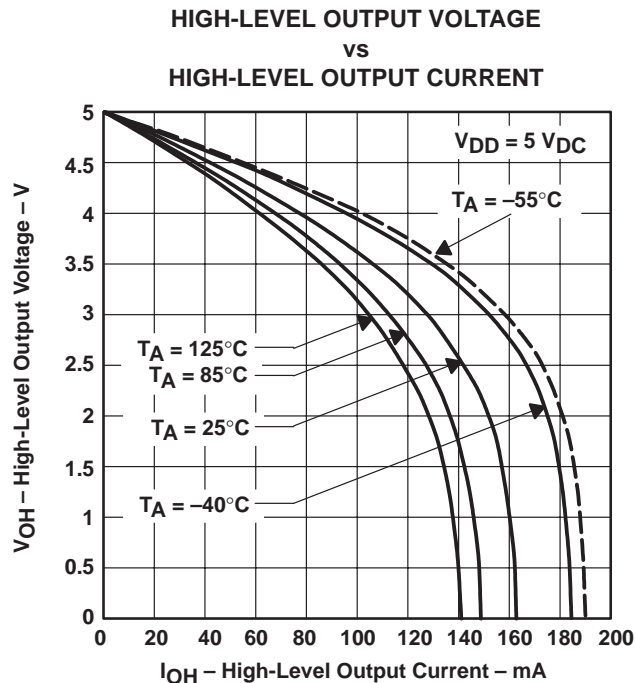


Figure 6

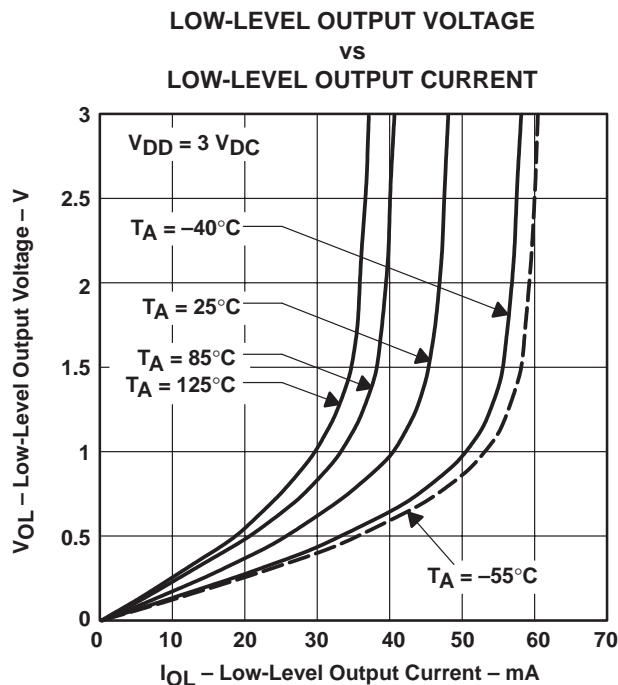


Figure 7

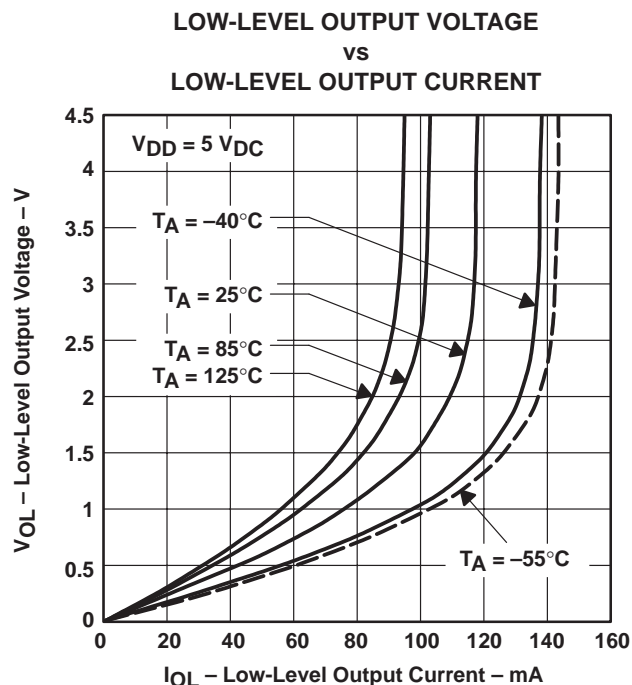


Figure 8

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
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TYPICAL CHARACTERISTICS

**PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

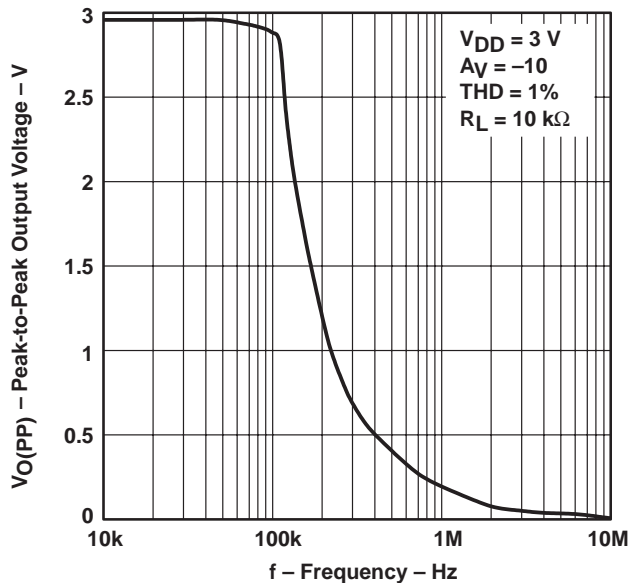


Figure 9

**PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

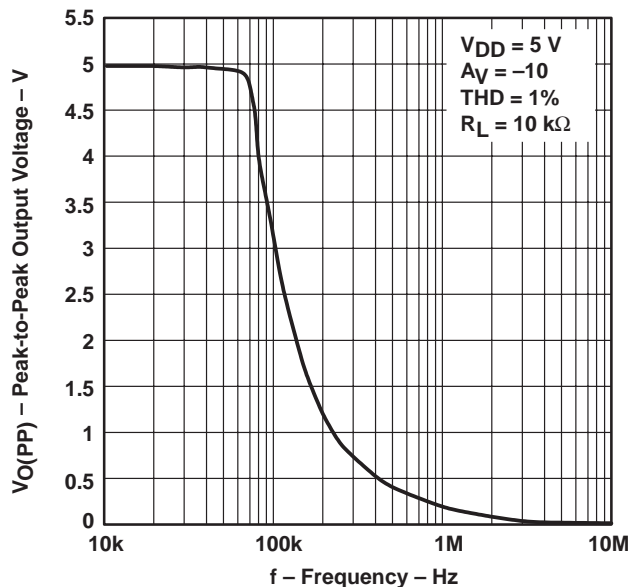


Figure 10

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

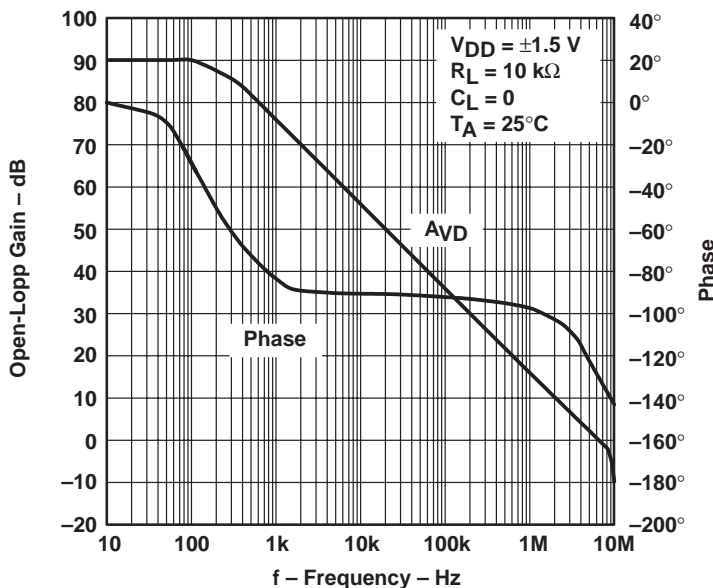


Figure 11

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
 vs
 FREQUENCY

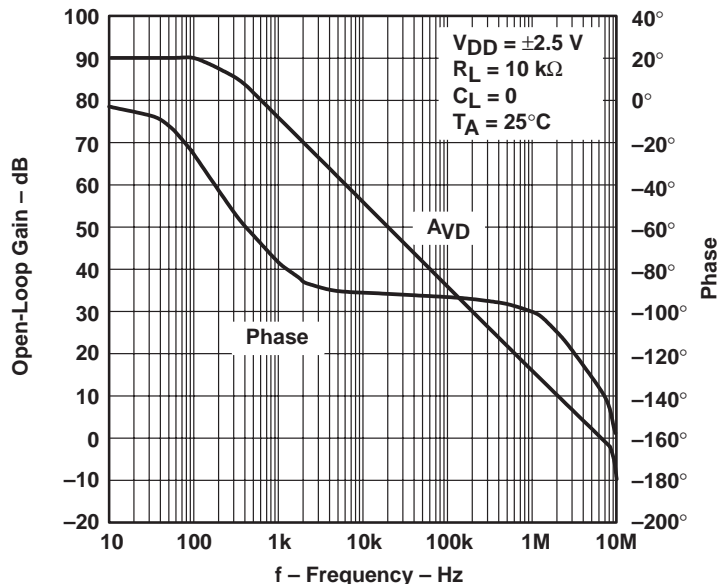


Figure 12

DIFFERENTIAL VOLTAGE AMPLIFICATION
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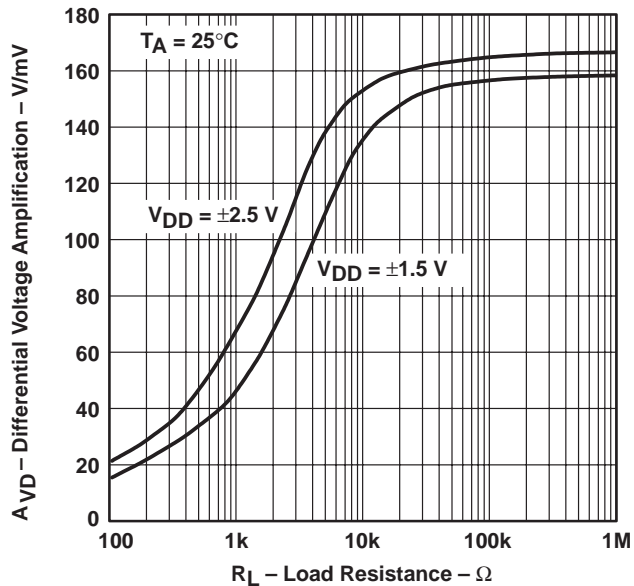


Figure 13

AMPLIFIER STABILITY
 vs
 LOAD

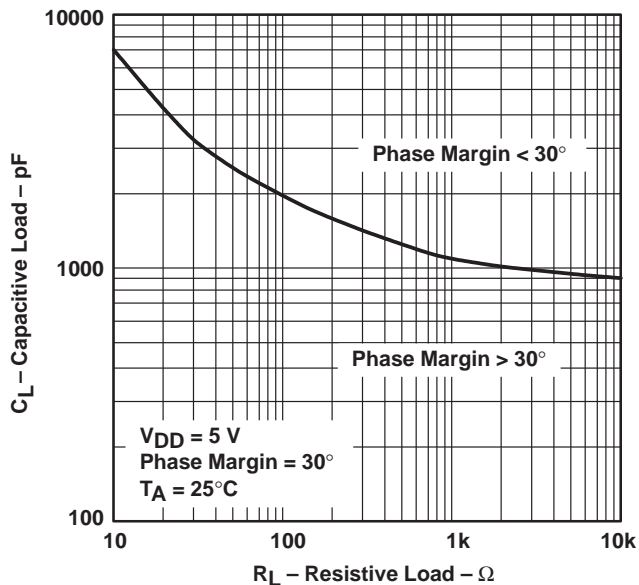


Figure 14

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

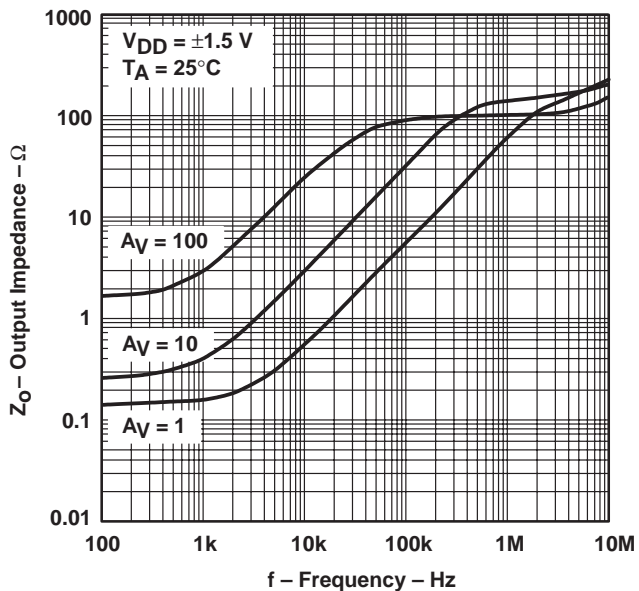


Figure 15

OUTPUT IMPEDANCE
vs
FREQUENCY

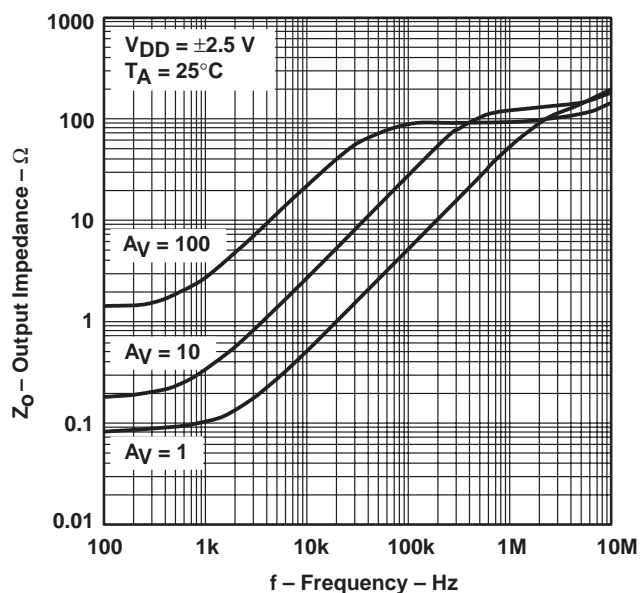


Figure 16

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

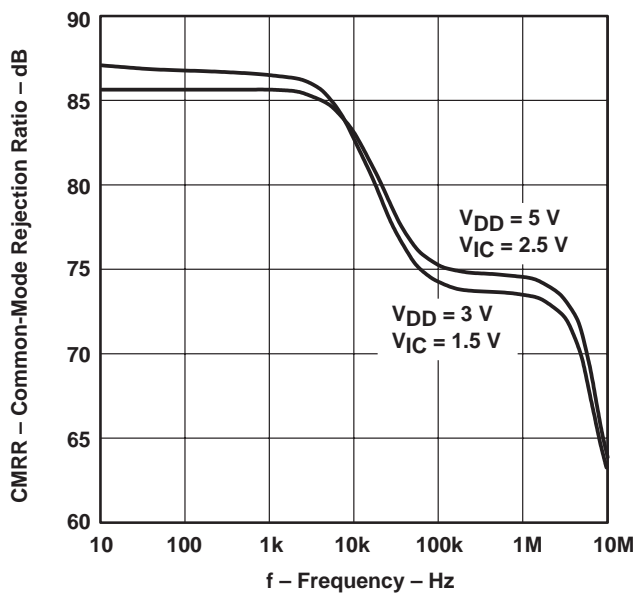


Figure 17

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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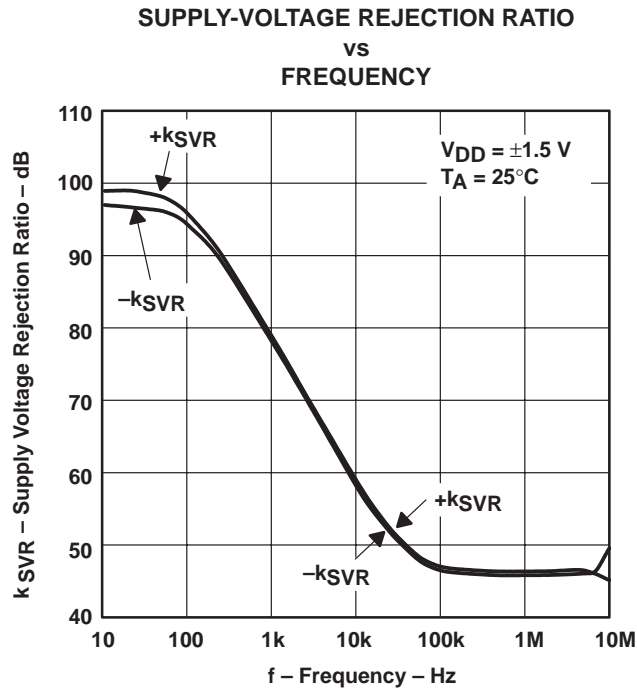


Figure 18

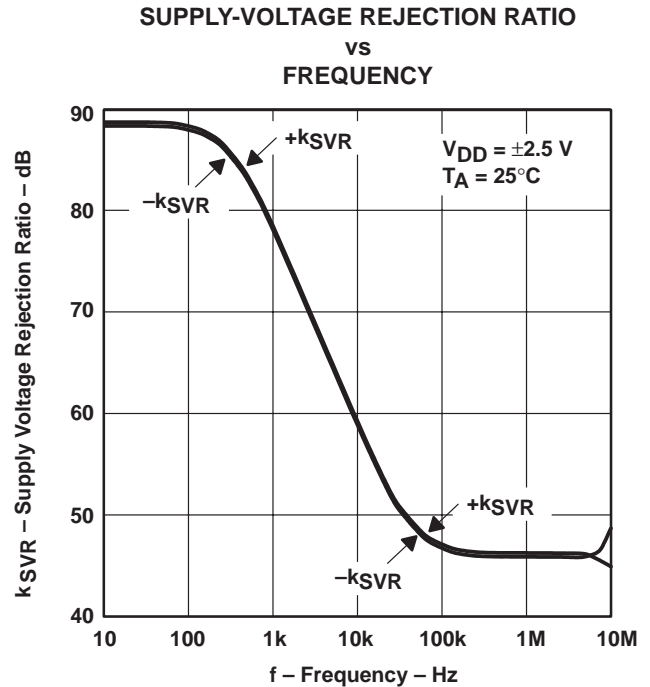


Figure 19

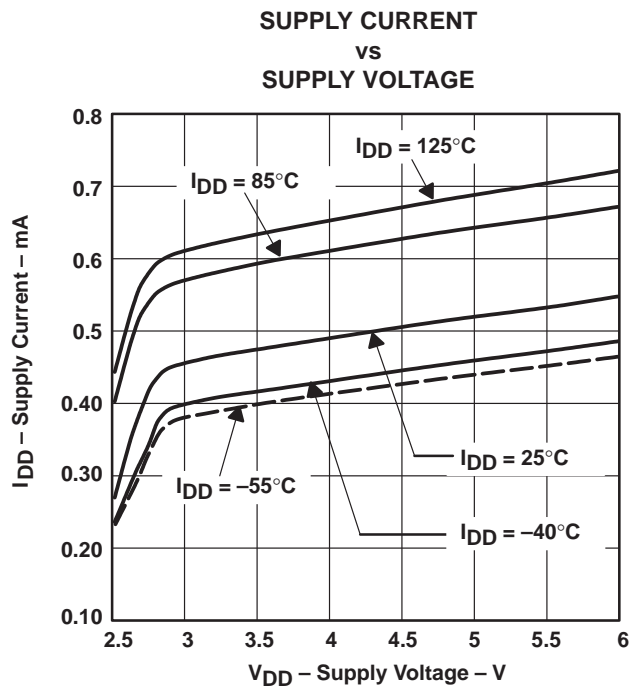


Figure 20

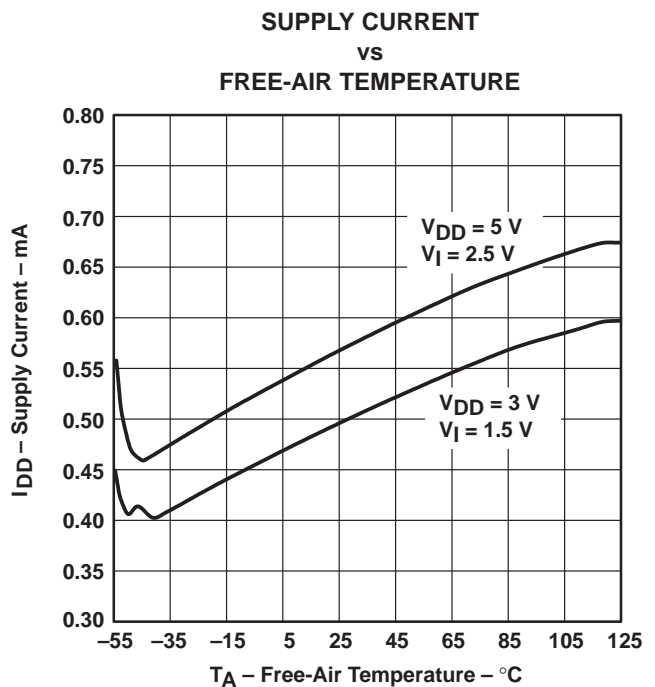


Figure 21

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
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TYPICAL CHARACTERISTICS

**AMPLIFIER WITH A SHUTDOWN PULSE
 TURNON CHARACTERISTICS**

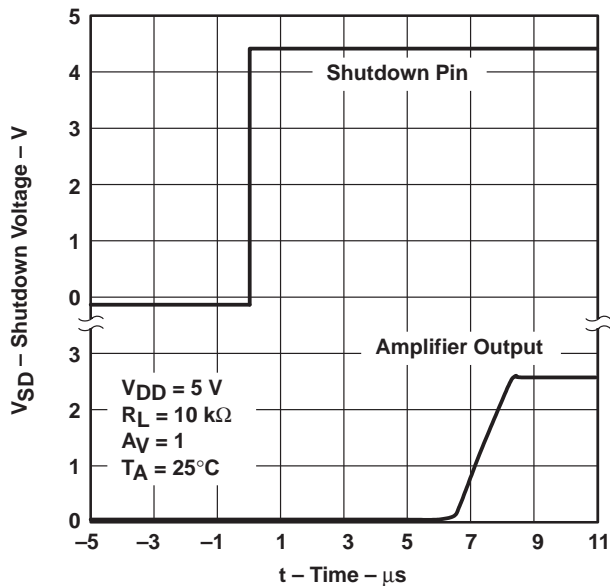


Figure 22

**AMPLIFIER WITH A SHUTDOWN PULSE
 TURNOFF CHARACTERISTICS**

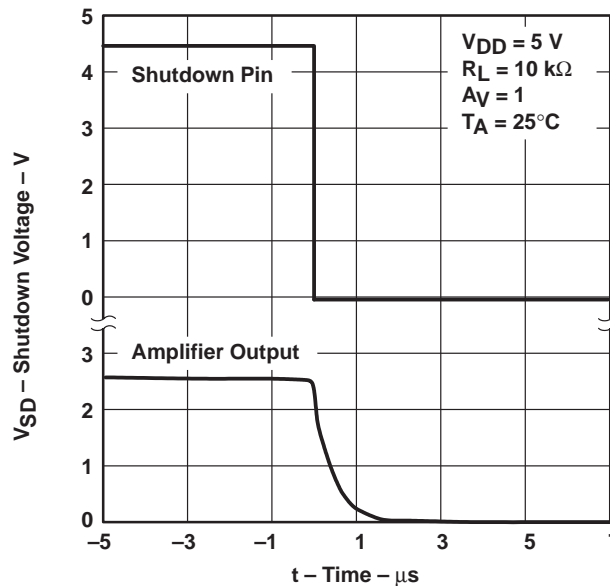


Figure 23

**SUPPLY CURRENT WITH A SHUTDOWN PULSE
 TURNON CHARACTERISTICS**

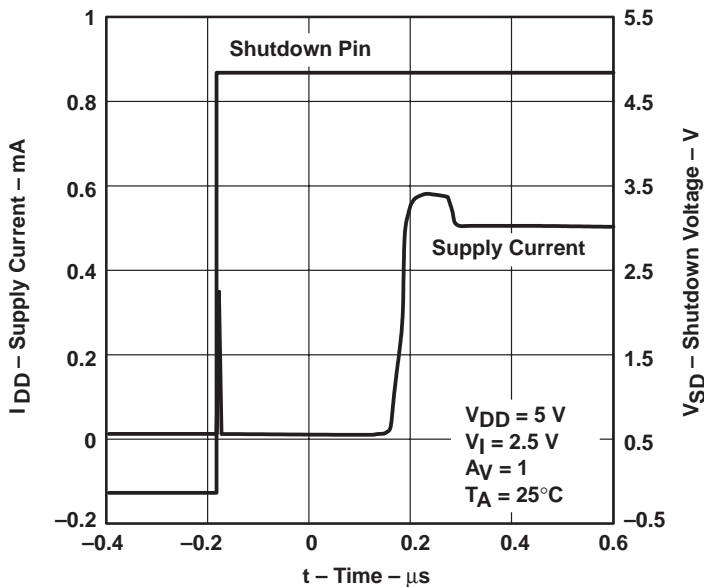


Figure 24

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
 FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
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TYPICAL CHARACTERISTICS

TURN-OFF SUPPLY CURRENT
 WITH A SHUTDOWN PULSE

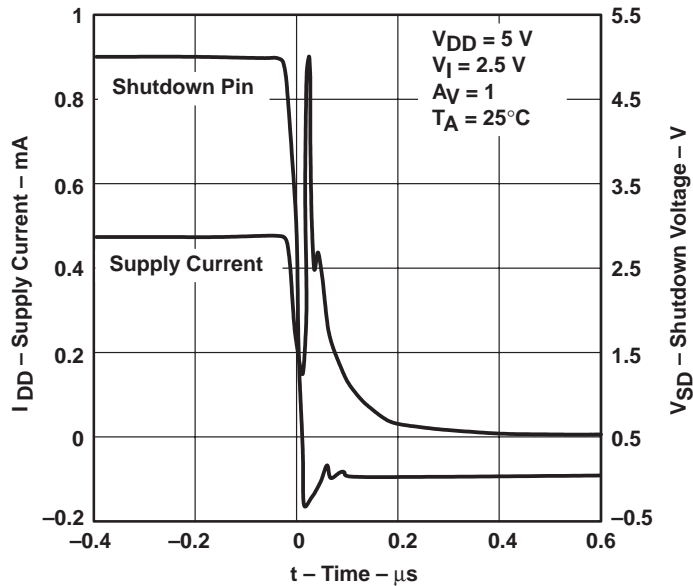


Figure 25

SHUTDOWN SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE

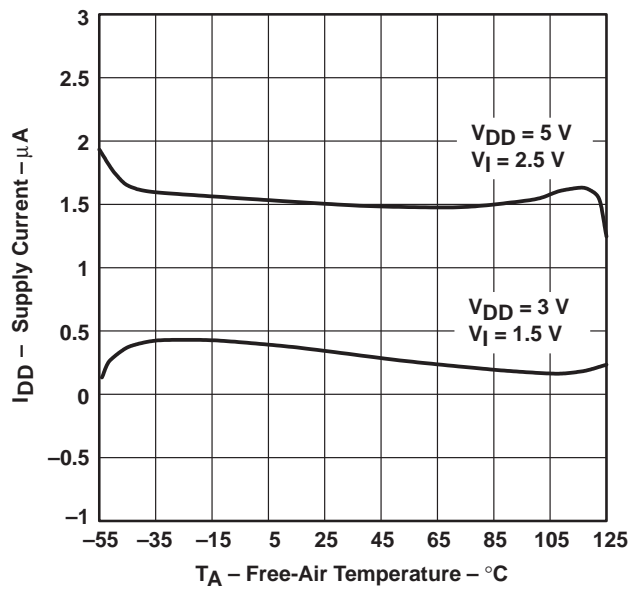


Figure 26

SLEW RATE
 vs
 SUPPLY VOLTAGE

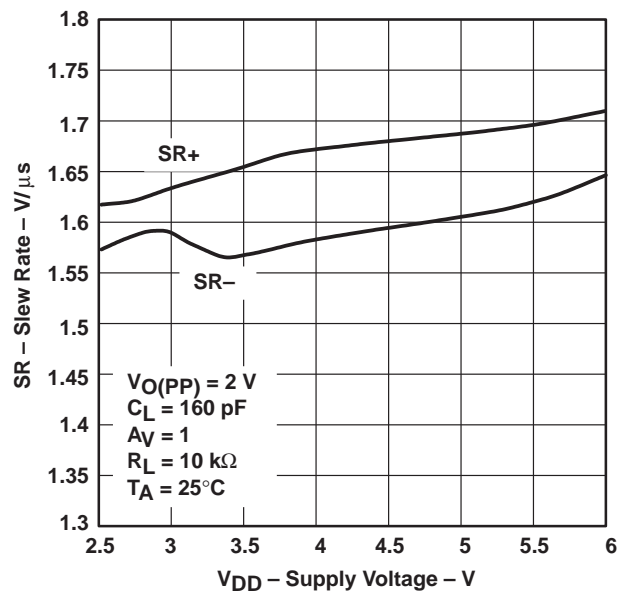


Figure 27

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

**EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY**

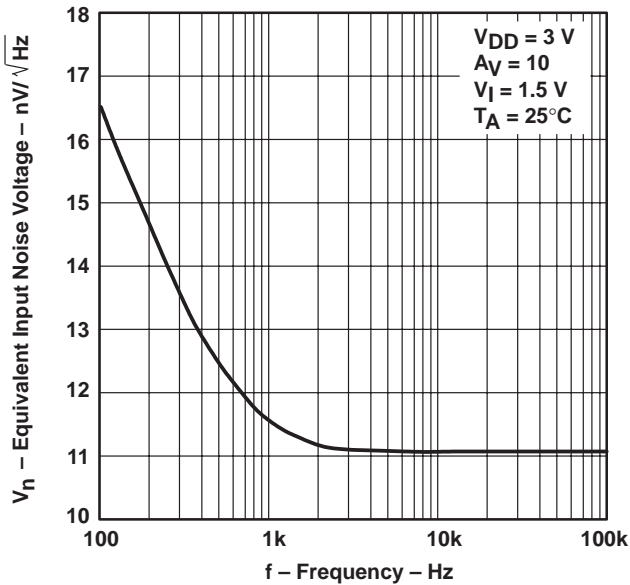


Figure 28

**EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY**

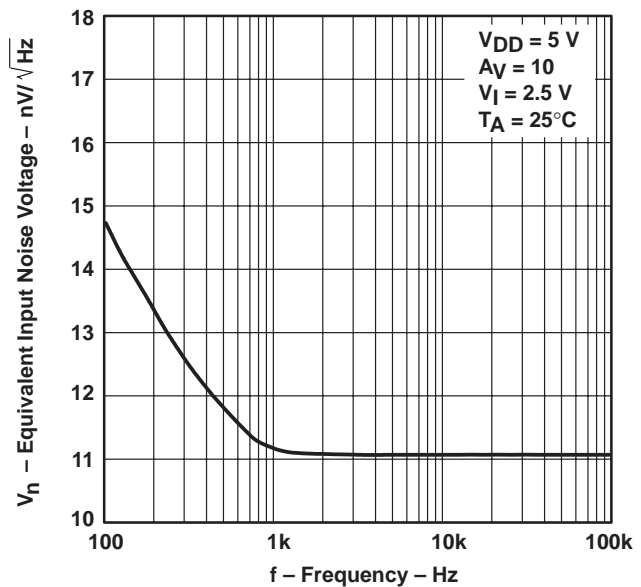


Figure 29

**EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

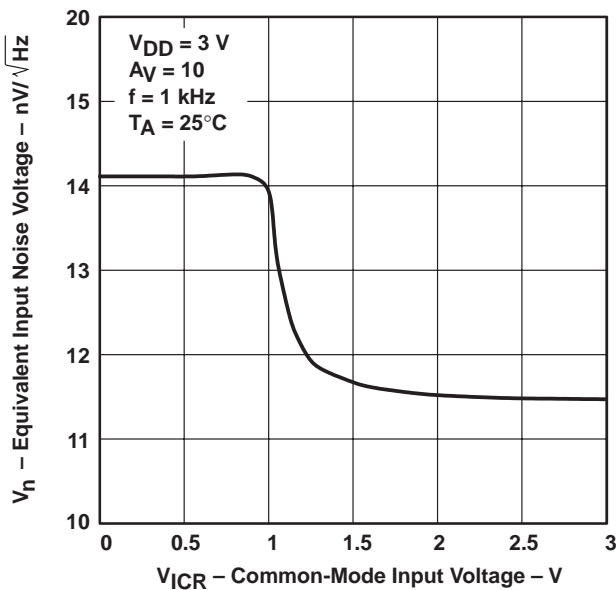


Figure 30

**EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

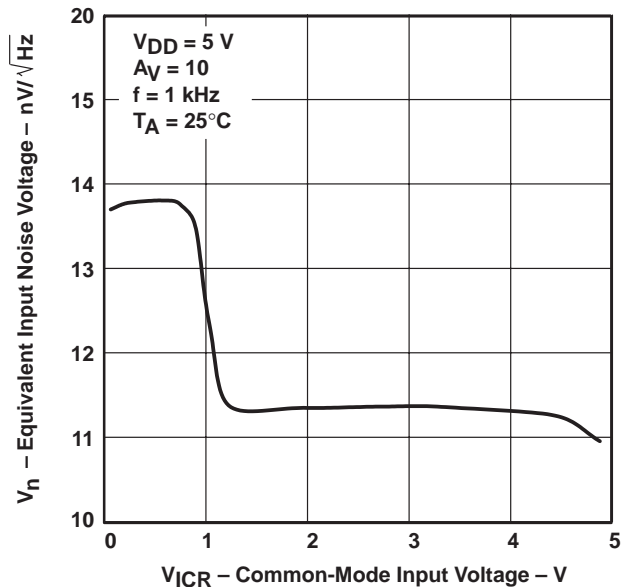


Figure 31

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

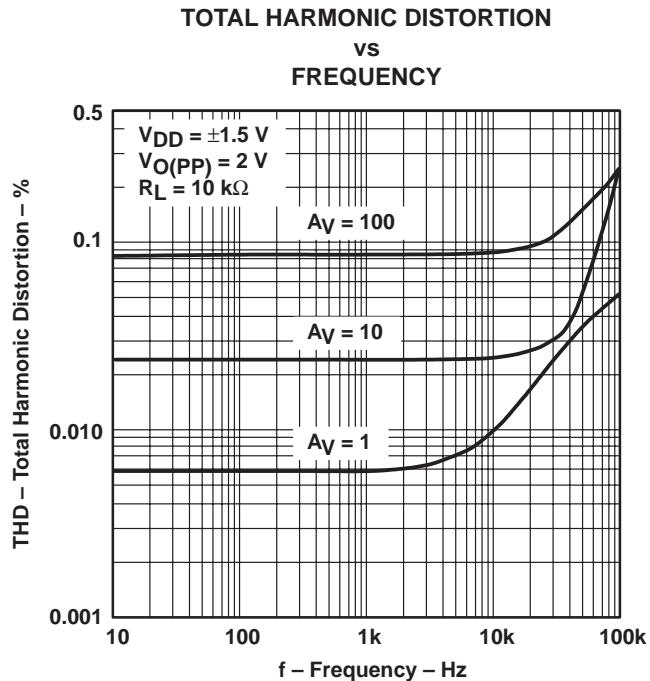


Figure 32

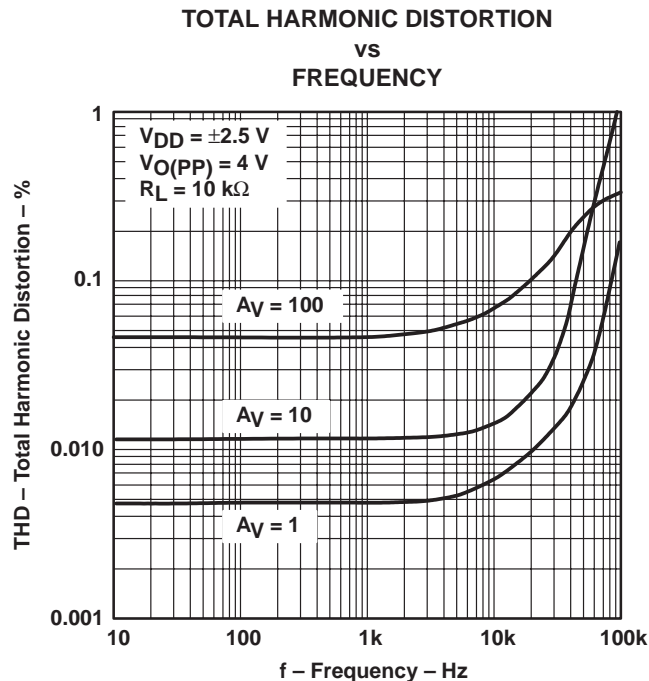


Figure 33

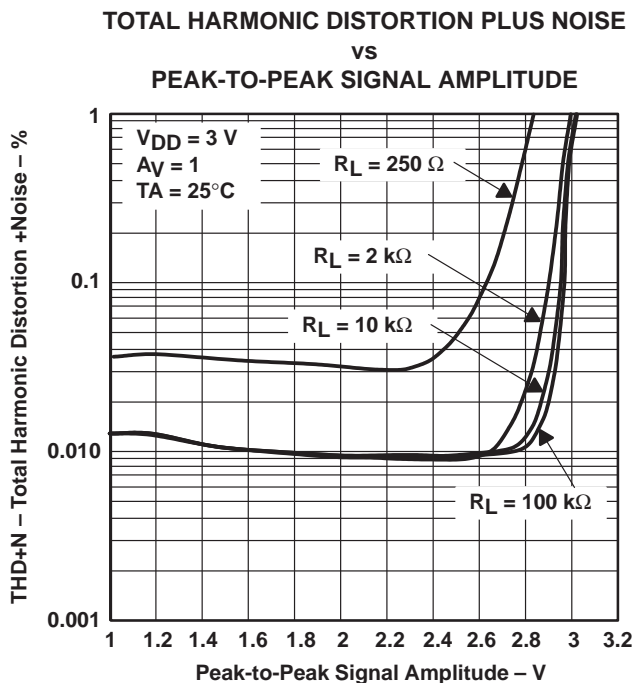


Figure 34

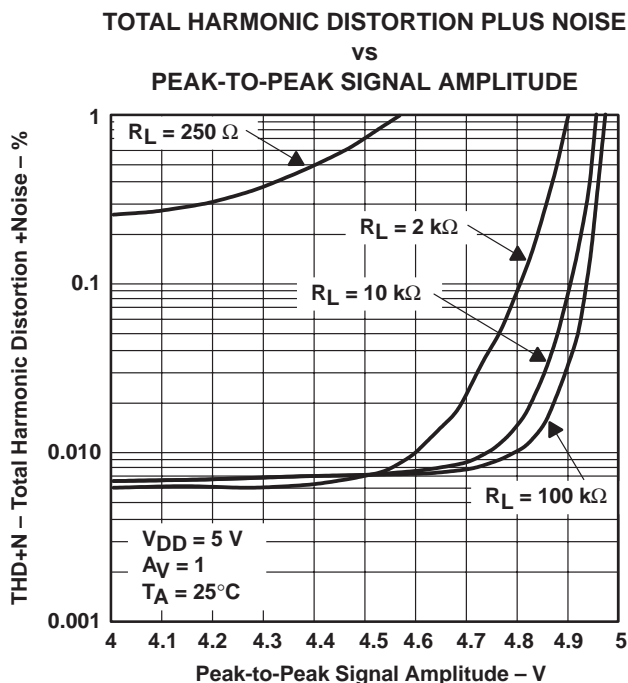


Figure 35

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

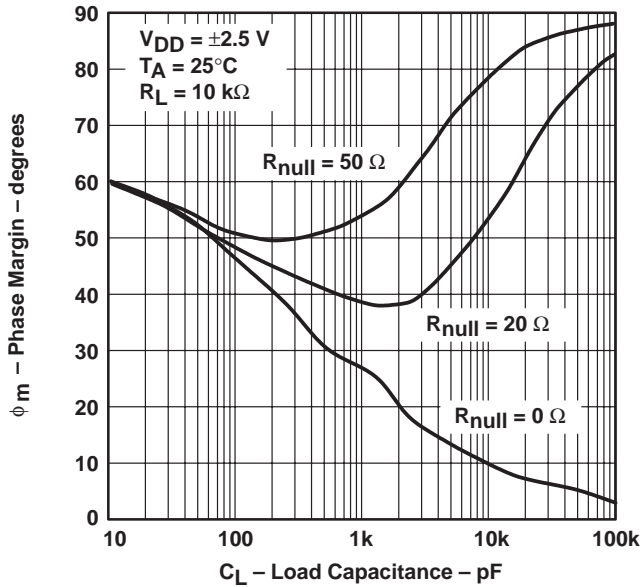


Figure 36

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

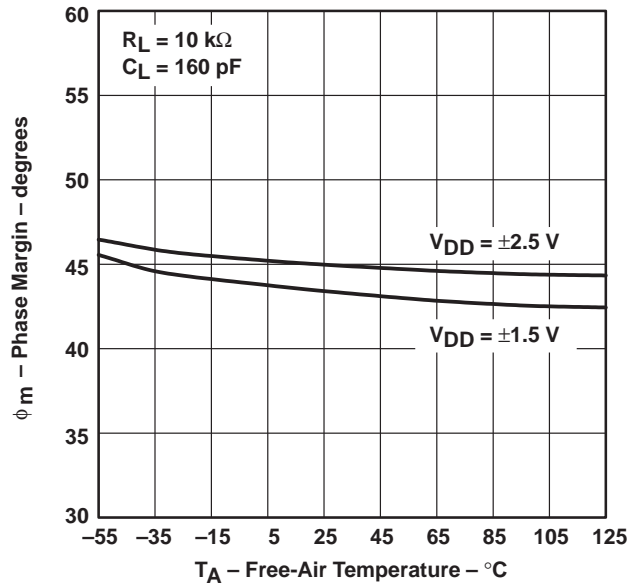


Figure 37

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

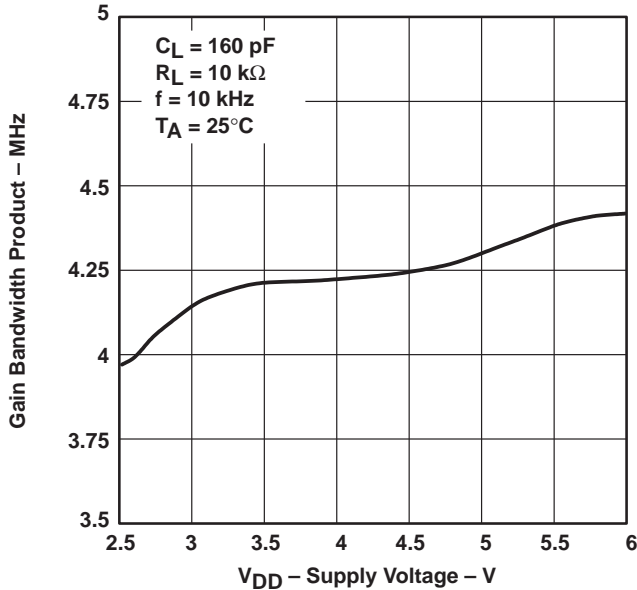


Figure 38

GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

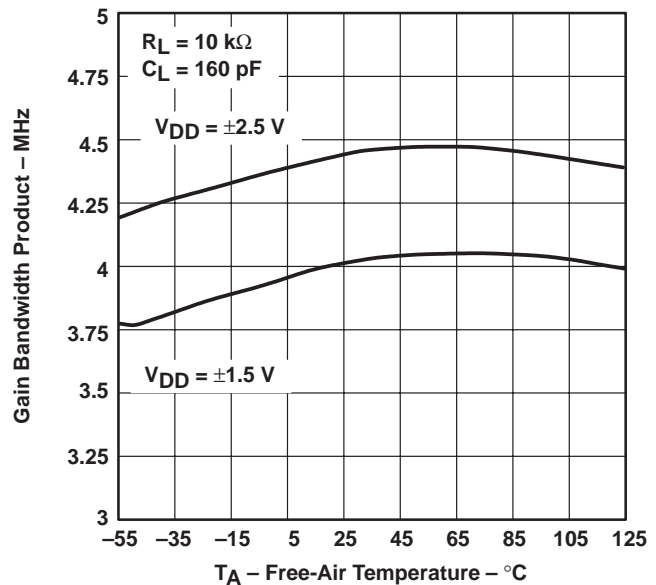


Figure 39

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS

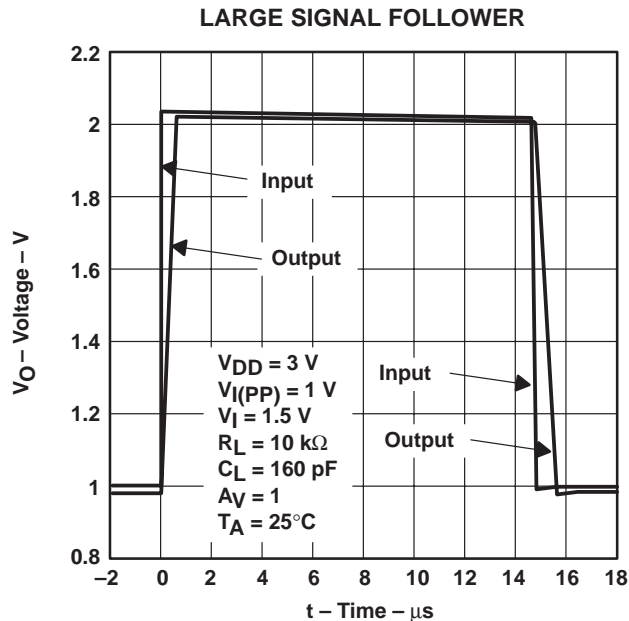


Figure 40

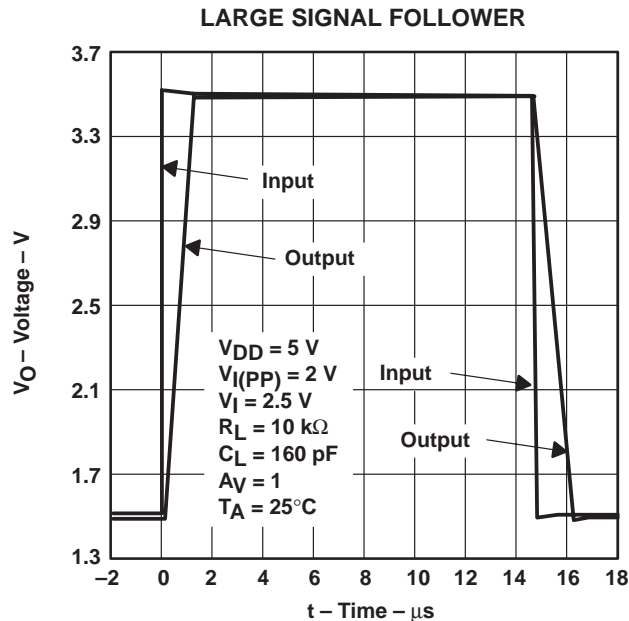


Figure 41

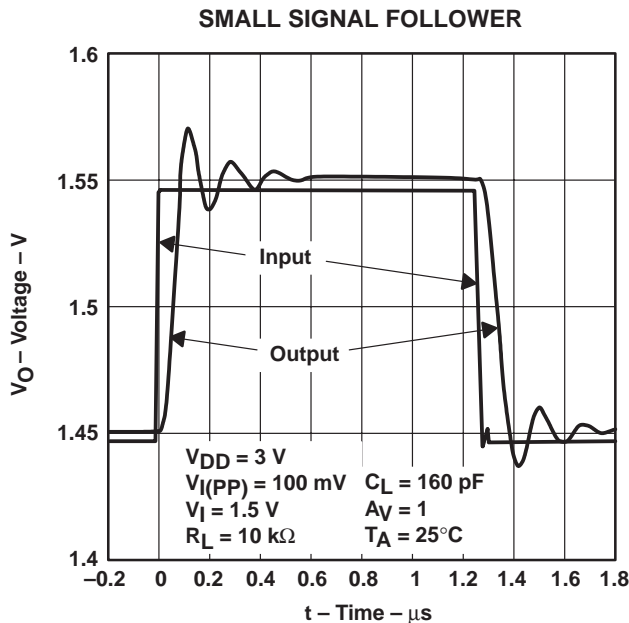


Figure 42

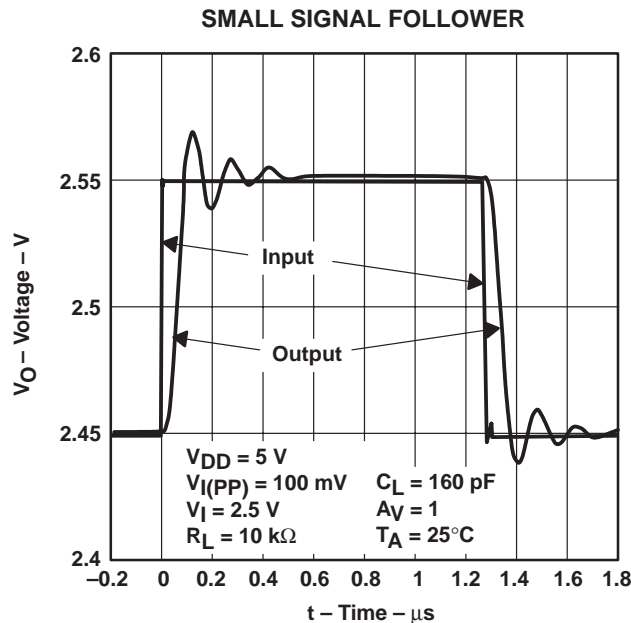
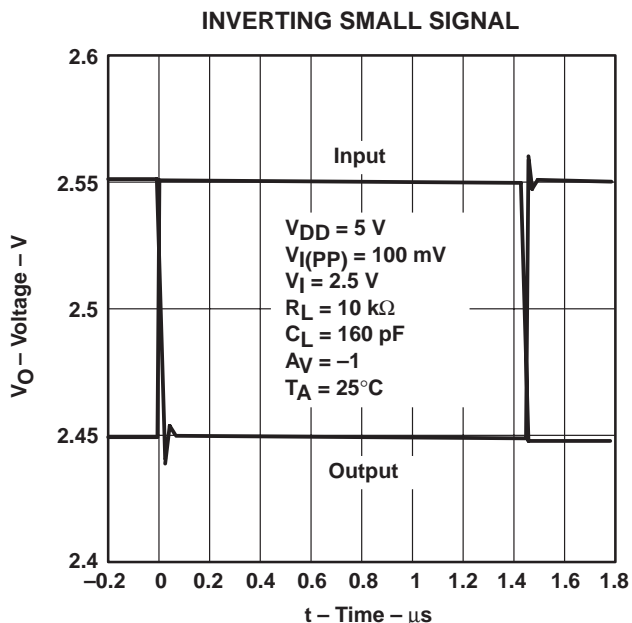
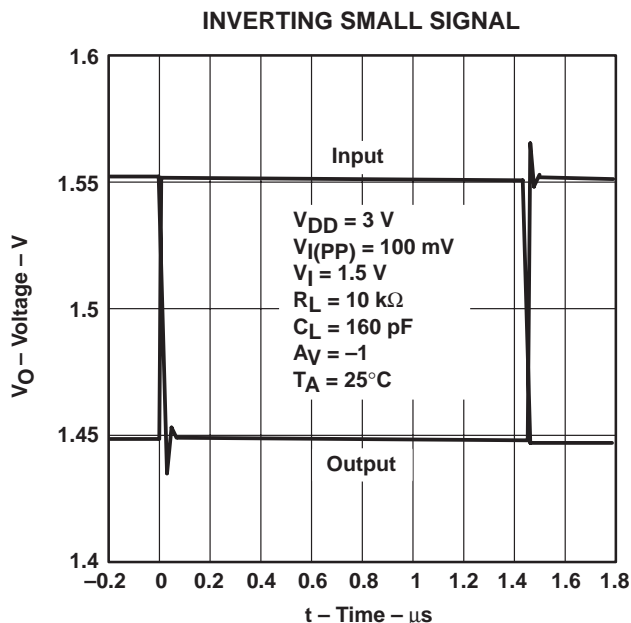
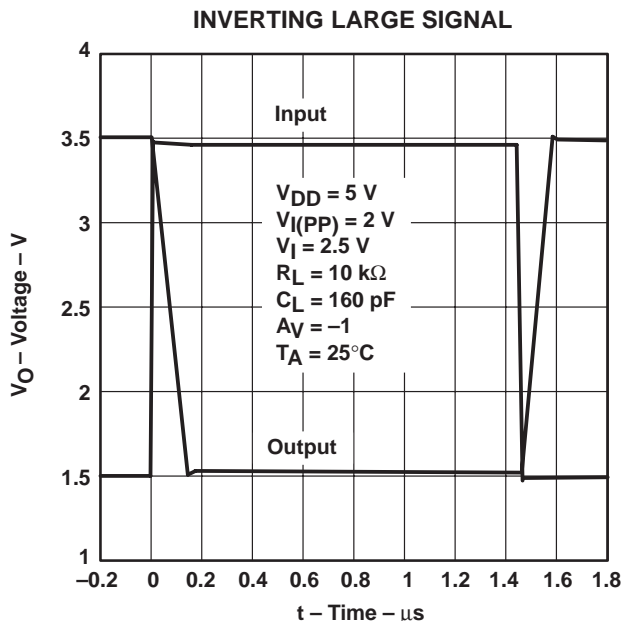
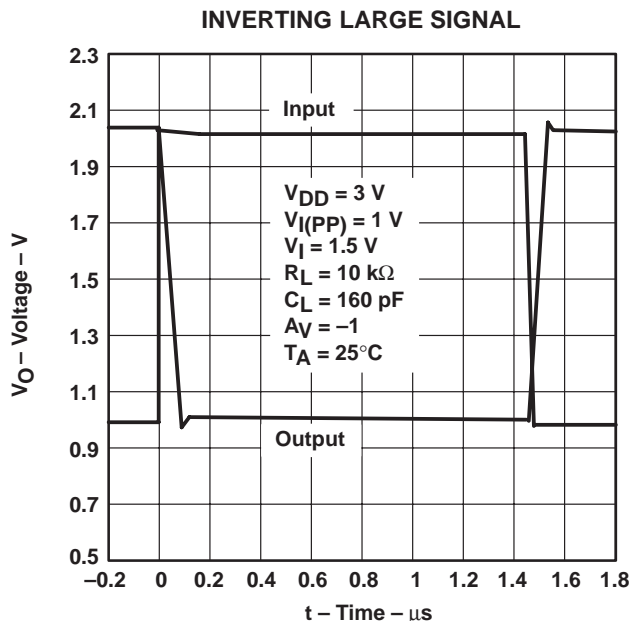


Figure 43

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
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TYPICAL CHARACTERISTICS



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PARAMETER MEASUREMENT INFORMATION

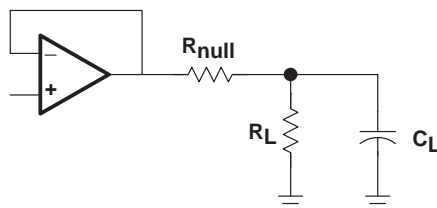


Figure 48

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

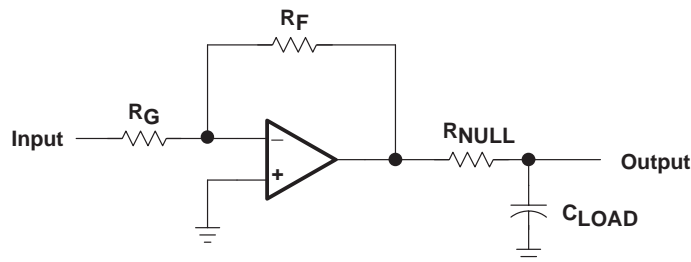


Figure 49. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

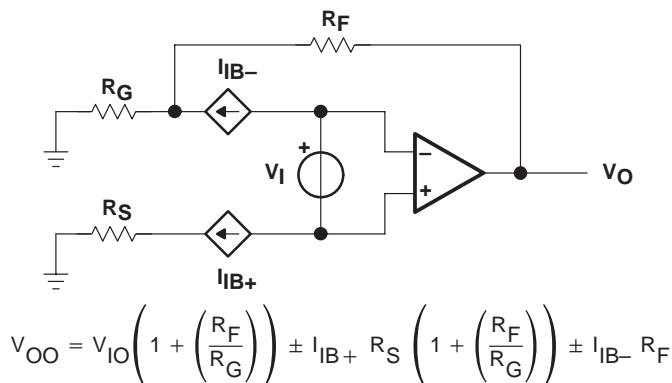


Figure 50. Output Offset Voltage Model

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APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

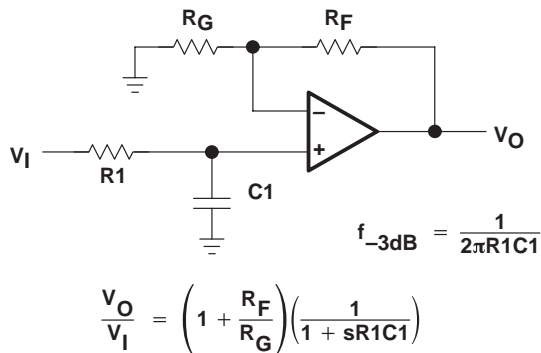


Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

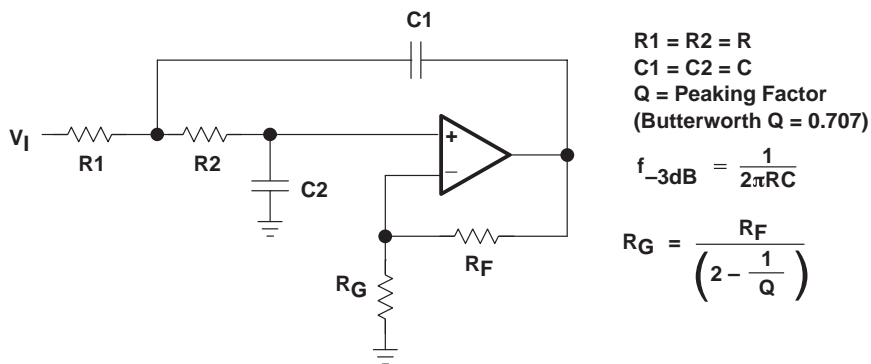


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

shutdown function

Three members of the TLV246x family (TLV2460/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 $\mu\text{A}/\text{channel}$, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{\text{DD}}/2$. Therefore, when operating the device with split supply voltages (e.g. $\pm 2.5\text{ V}$), the shutdown terminal needs to be pulled to $V_{\text{DD-}}$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

circuit layout considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS246x IC (watts)

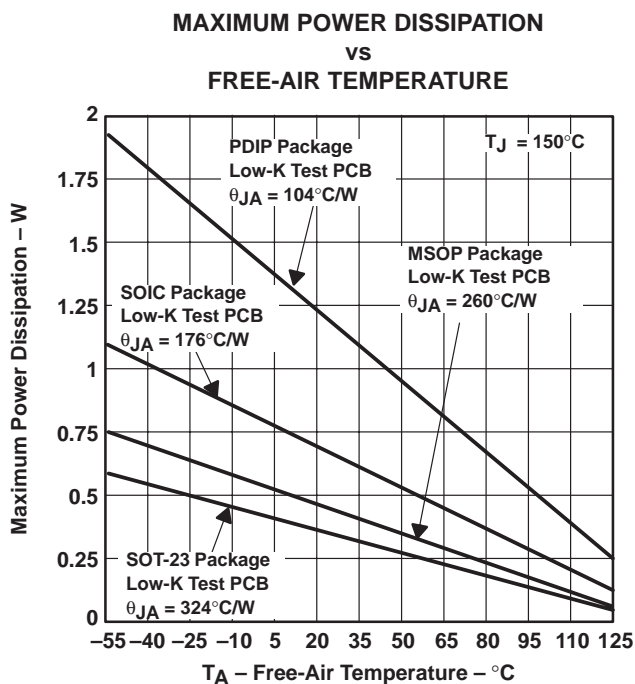
T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSPice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 54 are generated using the TLV246x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

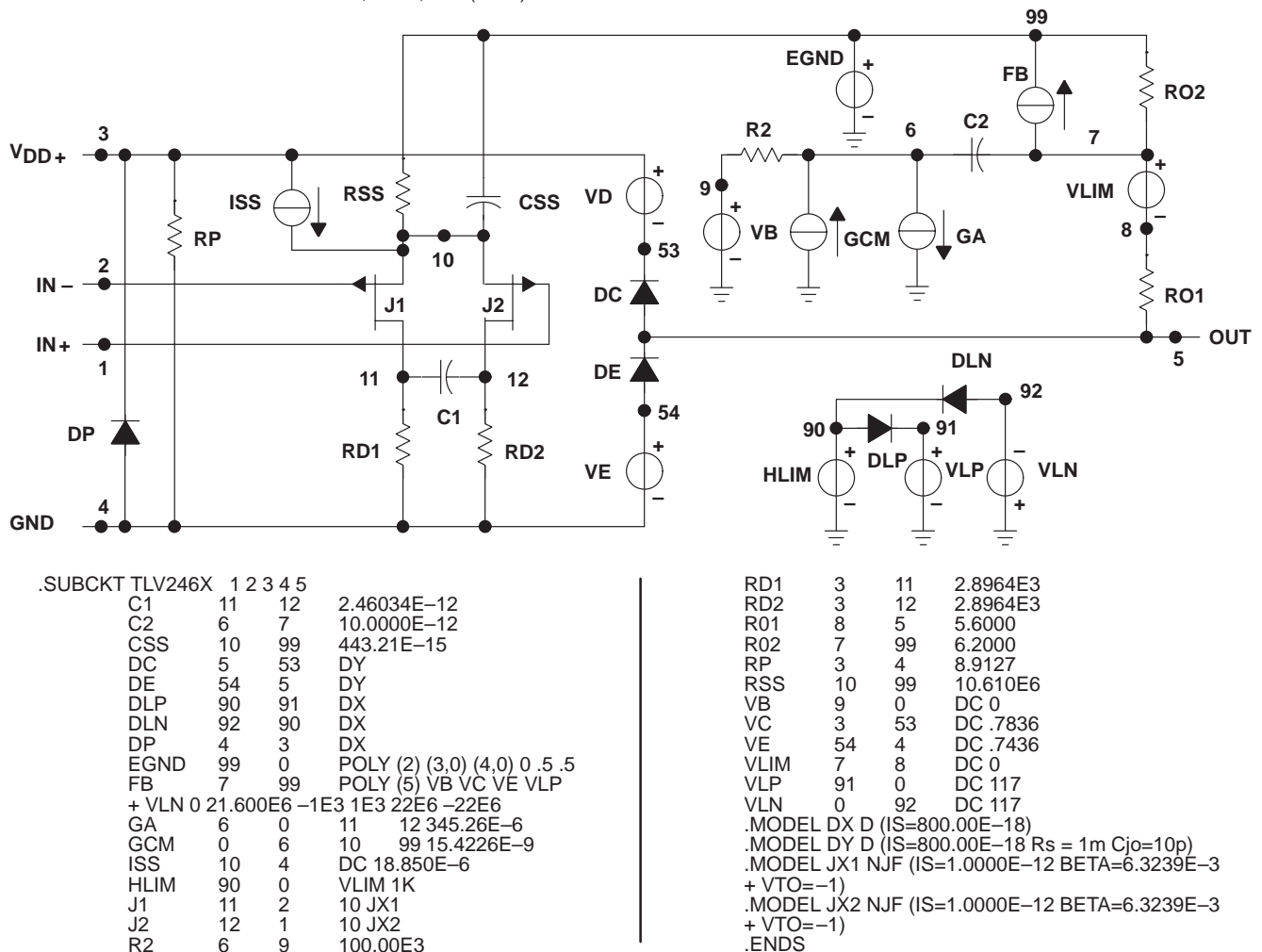


Figure 54. Boyle Macromodels and Subcircuit

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macromodel information (continued)

.subckt TLV_246Y 1 2 3 4 5 6	rp	3	71	8.9127
c1 11 12 2.4603E-12	rss	10	99	10.610E6
c2 72 7 10.000E-12	rs1	6	4	1G
css 10 99 443.21E-15	rs2	6	4	1G
dc 70 53 dy	rs3	6	4	1G
de 54 70 dy	rs4	6	4	1G
dlp 90 91 dx	s1	71	4	6 4 s1x
dln 92 90 dx	s2	70	5	6 4 s1x
dp 4 3 dx	s3	10	74	6 4 s1x
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5	s4	74	4	6 4 s2x
fb 7 99 poly(5) vb vc ve vlp vln 0	vb	9	0	dc 0
21.600E6 -1E3 1E3 22E6 -22E6	vc	3	53	dc .7836
ga 72 0 11 12 345.26E-6	ve	54	4	dc .7436
gcm 0 72 10 99 15.422E-9	vlim	7	8	dc 0
iss 74 4 dc 18.850E-6	vlp	91	0	dc 117
hlim 90 0 vlim 1K	vln	0	92	dc 117
j1 11 2 10 jx1	.model dx D(Is=800.00E-18)			
j2 12 1 10 jx2	.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)			
r2 72 9 100.00E3	.model jx1 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)			
rd1 3 11 2.8964E3	.model jx2 NJF(Is=1.0000E-12 Beta=6.3239E-3 Vto=-1)			
rd2 3 12 2.8964E3	.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)			
ro1 8 70 5.6000	.model s2x VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)			
ro2 7 99 6.2000	.ends			

Figure 54. Boyle Macromodels and Subcircuit (Continued)

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
 FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

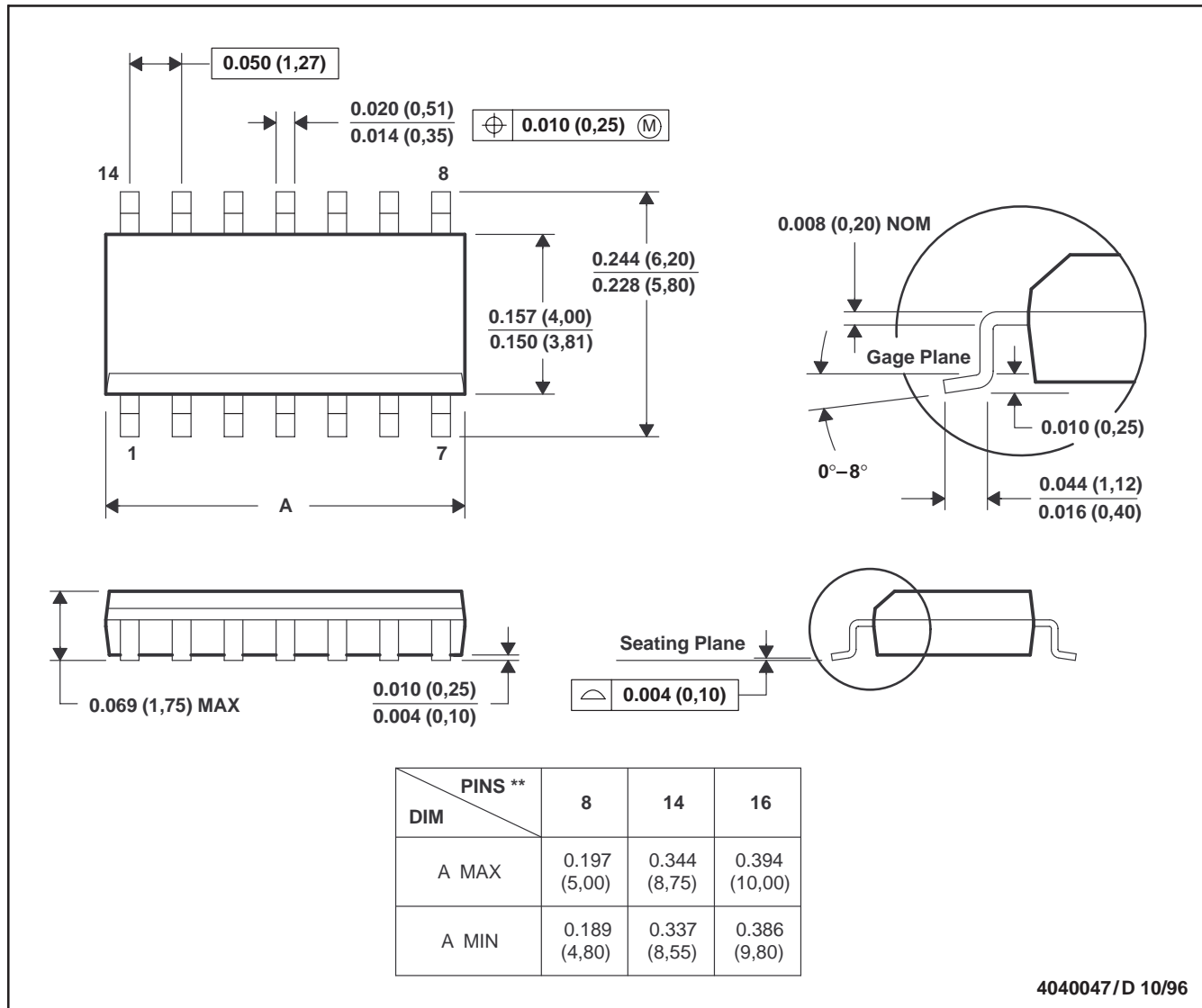
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: B. All linear dimensions are in inches (millimeters).
 C. This drawing is subject to change without notice.
 D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 E. Falls within JEDEC MS-012

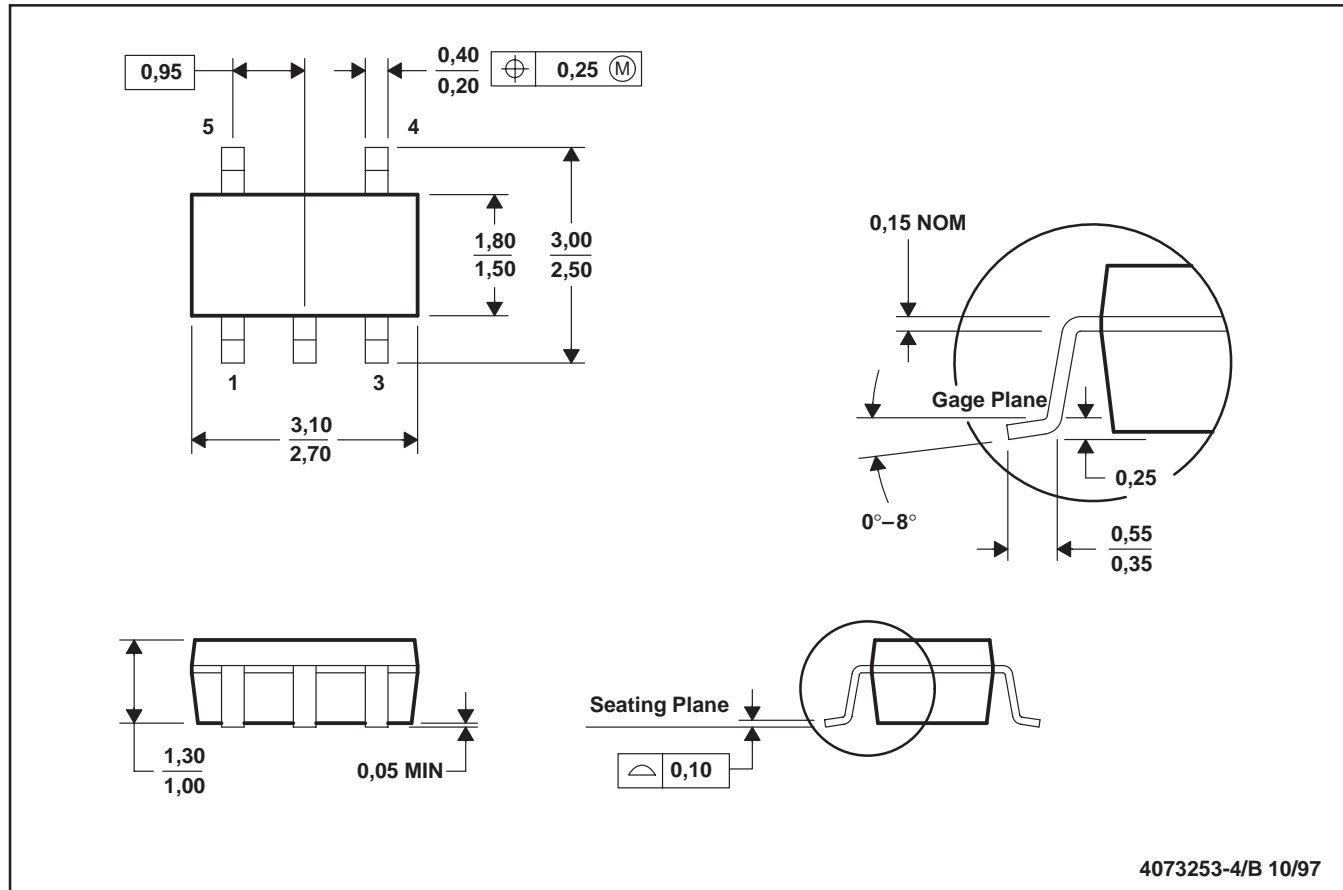
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/B 10/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

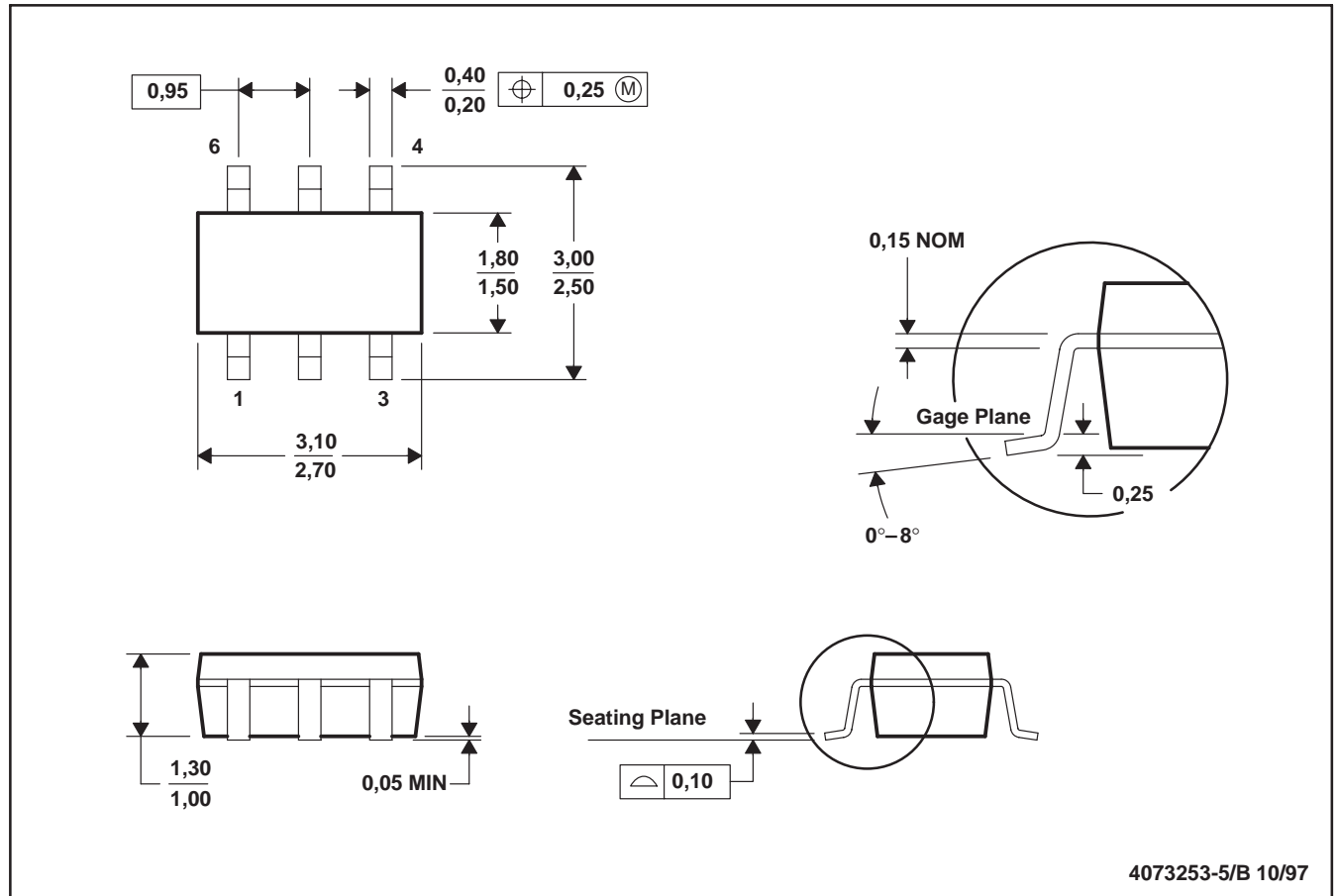
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
 FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/B 10/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

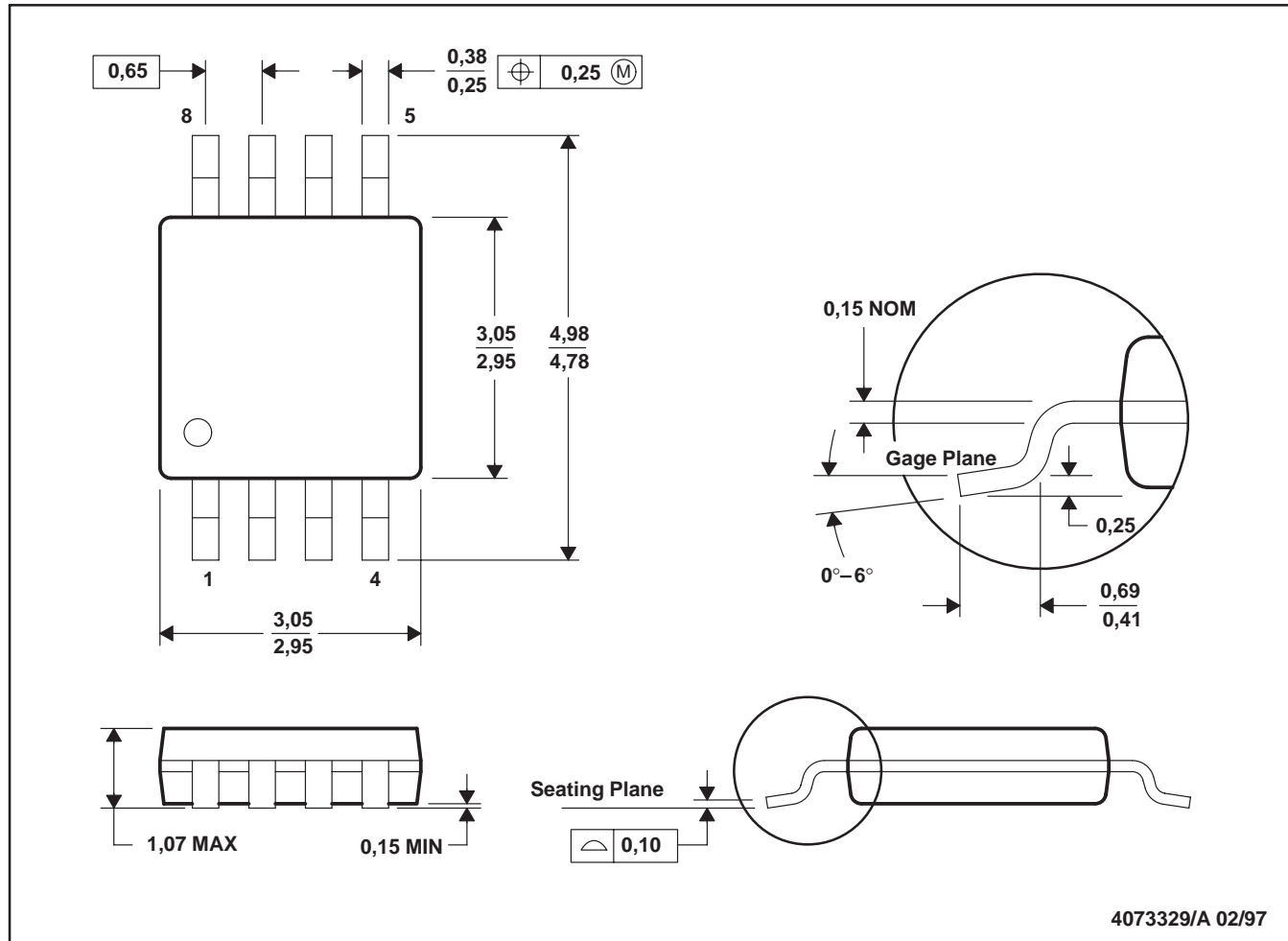
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-187

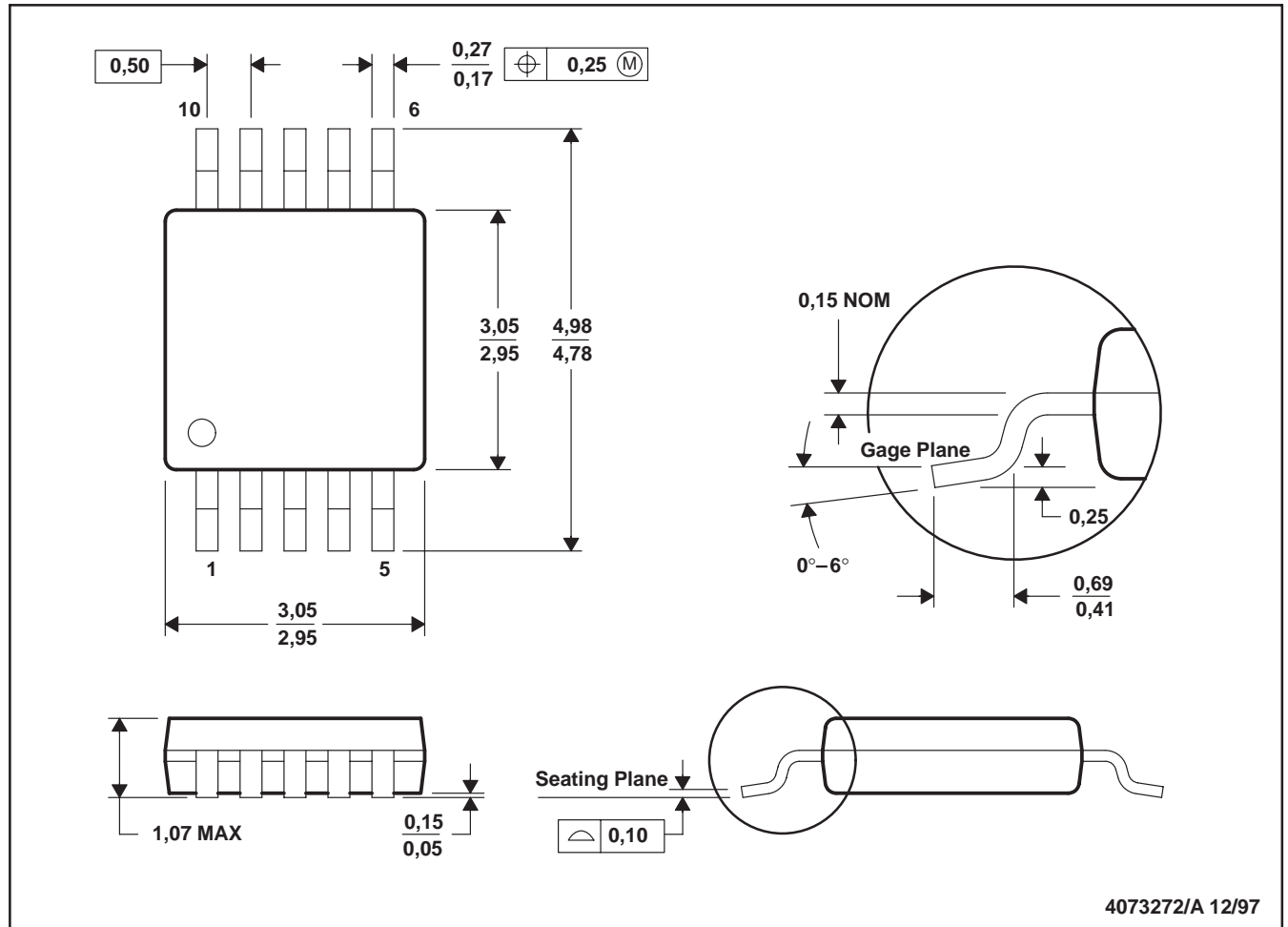
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
 FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



4073272/A 12/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

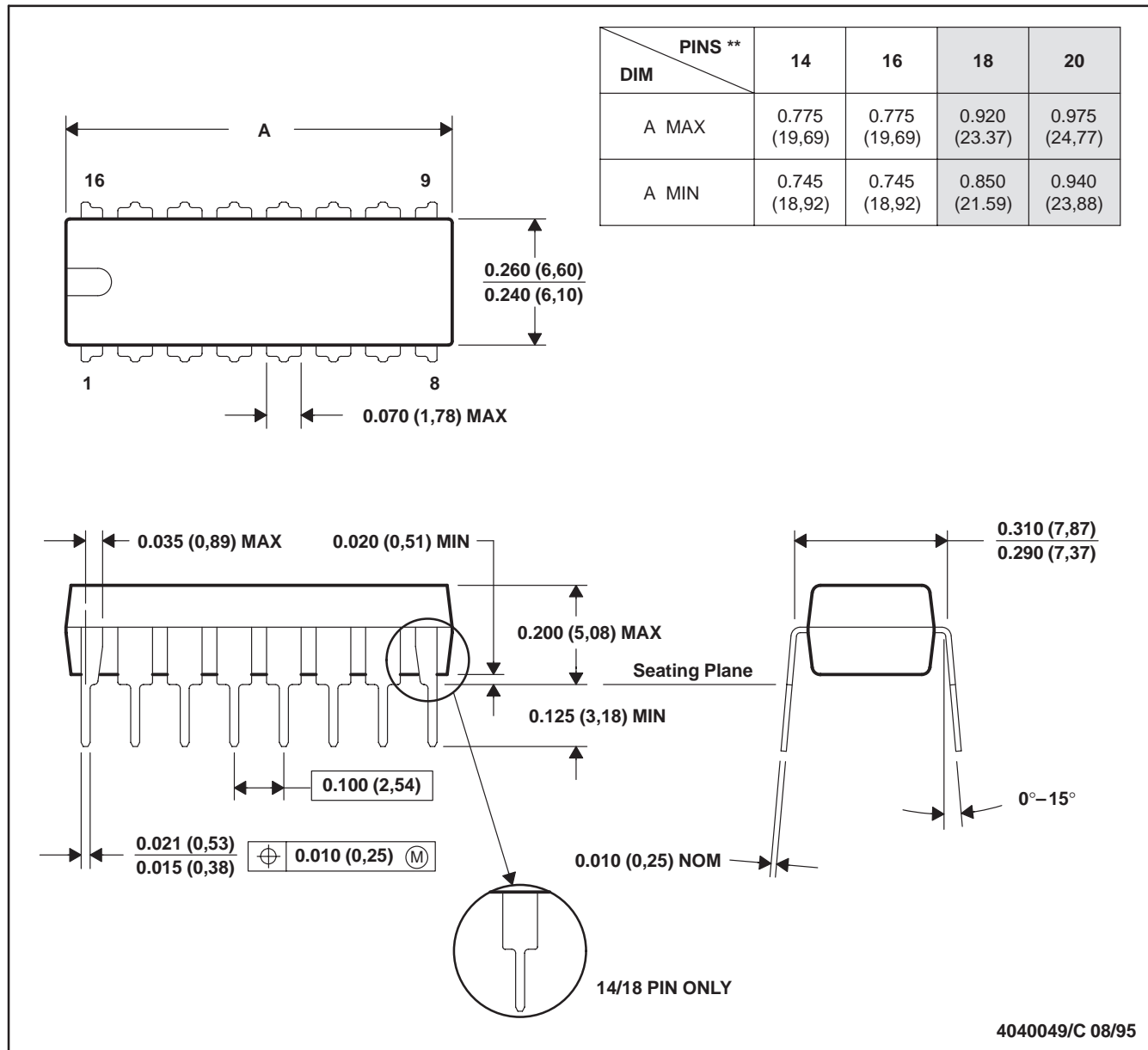
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MECHANICAL DATA

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



4040049/C 08/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

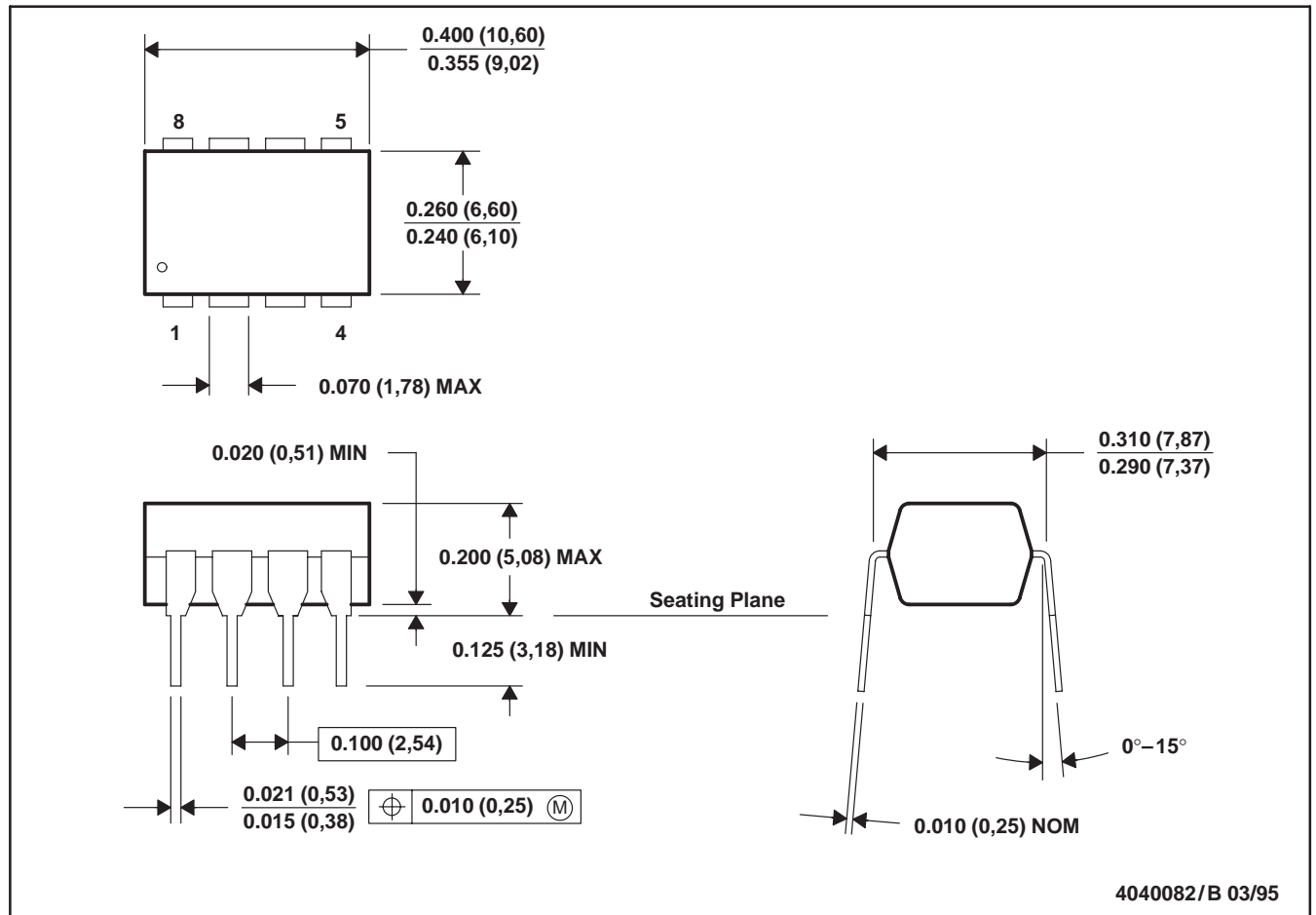
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
 FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
 OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

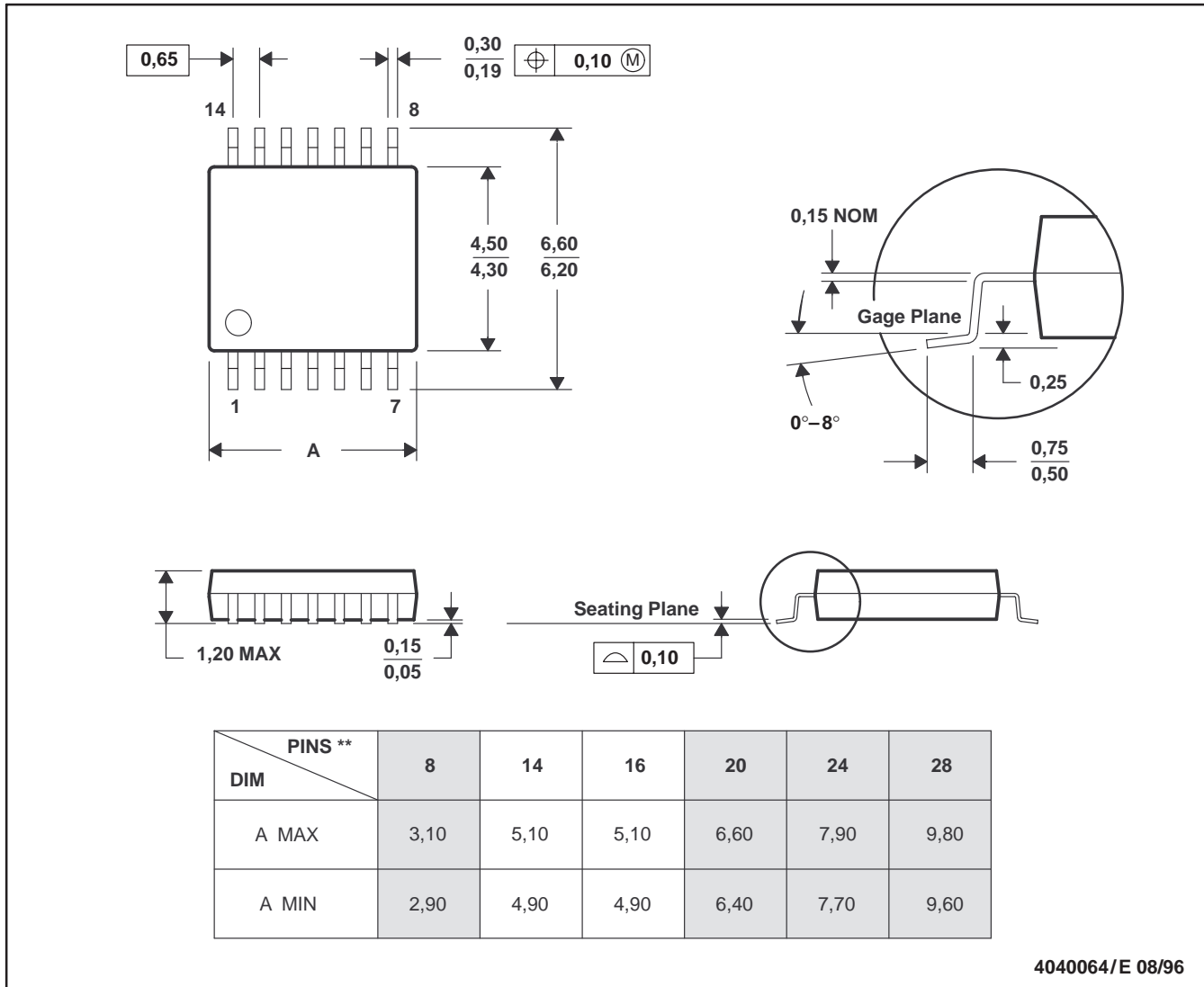
SLOS220F – JULY 1998 – REVISED OCTOBER 1999

MECHANICAL DATA

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/E 08/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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