# 3.3V CMOS 12-BIT TRI-PORT BUS EXCHANGER WITH 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCH16260A**

## FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range
- $V_{CC}$ = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

**Drive Features for LVCH16260A:**

- High Output Drivers: ±24mA
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

The LVCH16260A tri-port bus exchanger is built using advanced dual metal CMOS technology. The LVCH16260A is a high-speed 12-bit latched bus multiplexer/transceiver for use in high-speed microprocessor applications. This bus exchanger supports memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

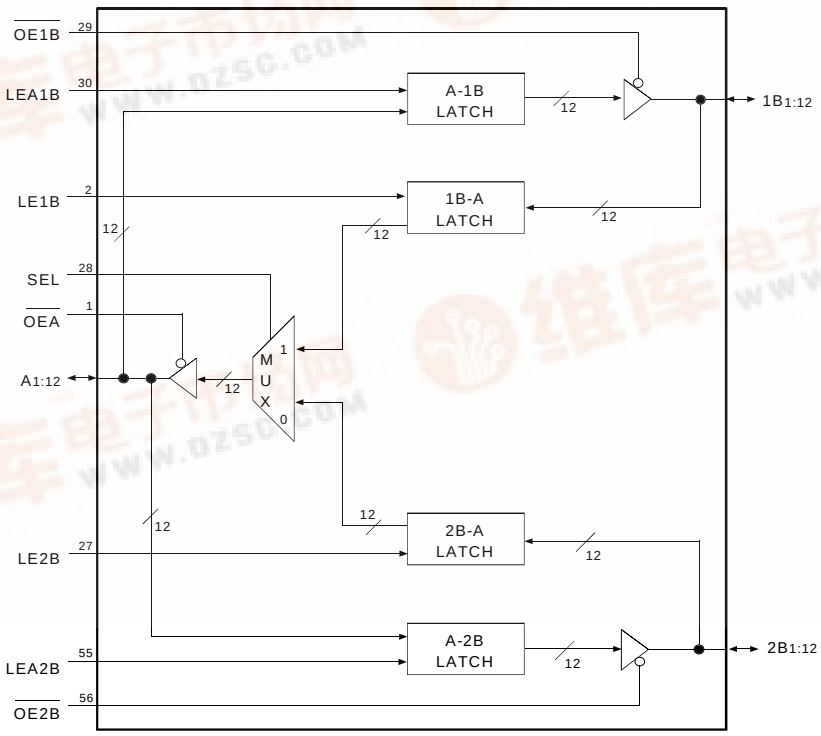
The LVCH16260A tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is high, the latch is transparent. When a latch-enable input is low, the data at the input is latched and remains latched until the latch enable input is returned high. Independent output enables ($\overline{OE1B}$ and $\overline{OE2B}$) allow reading from one port while writing to the other port.

All pins of the 12-bit Bus Exchanger can be driven from either 3.3V or 5V devices. This feature allows the use of the device as a translator in a mixed 3.3V/5V supply system.

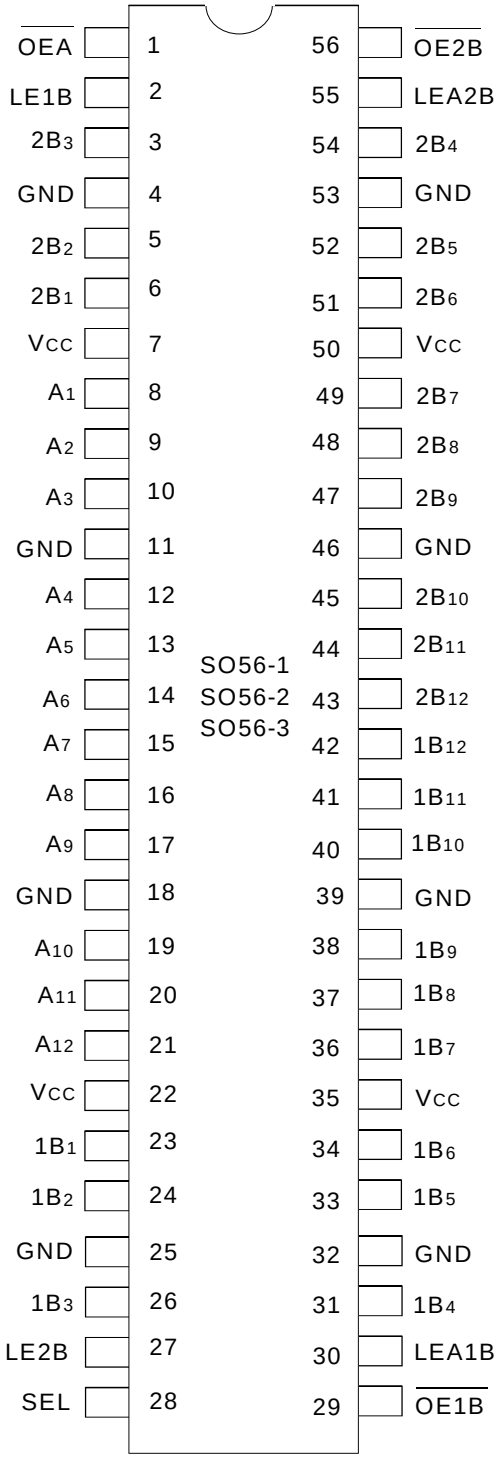
The LVCH16260A has been designed with a ±24mA output driver. The driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16260A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## Functional Block Diagram



## PIN CONFIGURATION




**SSOP/ TSSOP/ TVSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to +50 | mA |
| $I_{IK}$<br>$I_{OK}$ | Continuous Clamp Current,<br>$V_I < 0$ or $V_O < 0$ | – 50 | mA |
| $I_{CC}$<br>$I_{SS}$ | Continuous Current through<br>each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 6.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

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**NOTE:**
1. As applicable to the device type.

# FUNCTION TABLES (1)

| Inputs | | | | | | Outputs |
|---|---|---|---|---|---|---|
| 1Bx | 2Bx | SEL | LE1B | LE2B | $\overline{OEA}$ | Ax |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | $A_0$(2) |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | $A_0$(2) |
| X | X | X | X | X | H | Z |

**NOTES:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. $A_0$, $B_0$ = Output level before the indicated steady-state input conditions were established.

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| Ax | LEA1B | LEA2B | $\overline{OE1B}$ | $\overline{OE2B}$ | 1Bx | 2Bx |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | $B_0$(2) |
| L | H | L | L | L | L | $B_0$(2) |
| H | L | H | L | L | $B_0$(2) | H |
| L | L | H | L | L | $B_0$(2) | L |
| X | L | L | L | L | $B_0$(2) | $B_0$(2) |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

# PIN DESCRIPTION

| Signal | I/O | Description |
|---|---|---|
| A(1:12) | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.(1) |
| 1B(1:12) | I/O | Bidirectional Data Port 1B. Connected to the even path or even bank of memory.(1) |
| 2B(1:12) | I/O | Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.(1) |
| LEA1B | I | Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B. |
| LEA2B | I | Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA2B. |
| LE1B | I | Latch Enable Input for 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B. |
| LE2B | I | Latch Enable Input for 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B. |
| SEL | I | 1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port. |
| $\overline{OEA}$ | I | Output Enable for A Port (Active LOW). |
| $\overline{OE1B}$ | I | Output Enable for 1B Port (Active LOW). |
| $\overline{OE2B}$ | I | Output Enable for 2B Port (Active LOW). |

**NOTE:**
1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: TA = –40°C to +85°C**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$<br>$I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | High Impedance Output Current<br>(3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| $I_{CCZ}$ | | | $3.6 \leq V_{IN} \leq 5.5V$(2) | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V<br>other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

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**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

# BUS-HOLD CHARACTERISTICS

| Symbol | Parameter(1) | Test Conditions | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3.0V | $V_I$ = 2.0V | – 75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | — | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | — | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ± 500 | µA |
| $I_{BHLO}$ | | | | | | | |

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**NOTES:**
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = – 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

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**NOTE:**

1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to +85°C.

## OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance per bus exchanger Outputs enabled | $C_L$ = 0pF, f = 10Mhz | | pF |
| $C_{PD}$ | Power Dissipation Capacitance per bus exchanger Outputs disabled | | | pF |

## SWITCHING CHARACTERISTICS [1]

| Symbol | Parameter | Vcc = 2.7V±0.2V | | Vcc = 3.3V±0.3V | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_X$ to $1B_X$ or $A_X$ to $2B_X$ | 1.5 | 5.7 | 1.5 | 5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$1B_X$ to $A_X$ or $2B_X$ to $A_X$ | 1.5 | 6.1 | 1.5 | 5.2 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LE$_X$B to A$_X$ | 1.5 | 6.1 | 1.5 | 5.2 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LEA1B to $1B_X$ or LEA2B to $2B_X$ | 1.5 | 6.1 | 1.5 | 5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>SEL to A$_X$ | 1.5 | 6.3 | 1.5 | 5.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OEA}$ to A$_X$, $\overline{OE1B}$ to $1B_X$, or $\overline{OE2B}$ to $2B_X$ | 1.5 | 6.7 | 1.5 | 5.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>$\overline{OEA}$ to A$_X$, $\overline{OE1B}$ to $1B_X$, or $\overline{OE2B}$ to $2B_X$ | 1.5 | 5.9 | 1.5 | 5.2 | ns |
| $t_{SU}$ | Set-Up Time, HIGH or LOW Data to Latch | 1 | — | 1 | — | ns |
| $t_H$ | Hold Time, Latch to Data | 1.2 | — | 1 | — | ns |
| $t_W$ | Pulse Width, Latch HIGH | 3 | — | 3 | — | ns |
| $t_{SK(o)}$ | Output Skew [2] | — | — | — | 500 | ps |

**NOTES:**

1. See test circuits and waveforms. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$= 3.3V ±0.3V | $V_{CC}^{(1)}$ = 2.7V | $V_{CC}^{(2)}$= 2.5V ±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

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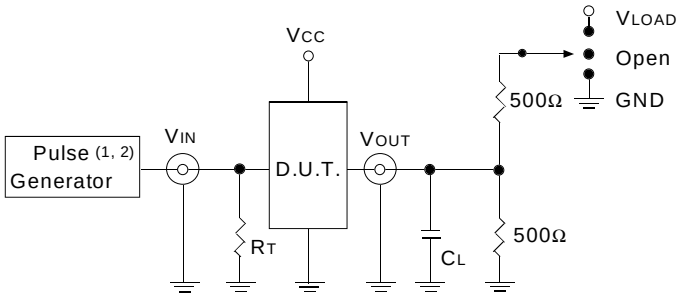
## TEST CIRCUITS FOR ALL OUTPUTS

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**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTE:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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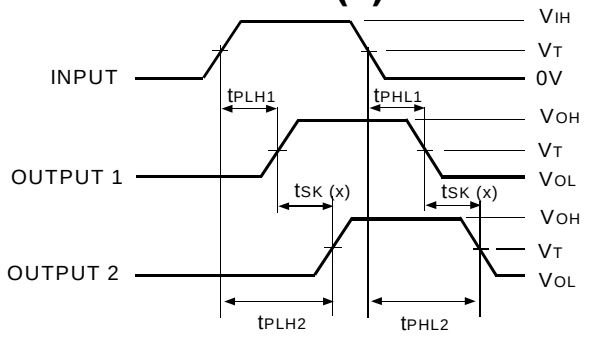
## OUTPUT SKEW - tsk (x)




$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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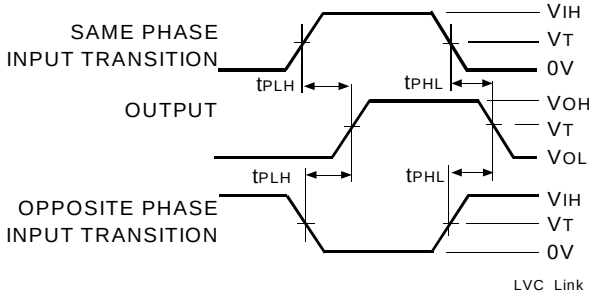
**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY

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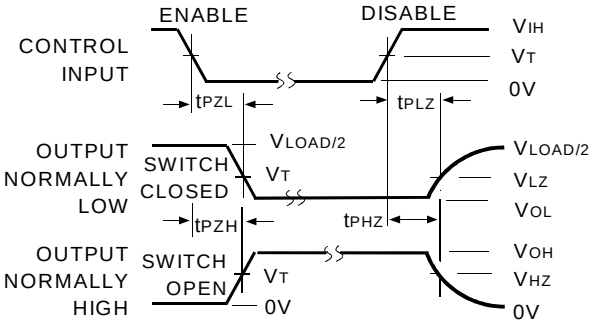
## ENABLE AND DISABLE TIMES

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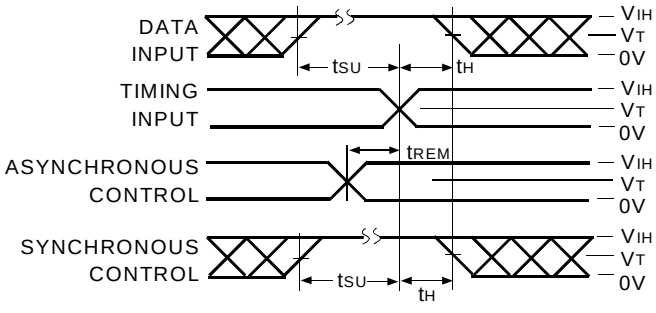
**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES

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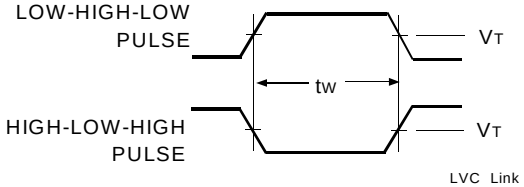
## PULSE WIDTH

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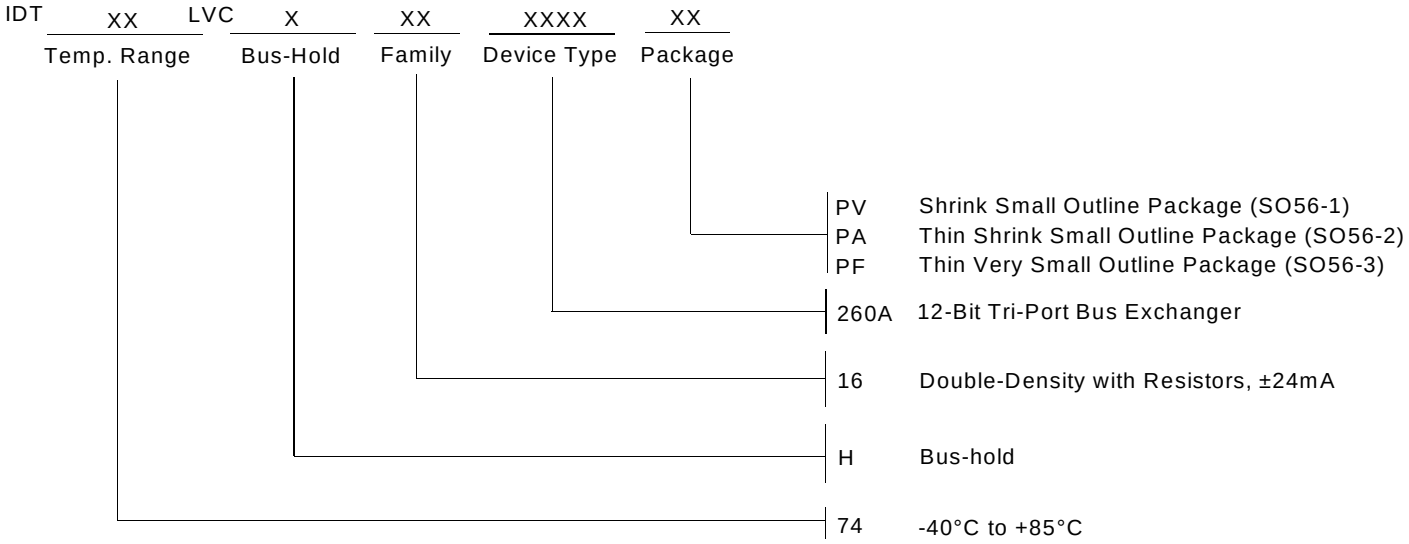
## ORDERING INFORMATION

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