TMPZ84C20AP-6 / TMPZ84C20AM-6 / TMPZ84C20AT-6
TMPZ84C20AP-8
TLCS-Z80 PIO : PARALLEL INPUT / OUTPUT CONTROLLER

1. GENERAL DESCRIPTION AND FEATURES

The TMPZ84C20A (hereinafter referred to as PIO) is CMOS version of Z80 PIO and has been designed to provide low power operation.

The PIO is a general purpose parallel input/output port device with two programmable independent 8-bit ports, which provides a direct interface between the Z80 microprocessor (hereinafter referred to as MPU) and peripheral devices.

This PIO provides excellent data transfer processing by the interrupt and allows the interrupt in Mode 2 of MPU.

The TMPZ84C20A is fabricated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the TMP84C20A are as follows.

(1) Compatible with the functions and pin connections of Zilog Z80 PIO.

(2) Low power consumption
3mA Typ. (@5V @6MHz) ··· TMPZ84C20AP-6/AM-6/AT-6
4mA Typ. (@5V @8MHz) ··· TMPZ84C20AP-8
10μA Max.(@5V, Stand-by)

(3) Operationg temperature
−40 °C to 85°C 6MHz VERSION
−10 °C to 70°C 8MHz VERSION

(4) DC to 6MHz operation ··· TMPZ84C20AP-6/AM-6/AT-6
DC to 8MHz operation ··· TMPZ84C20AP-8

(5) 2 programmable independent 8-bit input/output ports with handshake functions.

(6) 4 operation modes for each port:
Mode 0 (Byte Output Mode)
Mode 1 (Byte Input Mode)
Mode 3 (Byte Input/Output Mode) ..... Port A only
Mode 4 (Bit Mode)

(7) Built-in interrupt priority control circuit in daisy chain structure

(8) Port B outputs capable of driving Darlington transistors

(9) All input/output lines are TTL compatible.

(10) Single 5V power supply. Single-phase clock

(11) 40 pin DIP, SOP, 44pin PLCC Package.

Note : Z80 is a trademark of Zilog Inc., U.S.A.

2. PIN CONNECTIONS AND PIN FUNCTIONS

2.1 PIN CONNECTIONS (Top View)

The pin connections of the TMPZ84C20A are as shown in Figure 2.1, Figure 2.2.

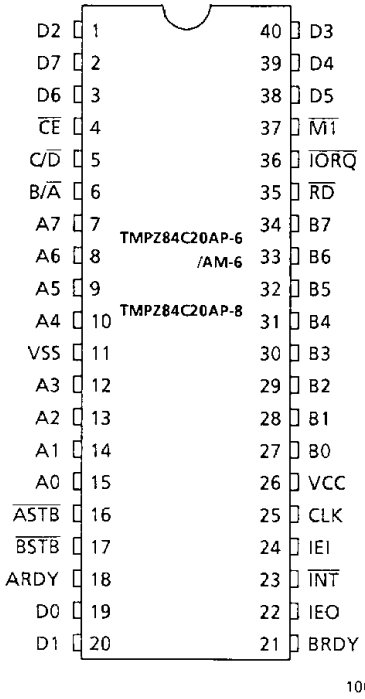

Figure 2.1 DIP, SOP Pin Connection

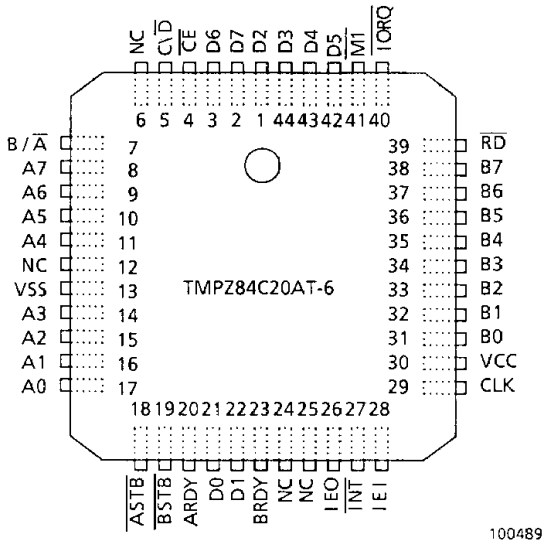

Figure 2.2 44-Pin PLCC Package

2.2 PIN NAMES AND FUNCTIONS

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions (1/3)

Pin Name	Number of Pin	Input/Output 3-state	Function
D0~D7	8	I/O 3-state	8-bit bidirectional data bus. Data transfer between MPU and PIO.
$\overline{CE}$	1	Input	Chip enable. Used for accessing MPU and PIO. When MPU selects this PIO, this terminal becomes L level (Refer to 3.4 Basic timing.) Normally, this terminal is connected to the address decoder output.
C/$\overline{D}$	1	Input	Control/data select. Indicates if signal on the data bus is control signal or data. Selects data at L level and command at H level. Normally, connected to address bit A1 of MPU.

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Table 2.1 Pin Names and Functions (2/3)

Pin Name	Number of Pin	Input/Output 3-state	Function
B/$\overline{A}$	1	Input	Port A/Port B select. Selects Port A at L level and Port B at H level. Normally, connected to address bit A0 of MPU.
A0~A7	8	I/O 3-state	Port A bus. Data transfer between Port A PIO and external device.
$\overline{ASTB}$	1	Input	Port A strobe input Handshake signal from the external device. Signal meaning differs depending upon operation mode. (Refer to 3.4 Basic timing.)
$\overline{BSTB}$	1	Input	Port B strobe input Handshake signal from the external device. Signal meaning is the same as $\overline{ASTB}$ but differs if Port A is in Mode 2. (Refer to 3.4 Basic timing.) Register A ready.
ARDY	1	Output	Port A ready. Handshake signal to the external device. Signal meaning differs depending upon operation mode. (Refer to 3.4 Basic timing.)
$\overline{M1}$	1	Input	Machine cycle 1. When both $\overline{M1}$ and $\overline{IORQ}$ are at L level, indicates that MPU is executing the interrupt acknowledge cycle. (Refer to 3.4 Basic timing.) Normally, connected to $\overline{M1}$ of MPU.
$\overline{IORQ}$	1	Input	I/O request. Used to access between MPU and PIO. This terminal becomes L level when I/O addresses are on the address in the write cycle and read cycle. Further, when $\overline{IORQ}$ and $\overline{M1}$ are both at L level, it indicates that MPU is executing the interrupt acknowredge cycle. (Refer to 3.4 Basic timing.) Normally, connected to $\overline{IORQ}$ of MPU.
$\overline{RD}$	1	Input	Read signal. Used to access between MPU and PIO. Controls the transfer direction. (Refer to 3.4 Basic timing) Normally, connected to $\overline{RD}$ of MPU.
B0~B7	8	I/O 3-state	Port B bus. Data transfer between Port B of PIO and external device. Capable of driving $-$ 1.5mA (@VoH = 1.5V) Darlington transistors.
CLK	1	Input	System clock. Signal-phase clock input. In DC state (either at H or L level), PIO is in a stand-by state and power consumption becomes extermely less.

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Table 2.1 Pin Names and Functions (3/3)

Pin name	Number of Pin	Input/Output 3-state	Function
IEI	1	Input	Interrupt enable input. Together with IEO and $\overline{INT}$, forms daisy chain interrupt control signal. Connected to IEO of high priority peripheral LSI. However, to give higher priority than other peripheral LSI's to this PIO, connect this terminal to the + 5V power. (Refer to 3.3.2 Interruption.)
$\overline{INT}$	1	Output	interrupt request. interrupt request signal for MPU. Connect to $\overline{INT}$ of MPU. (Open drain)
IEO	1	Output	Interrupt enable output. Together with IEI and $\overline{INT}$, forms daisy chain interrupt control signal. Connected to IEI or low prioirity peripheral LSI. However, if this PIO has the lowest priority than any other peripheral LSI's, this IEO is not used. (Refer to 3.3.2 Interruption.)
BRDY	1	Output	Port B ready Handshake signal to the external device. Signal meaning is the same as that of ARDY. However, it differs when Port A is in Mode 2. (Rerfer to 3.4 Basic timing.)
V_{CC}	1	Power supply	+ 5V
V_{SS}	1	Power supply	0V

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3. FUNCTIONAL DESCRIPTION

3.1 PIO BLOCK DIAGRAM

Figure 3.1 shows the PIO block diagram.

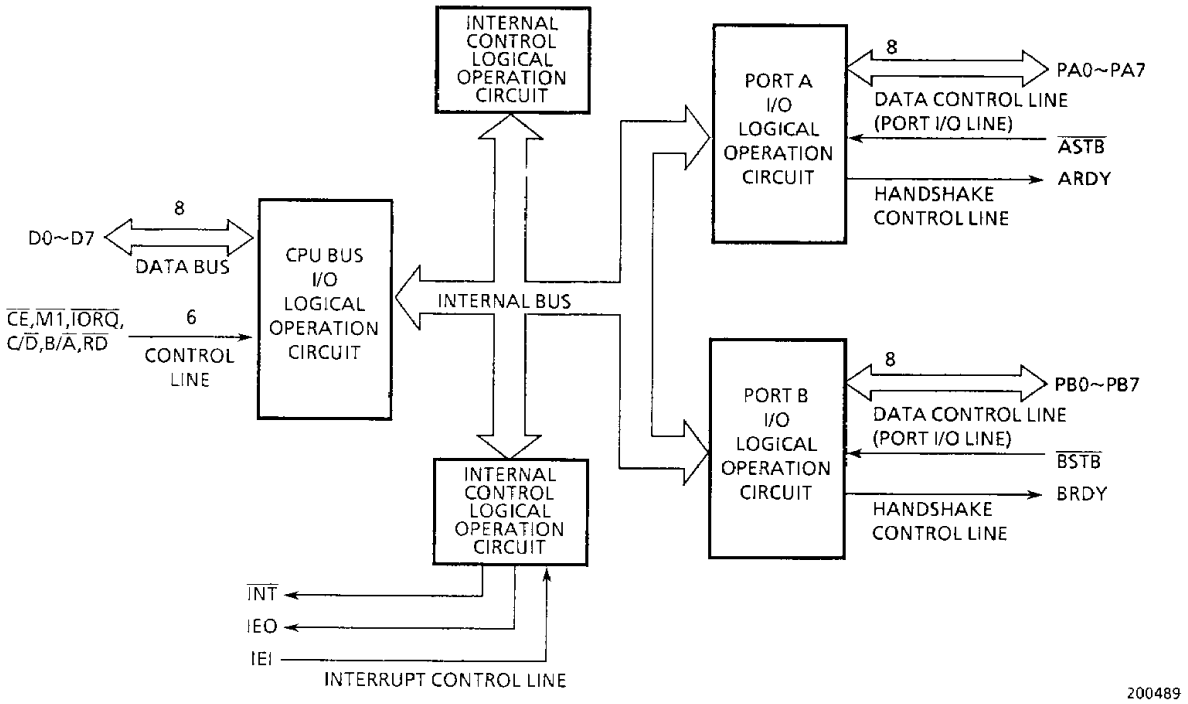


Figure 3.1 PIO Block Diagram

3.2 PIO SYSTEM CONFIGURATION

The PIO system consists of the four logic circuits:

(1) MPU bus I/O logic circuit

(2) Internal control logic circuit

(3) Interrupt control logic circuit

(4) Port I/O logic circuit

[1] MPU Bus I/O Logic Circuit

The MPU bus I/O logic circuit transfers data between the MPU and the PIO.

[2] Internal Control Logic Circuit

The internal control logic circuit controls the PIO operating functions like the PIO selecting chip enable and the read/write circuits.

[3] Interrupt Control Logic Circuit

The interrupt control logic circuit performs the MPU interrupt-associated processing such as determining interrupt priorities. The priorities with other LSI peripherals are determined by the physical location chain connection.

[4] Port I/O Logic Circuit

The port I/O logic circuits are used to directly connect to peripheral devices. Each consists of the following 7 registers and 1 flip-flop. Data are written in the registers by the MPU as specified in the program. Figure 3.2 shows the internal configuration of the ports.

- Data output register (8 bits)
- Data input register (8 bits)
- Mode control register (2 bits)
- Interrupt vector register (8 bits)
- Interrupt control register (2 bits)
- Mask control register (8 bits)
- Data I/O control register (8 bits)
- Handshake control logic circuit

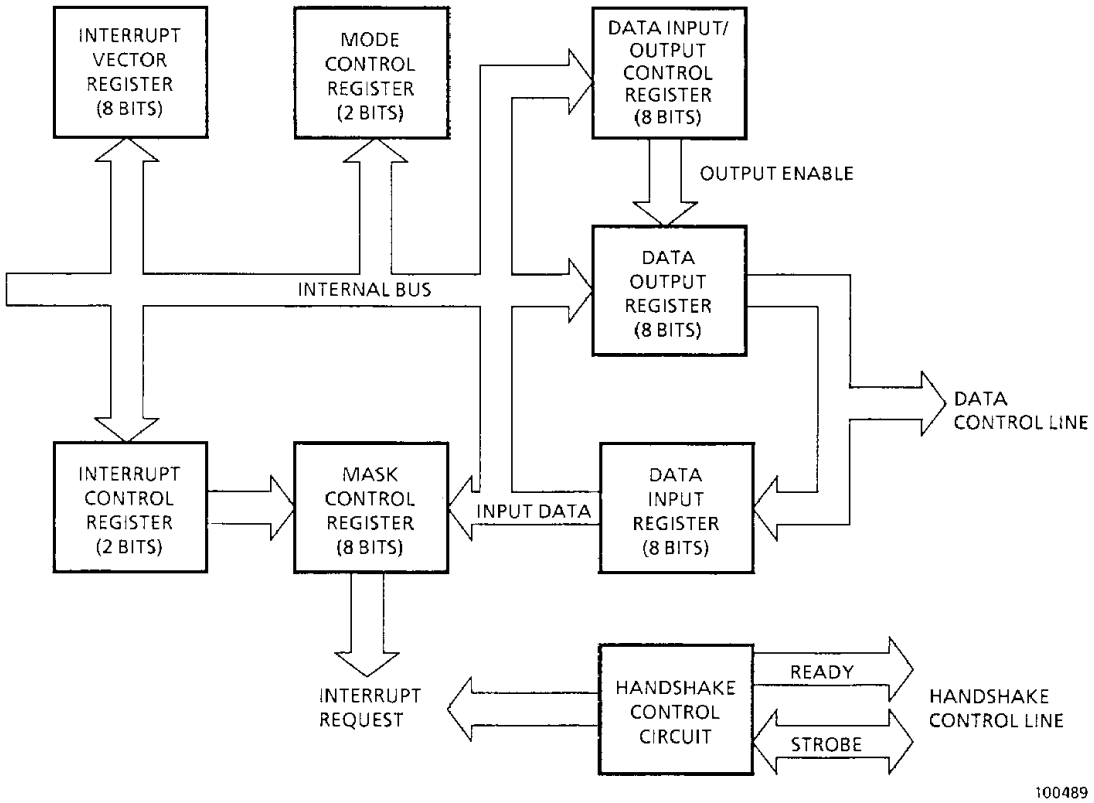


Figure 3.2 Port Internal Configuration

(1) Data Output Register

This register holds the data to be teansferred from the MPU to peripheral devices.

(2) Data Input Register

This register latches the data to be transferres from peripheral devices to the MPU.

The input data to the MPU is read through this register.

(3) Mode Control Register

This register specifies the operation mode. The operation mode is set by MPU control.

(4) Interrupt Vector Register

This register holds the vector which makes up the address of the table storing the start adress of the interrupt processing routine.

This register is used only for interrupt processing.

(5) Interrupt Control Register

This register specifies how the I/O ports are to be monitored. This register is used only in the PIO mode 3.

(6) Mask Control Register

This register specifies which I/O port pin is to be monitored. This register is used only in the PIO mode 3.

(7) Data I/O Control Register

This register specifies whether each port pin is to be used as output or input. This register is used only in PIO mode 3.

(8) Handshake Control Logic

This cirsuit controls the data transfer to the peripheral devices connected to the 8-bit I/O ports.

3.3 PIO BASIC OPERATIONS

[1] Reset

The PIO provides the following two reset capabilities:

When PIO is connected with the MPU (TMPZ84C00A, 01A, 02A) of Z80 series, or ASSP (TMPZ84C011A, 013A, 015A, 710A, 810A), it is necessary to connect with external logic as Figure 3.3.

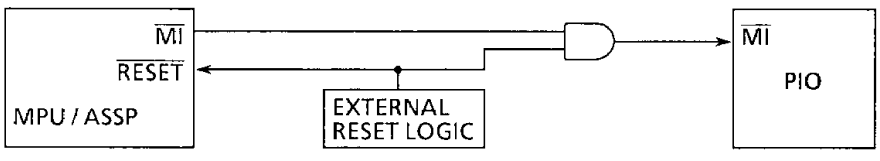


Figure 3.3 External Signal Reset Logic

(1) Power-on Reset

The PIO contains the circuit which automatically resets the PIO at the time of power-on.

(2) Hardware Reset

Making the $\overline{M1}$ pin low for 2 system clock periods with the $\overline{RD}$ and $\overline{IORQ}$ pins being high resets the PIO on the rising edge of the $\overline{M1}$ pin.

Reset State

(a) The operation mode is set to mode 1 for both ports.
(b) Interrupt is disabled.
(c) All the bits of the data I/O register of each port are reset.
(d) All the bits of the mask control register of each port are set and masked.
(e) The port I/O lines of each port are put in the high-impedance state (floating).
(f) The RDY pin of each port goes low.

The reset state is held until the control word is written. For the function of the control word, see Subsection 3.5 "Operational Procedure".

[2] Interrupt

The PIO can cause an interrupt when the MPU is operating in mode 2. The interrupt request signal ($\overline{INT}$) from the PIO is accepted when the MPU is in the inetrrupt enabled state (caused after the execution of EI instruction). Receiving the $\overline{INT}$ signal, the MPU latches the interrupt vector (8-bit data) sent from PIO, specifies the start address of the interrupt processing routine based on the vector, and calls the routine to start the processing.

Thus, since the start address of the interrupt processing routine can be specified by the interrupt vector sent from the PIO, the user can change the vector value to call any desired address.

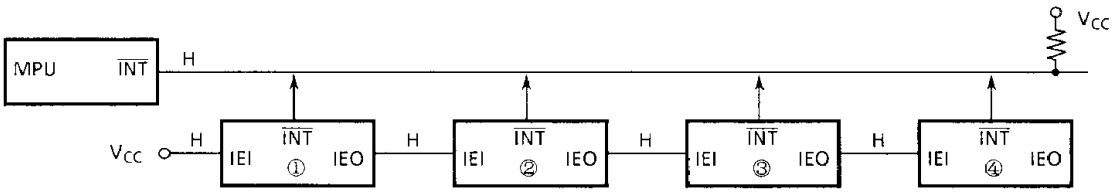
Interrupt processing is terminated when the MPU executes the RETI instruction. The PIO has the circuit to decode the RETI instruction to detect the termination of interrupt processing by constantly monitoring the data bus.

The interrupt priority among the Z80 peripharal LSIs is determined by the daisy chain structure. In daisy chain, the peripheral LSIs are connected one after another as shown in Figure 3.4. The more a peripheral LSIs is physically located near the MPU, the higher the priority of the peripheral is. Within the PIO, port A is given higher priority than port B. The Z80 peripheral LSIs have the signal lines IEO and IEI connected to the IEO of a higher peripheral LSIs and IEI of a lower peripheral LSI respectively. However, the IEI of the highest peripheral LSIs is connected to the IEI pin and the IEO of the lowest peripheral LSI is connected to the IEO pin. In this state, the PIO interrupt follows the conditions:

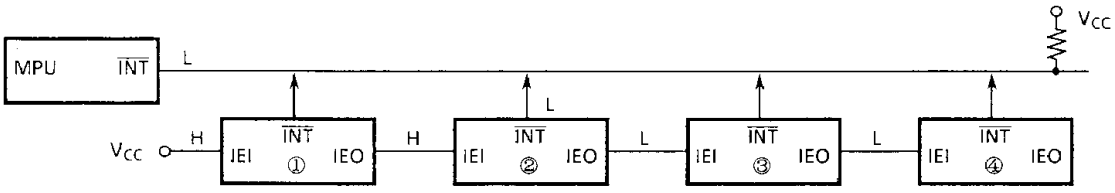
- When both IEI and IEO are high, no interrupt has occurred. This time, the interrupt request signal ($\overline{INT}$) is high. In this state, the PIO can request interrupt.
- When the PIO sends the $\overline{INT}$ signal, it sets the IEO line to the low level. When the interrupt request is accepted by the MPU, $\overline{INT}$ goes back to the low level.
- When the IEI goes low, the IEO also goes low.
- When the IEI is low, the PIO cannot request an interrupt.
- If the IEI goes low during interrupt occurrence, the interrupt processing is suspended.

The operations of the four Z80 peripheral LSIs (the states of IEI, IEO and $\overline{INT}$ signal) daisy-chained as shown in Figure 3.4 are as follows:

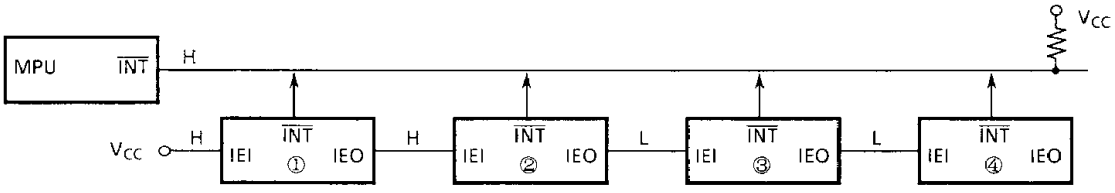
(1) Before interrupt occurrence



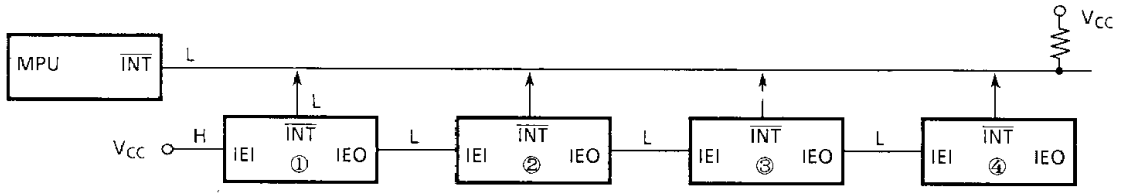
(2) Interrupt request from LSI-2 to the MPU



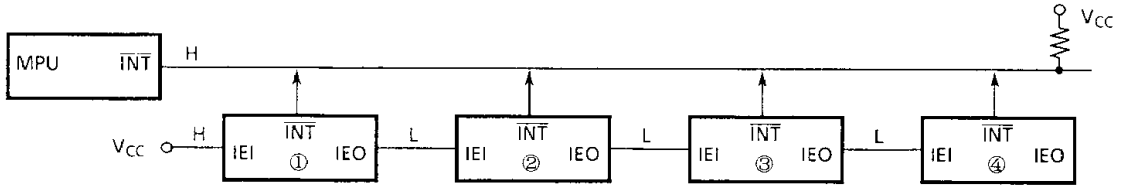
(3) The MPU acknowledges (enables) the interrupt. Interrupt processing for LSI-2 is performed.



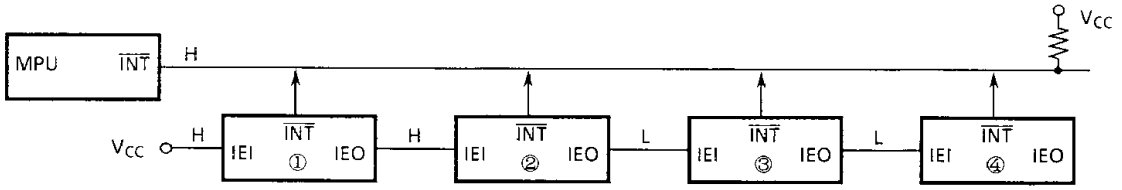
(4) Interrupt request from LSI-1 to the MPU. The interrupt processing for LSI-2 is suspended.



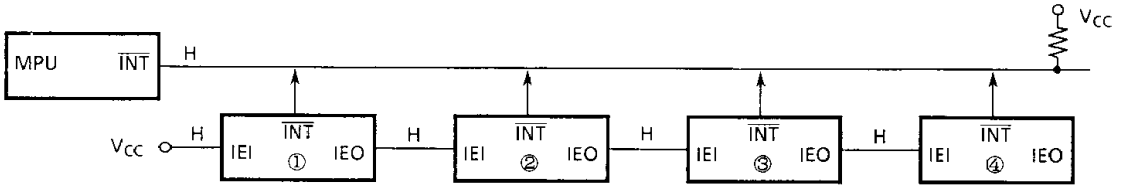
(5) The MPU acknowledges (enables) the interrupt. Interrupt processing for LSI-1 is performed.



(6) Interrupt processing for LSI-1 terminates (upon execution of the RETI instruction). Interrupt processing for LSI-2 is restarted.



(7) Interrupt processing for LSI-2 terminates (upon execution of the RETI instruction).



Interrupt priority is given to LSI-1, LSI-2, LSI-3 and LSI-4 in this order.

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Figure 3.4 Signal States in Daisy Chain Structure

[3] Operation Modes

The PIO operates in one of the 4 operation modes. The mode is selected by writing the mode control word.

- Mode 0 (byte output mode)
- Mode 1 (byte input mode)
- Mode 2 (byte I/O mode)
- Mode 3 (bite mode)

(1) Mode 0 (byte output mode)

In mode 0, the PIO sends the data received from the MPU to the external device through the port data output register. The contents of this register can be rewritten by using an output instruction. If the data on the bus change, the register contents remain unchanged until the next output instruction is executed. When the MPU executes an output instruction, the write signal is generated in the PIO in the write cycle. Using the signal, data on the data bus can be latched in the data output register.

(2) Mode 1 (byte input mode)

In this mode, the PIO sends the data received from the external device to the MPU through the port data input register. The data transfer to the MPU is suspended until the MPU has read the current data.

(3) Mode 2 (byte I/O mode)

Mode 2 is a combination of mode 0 and mode 1. This mode is used only for port A. In this mode, all 4 handshake control lines are used. Port A's handshake control lines are used for data output and the port B's handshake control lines are used for data input. For data transfer, port A is used. Port B is set in mode 3 (bit mode) in which no handshake control line is used.

In this mode, the interrupt timing occurs almost at the same time in mode 0 and mode 1. In an input operation, the port B's handshake control lines are used, so that the interrupt vetor written in port B is transferred. Therefore, the interrupts in input and output can be controlled by different vectors.

(4) Mode 3 (bit mode)

In mode 3, the 8-bit port I/O lines are controlled for each bit. Since no handshake control lines are used, ordinaly read/write operations can be performed. I/O operations can be performed on the port as well. In a write operation, the data sent from the MPU to the PIO are latched in the data output register corresponding to the bit set for output in the same timing as in mode 0.

An interrupt occurs in the interrupt enabled state and when the bit set for input satisfies the condition specified in the interrupt control word. However, if port A is operating in mode 2, port B cannot cause an interrupt in the bit mode. Note that, to use the interrupt capability, the mask control register bit corresponding to the bit set for output must be set to "1" to disable its interrupt.

3.4 PIO STATUS TRANSITION AND BASIC TIMING

[1] Status Transition

Figure 3.5 shows the PIO status transition diagram.

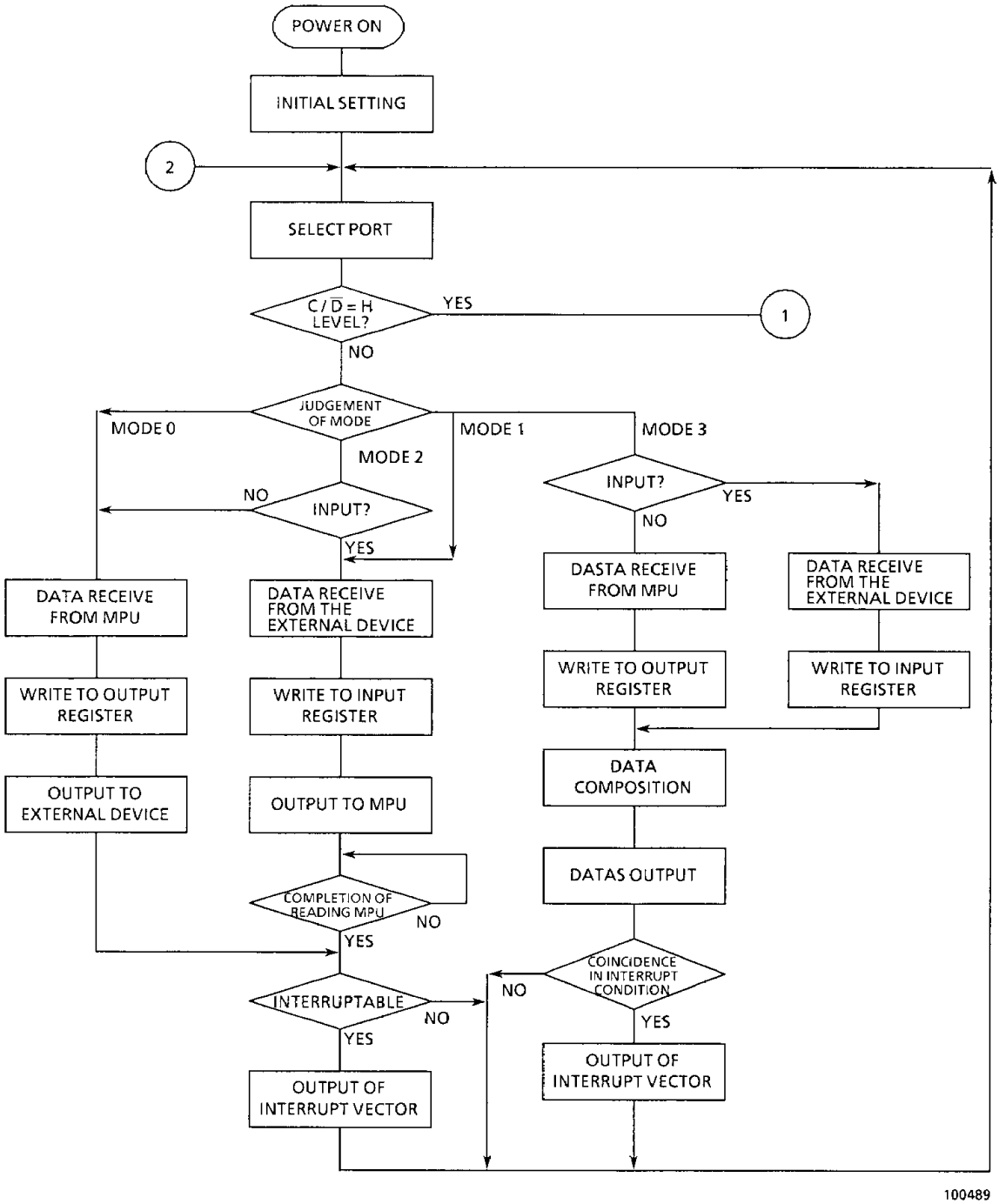

Figure 3.5 (a) PIO Status Transition

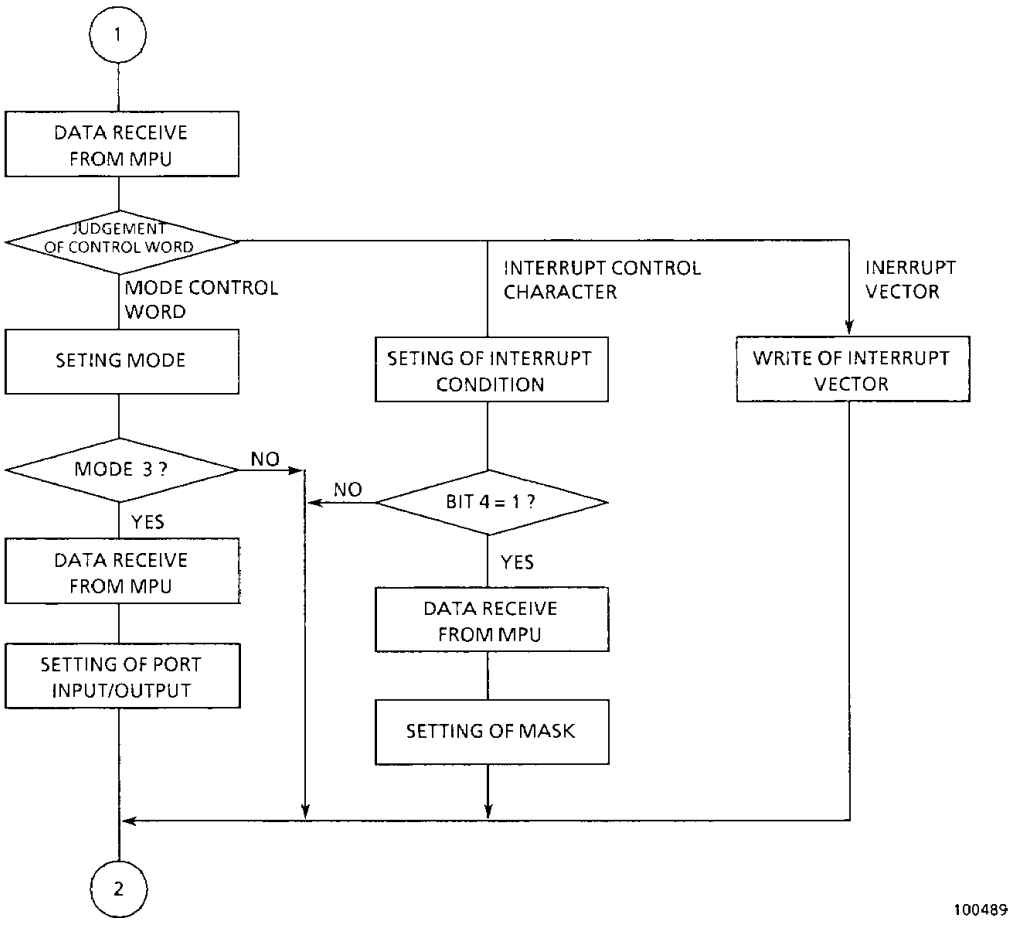

Figure 3.5 (b) PIO Status Transition

[2] Write Cycle

The $\overline{IORQ}$, $\overline{RD}$, C/$\overline{D}$ (A0), and $\overline{CE}$(A7 through A0) signals generate the write signal (*$\overline{WR}$) inside the PIO.

The MPU sets the PIO's $\overline{IORQ}$ signal to the low level at system clock T2, to start the write cycle. At this time, to indicate that this cycle is a write sycle, the PIO's $\overline{M1}$ signal must be set to the high level. At the same time, the MPU sends signals to the PIO's B/$\overline{A}$ (A1) and C/$\overline{D}$ (A0) to specify the port or select control signal or the data. This allows the port data ouput register of the PIO's selected port to latch the data at system clock T3. TW is a wait state automatically inserted by the MPU.

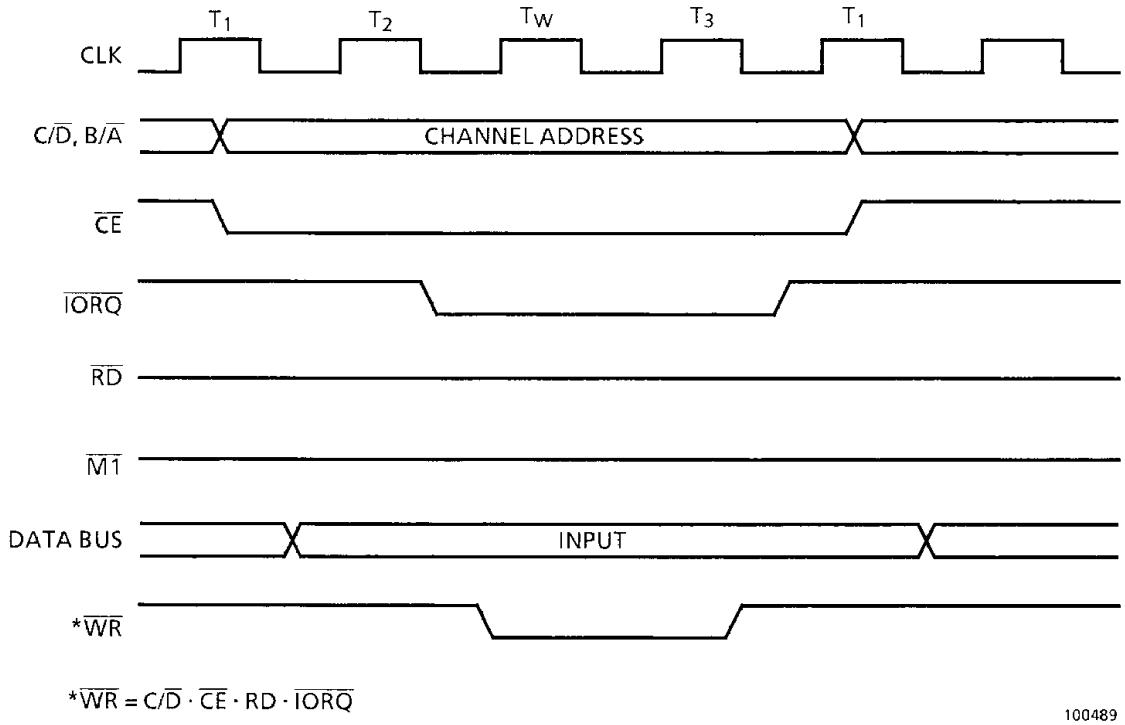

Figure 3.6 Write Cycle Timing

[3] Read Cycle

The MPU sets the PIO's, $\overline{RD}$ pin, $\overline{CE}$ signal, and $\overline{IORQ}$ pin to the low level at system clock T2 to start the read cycle. At this time, to indicate that this cycle is a read cycle, the PIO's M1 pin must be set to the high level. The PIO outputs data in the $\overline{CE}$, $\overline{IORQ}$, and $\overline{RD}$ signals. TW is a wait state automatically inserted by the MPU.

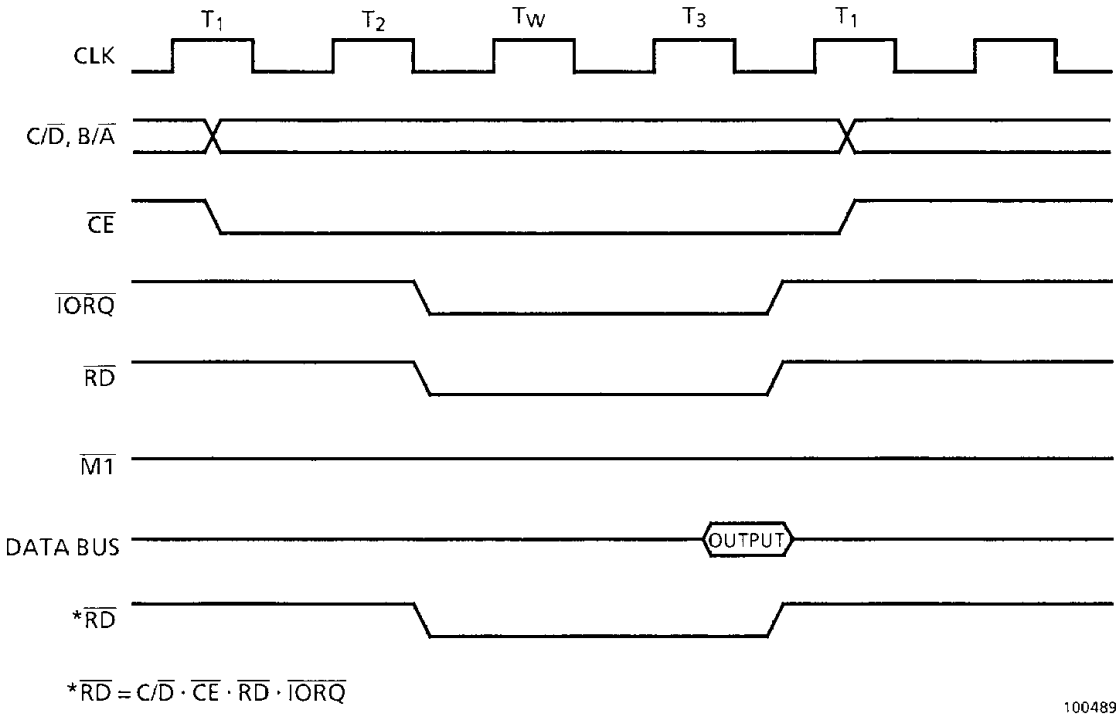

Figure 3.7 Read Cycle Timing

[4] Mode 0 (Byte Output Mode)

The mode 0 output cycle starts when the MPU executes an output instruction. When an output instruction is executed, he write signal (*$\overline{WR}$) is generated in the PIO in the write cycle. This signal latches the data on the data bus to the data output register of the selected port. The RDY pin goes high on the first falling edge of the system clock after the rise of the write signal (*$\overline{WR}$). This indicates that the data in the data output register are already on the port I/O pin. The peripheral device sets the RDY pin to the low level on the first falling edge of the system clock after the rise of the $\overline{STB}$ pin to be input to the PIO to indicate that the peripheral device has received the data from the port I/O pin, waiting for the next output instruction. If, at this time, the PIO is enabled for interrupts, it sets the $\overline{INT}$ pin to the low level on the rising edge of the $\overline{STB}$ signal to output the interrupt request signal to the MPU. Figure 3.8 shows the timing chart of mode 0.

[5] Mode 1 (Byte Input Mode)

The input cycle starts when the MPU has completed the previous data read operation. The peripheral device sets the PIO's $\overline{STB}$ pin to the lower level, putting data on the port I/O line.

The RDY pin is driven low on the first falling edge of the system clock after the rise of the $\overline{STB}$ pin, disabling the peripheral device to send the next data. If, at this time, the

PIO is enabled for interrupts, it sets the $\overline{INT}$ pin to the low level on the rising edge of the $\overline{STB}$ pin, making an interrupt request to the MPU. When the MPU executes the input instruction in the interrupt processing routine, the read signal (*$\overline{RD}$) is generated in the PIO in the read cycle. This signal puts the data in the data input register of the selected port on the data bus. The MPU receives this data. The PIO sets the RDY pin to the high level on the first falling edge of the system clock after the rise of the read signal (*$\overline{RD}$) to wait for the input of the next data. Figure 3.9 shows the mode 1 timing chart.

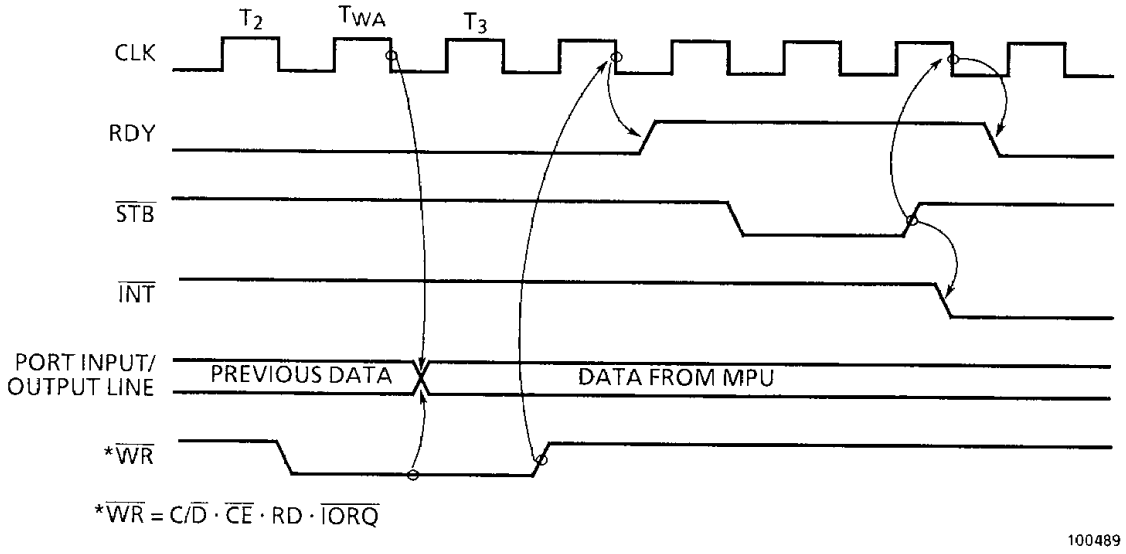

Figure 3.8 Mode 0 Timing Chart

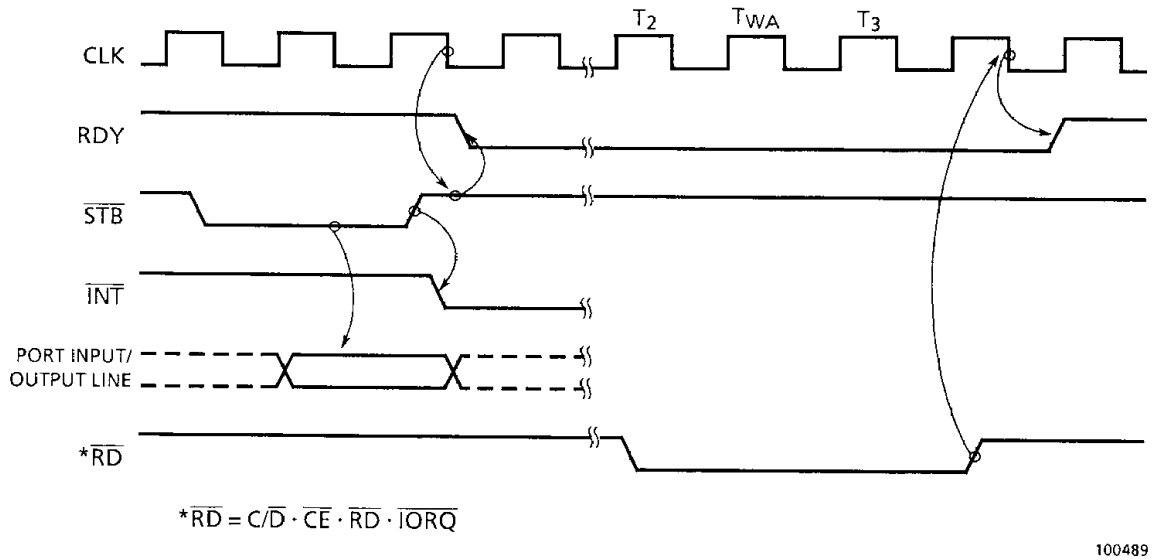

Figure 3.9 Mode 1 Timing Chart

[6] Mode 2 (Byte I/O Mode)

Mode 2 is a combination of mode 0 and mode 1. The timing for output operation is generally the same as in mode 0 except that, in mode 2, data is output only when the $\overline{ASTB}$ pin is low while, in mode 0, data is always on the port I/O line. The peripheral device can receive data on the rising edge of the $\overline{ASTB}$ signal being used as the latch signal.

The input timing is the same as in mode 1.

The port A handshake line is used as output control and the port B handshake line is as input control.

The value of the interrupt vector generated by the $\overline{BSTB}$ signal during port A input operation is the same as the value of the interrupt vector generated when port B is used in mode 3. Hence, all port B bits are masked by setting the mask control word to disable port B for the interrupt capability.

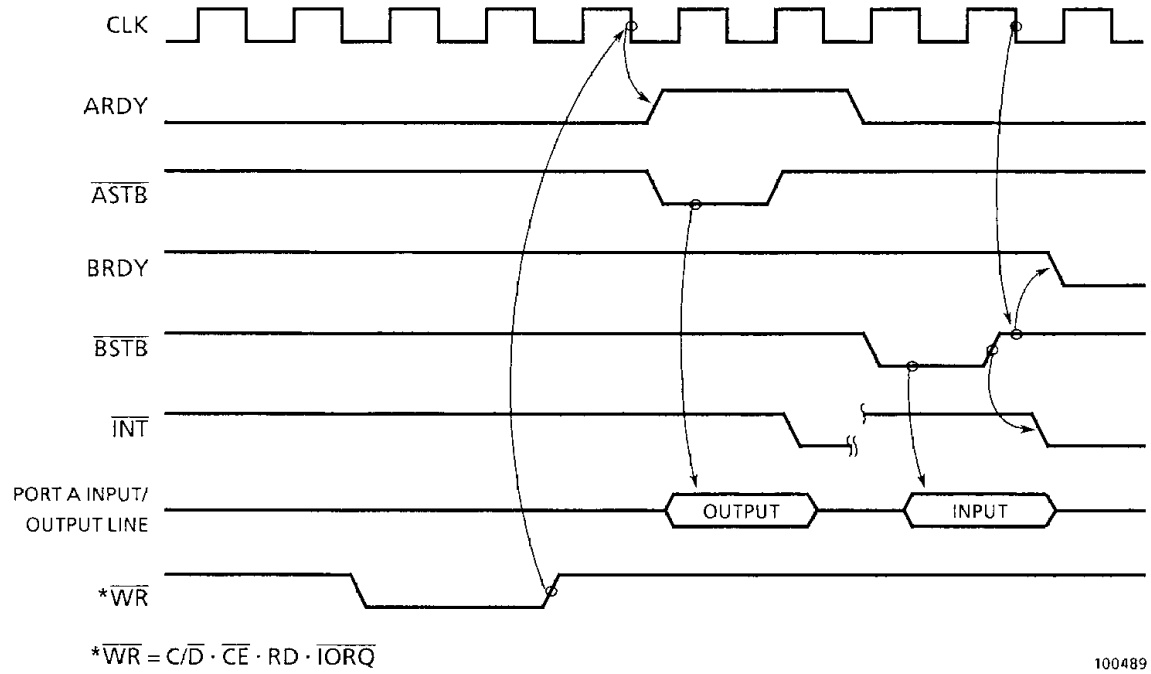

Figure 3.10 Mode 2 Timing Chart

[7] Mode 3 (Bit Mode)

In this mode, no handshake line is used. Therefore, the ordinary port read/write operations can be performed, permitting access to the ports any time. The write data from the MPU is latched to the data output register corresponding to the bit set for output in the same timing as in mode 0. Except when port B is used in mode 2, the $\overline{STB}$ pin of the port operating in mode 3 is fixed to the low level. The transfer data consists of the data in the data output register and in the data input register. That is, the data of the bit set for output and the data of the bit set for input make up the transfer data.

An interrupt occurs when the interrupt enabled state is on and the bits set for input safety the condition specified by the mask control word, etc. However, if port A is operating in mode 2, port B is disabled for interrupt in the bit mode. Note that, to use the interrupt capability, the bit on the mask register corresponding to the bit set for output must be set to "1" to disable it for interrupts.

An interrupt request occurs when the logic condition becomes true. If the logic condition becomes true immediately before the $\overline{M1}$ pin becomes low or while $\overline{M1}$ pin low, an interrupt request occurs on the rising edge on the $\overline{M1}$ pin.

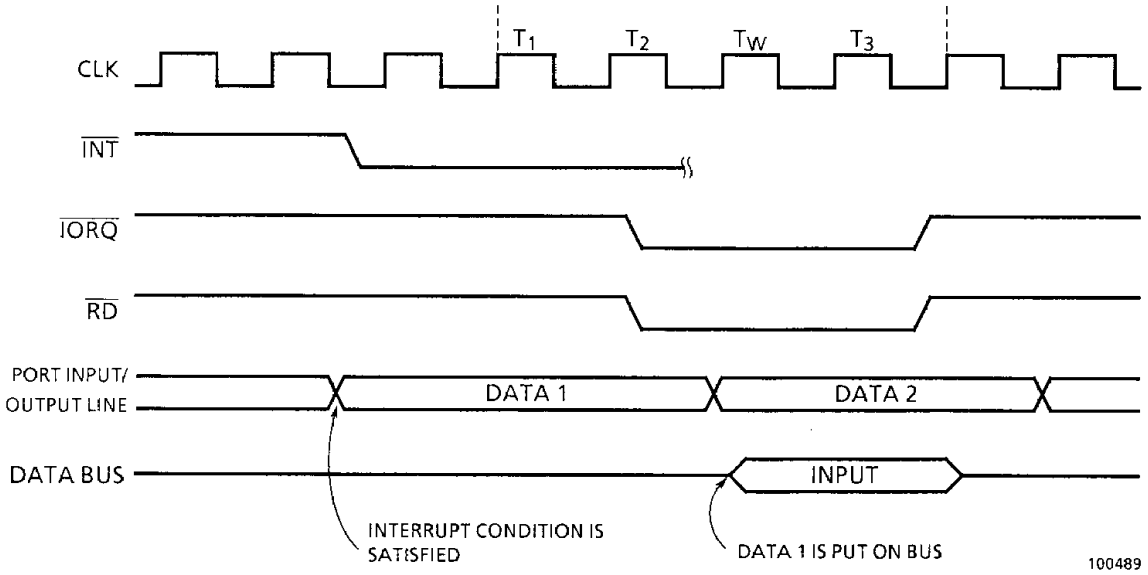

Figure 3.11 Mode 3 Timing Chart

[8] Interrupt Acknowredge Cycle

Outputting the interrupt request signal ($\overline{INT}$), the PIO sets the IEO signal to the low level, disabling the low-priority peripheral LSIs for interrupt requests.
Receiving the interrupt request signal ($\overline{INT}$) from the PIO, the MPU sets the PIO's $\overline{M1}$ and $\overline{IORQ}$ pins to the low level to indicate that the MPU has acknowledged the interrupt request. The $\overline{IORQ}$ pin goes low 2.5 system clocks later than the $\overline{M1}$ pin. To stabilize the daisy-chained signal lines (IEI and IEO), the ports and peripheral LSIs cannot change the interrupt request.

The $\overline{RD}$ pin remaines high to make distinction between the instruction fetch and interrupt acknowledge cycles. While the $\overline{RD}$ pin is high, the interrupt control logic in the PIO determines the interrupt requesting port of the highest priority. When the $\overline{IORQ}$ pin goes low with the IEI pin being high, the interrupt vector is put on the data bus from the interrupt requesting port. At the same time, two system clocks are automatically inserted by the MPU as a wait state to stabilize the daisy chain structure.

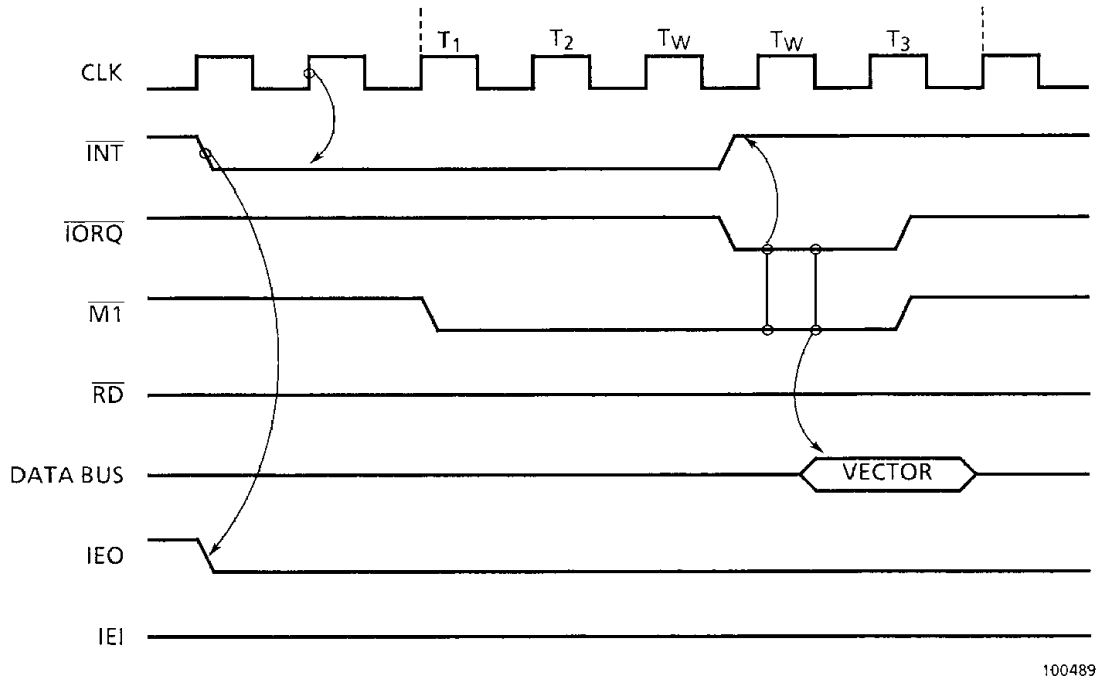

Figure 3.12 Interrupt Acknowledge Cycle Timing Charts

[9] Return from Interrupt Cycle

Return from interrupt processing is performed when the MPU executes the RETI instruction. This RETI instruction must be used at the end of the interrupt processing routine. When the MPU executes this instruction, the PIO's IEI and IEO return to the states active before interrupt processing.

The RETI instruction consists of two bytes and its code EDH and 4DH. The PIO decodes the RETI instruction to determine whether there is any interrupt requesting port. In the daisy chain structure, the IEI and IEO of the interrupting LSI remain high and low respectively at the time the instruction code EDH has been decoded. If the code following EDH is 4DH, only the peripheral LSI which has sent an interrupt vector immediately before, that is, the LSI whose IEI is high and IEO is low, returns from interrupt processing. This restarts the interrupt processing of the supended peripheral LSIs of lower interrupt priory.

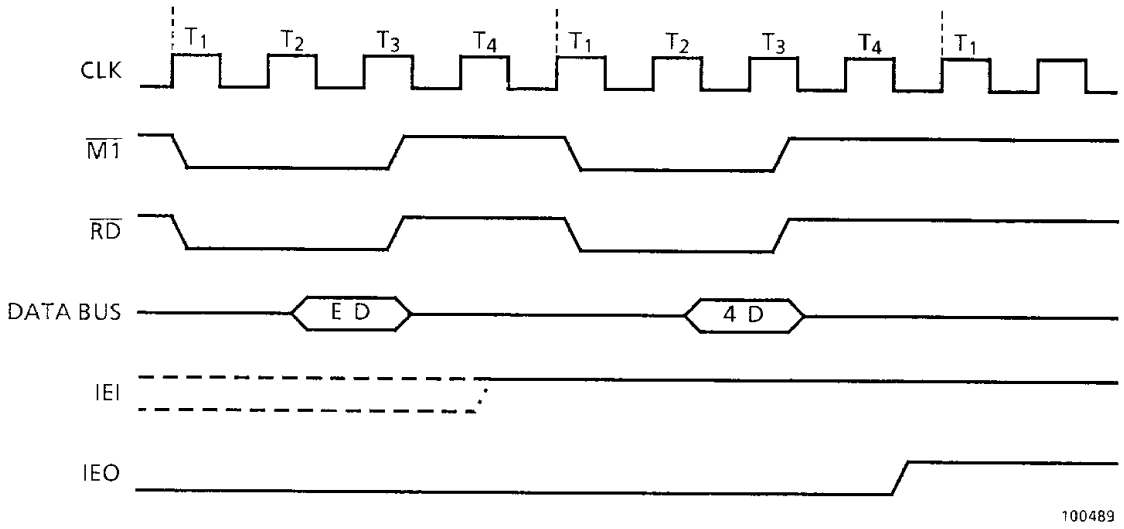

Figure 3.13 Interrupt Cycle Return Timing Chart

3.5 PIO OPERATIONAL PROCEDURE

To operate the PIO the control words shown below must be written in it as the initial settings. They must be wrriten in the PIO's ports, A and B, separately. Spesify the I/O address listed in Table 3.1 to write control words and data in the PIO.

Table 3.1 I/O Adreesses

I/O function	B/$\overline{A}$	C/$\overline{D}$	$\overline{CE}$
Port A data	0	0	0
Port B command	0	1	0
Port B data	1	0	0
Port B command	1	1	0

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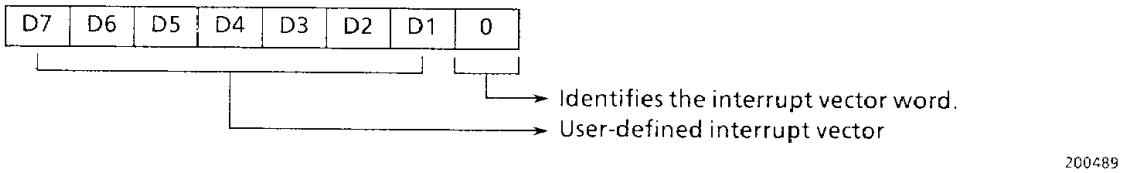
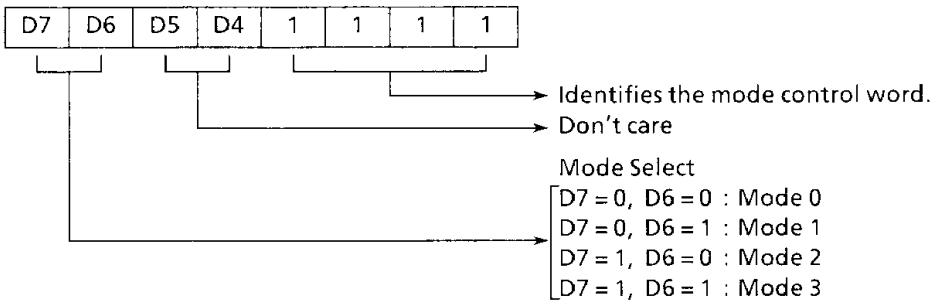
(1) Interrupt Vector Word



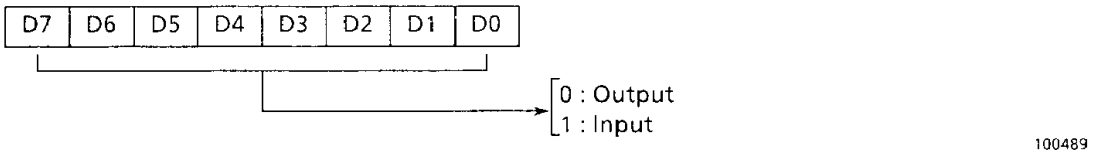
- Using this vector and the contents of the address indicated by the MPU's register, the MPU generates the start address of the interrupt processing routine.
- D0 through D7 are written in the interrupt processing register.
- This word is not needed when the interrupt capability is not used.

(2) Mode Control Word



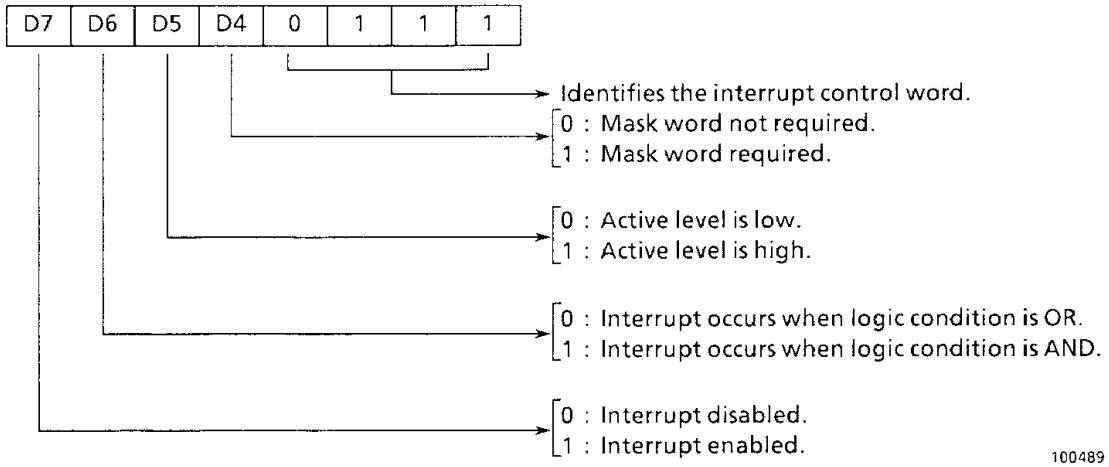
- This word specifies an operation mode.
- D7 and D6 are written in the mode control register.

(3) Data I/O Control Word



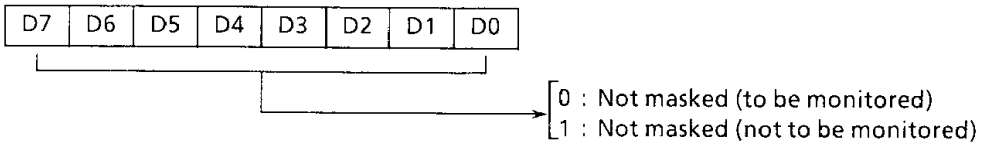
- This word is needed only in mode 3.
- When mode 3 is specified by the mode control word, the data I/O control word is written after it.
- Each port is specified for output or input.
- D0 through D7 are written in the data I/O register.

(4) Interrupt Control Word



- This word is for interrupt control such as interrupt condition setting.
- D4, D5, and D6 are used only in mode 3.
- With D6 = 0, interrupt occurs when one of the bits not masked (the bit to be monitored) by the mask control word goes active.
- With D6 = 1, interrupt occurs when all bits not masked (the bit to be monitored) by the mask control word goes active.
- With D4 = 1, the suspended interrupts are all reset regardless of the mode.
- D5 and D6 are written in the control register.

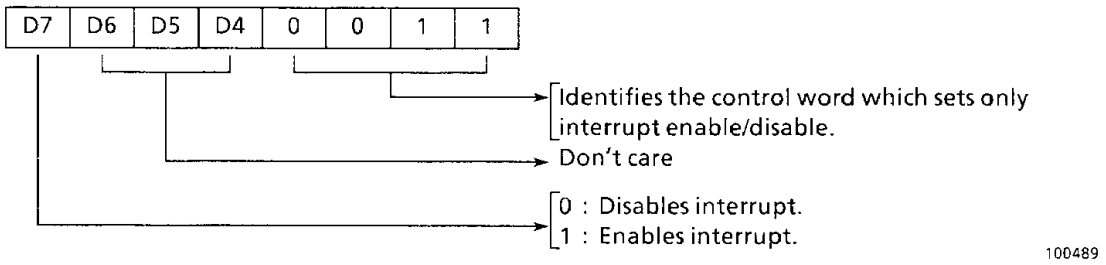
(5) Mask Control Word



- This word is needed only in mode 3.
- When D4 = 1 is set by the interrupt control word, the mask control word must be written after it.
- This word specifies whether to monitor the port I/O line specified for input by the data I/O control word.
- When the bit is set to 0, the corresponding input line is monitored and regarded as the input associated with interrupt occurrence.
- When the bit is set to 1, the corresponding input line is masked to provide the input not related to interrupt occurrence.
- The PIO checkes only the input line with the bit being 0 to see if the interrupt condition is satisfied. If the condition is satisfied, the PIO requests an interrupt.
- D0 through D7 are written in the mask control register.

When port A is put in mode 2, all 4 handshake lines are used, so that port B must be set in mode 3 which uses no handshake lines. At the same time, all mask control word bits must be set to 1 (masked).

Note : Only interrupt enable/disable can be set by the following control word:



3.6 USING PIO

The following is a programming example to operate the PIO's port in mode 3. This program is followed by the main routine and the interrupt processing program.

- The MPU is used in the mode 2 interrupt.
- The table storing the start address of the interrupt processing routine is 0802H.
- Interrupts occur when both PIO's port input lines A6 and A5 go high.
- The I/O addresses of the PIO are the address listed in Table 3.1.

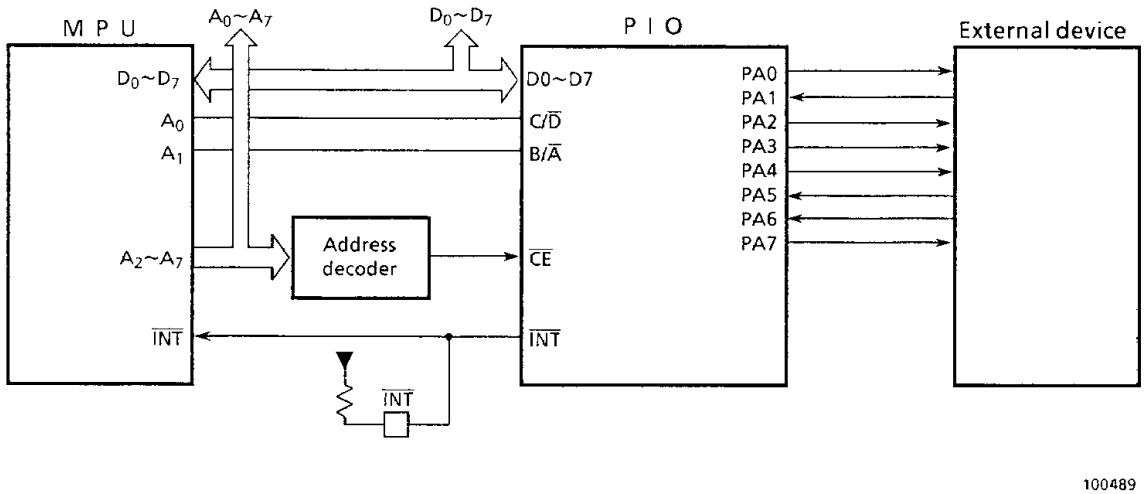


Figure 3.14 PIO Connection

```
        ORG 100H
        LD  SP,100H  ..... Sets the stack pointer.
        LM  2        ..... Sets for MPU mode 2 interrupt.
        LD  A,08H    ..... Writes data in MPU I register.
        LD  I,A
;
        LD  A,02H    ..... Writes the interrupt vector word.
        OUT (01H),A
        LD  A,0CFH   ..... Writes the mode control word.
        OUT (01H),A
        LD  A,62H    ..... Writes the data I/O control word, Sets PIO.
        OUT (01H),A
        LD  A,F7H    ..... Writes interrupt control word.
        OUT(01H),A
        LD  A,9FH    ..... Writes the mask control word.
        OUT (01H),A
;
        EI           ..... Set interrupt enable.
```

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATING

Symbol	Item		Rating	Unit
V_{CC}	Supply Voltage		-0.5~+7	V
V_{IN}	Input Voltage		-0.5~VCC+0.3	V
PD	Power Dissipation (6MHz VERSION : TA = 85°C) (8MHz VERSION : TA = 70°C)		250	mW
TSOLDER	Soldering Temperature (10 sec)		260	°C
TSTG	Storage Temperature		-65~150	°C
TOPR	Operating Temperature	6MHz VERSION	-40~85	°C
		8MHz VERSION	-10~70	

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4.2 DC ELECTRICAL CHARACTERISTICS

6MHz VERSION : $T_A = -40°C \sim 85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$
8MHz VERSION : $T_A = -10°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage			-0.3	—	0.6	V
VIHC	High Clock Input Voltage			V_{CC}-0.6	—	V_{CC}+0.3	V
VIL	Low Input Voltage (Except CLK)			-0.5	—	0.8	V
VIH	High Input Voltage (Except CLK)			2.2	—	V_{CC}	V
VOL	Output Low Voltage	IOL = 2.0mA		—	—	0.4	V
VOH1	Output High Voltage (I)	IOH = -1.6mA		2.4	—	—	V
VOH2	Output High Voltage (II)	IOH = -250μA		V_{CC}-0.8	—	—	V
ILI	Input Leakage Current	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		—	—	±10	μA
ILO	3-STATE Output Leakage Current in Float	$V_{SS}+0.4 \leqq V_{OUT} \leqq V_{CC}$		—	—	±10	μA
IOHD (2)	Darlington Drive Current	VOH = 1.5V REXT = 1.1KΩ		-1.5	—	-5.0	mA
ICC1	Power Supply Current	V_{CC} = 5V f_{CLK} = (1) $V_{ILC} = V_{IL}$ = 0.2V $V_{IHC} = V_{IH} = V_{CC}$ - 0.2V	AP-6/ AM-6/ AT-6	—	3	8	mA
			AP-8	—	4	10	
ICC2	Standly Supply Current	$V_{ILC} = V_{IL} = 0.2$ $V_{IHC} = V_{IH} = V_{CC}$-0.2V		—	0.5	10	μA

Note : (1) fCLK = 1/tcC (MIN.) (2) Port B only

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4.3 AC ELECTRICAL CHARACTERISTICS

6MHz VERSION : $T_A = -40°C \sim 85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$
8MHz VERSION : $T_A = -10°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

(1/2)

NO.	SYMBOL	PARAMETER	AP-6/AM-6/AT-6 (6MHz)		AP-8 (8MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	165	DC	125	DC	ns
2	TwCh	High clock pulse width	65	DC	50	DC	ns
3	TwCl	Low clock pulse width	65	DC	50	DC	ns
4	TfC	Clock falling time	—	20	—	15	ns
5	TrC	Clock rising time	—	20	—	15	ns
6	TsCS (RI)	$\overline{CE}$, B/$\overline{A}$ and C/$\overline{D}$ set-up time for $\overline{RD}$, $\overline{IORQ}$	50	—	50	—	ns
*7	Th	Hold time	40	—	40	—	ns
8	TsRI (C)	$\overline{RD}$, $\overline{IORQ}$ set-up time for clock rise	70	—	60	—	ns
9	TdRI (DO)	Delay from $\overline{RD}$, $\overline{IORQ}$ fall to data output	—	300	—	200	ns
10	TdRI (DOs)	Delay from $\overline{RD}$, $\overline{IORQ}$ rise to data float	—	70	—	70	ns
11	TsDI (C)	Data set-up time for clock rise	40	—	40	—	ns
12	TdIO (DOI)	Delay from $\overline{IORQ}$ fall of INTA cycle to data output	—	120	—	85	ns
13	TsM1 (Cr)	$\overline{M1}$ = L set-up time for clock rise	70	—	50	—	ns
14	TsM1 (Cf)	$\overline{M1}$ = H set-up time for clock fall ($\overline{M1}$ sycle)	0	—	0	—	ns
15	TdM1 (IEO)	Delay from $\overline{M1}$ fall to IEO fall	—	100 (1)	—	100 (1)	ns
16	TsIEI (IO)	IEI set-up time for $\overline{IORQ}$ fall (INTA cycle)	100	—	80	—	ns
17	TdIEI (IEOf)	Delay from IEI fall to IEO rise	—	120	—	100	ns
18	TdIEI (IEOr)	Delay from IEI rise to IEO fall	—	150	—	120	ns
19	TcIO (C)	$\overline{IORQ}$ = H set-up time for clock fall (in case of making READY to active by next cycle)	170	—	120	—	ns
20	TdC (RDYr)	Delay from clock fall to READY rise	—	170	—	150	ns
21	TdC (RDYf)	Delay from clock fall to READY fall	—	120	—	110	ns
22	TwSTB (C)	STROBE pulse width	120 (2)	—	100 (2)	—	ns
23	TsSTB (C)	Set-up time of $\overline{STROBE}$ rise for clock fall (in case of making READY to active by next cycle)	150	—	100	—	ns

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(2/2)

NO.	SYMBOL	PARAMETER	AP-6/AM-6/AT-6 (6MHz)		AP-8 (8MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	
24	TdIO (PD)	Delay from $\overline{IORQ}$ rise to port data stable (Mode 0)	—	160	—	140	ns
25	TsPD (STB)	Data set-up time for $\overline{STROBE}$ rise (Mode 1)	190	—	150	—	ns
26	TdSTB (PD)	Output data delay time from $\overline{STROBE}$ fall (Mode 2)	—	180	—	150	ns
27	TdSTB (PDr)	Delay from $\overline{STROBE}$ rise to data float (Mode 2)	—	160	—	120	ns
28	TdPD (INT)	Delay from port data match to $\overline{INT}$ fall (Mode 3)	—	430	—	350	ns
29	TdSTB (INT)	Delay from $\overline{STROBE}$ rise to $\overline{INT}$ fall (Mode 2)	—	350	—	250	ns

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Note :

1 Item with * mark (No.7) is not compatible with NMOS Z80 PIO.

2 (1) If the daisy chain is at N stage,
2.5 TcC > (N-2)TdIEI(IEOf) + TdM1(IEO) + TsIEI(IO) + TTL buffer delay must be satisfied.

(2) In Mode 2, TwSTB > TsPD(STB) must be satisfied.

(3) At test condition : Input : VIH = 2.4V, VIHC = VCC-0.6V, VIL = 0.4V, VILC = 0.6V
Output : VOH = 2.2V, VOL = 0.8V, CL = 100pF

4.4 CAPACITANCE

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f = 1MHz All terminals except that to be measured should be earthed.	—	—	10	pF
CIN	Input Capacitance		—	—	5	pF
COUT	Output Capacitance		—	—	10	pF

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4.5 TIMING DIAGRAM

Numbers shown in the following figures correspond with those in the 4.3 A.C Electrical Characteristics Table.

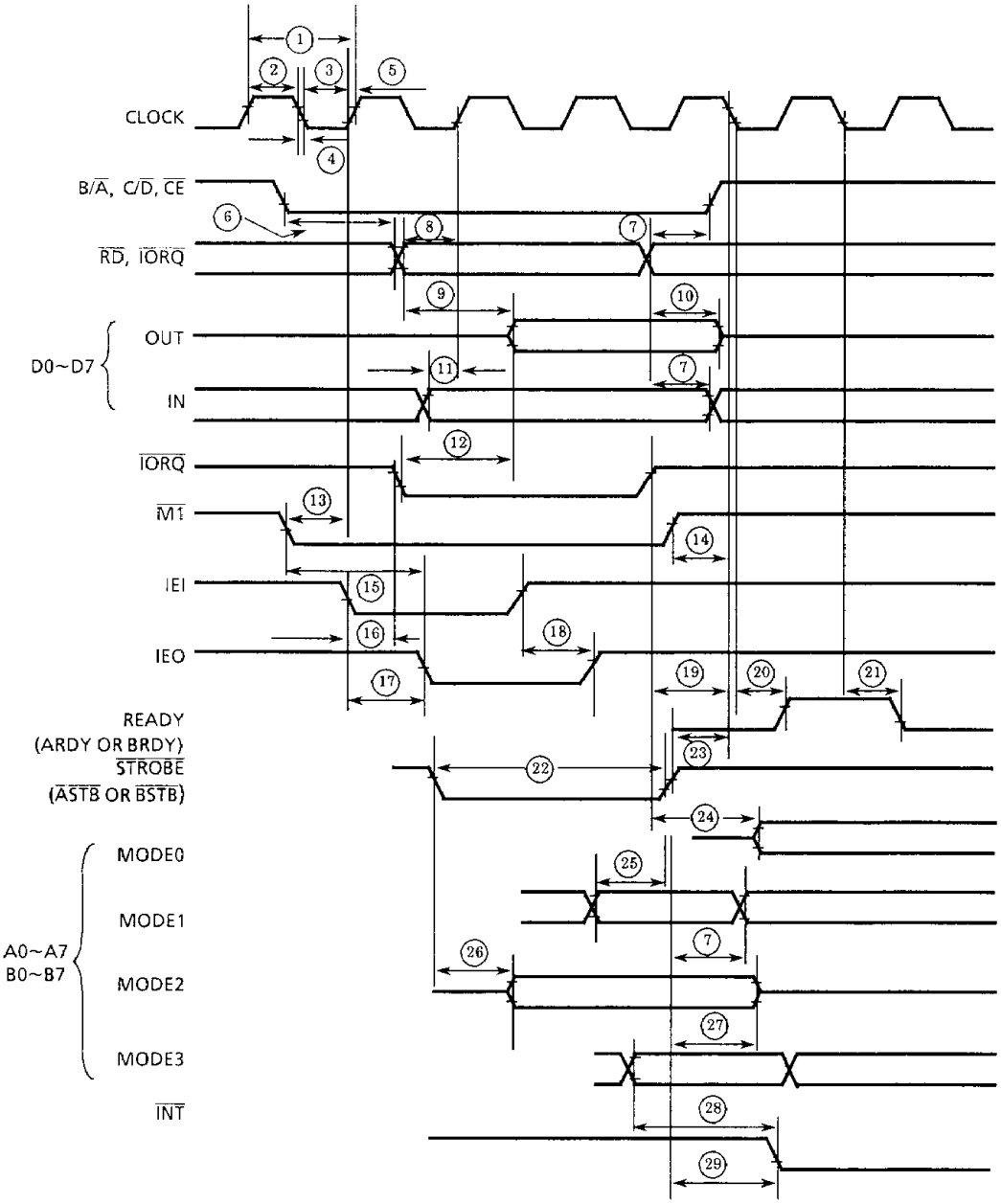


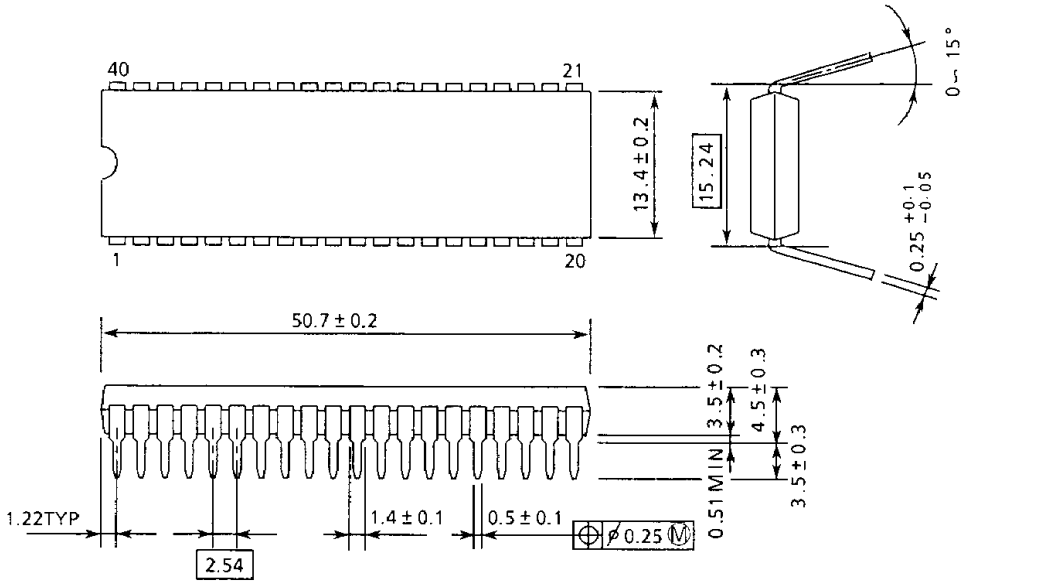
Figure 4.1 Timing Diagram

5. PACKAGE DIMENSION

5.1 40-PIN PLASTIC PACKAGE

DIP40-P-600

Unit : mm



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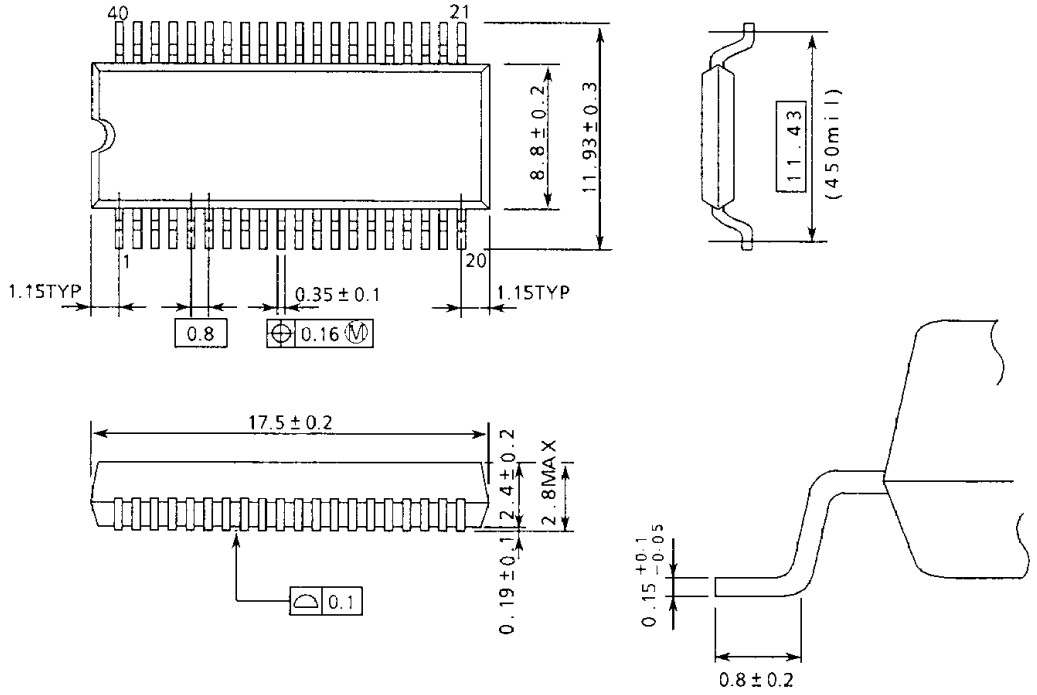
Note 1 : This dimention is measured at the center of bending point of leads.

Note 2 : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

5.2 40-PIN SMALL OUTLINE PACKAGE

SSOP40-P-450

Unit : mm



Note : Package Width and length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

5.3 44-PIN PLCC PACKAGE

QFJ44-P-S650

Unit : mm