TMPZ84C30AP-6 / TMPZ84C30AM-6 / TMPZ84C30AT-6
TMPZ84C30AP-8

TLCS-Z80 CTC : COUNTER TIMER CIRCUIT

1. GENERAL DESCRIPTION AND FEATURES

The TMPZ84C30A (hereinafter referred to as CTC) is CMOS version of Z80 CTC and has been designed to provide low power operation.

The TMPZ84C30A is fablicated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the CTC are as follows.

(1) Compatible with the Zilog Z80 CTC.

(2) Low power consumption.
4mA Typ. (@5V @6MHz) ··· TMPZ84C30AP-6/AM-6/AT-6
5mA Typ. (@5V @8MHz) ··· TMPZ84C30AP-8
10μA Max. (@5V, Stand-by)

(3) DC to 6MHz operation ··· TMPZ84C30AP-6/AM-6/AT-6
DC to 8MHz operation ··· TMPZ84C30AP-8

(4) Single 5V power supply and single-phase clock. 5V ±10% (6MHz VERSION)
5V ± 5% (8MHz VERSION)

(5) Capable of driving Darlington transistors.

(6) Four independent counter/timer channels each of which is capable of independently selecting Timer Mode and Counter Mode.

(7) Each channel is provided with a prescaler to divide system clock into 16 or 256.

(8) Built-in interrupt control logical operation circuit allows priority processing of interrupt in Daisy-chain structure and automatic loading of 8 bit interrupt vector on the system bus.

(9) Four channels occupy 4 successive positions in the Daisy-chain structure. Most significant channel is Channel 0 and least significant channel is Channel 3.

(10) In both modes, at the zero count, the content of the time constant register is automatically loaded on the down counter.

(11) In either Counter Mode or Timer Mode, the content of the down counter is readable by the microprocessor (hereinafter referred to as MPU).

(12) Interrupt function available in Z80 MPU Mode 2.

(13) In Timer Mode, the timer operation is selectable at the rise or fall of the starting trigger. In addition, in Counter Mode the decrement (-1) of the content of the down counter either at the rise or fall of external clock is selectable.

(14) Programming to generate interrupt by zero count by the down counter in each channel is possible.

(15) 40 pin DIP package, 40 pin SOP, 44 pin PLCC package.

Note : Z80 is a trademark of Zilog Inc., U.S.A.

2. PIN CONNECTIONS AND PIN FUNCTIONS

2.1 PIN CONNECTIONS (Top View)

The pin connections of the CTC are as shown in Figure 2.1 and Figure 2.2.

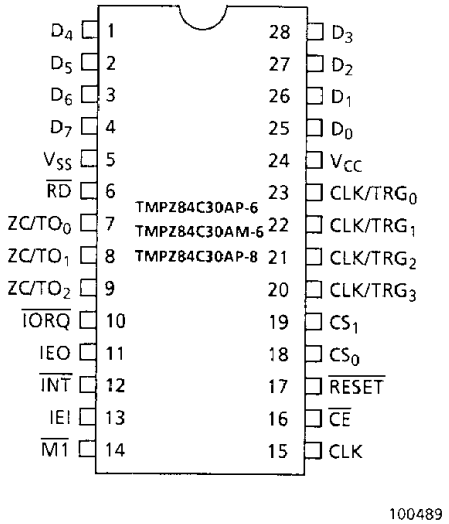

Figure 2.1 DIP, SOP Pin Connections

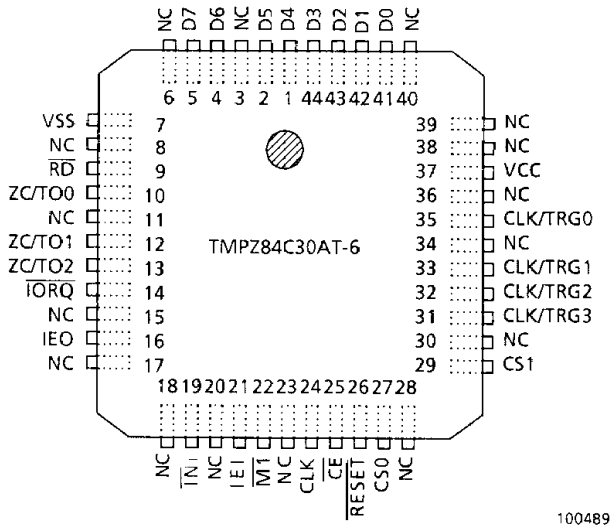

Figure 2.2 44-Pin PLCC Package

2.2 PIN NAMES AND FUNCTIONS

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions (1/2)

Pin Name	Number of Pin	Input/Output 3-state	Function
D0~D7	8	I/O 3-state	8-bit bi-directional data bus.
$\overline{RD}$	1	Input	The read signal. This signal is used in combination with $\overline{IORQ}$ and $\overline{CE}$ signals for transfer of data and channel control words between MPU and CTC.
ZC/TO0 ~ ZC/TO2	1	Output	The Zero Count/Timer Out signal. In either the Timer mode, or counter mode, pulses are output from these pins when the down counter has reached zero.
$\overline{IORQ}$	1	Input	I/O request signal. This signal is used in combine with $\overline{RD}$ and $\overline{CE}$ signals for transfer of data and channel control words between MPU and CTC.
IEO	1	Output	Interruption enable output. Controls interruptions by subordinate peripheral LSI's in the Daisy-chain structure. This terminal becomes H level only when the IEI terminal is at H level and MPU is not providing the interruption service to channels in CTC.

100489

Table 2.1 Pin Names and Functions (2/2)

Pin Name	Number of Pin	Input/output 3-state	Function
$\overline{INT}$	1	Output	Interruption request. This terminal becomes L level if a down-counter for any channel in CTC counts zero when the IEI terminal is at H level and interruption is authorized by a program.
IEI	1	Input	The interrupt Enable Input signal. This signal is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral LSI.
$\overline{M1}$	1	Input	Machine cycle 1. Informs the machine cycle from MPU. In combination with the $\overline{RD}$ signal, indiates that MPU fetches commands from the memory, and in combination with the $\overline{IORQ}$ signal, indicates that MPU is in the interruption acknowledge cycle. This terminal is used, in combination with the $\overline{IORQ}$ signal, to send the interruption vector to MPU.
CLK	1	Input	Single-phase clock input. Single-phase Z80 standard system clock is inputted to this terminal. When this CLK terminal is in the DC state (high or low level), the CTC is placed in the stationary state.
$\overline{CE}$	1	Input	Chip enable. Used to write MPU-CTC channel control word, interruption vector, and time constant or to read the content of a downcounter for each channel in combination with the $\overline{IORQ}$ and $\overline{RD}$ terminals.
$\overline{RESET}$	1	Input	Reset signal . When the reset signal is inputted to this terminal, all channels stop to operate and interruption enable bits in all channel control registers are reset. This $\overline{RESET}$ terminal must be kept at "L" level for at least 3 system clocks.
CS0~CS1	2	Input	Channel selection. Any one of four channels of the CTC is selected by 2-bit code at time of read/write.
CLK / TRG0~ CLK / TRG3	4	Input	The external clock/timer trigger. These 4 CLK/TRG pins correspond to 4 channels. In the counter mode, the down counter is decremented by 1 and in the timer mode, the timer is activated at each active edge (a rising of falling edge) of the signal which are input by these pins. It can be selected by program whether the active edge is a rising or falling edge.
Vcc	1		The power supply (+ 5V) pin
Vss	1		The ground (0V) pin

100489

3. FUNCTIONAL DESCRIPTION

3.1 BLOCK DIAGRAM

The block diagram of CTC is shown in Figure 3.1.

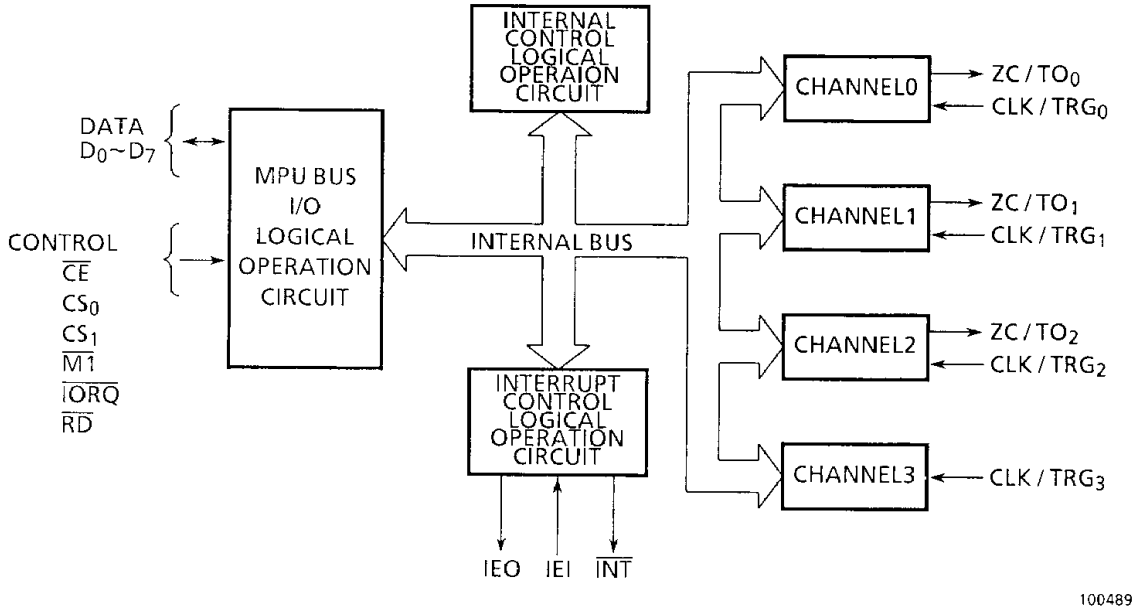

Figure 3.1 Block Diagram

3.2 SYSTEM CONFIGURATION

The CTC system consists of the following 4 logic circuits.

(1) MPU bus Input/Output Logic Circuit

(2) Internal control logic circuit

(3) Interrupt Control Logic Circuit

(4) 4 Independent Counter/Timer Channel Logic Circuit

3.2.1 MPU bus input/output logic circuit

This circuit transfers data between the MPU and the CTC.

3.2.2 Internal control logic circuit

This circuit controls the CTC operational functions such as the CTC selecting enable, reset, and read/write circuit.

3.2.3 Interrupt control logic circuit

This circuit performs the MPU interrupt related processing such as priority determination. The order of priority with other LSIs determined according to the physical location in daisy chain connection.

3.2.4 Counter/timer channel logic circuit

This circuit consists of the following 2 registers and 2 counters.

Figure 3.2 shows the configuration of this circuit.

- Time-constant register (8 bits)
- Channel control register (8 bits)
- Down-counter (8 bits)
- Prescaler (8 bits)

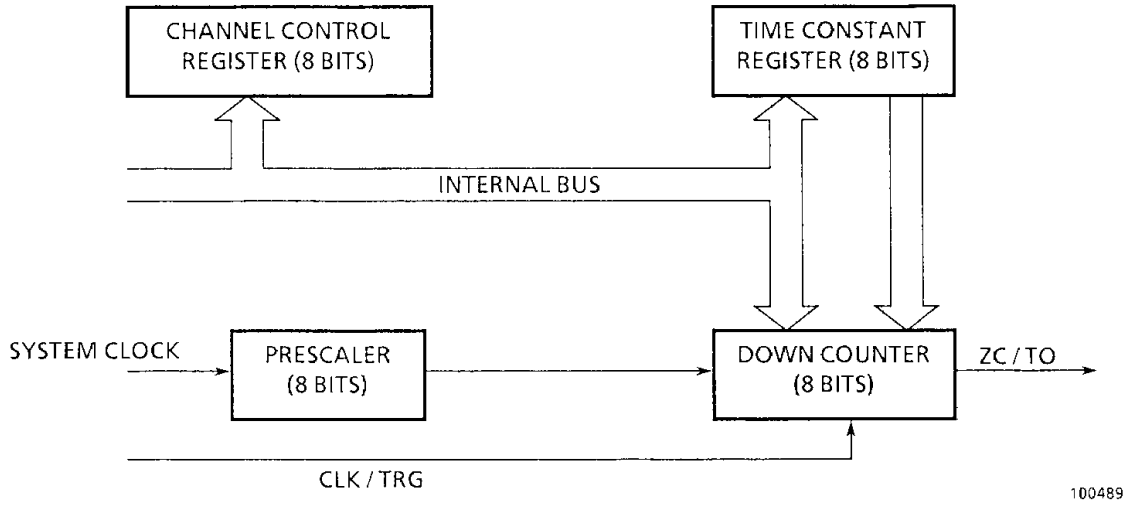

Figure 3.2 Configuration Counter/Timer Channel Logic Circuit

(1) Time-constant register

This register holds the time constant to be written in the down counter. When the CTC is initialized or the down-counter has reached zero, the time constant is loaded into down-counter. The time constant is set immediately after the MPU has written the channel control word in the channel control register. For a time constant, an integer from 1 to 256 can be used.

(2) Channel control register

This register is used to choose the channel mode or condition according to the channel control word sent from the MPU.

(3) Down-counter

The contents of the time-constant register are loaded into the down counter. In the counter mode, these contents are decremented for each edge of the external clock. In the timer mode, they are decremented for each prescaler clock output. The contents of the time-constant register are loaded at intialization or when the down-counter has reached zero.

The contents of the down-counter can be read any time. Also, the system can be programmed so that an interrupt request is generated each time the down-counter has reached zero.

(4) Prescaler

The prescaler, used only in the timer mode, divides the system clock by 16 or 256. The dividing number is programmed by channel control word. The output of the prescaler becomes the clock input to the down-counter.

3.3 CTC BASIC OPERATIONS

3.3.1 Reset

The state of the CTC is unstable after it is powered on. To stabilize the CTC, the low level signal needs to be applied to the $\overline{\text{RESET}}$ pin. On any channel, the channel control word and time-constant data must be written to be started before it is started in the counter or timer mode. To program the system to enable interrupts, the interrupt vector word must be written in the interrupt controller. When these data have been written in the CTC, it is ready to start.

3.3.2 Interrupt

The CTC can cause an interrupt when the MPU is operating on the mode 2. The CTC interrupt can be programmed for each channel. Each time the channel's down-counter has reached zero, the CTC outputs the interrupt request signal ($\overline{\text{INT}}$). When the MPU accepts the CTC's interrupt request, the CTC outputs the interrupt vector. Based on this interrupt vector, the MPU specifies the start address of the interrupt processing routine and calls it to start interrupt processing.

The MPU specifies the start address of the interrupt processing routine by the interrupt vector output from the CTC, so that the user can change the vector value to call any desired address.

The interrupt processing is terminated when the MPU executes an RETI instruction. The CTC has the circuit which decodes the RETI instruction. By constantly monitoring the data bus the CTC can detect the termination of the interrupt procrssing.

The order of interrupt priority with the Z80 peripheral LSIs is determined by the daisy chain connection. That is, the peripheral LSIs are connected one after another and the one physically near MPU is given a higher priority.

Inside the CTC, channel 0 is given the highest priority, followed by channels 1, 2 and 3 in this order.

The CTC and other peripheral LSIs have the signal lines IEO and IEI. Connect the IEO of a higher peripheral LSI to the IEI of a lower peripheral LSI. Connect the IEI of the highest peripheral LSI to VCC. Leave the IEO of the peripheral LSI unused. In this connection, the CTC interrupt is caused under the following conditions:

- When both IEI and IEO are high, no interrupt is caused. At this time, the $\overline{INT}$ signal is high. An interrupt can be requested in this state.
- When the CTC outputs the interrupt request signal ($\overline{INT}$), the IEO of the CTC becomes low. When the MPU accepts the interrupt, the $\overline{INT}$ goes high again.
- When the IEI goes low, the IEO also goes low.
- While the IEI is low, no interrupt can be requested.
- When the IEI goes low while an interrupt is being serviced, the interrupt processiong is aborted.

3.3.3 Operation modes

The CTC oprates in either the counter mode or the timer mode. Mode is selected by writing the channel control word.

(1) Counter mode

In the counter mode, the number of edge of the pulse applied to the channel's CLK/TRG pin is counted. When pulses have been input, the contents of the down-counter are decremented synchronizing with the rising edge of the next system clock. The pulse's rising edge or falling esge to be counted can be specified by the channel control word.

When the contents of the down-counter has reached zero, the high level pulse is output from the ZC/TO pin. When the interrupt is enabled by the channel control word, the $\overline{INT}$ pin goes low and an interrupt is requested. When the contents of the down-counter has reached zero, the time constant data written in the time constant register is automatically loaded into the down-counter. To load a new time constant value into the down-counter, write the data to the time constant register, and it is loaded into the down-counter after the current count operation is terminated.

(2) Timer mode

In the timer mode, the time intervals which are integral multiples of the system clock period. A timer interval is measured according to the system clock. The system clock is supplied to the prescaler which divides it by a factor of 16 or 256. The output of the prescaler provides the clock to decrement the down-counter by 1. The time constant data

is automatically loaded into the down-counter each time it has reached zero as in the counter mode. When the contents of the down-counter has reached zero, the high level pulse is output from the ZC/TO pin.

This pulse period is given by the following expression:

tc * P * TC

Where, tc = System clock period
P = Prescaler value (16 or 256)
TC = Time constant data (256 for 00H)

The user can select, by means of the channel control word, to start the timer automatically or to start the timer on the edge of the pulse at CLK/TRG pin. In case the user select the CLK/TRG pin, the user can also select the rising edge or falling edge of the pulse.

3.4 CTC STATUS TRANSITION DIAGRAM AND BASIC TIMING

3.4.1 Transition diagram

Figure 3.3 shows the CTC status transition diagram.

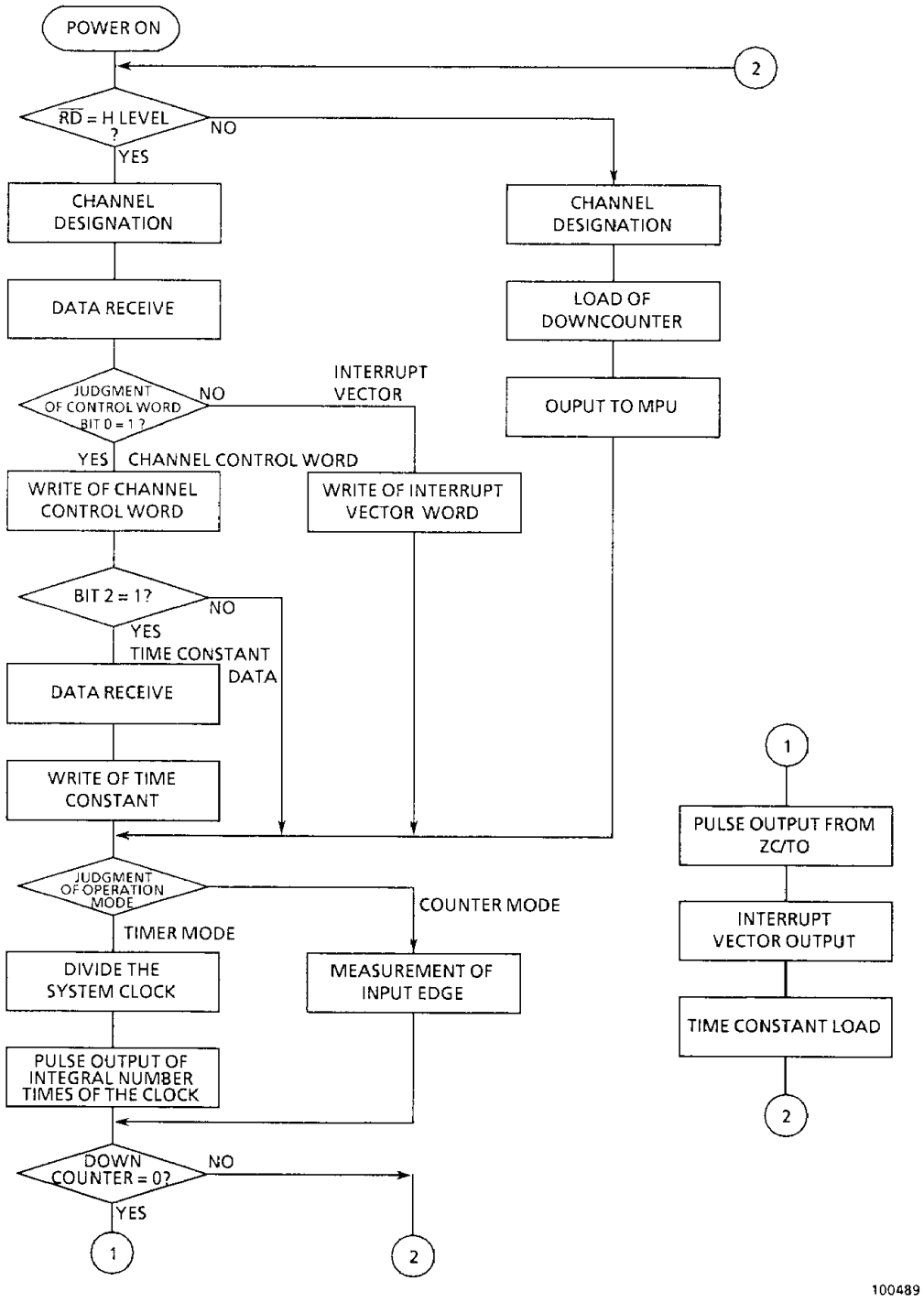

Figure 3.3(a) CTC Transition Diagram (a)

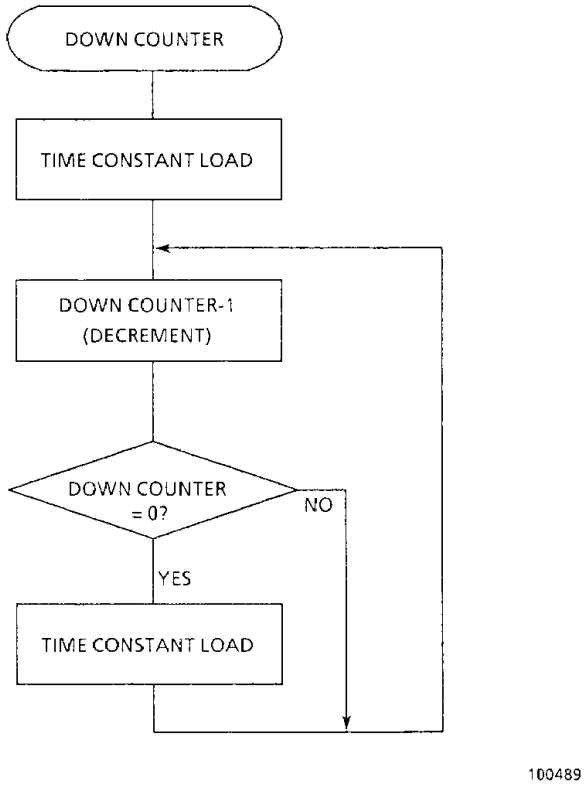

Figure 3.3(b) CTC Transition Diagram (b)

3.4.2 Write cycle

The write cycle is used to write a channel control word, an interrupt vector, or a time constant. The MPU drives the $\overline{IORQ}$ pin of the CTC low in the subsequent system clock cycle T2 to start the write cycle.

It is required to make the $\overline{M1}$ pin of the CTC high to indicate that the write cycle is on.

At the state of the cycle, the channel is specified by CS1 or CS0 of the CTC. Thus, the CTC's internal registers are ready to accept data in system clock T3. Tw is the state to be automatically inserted by the MPU.

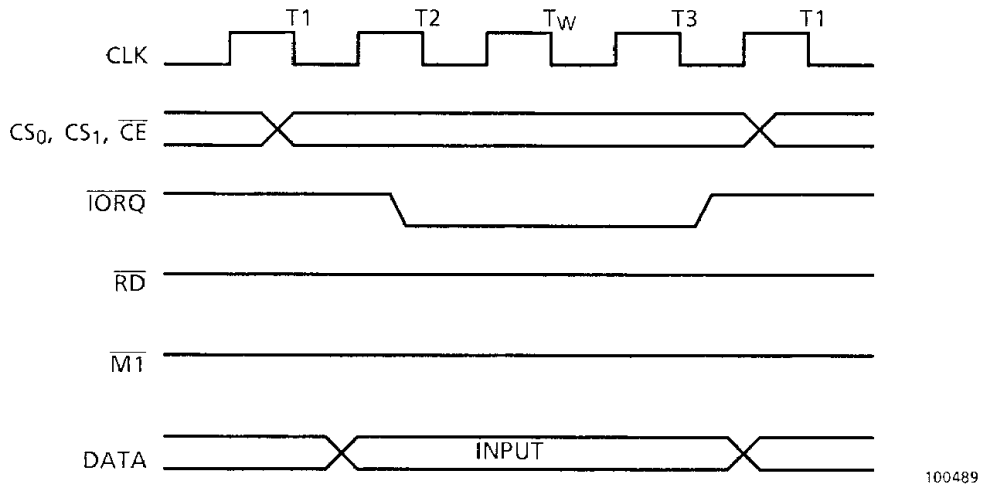

Figure 3.4 Write Timing

3.4.3 Read cycle

The read cycle is used to read the contents of the down-counter. During clock cycle T2, the MPU initiates a read cycle by driving the $\overline{RD}$ and $\overline{IORQ}$ pins low. It is required to make the $\overline{M1}$ pin high to indicate that the read cycle is on. At the start of the read cycle, the channel is specified by CS1 or CS0 of the CTC.

At the rising edge of system clock TW, the contents of the down-counter at the time of the rising edge of T2 are put on the data bus. TW is the wait state to be automatically inserted by the MPU.

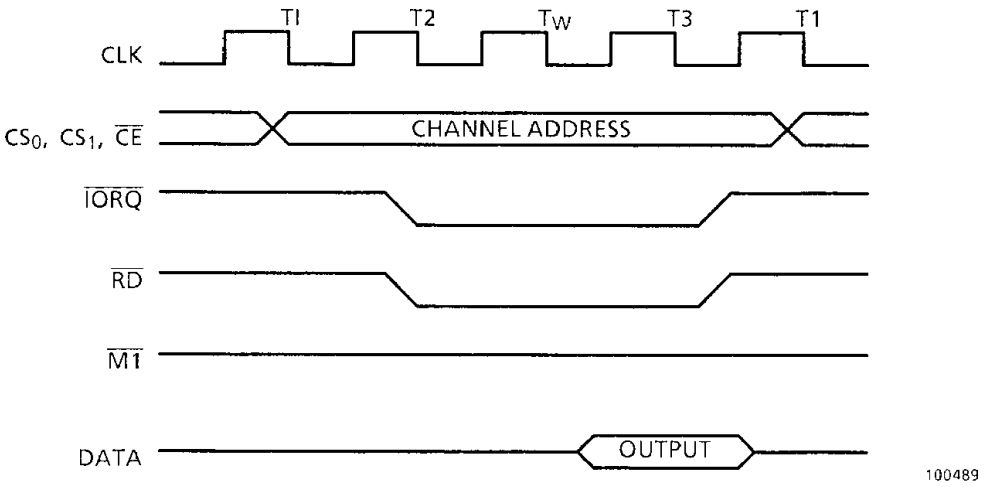

Figure 3.5 Read Timing

3.4.4 Counter mode

In the counter mode, the down-counter is decremented synchronizing with the system clock, at the edge of the pulse applied from the external circuit connected to the CLK/TRG pin. The period of the pulse to be applied to the CLK/TRG pin must be greater than 2 times the system clock period. Also, it is required to insert the setup time between the active edge of the CLK/TRG pin signal and the rising edge of the succeeding system clock. When the interval between these pulses is short, the down-counter is decremented one system clock later. When the down-counter has reached zero, a high level pulse is output from the ZC/TO pin.

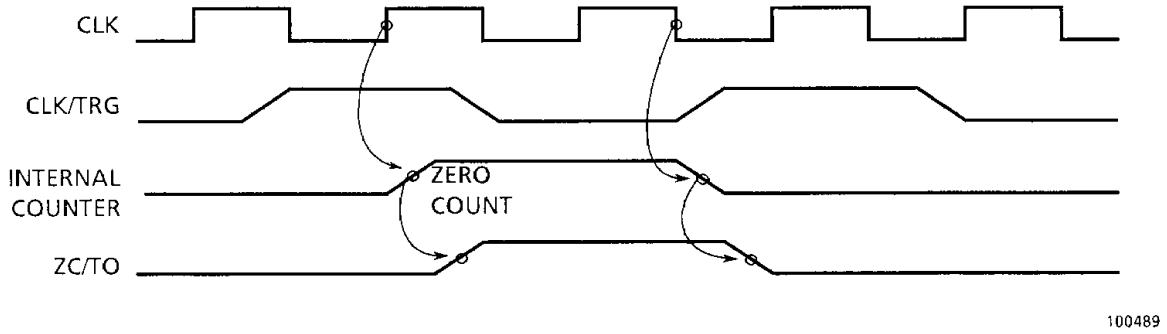

Figure 3.6 Couner Mode Timing

3.4.5 Timer mode

The timer starts operating at the second rising edge of the system clock from the rising edge of the pulse applied from the external circuit connected to the CLK/TRG pin. The period of the pulse to be apllied to the CLK/TRG pin must be greater than 2 times the system clock period. Also, it is required to insert the setup time between the active edge of the CLK/TRG pin signal and the rising edge of the succeeding system clock. When the interval between these pulses is short, the timer starts one system clock cycle later.

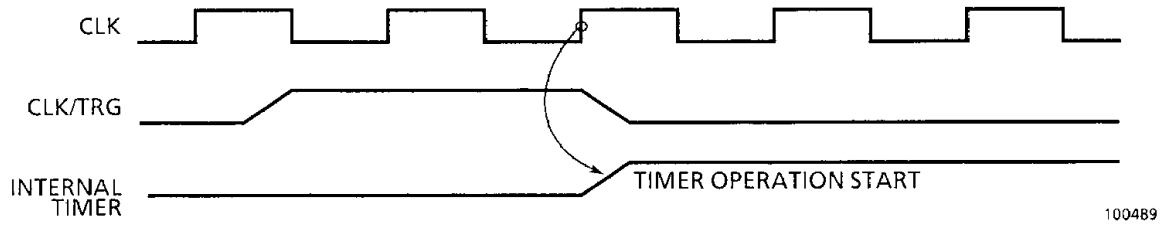

Figure 3.7 Timer Mode Timing

3.4.6 Interrupt acknowledge cycle

Having received the interrupt request signal ($\overline{INT}$) from the CTC, the MPU drives the CTC's $\overline{M1}$ pin and $\overline{IORQ}$ pin low to provide the acknowledge signal. The $\overline{IORQ}$ pin goes low 2.5 system clocks later than the $\overline{M1}$ pin. To stabilize the signal lines (IEI and IEO) in daisy chain connection, the interrupt request cannot be changed on each channel while the $\overline{M1}$ pin is low. The $\overline{RD}$ pin is held high to make distinction between the instruction fetch cycle and the interrupt acknowledge cycle. While the $\overline{RD}$ pin is high, the CTC's interrupt control circuit determines the interrupt-requesting channel of highest priority. When the CTC's IEI is high and the $\overline{M1}$ pin and $\overline{IORQ}$ pin go low, the interrupt vector is output from the interrupt requesting channel of highest priority. At this time, 2 system clock cycles are automatically inserted by the MPU as a wait state maintain the stabilization of the daisy chain connection.

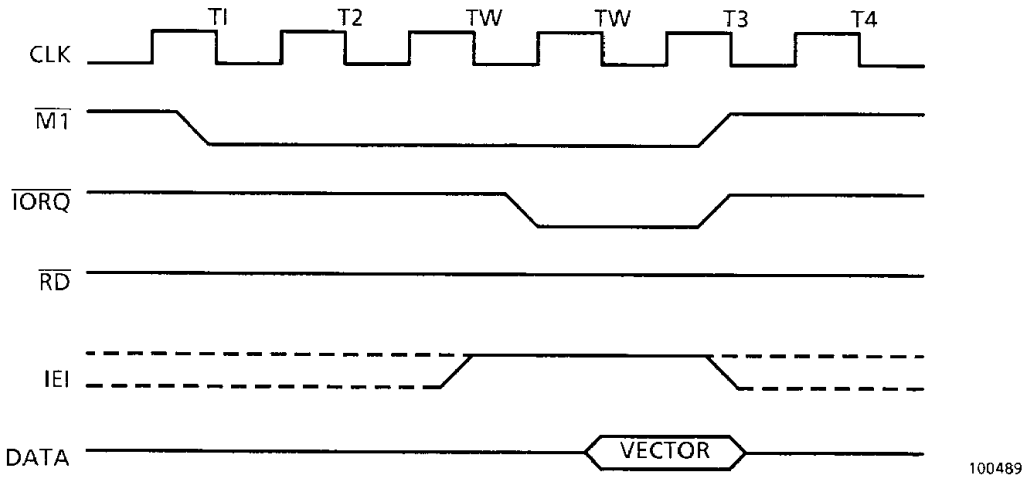

Figure 3.8 Interrupt Acknowledge Timing

3.4.7 Return from interrupt processing

Return from the interrupt processing is performed when the MPU executes the RETI instruction. This RETI instruction must be used at the end of the interrupt processing routine. When this instruction is executed by the MPU, the CTC's IEI and IEO return to the active state brfore the interrupt has been serviced.

The RETI instruction is a 2-byte instruction. Its code is EDH 4DH. The CTC decodes this instruction to check if there is the next interrupt request channel.

In the daisy chain structure, the interrupting LSI's IEI and IEO are held high and low respectively at the time the instruction code EDH has been decoded.

The code following EDH is 4DH, only the peripheral LSI which has sent the last interrupt vector (that is, the LSI whose IEI is high and IEO is low) returns from the interrupt processing. This restarts the processing of the suspended interrupt of the peripheral LSI of the next higher priority.

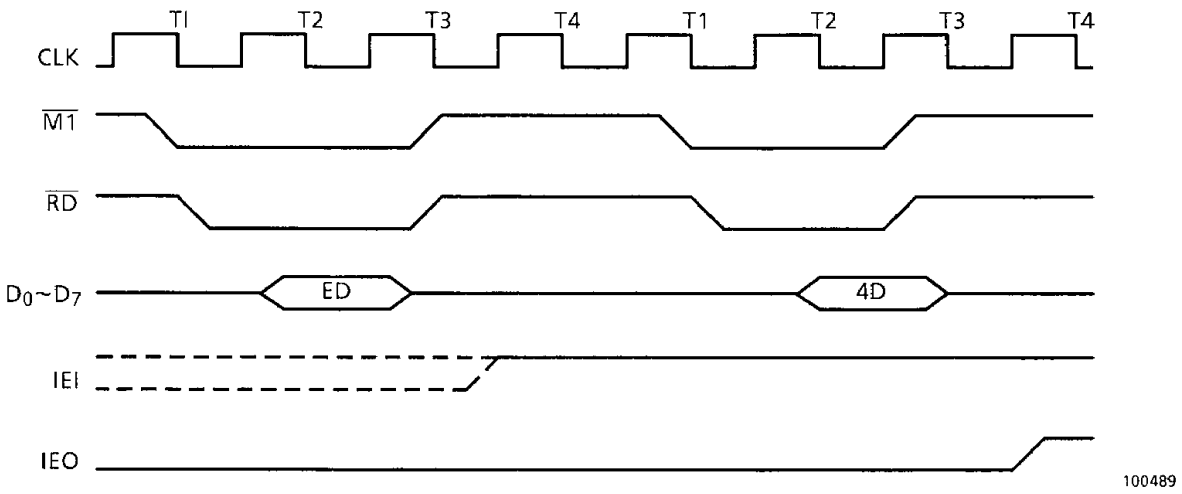

Figure 3.9 Interrupt Return Timing

3.5 CTC OPERATIONAL PROCEDURE

To operate the CTC in the counter mode or the timer mode, the channel control word and time-constant data must be written in the CTC. To enable interrupt by the channel control word, the interrupt vector must be written in the CTC.

(1) Channel control word

To write the channel control word in the CTC, the channel must be specified by the corresponding channel codes. Table 3.1 shows the channel codes.

Table 3.1 Channel codes

Channel	Input Terminal	
	CS1	CS0
0	0	0
1	0	1
2	1	0
3	1	1

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The channel control word to be written in the CTC consists of 8 bits. The system data bus D0 through D7 correspond to bit 0 through 7 respectively. Figure 3.10 shows the meaning of each bit. Table 3.2 shows the function of each bit.

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt	Counter/ timer	Prescaler	Edge	Trigger	Time constant	Stop	1

100489

Figure 3.10 Channel Control Word

For the channel control words, D0 must always be 1.

Table 3.2 Meanings and Function of Channel Control Words (1/2)

Bit	Meaning and function	
	0	1
Bit 7 (D7)	Disable channel interrupt	Enables channel interrupt. In either counter or timer mode, the interupt is requested every time the down-counter has reached zero. When this bit is set to "1", the interupt vector must be written in the CTC before the down-counter starts. When the channel control word whose D7 bit is "1" is written in an already operating channel, the interrupt occurs only when the down-counter has reached zero for the first time after the writing of the new channel control word.
Bit 6 (D6)	Puts the channel in the timer mode. Puts the system clock into the prescaler and outputs the divided signal to the down-counter.	Puts the channel in the counter mode. The down-counter is decremented for each edge trigger applied to the CLK/TRG pin. In the counter mode, the prescaler is not used.
Bit 5 (D5)	Used only in the timer mode. The prescaler is set to divide the system clock by 16.	Used only in the timer mode. The prescaler is set to divide the system clock by 256.
Bit 4 (D4)	In the timer mode, the timer operation starts on the falling edge of the trigger PULSE (CLK/TRG). In the counter mode, the down-counter is decremented on the falling edge of the external clock pulse (CLK/TRG).	In the timer mode, the timer operation sarts on the rising edge of the trigger pulse (CLK/TRG). In the counter mode, the down-counter is decremented on the rising edge of the trigger pulse (CLK/TRG).
Bit 3 (D3)	Used only in the timer mode. The timer operation sarts on the rising edge of the trigger pulse clock after a time constant is loaded onto the down-counter.	Used only in the timer mode. The timer operation is started at the leading edge of the external triger pulse that inputs 2 system clocks after a time constant is loaded onto the down-counter. When a time lag between the system clock and trigger pulse satisfies a setup time, the prescaler starts to operate from the second leading edge of the trigger pulse. If a time lag between the system clock and trigger pulse does not satisfy the setup time, the prescaler starts to operate at the leading edge of the trigger pulse after 3 system clocks. If the trigger pulse is input before loading of a time constant, the operation is the same as that when Bit 3 = 0.

100489

Figure 3.2 Meanings and Function of Channel Control Words (2/2)

Bit	Meaning and function	
	0	1
Bit 2 (D2)	This bit (0) indicates that there is no time constant written after channel control word. However, when the channel is in the reset state and this bit cannot be changed to "0" in the channel control word which is given first after the channel reset. To change other state without changing a time constant, input a channel control word with this bit changed to 0.	This bit (1) indicates that there is a time constant written immediately after a channel control word. If a time constant is written while the downcounter is operating a new time constant is set in the time constant register. The counting which is in progress is carried out continuously when the downcounter becomes zero and a new time constant is loaded onto the downcouner.
Bit 1 (D1)	Continues the current channel operation.	Stops the down-counter operation. When this bit is set to "1", the channel operation stops but all the channel control register bits remain unchanged. When bit 2 = "1" and bit 1 = "1", the channel operation remains stopped until a new time constant is written. The channel is set up after the new time constant is programmed. The channel is restarted according to the state of bit 3. When bit 2 = "0" and bit 1 = "1", the channel operation does not start until a new channel control word is written.

100489

(2) Time-constant data

In either the time mode or the counter mode, the time-constant data must be loaded into the time constant register. When bit 2 (D2) of the channel control word is "1", the time constant is loaded into the time constant register immediately after the channel control word is written. A time constant value must be an integer in a range of 1 to 256. When the 8 bits of a time constant are all "0"s, such a time constant is assumed to be 256. Figure 3.11 shows the bit configuration of time-constant data.

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

100489

Figure 3.11 Time-Constant Data

(3) Interrupt Vector

In interrupt in the MPU mode-2, the interrupting channel must give an interrupt vector to the MPU. An interrupt vector is written in the channel-0 interrupt vector register with bit 0 (D0) ="0". The vector is written in the same way as the channel control word is written on channel 0. However, bit 0 (D0) of the vector should always be "0". Bit 7 (D7) thrutgh bit 3 (D3) are user-defined values. Bit 2 (D2) and bit 1 (D1) are automatically given and contain the code of the interrupt-requesting channel having the highest priority. Table 3.3 shows the channel codes. Figure 3.12 shows the interrupt vector bit configuration.

Table 3.3 Channel Codes

Bit 2 (D2)	Bit 1 (D1)	Channel number	
0	0	0	↑ (high)
0	1	1	
1	0	2	Priority
1	1	3	↓ (low)

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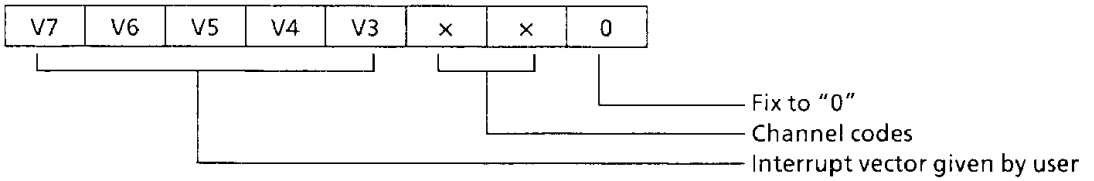

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Figure 3.12 Interrupt Vector

3.6 USING CTC

(1) Counter mode

The following describes how to use the CTC by referring to a program using channel 0 with interrupt disabled.

(a) The counter programming procedure is shown in Figure 3.13.

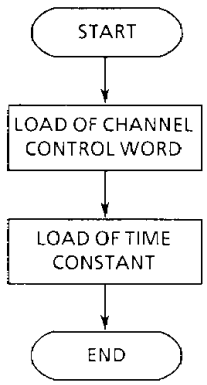

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Figure 3.13 Counter Programming Procedure

(b) The block diagram for converting the 100kHz system clock into the 10kHz equivalent is shown in Figure 3.14.

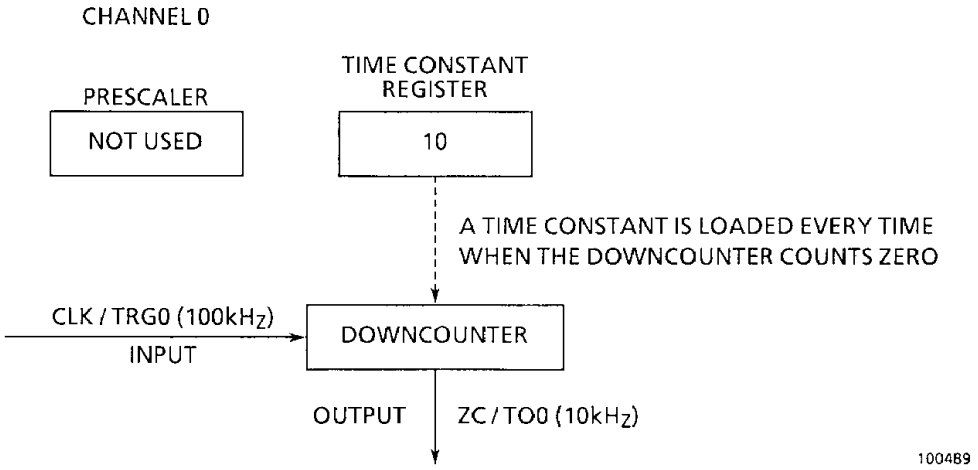


Figure 3.14 Down-Counter Block Diagram

(c) The channel control word configuration is shown in Figure 3.15.

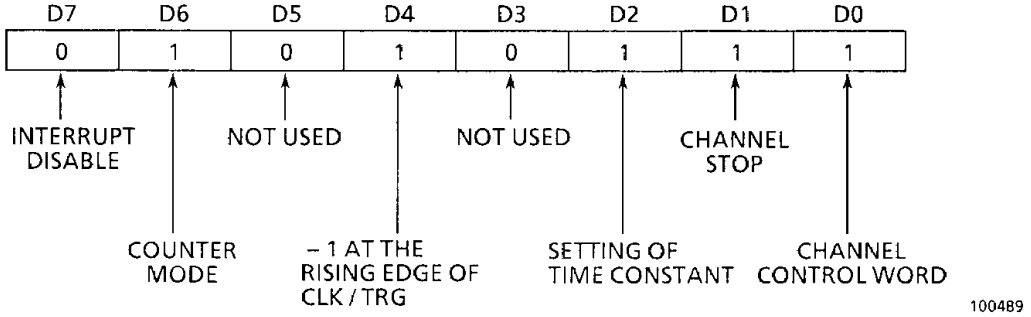


Figure 3.15 Channel Control Word Configuration

(2) Timer mode

(a) The timer programming procedure with interrupt disabled is shown in Figure 3.16

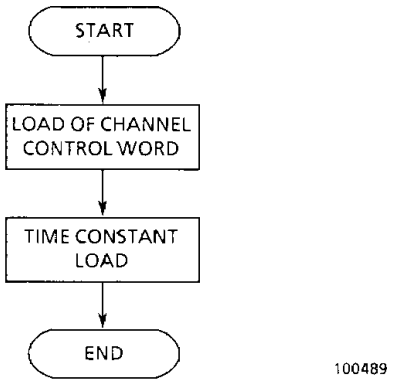


Figure 3.16 Timer Programing Procedure

(b) The block diagram for converting the 4MHz system clock into the 1 kHz equivalent is shown in Figure 3.17.

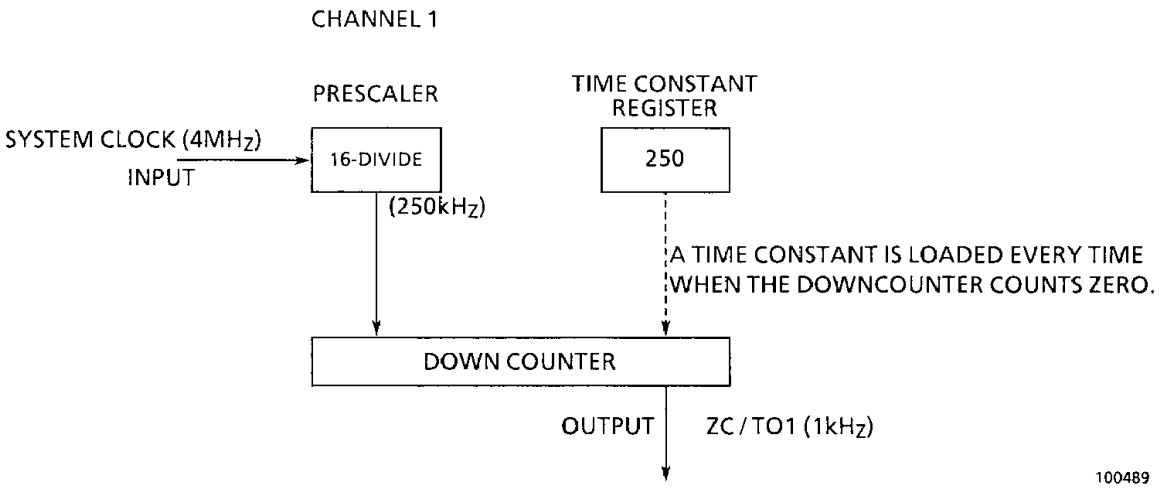


Figure 3.17 Timer Block Diagram

(c) The channel control word is shown in Figure 3.18.

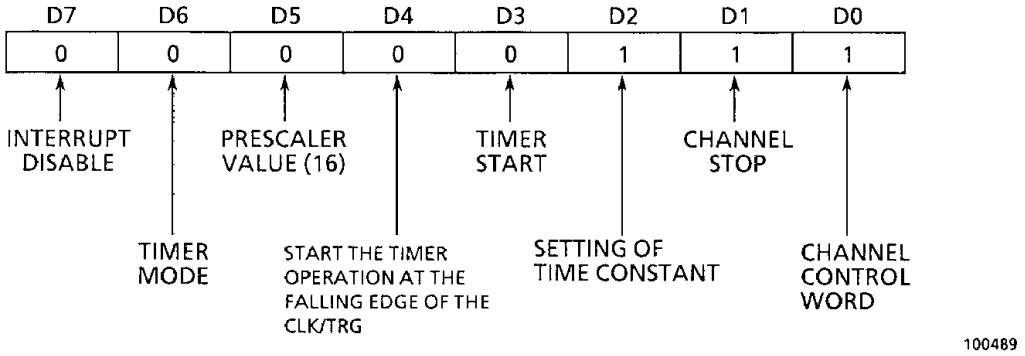


Figure 3.18 Channel Control Word

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
Vcc	Supply Voltage		−0.5 to +7	V
VIN	Input Voltage		−0.5 to Vcc + 0.5	V
PD	Power Dissipation (6MHz VERSION : TA = 85°C) (8MHz VERSION : TA = 70°C)		250	mW
TSOLDER	Soldering Temperature (10 sec)		260	°C
TSTG	Storage Temperature		−65 to 150	°C
TOPR	Operating Temperature	6MHz VERSION	−40 to 85	°C
		8MHz VERSION	−10 to 70	

050489

4.2 DC ELECTRICAL CHARACTERISTICS

6MHz VERSION : $T_A = -40°C \sim 85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$
8MHz VERSION : $T_A = -10°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage			−0.3	—	0.6	V
VIHC	High Clock Input Voltage			Vcc − 0.6	—	Vcc + 0.3	V
VIL	Low input Voltage (Except CLK)			−0.5	—	0.8	V
VIH	High input Voltage (Except CLK)			2.2	—	Vcc	V
VOL	Output Low Voltage	IOL = 2.0mA		—	—	0.4	V
VOH1	Output High Voltage (I)	IOH = −1.6mA		2.4	—	—	V
VOH2	Output High Voltage (II)	IOH = −250μA		Vcc − 0.8	—	—	V
ILI	Input Leak Current	Vss ≦ VIN ≦ Vcc		—	—	±10	μA
ILO	3-state Output Leakage Current in Float	Vss + 0.4 ≦ VOUT ≦ Vcc		—	—	±10	μA
IOHD*	Darlington Drive Current, (2)	VOH = 1.5V, REXT = 1.1KΩ Applied to ZC / TO0~ZC / TO2		−1.5	—	−5.0	mA
Icc1	Power Suuply Current	Vcc = 5V fCLK = (1) VIH = VIHC = Vcc − 0.2V VIL = VILC = 0.2V	AP-6/ AM-6/ AT-6	—	4	7	mA
			AP-8	—	5	10	
Icc2	Standby Supply Current	Vcc = 5V, CLK = VIH = Vcc − 0.2, VIL = VILC = 0.2V		—	0.5	10	μA

Note : (1) $f_{CLK} = 1 / TcC$ (MIN.)
(2) Applied to ZC / TO0, ZC / TO1 and ZC / TO2.

050489

4.3 AC ELECTRICAL CHARACTERISTICS

6MHz VERSION : $T_{OPR} = -40°C \sim 85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

8MHz VERSION : $T_A = -10°C \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$

(1/2)

NO.	SYMBOL	PARAMETER	AP-6/AM-6/AT-6 (6MHz)		AP-8 (6MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	165	DC	125	DC	ns
2	TwCh	High clock pulse width	65	DC	50	DC	ns
3	TwCl	low clock pulse width	65	DC	50	DC	ns
4	TfC	Clock falling time	—	20	—	15	ns
5	TrC	Clock rising time	—	20	—	15	ns
6	Th	Hold time	0	—	0	—	ns
7	TsCS (C)	Set-up time for clock rise	100	—	100	—	ns
8	TsCE (C)	$\overline{CE}$ Set-up time for clock rise	100	—	80	—	ns
9	TsIO (C)	Set-up time up to $\overline{IORQ}$ fall for clock rise	70	—	65	—	ns
10	TsRD (C)	Set-up time up to $\overline{RD}$ fall for clock rise	70	—	55	—	ns
11	TdC (DO)	Delay from clock rise to data output	—	130	—	110	ns
12	TdC (DOZ)	Delay from $\overline{IORQ}$, $\overline{RD}$ rise to data float	—	90	—	85	ns
13	TsDI (C)	Data input set-up time for clock rise	40	—	40	—	ns
14	TsM1 (C)	$\overline{M1}$ set-up time for clock rise	70	—	55	—	ns
15	TdM1 (IEO)	Delay from $\overline{M1}$ fall to IEO fall (in case of generating only interruption immediately before M1 cycle)	—	130	—	110	ns
16	TdI0 (DOI)	Delay from $\overline{IORQ}$ fall to data output (INTA cycle)	—	110	—	85	ns
17	TdIEI (IEOf)	Delay from IEI fall to IEO fall	—	100	—	75	ns
18	TdIEI (IEOr)	Delay from IEI rise to IEO rise (after ED decode)	—	110	—	80	ns
19	TdC (INT)	Delay from clock rise to $\overline{INT}$ fall	—	(1) + 120	—	(1) + 100	ns
20	TdCLK (INT)	Delay from CLK/TRG rise to $\overline{INT}$ fall (Counter mode) tsCTR (C) Satisfied tsCTR (C) not Satisfied	 — —	 (19) + (26) (1) + (19) + (26)	 — —	 (19) + (26) (1) + (19) + (26)	 ns ns

050489

(2/2)

NO.	SYMBOL	PARAMETER	AP-6/AM-6/AT-6 (6MHz)		AP-8 (8MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	
21	TcCTR	CLK / TRG Frequency (COUNT MODE)	2TcC	—	2TcC	—	ns
22	TrCTR	CLK / TRG rising time	—	40	—	30	ns
23	TfCTR	CLK / TRG falling time	—	40	—	30	ns
24	TwCTRl	Low CLK/TRG pulse width	120	—	90	—	ns
25	TwCTRh	High CLK/TRG pulse width	120	—	90	—	ns
26	TsCTR (Cs)	Set-up time up to CLK/TRG rise for clock rise requiring immediate count (counter mode)	150	—	110	—	ns
27	TsCTR (Ct)	Set-up time up to CLK/TRG rise for clock rise requiring immediate start of prescaler (timer mode)	150	—	110	—	ns
28	TdC (ZC / TOr)	Delay from clock rise to ZC/TO rise	—	140	—	110	ns
29	TdC (ZC / TOf)	Delay from clock fall to ZC/TO fall	—	140	—	110	ns

050489

Note 1 : AC test condition
VIH = 2.4V, VIHC = V_{CC}-0.6V, VIL = 0.4V, VOH = 2.2V, VOL = 0.8V CL = 100pF

Note 2 : If the daisy chain is at N stage,
2.5TcC > (N-2) TdIEI (IEOf) + TdM1 (IEO) + TsIEI + TTL buffer delay must be satisfied.

Note 3 : (1) : Tcc, (19) : Tdc (INT), (26) : TsCTR (Cs)

4.4 CAPACITANCE

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f = 1MHz All terminals except that to be measured should be earthed.	—	—	5	pF
CIN	Input Capacitance		—	—	6	pF
COUT	Output Capacitance		—	—	10	pF

050489

4.5 AC TIMING CHARTS

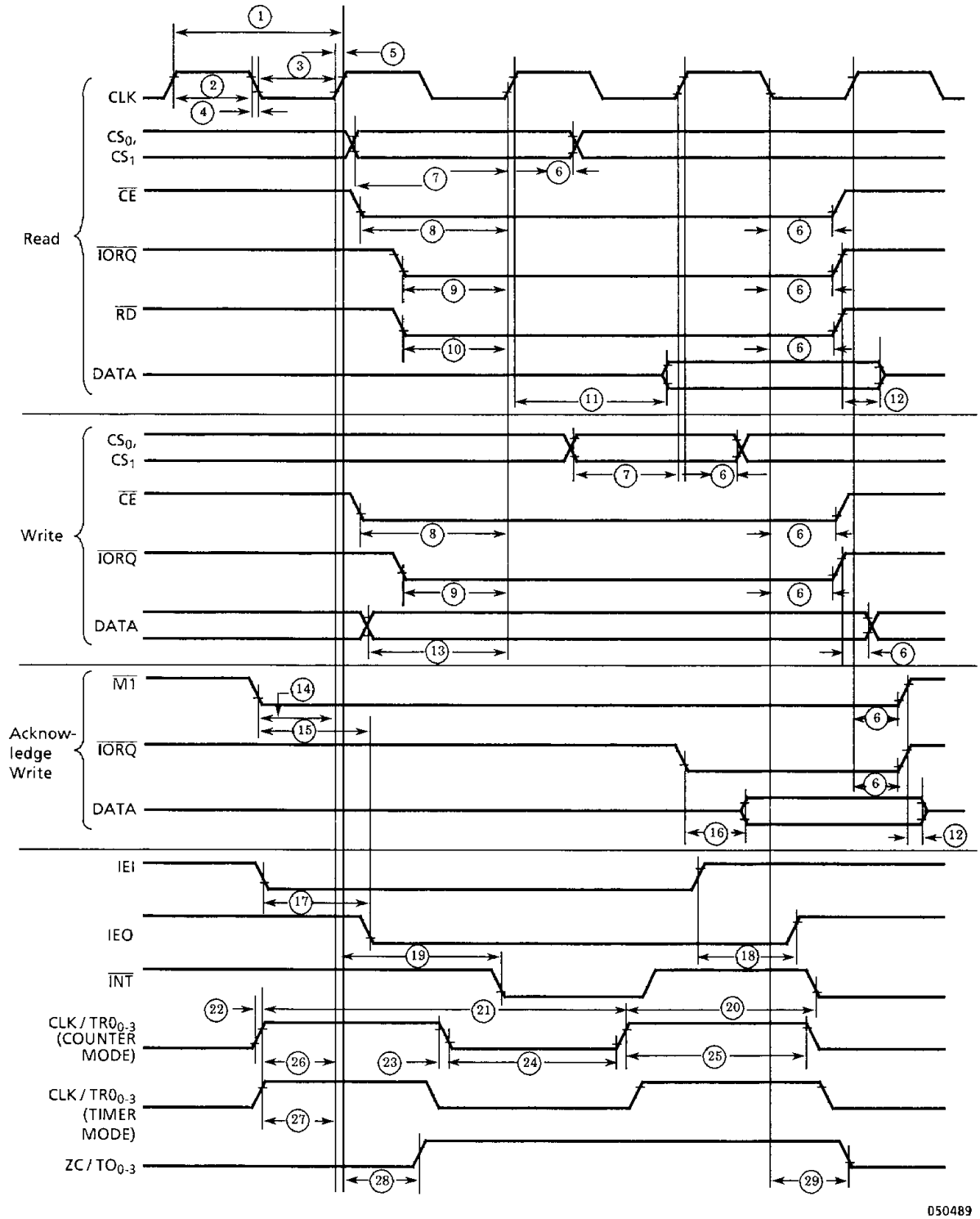


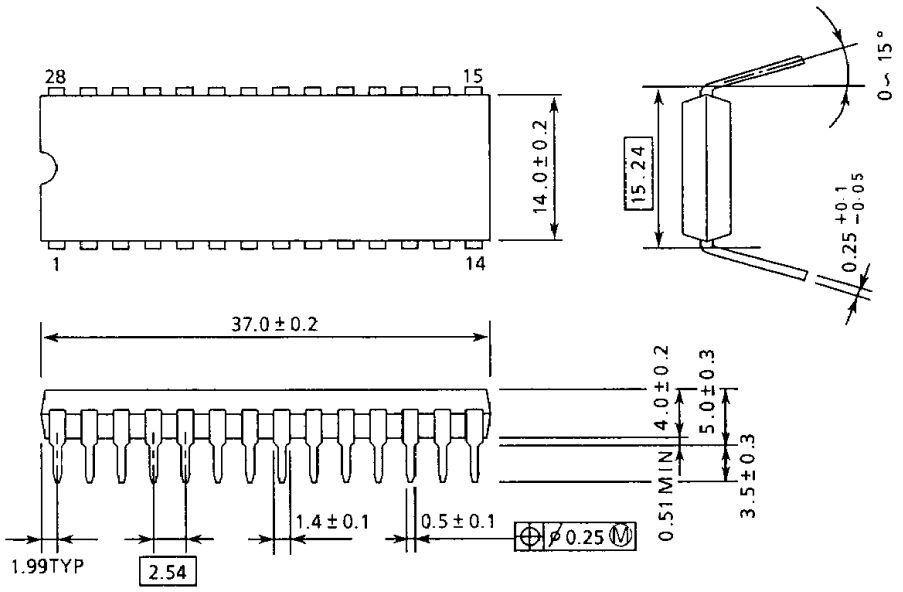
Figure 4.1 Timing Diagram

5. PACKAGE DIMENSION

5.1 DIP PACKAGE

DIP28-P-600

Unit : mm



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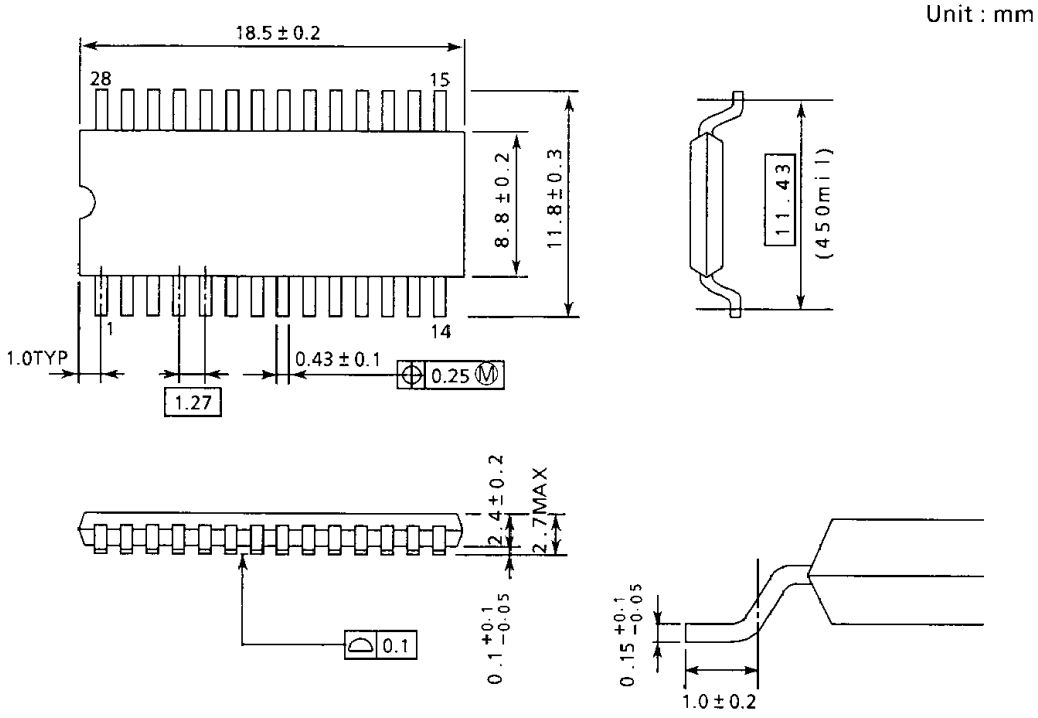
Note 1 : This dimension is measured at the center of bending points of leads.

Note 2 : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.28 leads.

5.2 SOP PACKAGE

SOP28-P-450

Unit : mm

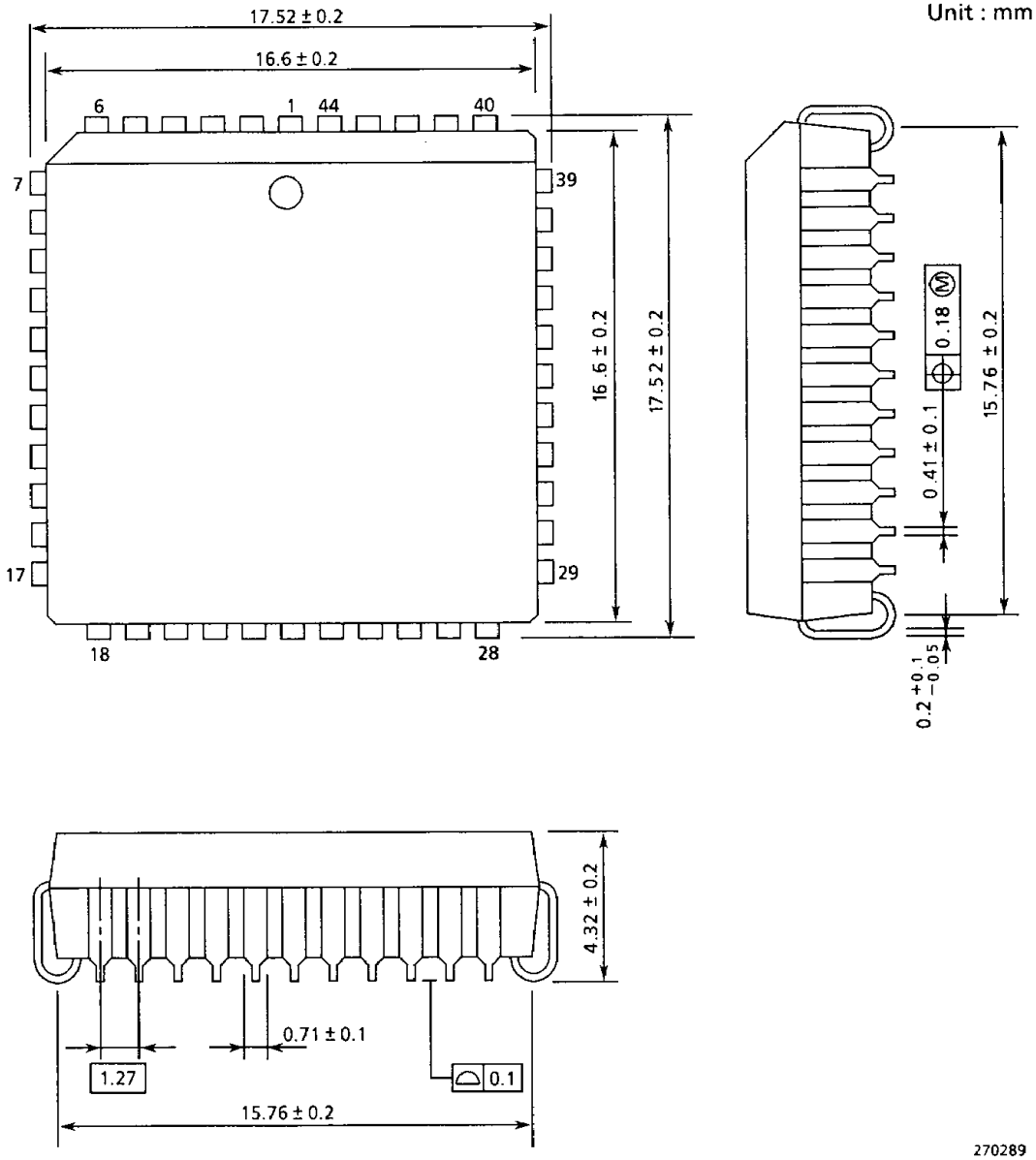


Note : Package Width and length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

5.3 44-PIN PLCC PACKAGE

QFJ44-P-S650

Unit : mm



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