19-4793; Rev 2; 11/03

MAXIM

Low-Voltage, Quad, SPST CMOS Analog Switches

General Description

The MAX4610/MAX4611/MAX4612 are quad, low-voltage, single-pole/single-throw (SPST) analog switches. On-resistance (100Ω, max) is matched between switches to 4Ω, max and is flat (4Ω, max) over the specified signal range. Each switch handles V+ to GND analog signal levels. Maximum off-leakage current is only 1nA at T_A = +25°C and 2nA at T_A = +85°C.

The MAX4610 has four normally open (NO) switches, and the MAX4611 has four normally closed (NC) switches. The MAX4612 has two NO switches and two NC switches. These CMOS switches operate from a single +2V to +12V supply. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

Applications

Battery-Operated Equipment

Audio/Video Signal Routing

Low-Voltage Data-Acquisition Systems

Sample-and-Hold Circuits

Communication Circuits

Features

- **Offered in Automotive Temperature Range (-40°C to +125°C)**
- **Guaranteed On-Resistance**
  100Ω max (5V Supply)
  46Ω max (12V Supply)
- **Guaranteed Match Between Channels (4Ω, max)**
- **Guaranteed Flatness Over Signal Range (18Ω, max)**
- **Off-Leakage Current Over Temperature <2nA at T_A = +85°C**
- **>2kV ESD Protection per Method 3015.7**
- **Rail-to-Rail® Signal Handling**
- **TTL/CMOS-Logic Compatible**

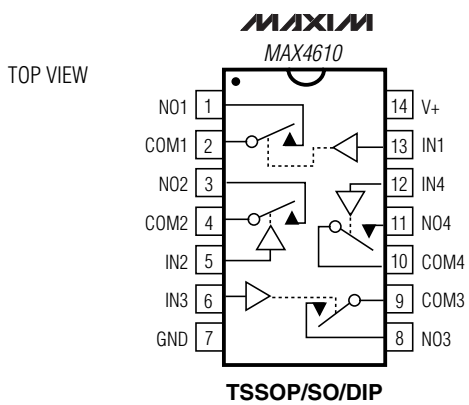
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4610CUD	0°C to +70°C	14 TSSOP
MAX4610CSD	0°C to +70°C	14 Narrow SO
MAX4610CPD	0°C to +70°C	14 Plastic DIP
MAX4610C/D	0°C to +70°C	Dice*
MAX4610EGE	-40°C to +85°C	16 QFN
MAX4610EUD	-40°C to +85°C	14 TSSOP
MAX4610ESD	-40°C to +85°C	14 Narrow SO
MAX4610EPD	-40°C to +125°C	14 Plastic DIP

Ordering Information continued at end of data sheet.

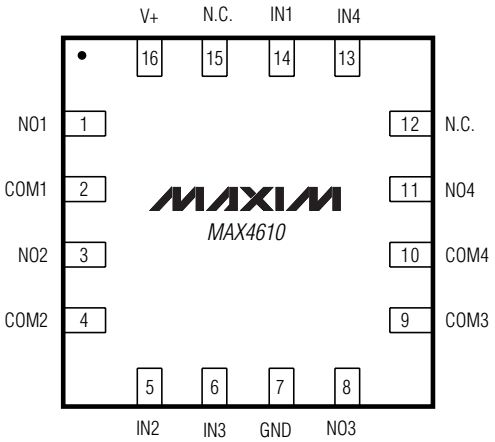
**Contact factory for dice specifications.*

Pin Configurations/Truth Tables



TSSOP/SO/DIP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON



QFN

MAX4611/MAX4612 Pin Configurations/Truth Tables appear at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-Voltage, Quad, SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
V+ .....-0.3V to +13V
IN_, COM_, NO_, NC_ (Note 1).....-0.3V to (V + +0.3V)
Continuous Current (any terminal)
(pulsed at 1ms, 10% duty cycle) 20mA
Peak Current (any terminal)
(pulsed at 1ms, 10% duty cycle) 40mA
ESD per Method 3015.7.....>2kV

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 6.3mW/°C above +70°C) 500mW
14-Pin Narrow SO (derate 8.00mW/°C above +70°C) ..640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
16-Pin QFN (derate 18.5mW/°C above +70°C) 1481mW
Operating Temperature Ranges
MAX461_C_ _ .....0°C to +70°C
MAX461_E_ _.....-40°C to +85°C
MAX461_A_ _ .....-40°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NO_, NC_, COM_, or IN_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ = $V_{NC\_}$ = 3V	T_A = +25°C		70	100	Ω
			T_A = T_{MIN} to T_{MAX}			150	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.5V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ = $V_{NC\_}$ = 3V	T_A = +25°C		1.0	4	Ω
			T_A = T_{MIN} to T_{MAX}			8	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 4.5V; $I_{COM\_}$ = 1mA; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 2V, 1V	T_A = +25°C		12	18	Ω
			T_A = T_{MIN} to T_{MAX}			25	
NO or NC Off-Leakage Current (Note 6)	$I_{NO(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; V_{NO} = 4.5V, 1V	T_A = +25°C	-0.1		0.1	nA
			T_A = -40°C to +85°C	-2		2	
			T_A = -40°C to +125°C	-30		30	
COM Off-Leakage Current (Note 6)	$I_{COM(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ = $V_{NC\_}$ = 4.5V, 1V	T_A = +25°C	-0.1		0.1	nA
			T_A = -40°C to +85°C	-2		2	
			T_A = -40°C to +125°C	-30		30	
COM On-Leakage Current (Note 6)	$I_{COM(ON)}$	V+ = 5.5V; V_{COM} = 1V, 4.5V; $V_{NO\_}$ = $V_{NC\_}$ = 1V, 4.5V, or floating	T_A = +25°C	-0.2		0.2	nA
			T_A = -40°C to +85°C	-4		4	
			T_A = -40°C to +125°C	-30		30	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Input Current with Input Voltage High	I_{IN_H}	$V_{IN\_}$ = 2.4V, all others = 0.8V		-0.1	0.001	0.1	µA
Input Current with Input Voltage Low	I_{IN_L}	$V_{IN\_}$ = 0.8V, all others = 2.4V		-0.1	0.001	0.1	µA
Input High Voltage	V_{IN_H}			2.4	1.5		V
Input Low Voltage	V_{IN_L}				1.4	0.8	V
DYNAMIC (Note 3)							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 3V, Figure 2	T_A = +25°C		35	60	ns
			T_A = T_{MIN} to T_{MAX}			80	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 3V, Figure 2	T_A = +25°C		15	20	ns
			T_A = T_{MIN} to T_{MAX}			30	
On-Channel Bandwidth	BW	Signal = 0dBm, Figure 4, 50Ω in and out	T_A = +25°C		300		MHz
Charge Injection	V_{CTE}	C_L = 1.0nF, V_{GEN} = 0, R_{GEN} = 0, Figure 3	T_A = +25°C		1	5	pC
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		-60		dB
Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		-80		dB
NO_ or NC_ Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		16		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		16		pF
COM_ On-Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6	T_A = +25°C		23		pF
Total Harmonic Distortion	THD	600Ω IN and OUT, 20Hz to 20kHz, 2Vp-p	T_A = +25°C		0.009		%
SUPPLY							
Power-Supply Range				2		12	V
Supply Current	I+	V_{IN} = 0 or V+, all switches on or off		-1	0.001	1	µA

Low-Voltage, Quad, SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3V, V_{IN_H} = 2.4V, V_{IN_L} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ = $V_{NC\_}$ = 1V	T_A = +25°C		175	360	Ω
			T_A = T_{MIN} to T_{MAX}			450	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ = $V_{NC\_}$ = 1V	T_A = +25°C		2	5	Ω
			T_A = T_{MIN} to T_{MAX}			10	
NO_ or NC_ Off-Leakage Current (Notes 3, 6)	$I_{NO(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 0.5V	T_A = +25°C	-0.1		0.1	nA
			T_A = -40°C to + 85°C	-2		2	
			T_A = -40°C to + 125°C	-30		30	
COM_ Off-Leakage Current (Notes 3, 6)	$I_{COM(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 0.5V	T_A =+25°C	-0.1		0.1	nA
			T_A = -40°C to + 85°C	-2		2	
			T_A = -40°C to + 125°C	-30		30	
COM_On-Leakage Current (Notes 3, 6)	$I_{COM(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.5V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 0.5V, 3V, or floating	T_A = +25°C	-0.2		0.2	nA
			T_A = -40°C to +85°C	-4		4	
			T_A = -40°C to +125°C	-30		30	
LOGIC INPUTS							
Input High Voltage	V_{IN_H}			2.4	1.0		V
Input Low Voltage	V_{IN_L}				1.0	0.5	V
DYNAMIC (Note 3)							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 1.5V, Figure 2	T_A = +25°C		50	90	ns
			T_A = -40°C to +85°C			120	
			T_A = -40°C to +125°C			140	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 1.5V, Figure 2	T_A = +25°C		30	45	ns
			T_A = T_{MIN} to T_{MAX}			60	

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +12V, V_{IN_H} = 4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$,			0		V+	V
On-Resistance	R_{ON}	V+ = 12V, I_{COM} = 2mA, $V_{NO\_}$ = $V_{NC\_}$ = 10V	T_A = +25°C		30	45	Ω
			T_A = T_{MIN} to T_{MAX}			60	
LOGIC INPUTS							
Input High Voltage	V_{IN_H}			4.0	2.8		V
Input Low Voltage	V_{IN_L}				2.5	0.8	V
SUPPLY							
Positive Supply Current	I+	$V_{IN\_}$ = 0 or V+, all switches on or off		-1	0.001	1	µA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = R_{ON} (max) - R_{ON} (min).

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 6: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at +25°C.

Note 7: Off-Isolation = $20\log_{10}$ ($V_{COM\_}$ / $V_{NO\_}$), $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.

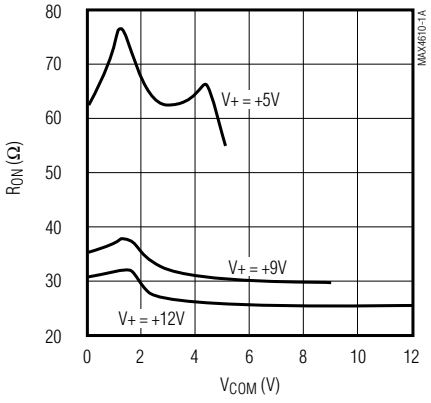
Note 8: Between any two switches.

Low-Voltage, Quad, SPST CMOS Analog Switches

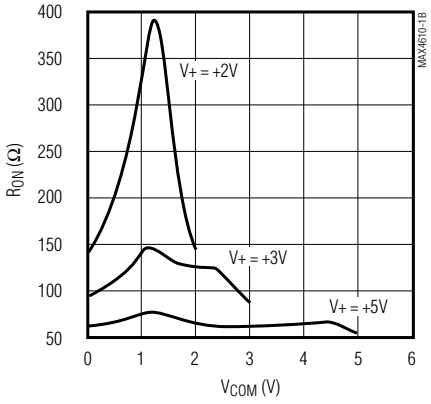
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

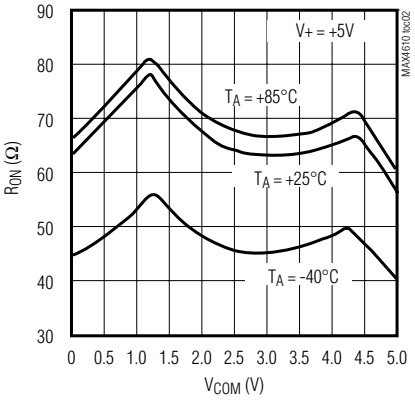
ON-RESISTANCE vs. V_{COM}



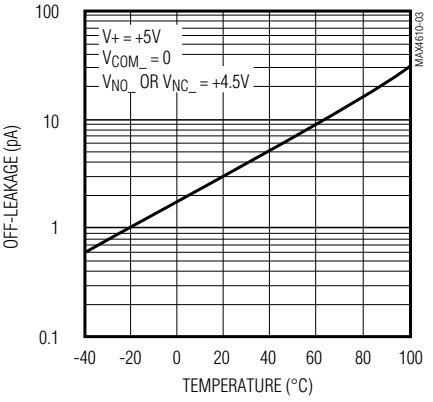
ON-RESISTANCE vs. V_{COM}



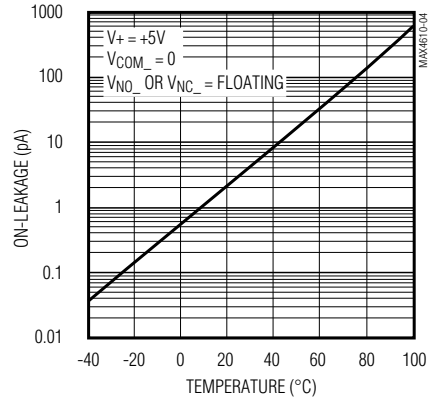
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



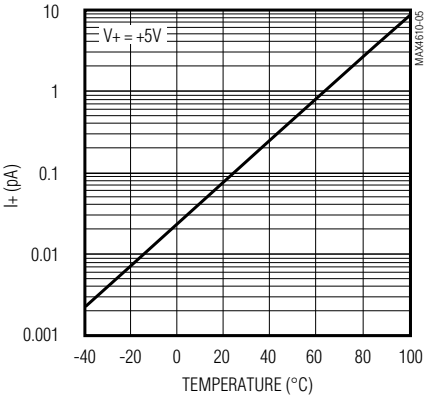
OFF-LEAKAGE vs. TEMPERATURE



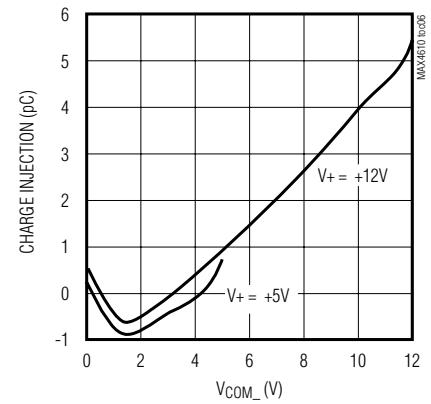
ON-LEAKAGE vs. TEMPERATURE



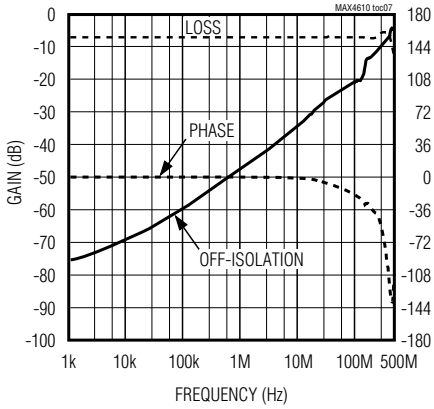
SUPPLY CURRENT vs. TEMPERATURE



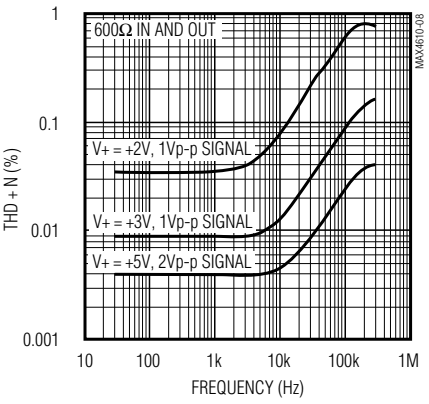
CHARGE INJECTION vs. V_{COM}



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



Pin Description

PIN						NAME	FUNCTION
MAX4610		MAX4611		MAX4612			
TSSOP/SO/ DIP	QFN	TSSOP/SO/DIP	QFN	TSSOP/SO/DIP	QFN		
1, 3, 8, 11	1, 3, 8, 11	—	—	—	—	NO1–NO4	Analog Switch Normally Open Terminals
—	—	1, 3, 8, 11	1, 3, 8, 11	—	—	NC1–NC4	Analog Switch Normally Closed Terminals
—	—	—	—	1, 8	1, 8	NO1, NO3	Analog Switch Normally Open Terminals
—	—	—	—	3, 11	3, 11	NC2, NC4	Analog Switch Normally Closed Terminals
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	COM1–COM4	Analog Switch Common Terminals
13, 5, 6, 12	14, 5, 6, 13	13, 5, 6, 12	14, 5, 6, 13	13, 5, 6, 12	14, 5, 6, 13	IN1–IN4	Logic-Control Digital Input
7	7	7	7	7	7	GND	Ground. Connect to digital ground.
—	12, 15	—	12, 15	—	12, 15	N.C.	No Connection. Not internally connected.
14	16	14	16	14	16	V+	Positive Analog and Digital-Supply Voltage Input. Internally connected to substrate.

Applications Information

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to 20mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 13V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

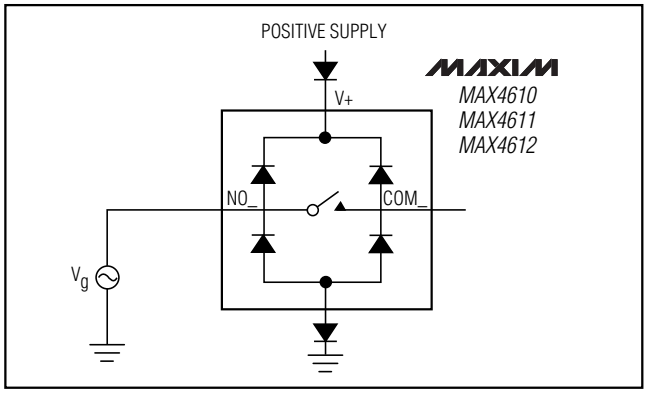


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Low-Voltage, Quad, SPST CMOS Analog Switches

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Operating Considerations for High-Voltage Supply

The MAX4610/MAX4611/MAX4612 are pin-compatible with the industry-standard 74HC4066 and the MAX4066, and are optimized for +5V single-supply operation. The MAX4610 family is capable of +12V single-supply operation with some precautions. The absolute maximum rating for V+ is +13.2V (referenced to GND). When operating near this region, bypass V+ with a minimum 0.1µF capacitor to ground as close to the IC as possible.

Caution: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or 12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4610/MAX4611/MAX4612. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Test Circuits/Timing Diagrams

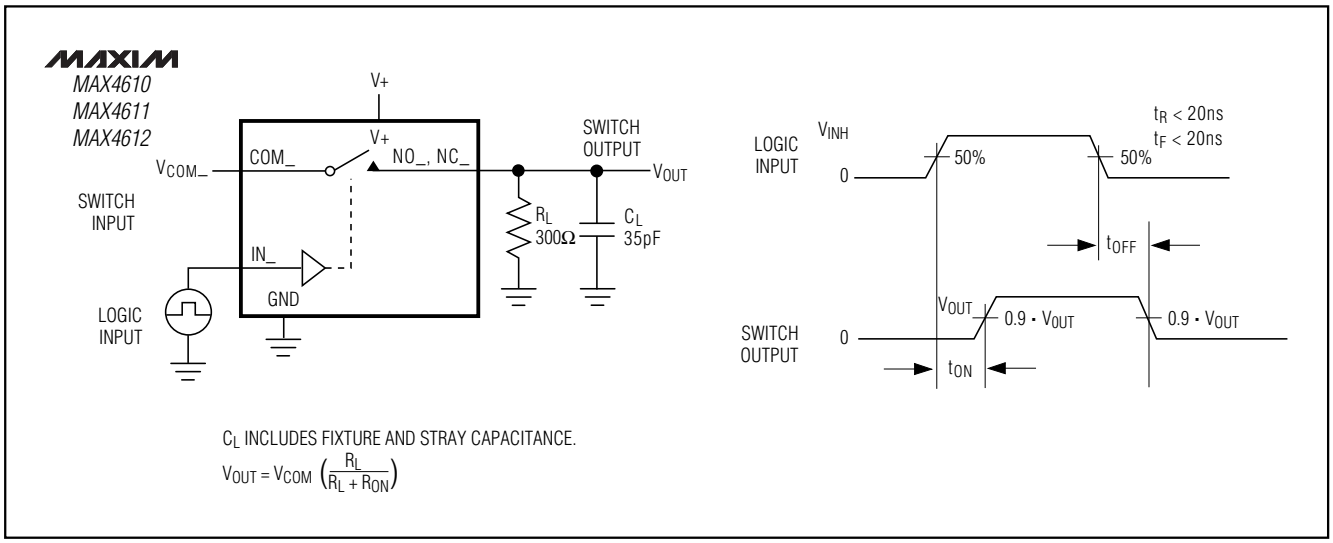


Figure 2. Switching Time

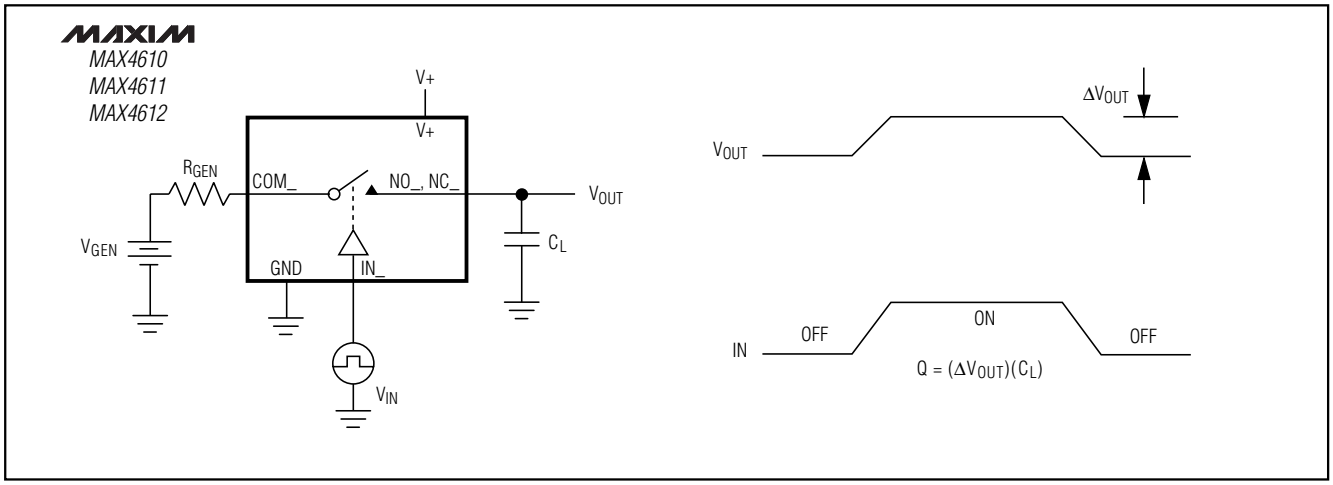


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

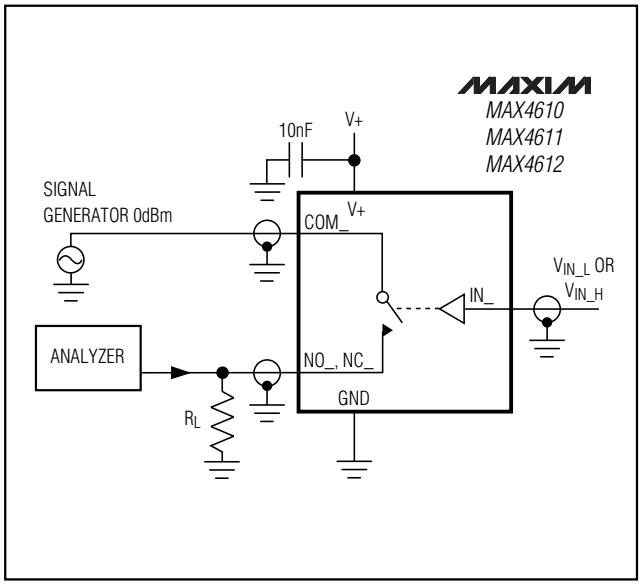


Figure 4. Off-Isolation/On-Channel Bandwidth

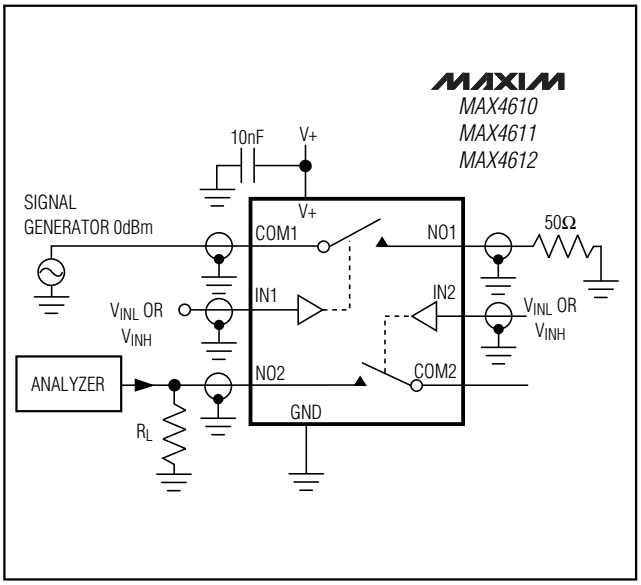


Figure 5. Crosstalk

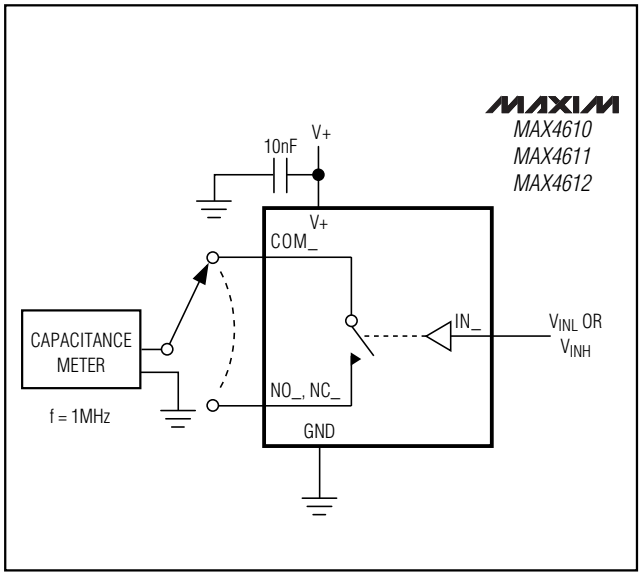


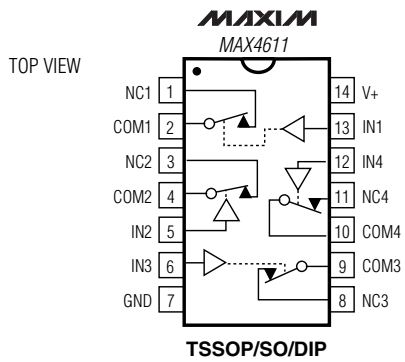
Figure 6. Channel Off/On-Capacitance

PART	TEMP RANGE	PIN-PACKAGE
MAX4610ASD	0°C to +70°C	-40°C to +125°C
MAX4611CUD	0°C to +70°C	14 TSSOP
MAX4611CSD	0°C to +70°C	14 Narrow SO
MAX4611CPD	0°C to +70°C	14 Plastic DIP
MAX4611C/D	0°C to +70°C	Dice*
MAX4611EGE	-40°C to +85°C	16 QFN
MAX4611EUD	-40°C to +85°C	14 TSSOP
MAX4611ESD	-40°C to +85°C	14 Narrow SO
MAX4611EPD	-40°C to +85°C	14 Plastic DIP
MAX4611AUD	-40°C to +125°C	14 TSSOP
MAX4611ASD	-40°C to +125°C	14 Narrow SO
MAX4612CUD	0°C to +70°C	14 TSSOP
MAX4612CSD	0°C to +70°C	14 Narrow SO
MAX4612CPD	0°C to +70°C	14 Plastic DIP
MAX4612C/D	0°C to +70°C	Dice*
MAX4612EUD	-40°C to +85°C	14 TSSOP
MAX4612ESD	-40°C to +85°C	14 Narrow SO
MAX4612EGE	-40°C to +85°C	16 QFN
MAX4612EPD	-40°C to +85°C	14 Plastic DIP
MAX4612AUD	-40°C to +125°C	14 TSSOP
MAX4612ASD	-40°C to +125°C	14 Narrow SO

**Contact factory for dice specifications.*

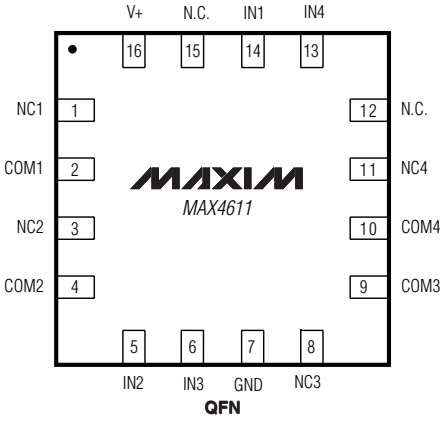
Low-Voltage, Quad, SPST CMOS Analog Switches

Pin Configurations/Truth Tables (continued)

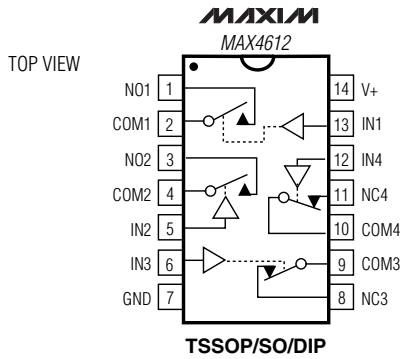


TSSOP/SO/DIP

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

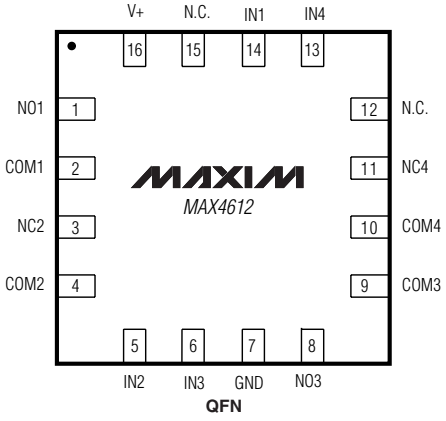


QFN



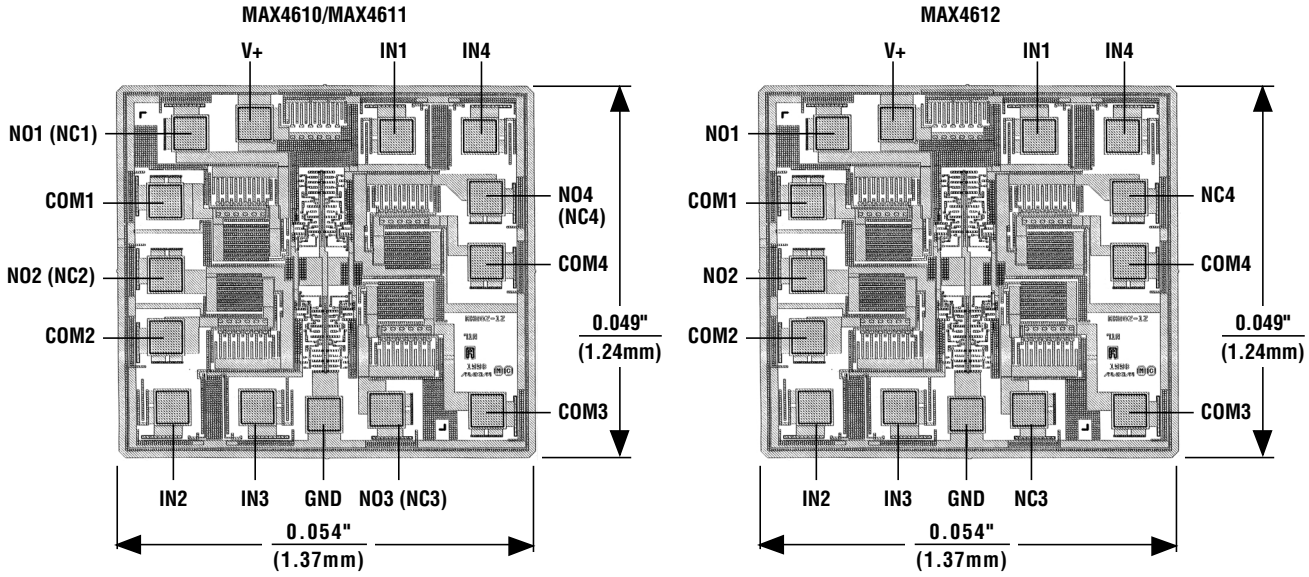
TSSOP/SO/DIP

INPUT	NO1, NO2	NC3, NC4
LOW	OFF	ON
HIGH	ON	OFF



QFN

Chip Topographies



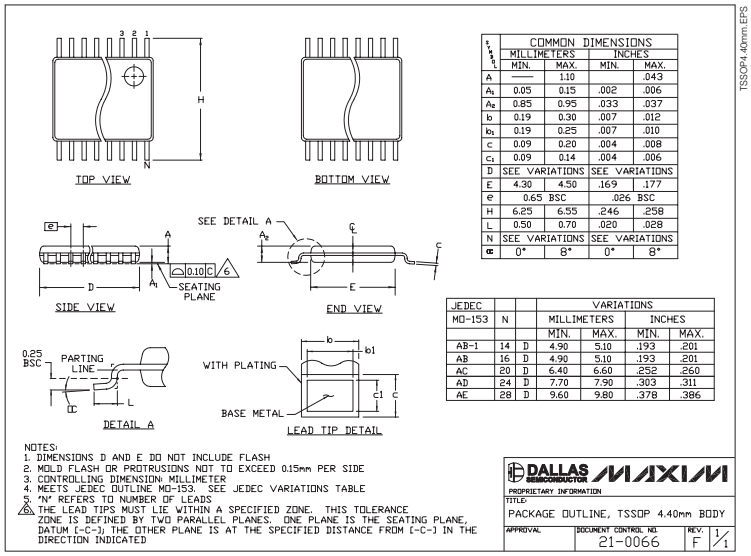
( ) ARE FOR MAX4611

TRANSISTOR COUNT: 132

SUBSTRATE CONNECTED TO V+

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

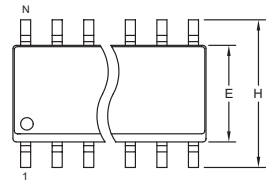
JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

Low-Voltage, Quad, SPST CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

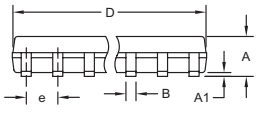


TOP VIEW

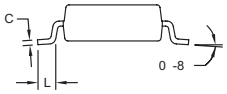
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

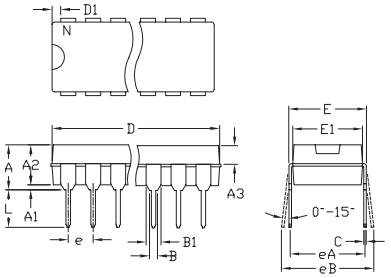
DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

PDIPN.EPS



	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

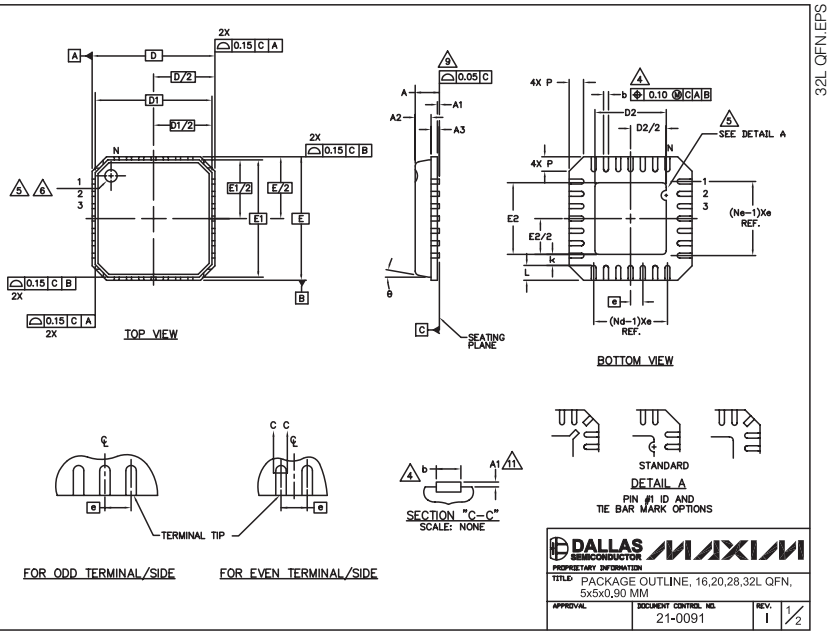
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 D

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV. I | 1/2

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV. I | 2/2

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