128-MBit Synchronous DRAM

- High Performance:

	-7	-7.5	-8	Units
f_{CK}	143	133	125	MHz
t_{CK3}	7	7.5	8	ns
t_{AC3}	5.4	5.4	6	ns
t_{CK2}	7.5	10	10	ns
t_{AC2}	5.4	6	6	ns

- Single Pulsed $\overline{RAS}$ Interface
- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write Control (x4, x8)
- Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 4096 Refresh Cycles / 64 ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface
- Plastic Packages: P-TSOPII-54 400mil x 875 mil width (x4, x8, x16)
- -7 for PC 133 2-2-2 applications
  -7.5 for PC 133 3-3-3 applications
  -8 for PC100 2-2-2 applications

The HYB 39S128400/800/160CT are four bank Synchronous DRAM's organized as 4 banks × 8MBit x4, 4 banks × 4MBit x8 and 4 banks × 2Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated using the Infineon advanced 0.17 micron process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

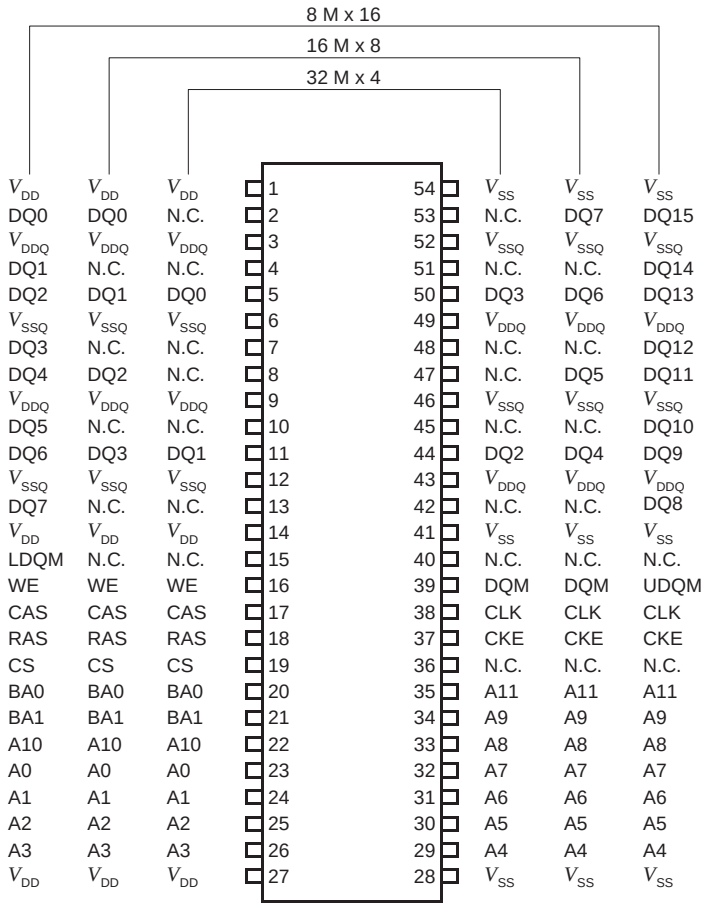
Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply and are available in TSOPII packages.

Ordering Information

Type	Function Code	Package	Description
HYB 39S128400CT-7	PC133-222-520	P-TSOP-54 (400mil)	143MHz 4B × 8M x4 SDRAM
HYB 39S128400CT-7.5	PC133-333-520	P-TSOP-54 (400mil)	133 MHz 4B × 8M x4 SDRAM
HYB 39S128400CT-8	PC100-222-620	P-TSOP-54 (400mil)	100 MHz 4B × 8M x4 SDRAM
HYB 39S128800CT-7	PC133-222-520	P-TSOP-54 (400mil)	143 MHz 4B × 4M x8 SDRAM
HYB 39S128800CT-7.5	PC133-333-520	P-TSOP-54 (400mil)	133 MHz 4B × 4M x8 SDRAM
HYB 39S128800CT-8	PC100-222-620	P-TSOP-54 (400mil)	100 MHz 4B × 4M x8 SDRAM
HYB 39S128160CT-7	PC133-222-520	P-TSOP-54 (400mil)	143 MHz 4B × 2M x16 SDRAM
HYB 39S128160CT-7.5	PC133-333-520	P-TSOP-54 (400mil)	133 MHz 4B × 2M x16 SDRAM
HYB 39S128160CT-8	PC100-222-620	P-TSOP-54 (400mil)	100 MHz 4B × 2M x16 SDRAM
HYB 39S128160CTL-8	PC100-222-620	P-TSOP-54 (400mil)	100 MHz 4B × 2M x16 SDRAM Low Power (“L”) version
HYB 39S128160CTL-7.5	PC133-333-520	P-TSOP-54 (400mil)	133 MHz 4B × 2M x16 SDRAM Low Power (“L”) version

Pin Definitions and Functions

CLK	Clock Input	DQ	Data Input/Output
CKE	Clock Enable	DQM, LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQ’s (+ 3.3 V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQ’s
A0 - A11	Address Inputs	N.C.	Not connected
BA0, BA1	Bank Select		

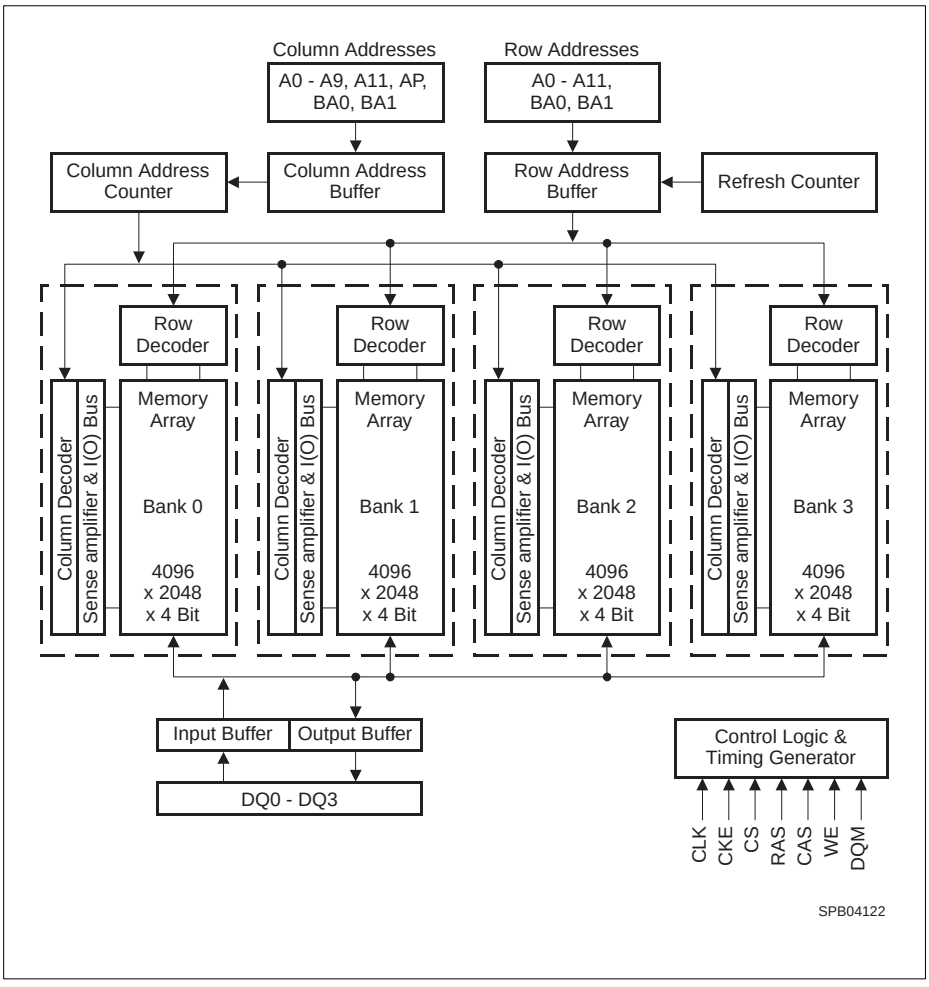


TSOPII-54 (10.16 mm x 22.22 mm, 0.8 mm pitch)

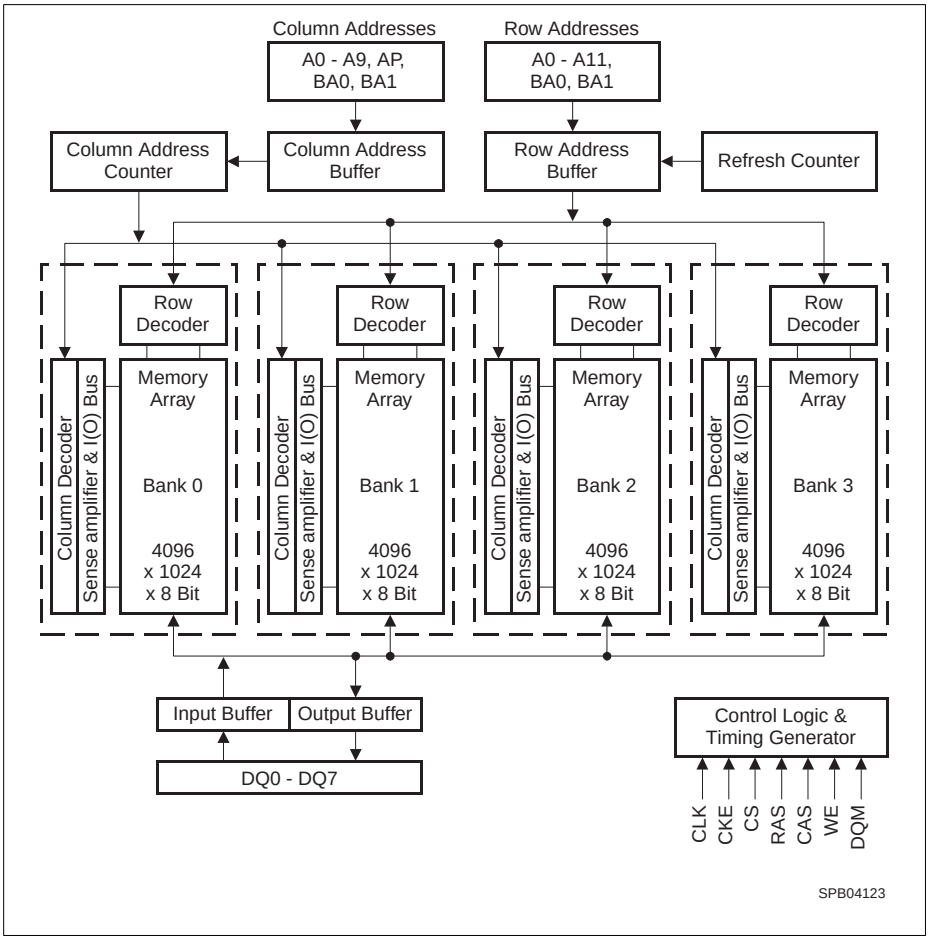
SPP04121

Pin Configuration for x4, x8 & x16 Organized 128M-DRAMs

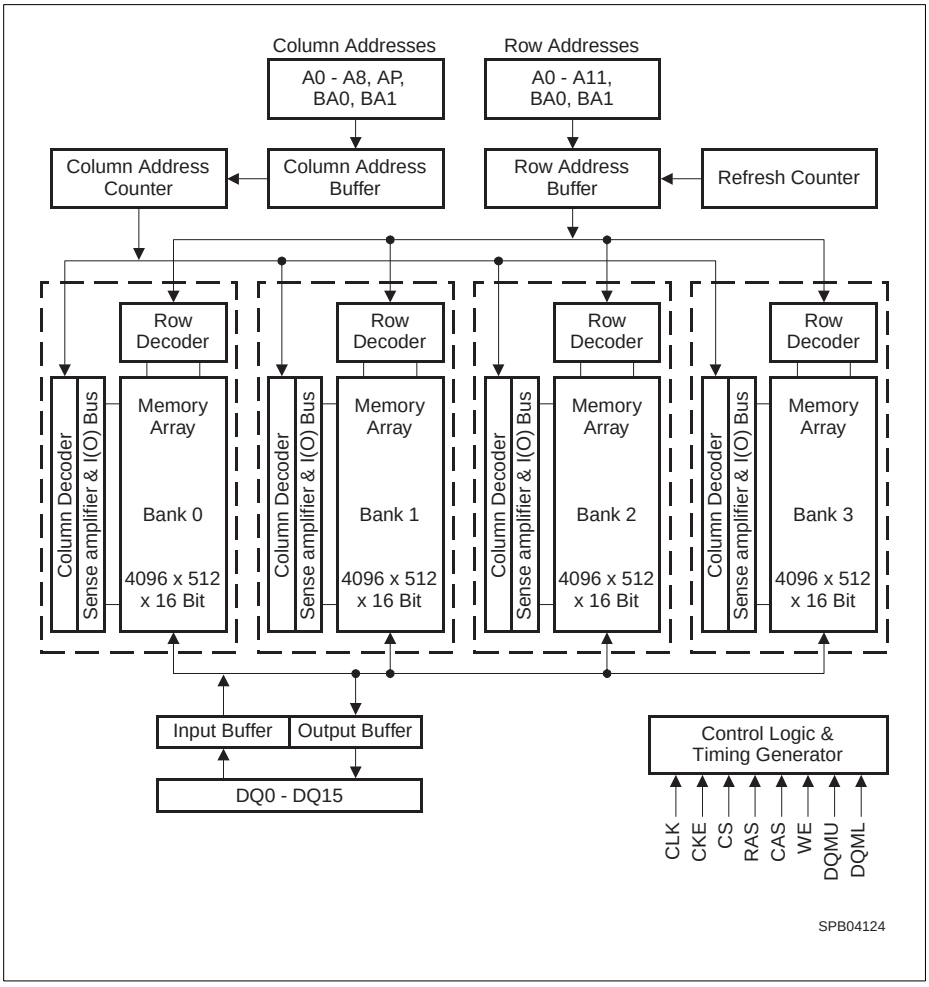
Functional Block Diagrams



Block Diagram: 32M x4 SDRAM (12 / 11 / 2 addressing)



Block Diagram: 16M x8 SDRAM (12 / 10 / 2 addressing)



Block Diagram: 8M x16 SDRAM (12 / 9 / 2 addressing)

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A11	Input	Level	–	During a Bank Activate command cycle, A0 - A11 define the row address (RA0 - RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0 - CAn) when sampled at the rising clock edge.CAn depends upon the SDRAM organization: 32M x4 SDRAM CA0 - CA9, CA11 (Page Length = 2048 bits) 16M x8 SDRAM CA0 - CA9 (Page Length = 1024 bits) 8M x16 SDRAM CA0 = CA8 (Page Length = 512 bits) In addition to the column address, A10(= AP) is used to invoke the autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	–	Bank Select Inputs. Selects which bank is to be active.
DQx	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs.

Signal Pin Description (cont'd)

Pin	Type	Signal	Polarity	Function
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input is present in x4 and x8 SDRAMs, LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs.
V_{DD} V_{SS}	Supply	–	–	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Operation Definition

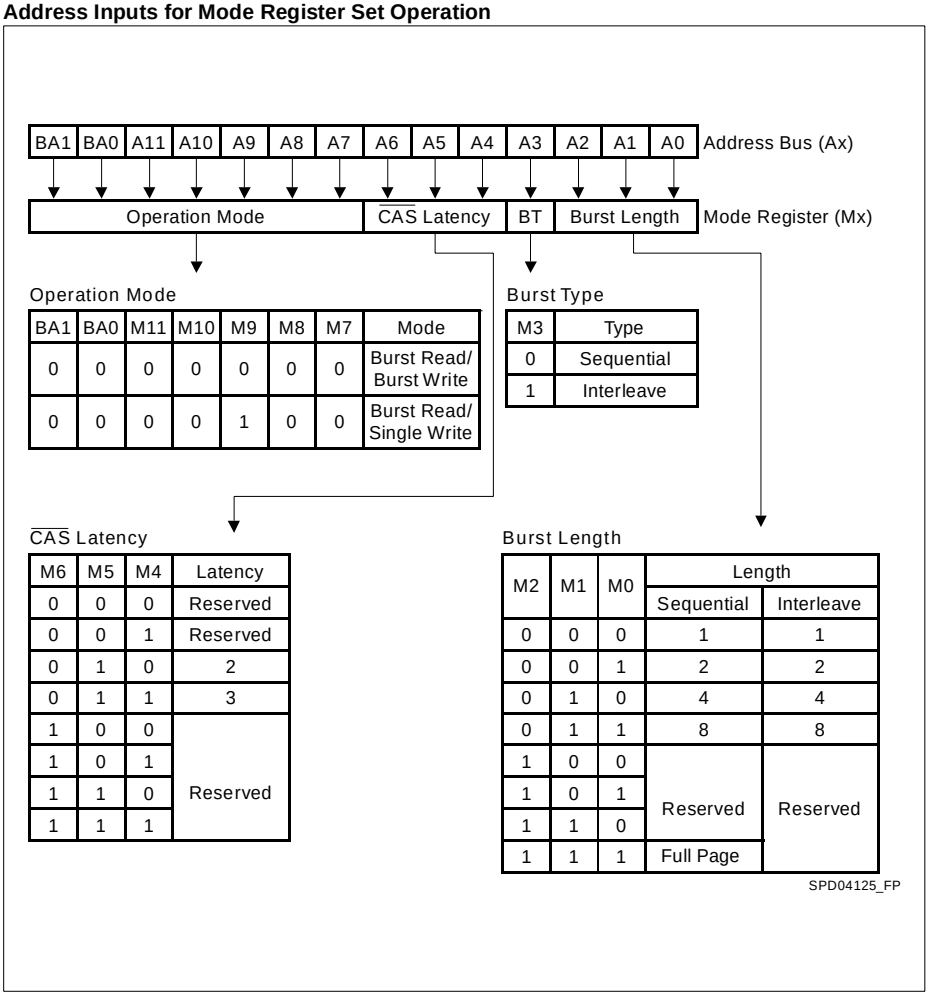
All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	DQM	BA0 BA1	AP= A10	Addr A11, A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle[3]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3]	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	L
Read	Active[3]	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down Entry (Precharge or active standby)	Idle Active[4]	H	L	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V = Valid, x = Don't Care, L = Low Level, H = High Level.
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. This is the state of the banks designated by BA0, BA1 signals.
4. Power Down Mode can not entry in the burst cycle. When this command is asserted in the burst mode cycle the device is in clock suspend mode.

Address Inputs for Mode Register Set Operation



BA1	BA0	M11	M10	M9	M8	M7	Mode
0	0	0	0	0	0	0	Burst Read/ Burst Write
0	0	0	0	1	0	0	Burst Read/ Single Write

M3	Type
0	Sequential
1	Interleave

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all V_{DD} and V_{DDQ} pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed V_{DD} + 0.3 V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a $\overline{\text{CAS}}$ **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

Read and Write Operation

When $\overline{\text{RAS}}$ is low and both $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the positive edge of the clock, a $\overline{\text{RAS}}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{\text{CAS}}$ cycle is triggered by setting $\overline{\text{RAS}}$ high and $\overline{\text{CAS}}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{\text{RAS}}$ timing. $\overline{\text{WE}}$ is used to define either a read ($\overline{\text{WE}}$ = H) or a write ($\overline{\text{WE}}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{\text{CAS}}$ cycle, serial data read or write operations are allowed at up to a 143 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{\text{CAS}}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation does not self terminate

once the burst length has been reached. In other words, unlike burst length of 2, 4, and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2....	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge

command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for power down mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2, two clocks before the last data out for $\overline{CAS}$ latency = 3 and three clocks before the last data out for $\overline{CAS}$ latency = 4. Writes require a time delay t_{WR} from the last data out to apply the precharge command.

Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	x	x	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Electrical Characteristics

Absolute Maximum Ratings

Operating Temperature Range ..... 0 to + 70 °C
Storage Temperature Range ..... – 55 to + 150 °C
Input/Output Voltage ..... – 0.3 to V_{DD} + 0.3 V
Power Supply Voltage V_{DD}/V_{DDQ} ..... – 0.3 to + 4.6 V
Power Dissipation ..... 1 W
Data out Current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	– 0.3	0.8	V	1, 2
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V	–
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V	–
Input Leakage Current, any input (0 V < V_{IN} < V_{DDQ}, all other inputs = 0 V)	$I_{I(L)}$	– 5	5	µA	–
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 5	5	µA	–

Notes
1.)All voltages are referenced to V_{SS}.
2.)V_{IH} may overshoot to V_{DD} + 2.0 V for pulse width of < 4 ns with 3.3 V. V_{IL} may undershoot to – 2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Values		Unit
		min.	max.	
Input Capacitance (CLK)	C_{I1}	2.5	3.5	pF
Input Capacitance (A0 - A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	2.5	3.8	pF
Input/Output Capacitance (DQ)	C_{IO}	4.0	6.0	pF

Operating Currents

T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-7	-7.5	-8	Unit	Note
			max.				
Operating current t_{CK} = $t_{CK(MIN.)}$,All banks operated in random access,all banks operated in ping-pong manner	–	I_{CC1}	170	160	150	mA	3,4
Precharge standby current in Power Down Mode $\overline{CS}$ = $V_{IH\ (MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min	I_{CC2P}	1.5			mA	3
Precharge standby current in Non Power Down Mode $\overline{CS}$ = $V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min	I_{CC2N}	45	40	35	mA	3
No operating current t_{CK} = min., $\overline{CS}$ = $V_{IH\ (MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	50	50	45	mA	3
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	10			mA	3
Burst Operating Current t_{CK} = min,Read command cycling	–	I_{CC4}	110	100	90	mA	3, 4
Auto Refresh Current t_{CK} = min, trc = trcmin. Auto Refresh command cycling	–	I_{CC5}	250	230	210	mA	3
Self Refresh Current Self Refresh Mode CKE = 0.2 V, tck=infinity	standard version	I_{CC6}	1.5			mA	
	L-version		690			µA	

Notes

5. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7 & -7.5 and at 100 MHz for -8 parts. Input signals are changed once during t_{CK}.
6. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 is assumed and the V_{DDQ} current is excluded.

AC Characteristics [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-7		-7.5		-8			
		min.	max.	min.	max.	min.	max.		
Clock and Clock Enable									
Clock Cycle Time									–
$\overline{CAS}$ Latency = 3	t_{CK}	7	–	7.5	–	8	–	ns	
$\overline{CAS}$ Latency = 2		7.5	–	10	–	10	–	ns	
Clock frequency									–
$\overline{CAS}$ Latency = 3	t_{CK}	–	143	–	133	–	125	MHz	
$\overline{CAS}$ Latency = 2		–	133	–	100	–	100	MHz	
Access Time from Clock									2, 3, 6
$\overline{CAS}$ Latency = 3	t_{AC}	–	5.4	–	5.4	–	6	ns	
$\overline{CAS}$ Latency = 2		–	5.4	–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	2.5	–	3	–	ns	–
Clock Low Pulse Width	t_{CL}	2.5	–	2.5	–	3	–	ns	–
Transition Time	t_T	0.3	1.2	0.3	1.2	0.5	10	ns	–
Setup and Hold Times									
Input Setup Time	t_{IS}	1.5	–	1.5	–	2	–	ns	4
Input Hold Time	t_{IH}	0.8	–	0.8	–	1	–	ns	4
CKE Setup Time	t_{CKS}	1.5	–	1.5	–	2	–	ns	4
CKE Hold Time	t_{CKH}	0.8	–	0.8	–	1	–	ns	4
Mode Register Set-up Time	t_{RSC}	2	–	2	–	2	–	CLK	–
Power Down Mode Entry Time	t_{SB}	0	7	0	7.5	0	8	ns	–
Common Parameters									
Row to Column Delay Time	t_{RCD}	15	–	20	–	20	–	ns	5
Row Precharge Time	t_{RP}	15	–	20	–	20	–	ns	5
Row Active Time	t_{RAS}	42	100k	45	100k	48	100k	ns	5
Row Cycle Time	t_{RC}	60	–	67	–	70	–	ns	5
Activate(a) to Activate(b) Command Period	t_{RRD}	14	–	15	–	16	–	ns	5
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	1	–	1	–	CLK	–

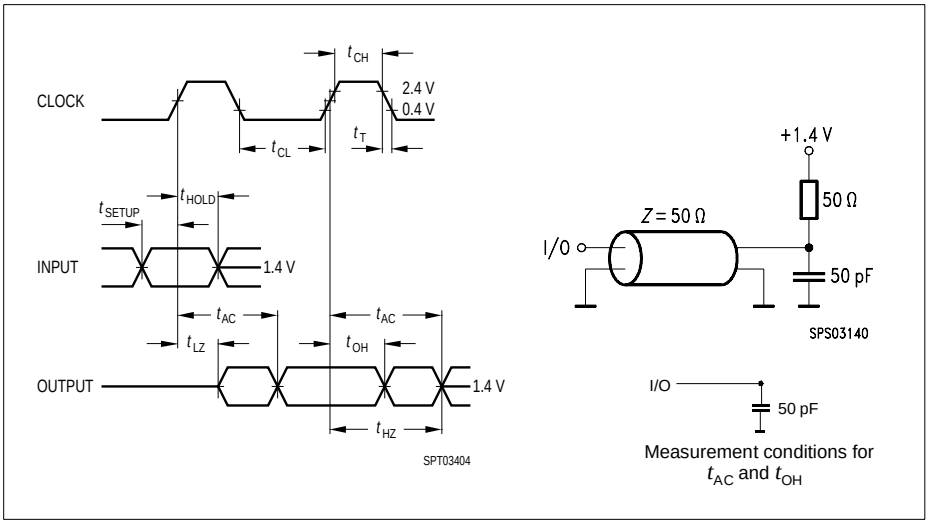
AC Characteristics (cont'd)[1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-7		-7.5		-8			
		min.	max.	min.	max.	min.	max.		
Refresh Cycle									
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	1	–	1	–	1	–	CLK	
Read Cycle									
Data Out Hold Time	t_{OH}	3	–	3	–	3	–	ns	[2, 5, 6]
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	0	–	ns	–
Data Out to High Impedance Time	t_{HZ}	3	7	3	7	3	8	ns	–
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	–
Write Cycle									
Write Recovery Time	t_{WR}	2	–	2	–	2	–	CLK	[7]
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	–

Notes

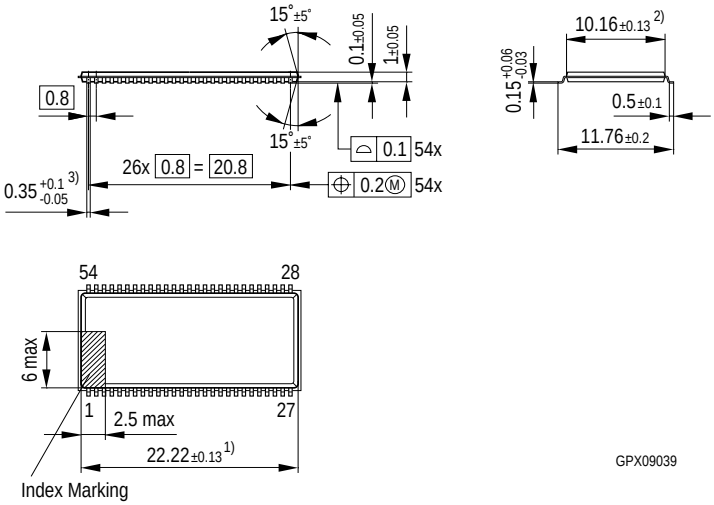
1. For proper power-up see the operation section of this data sheet.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8 V and 2.0 V.



3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
   the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
6. Access time from clock tac is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time toh is 1.8 ns for PC133 components with no termination and 0 pF load.
7. The write recovery time twr = 2 CLK cycles is a digital interlock on this device. Special devices with twr = 1 CLK for operations at less or equal 83 MHz will be available.

Package Outlines

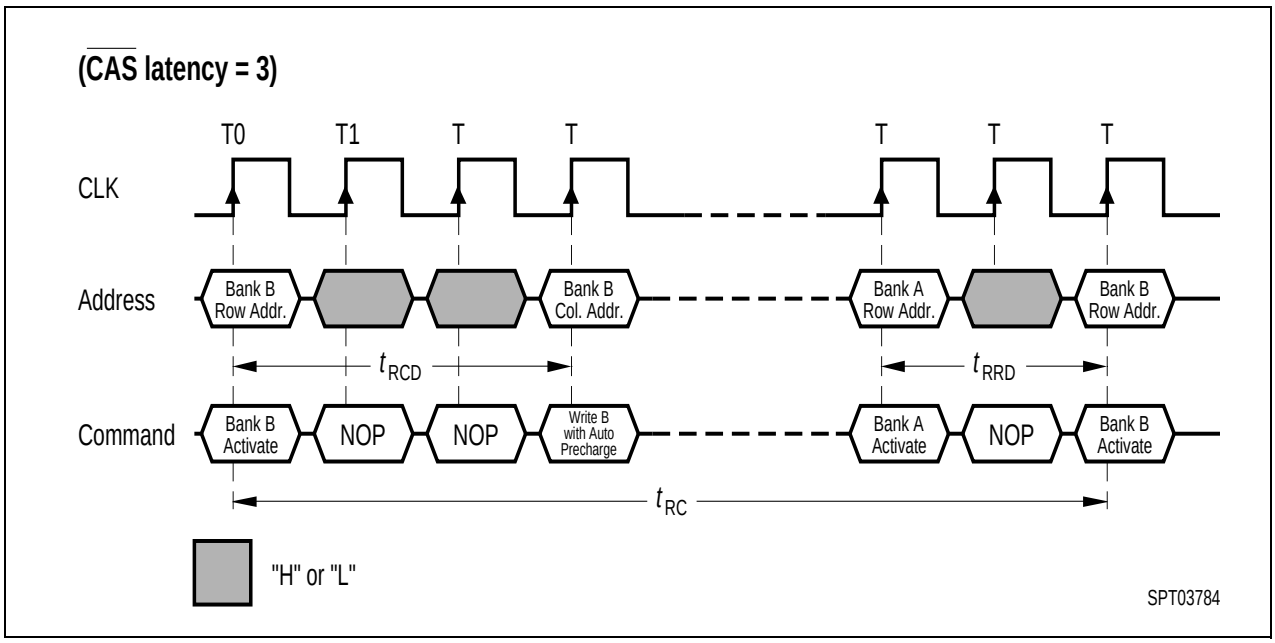
Plastic Package, P-TSOPII-54
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD



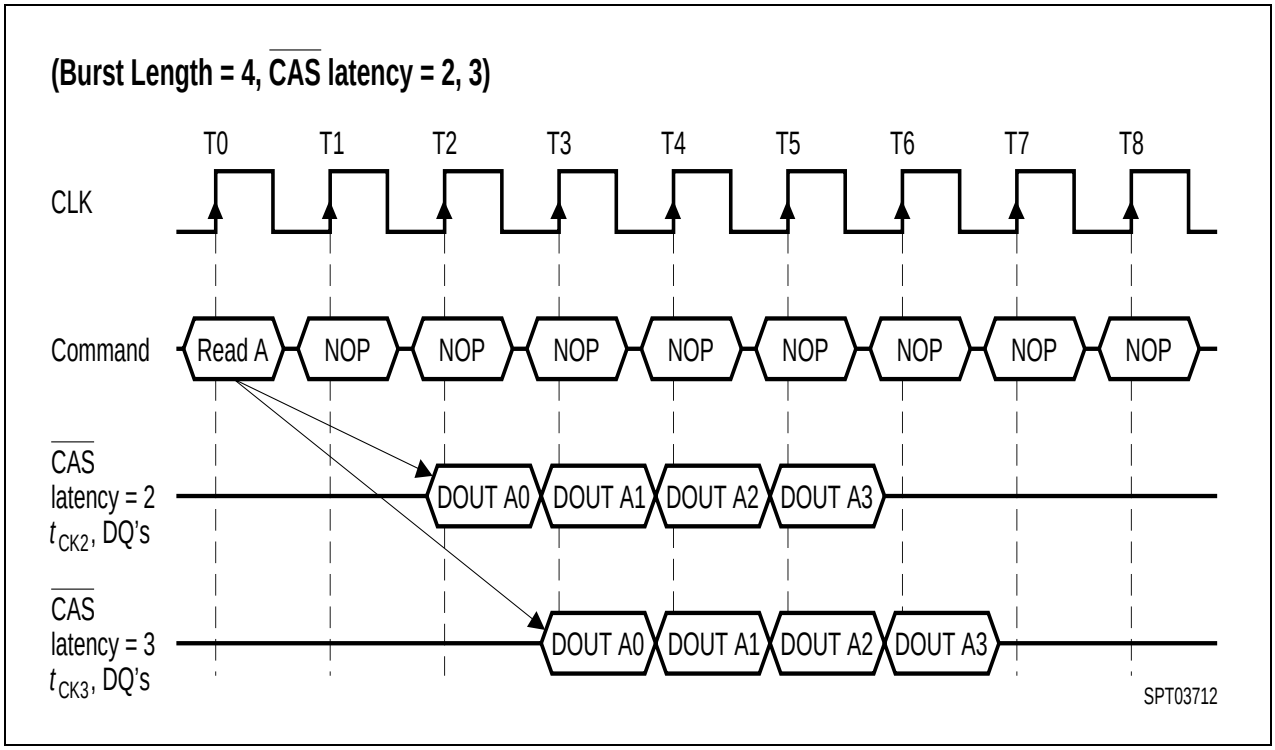
1) Does not include plastic or metal protrusion of 0.15 max per side
2) Does not include plastic protrusion of 0.25 max per side
3) Does not include dambar protrusion of 0.13 max per side

Timing Diagrams

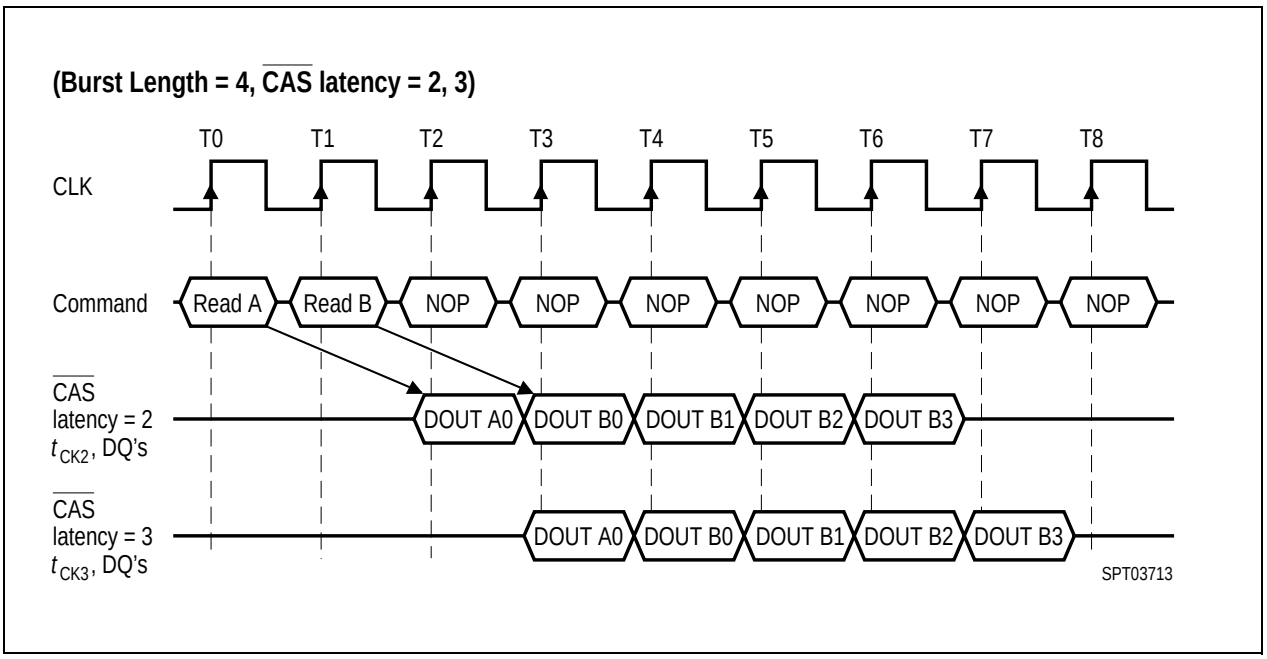
1. Bank Activate Command Cycle



2. Burst Read Operation

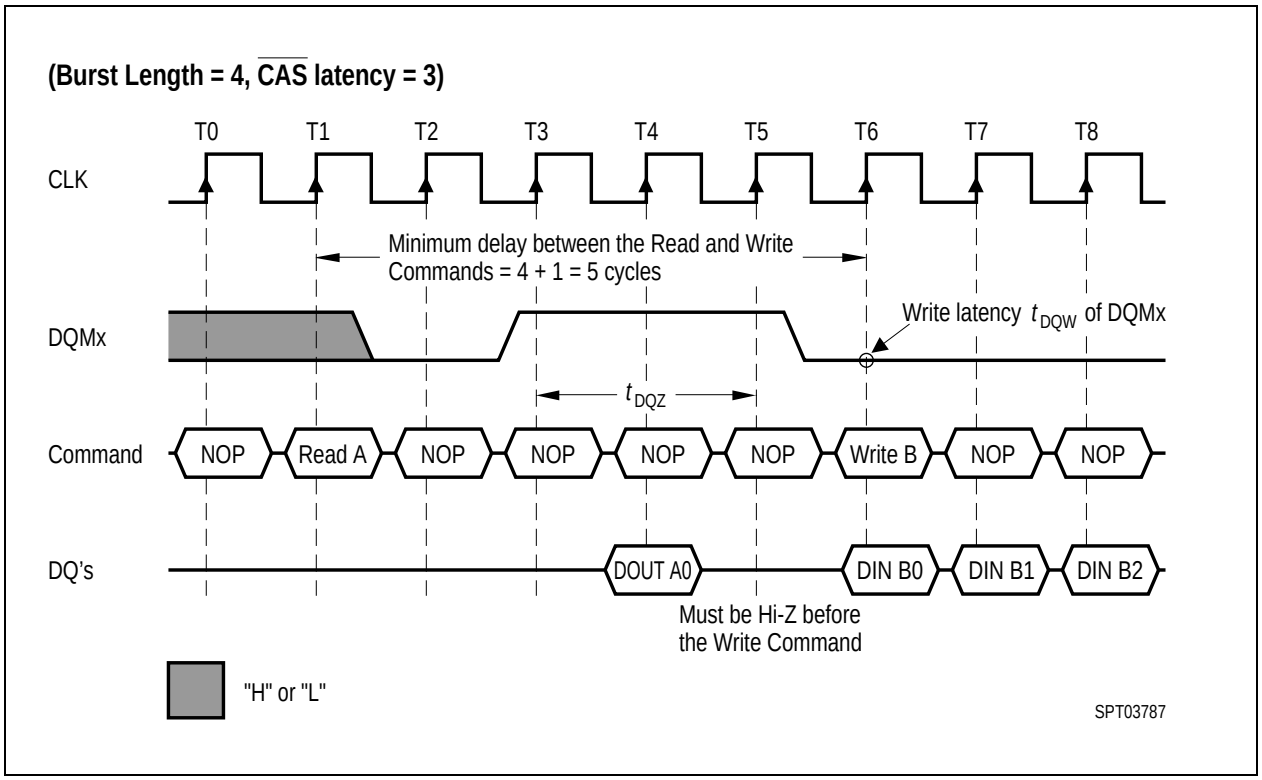


3. Read Interrupted by a Read

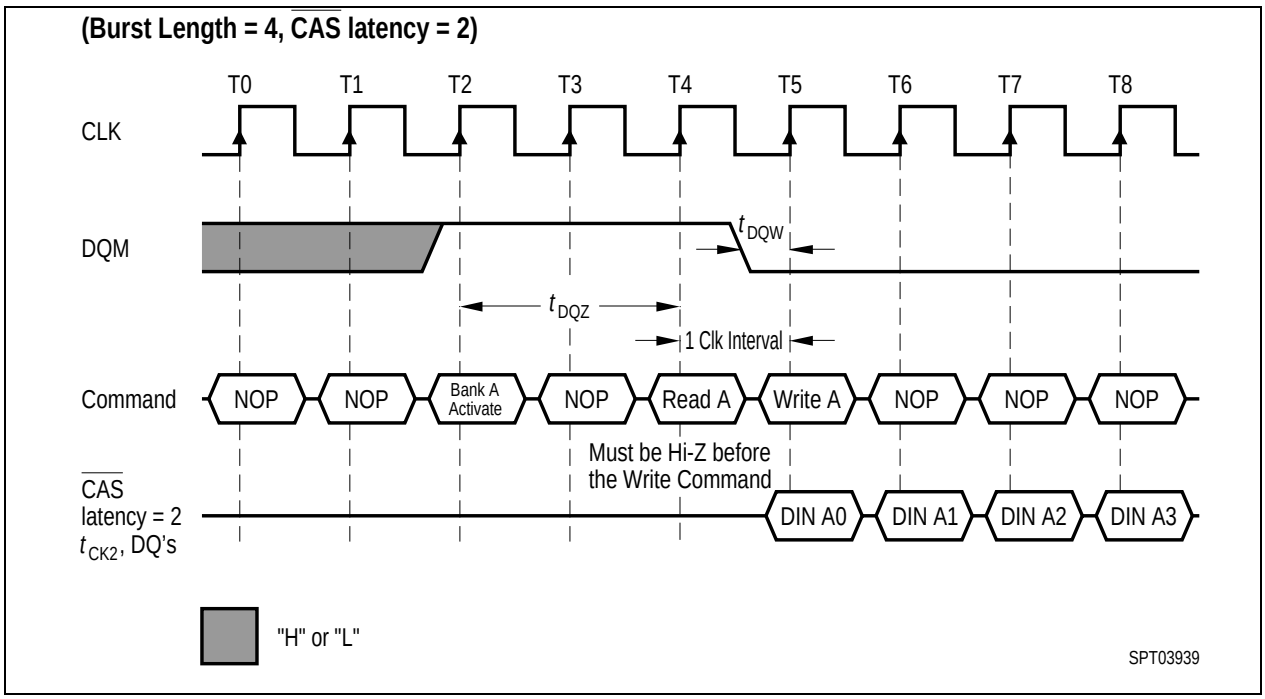


4. Read to Write Interval

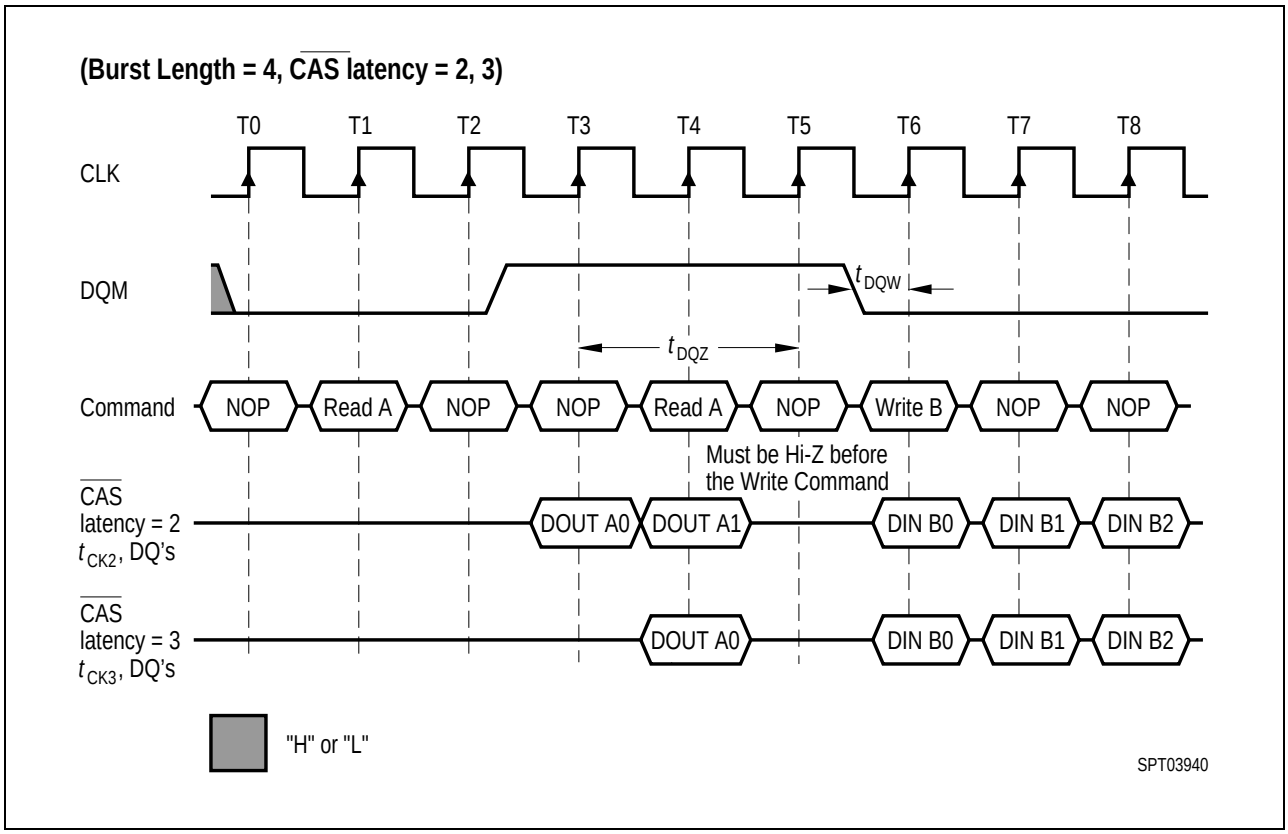
4.1 Read to Write Interval



4 2. Minimum Read to Write Interval

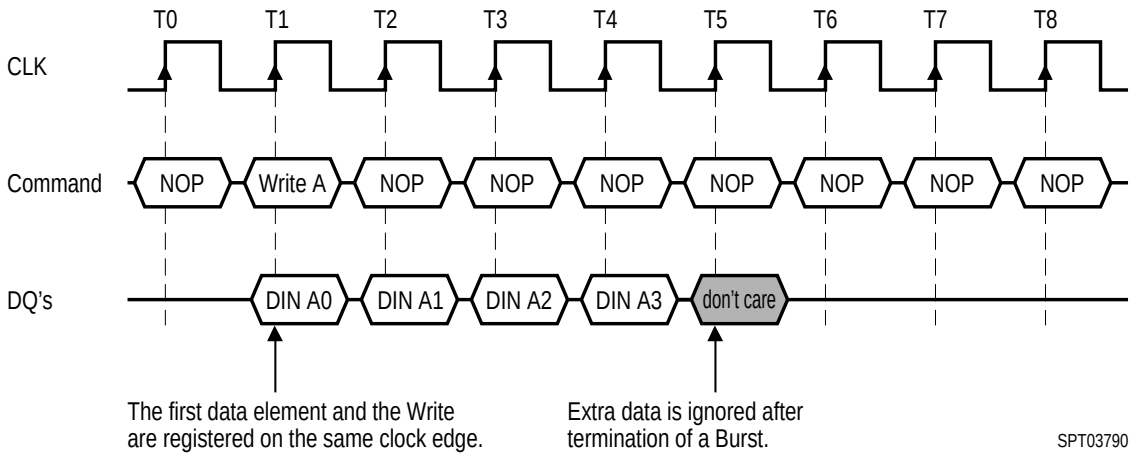


4. 3. Non-Minimum Read to Write Interval



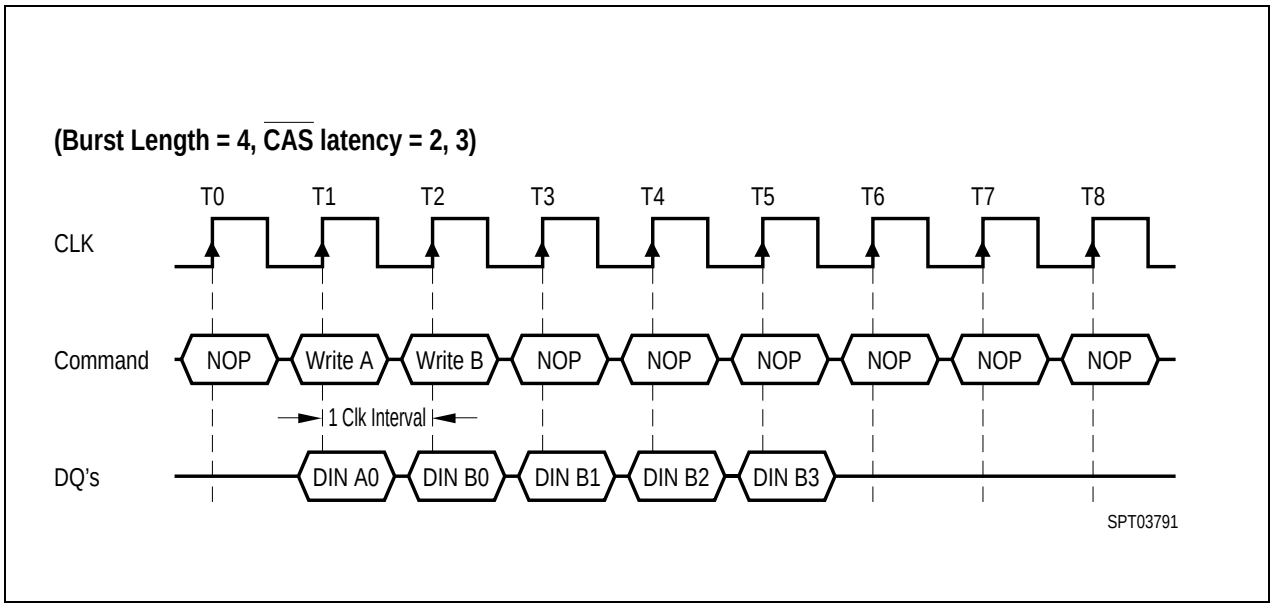
5. Burst Write Operation

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)

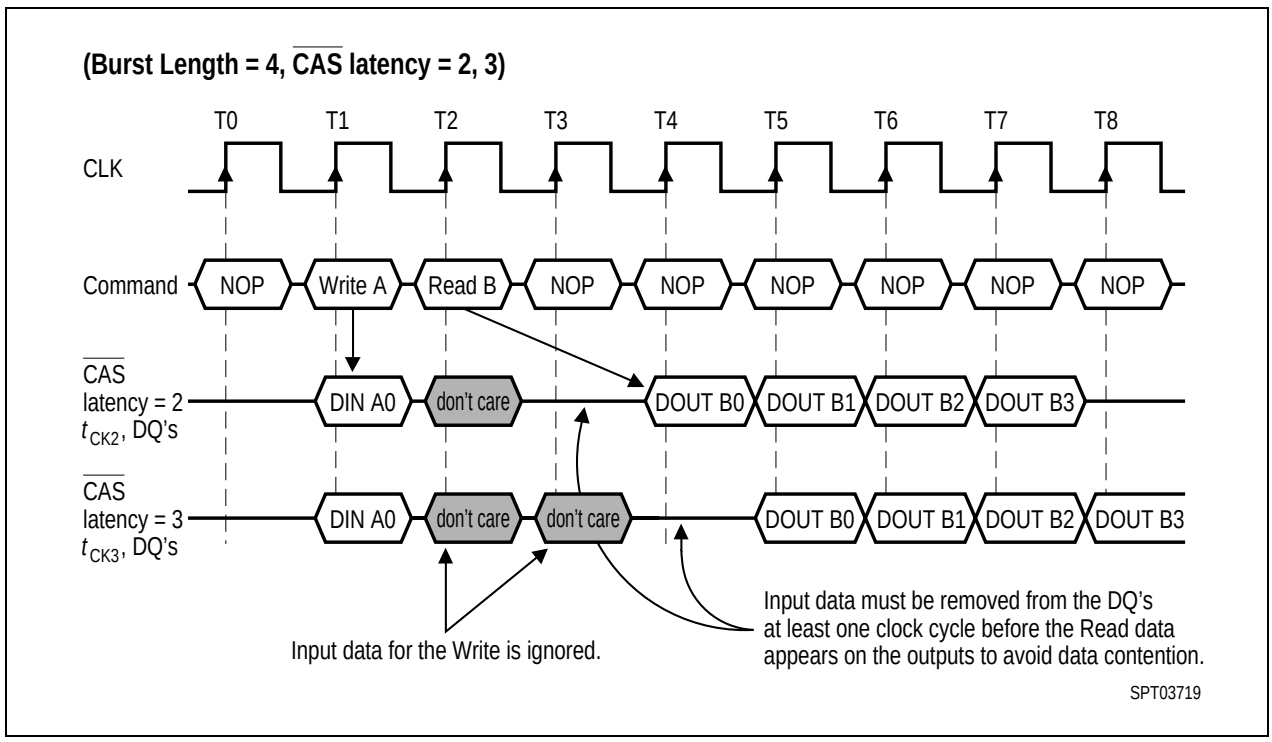


6. Write and Read Interrupt

6.1 Write Interrupted by a Write

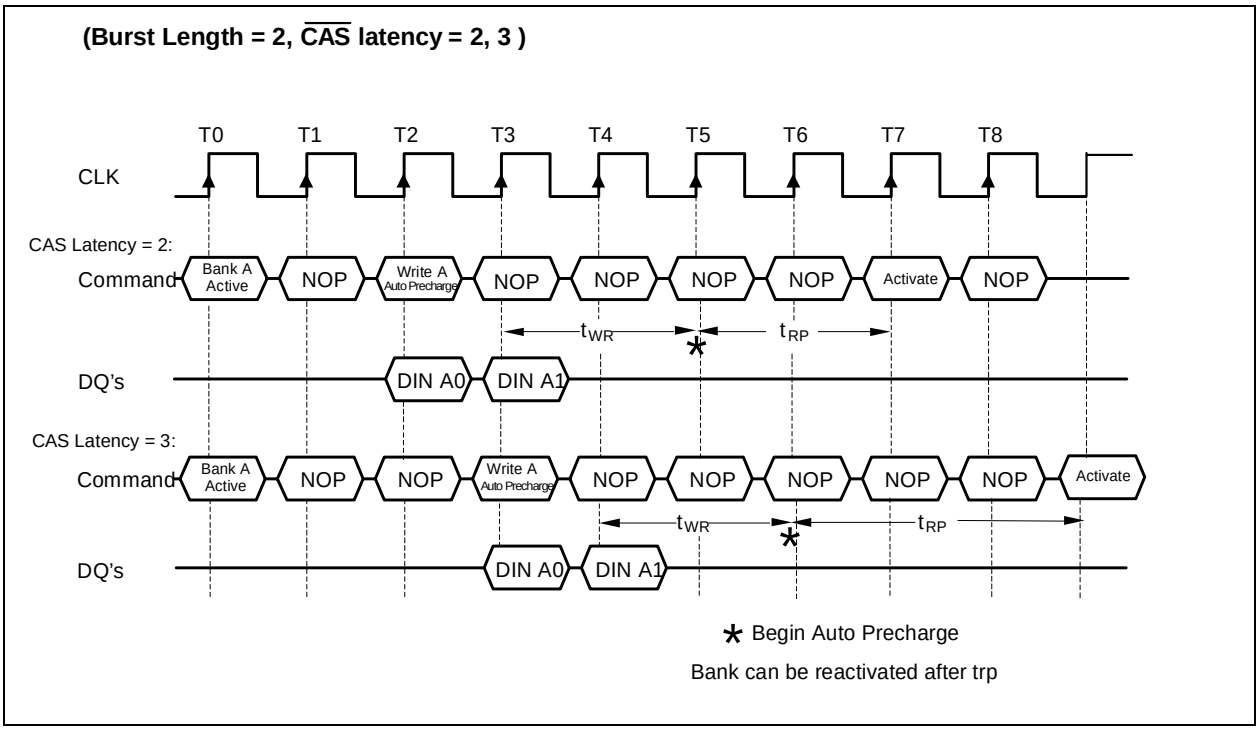


6.2 Write Interrupted by a Read

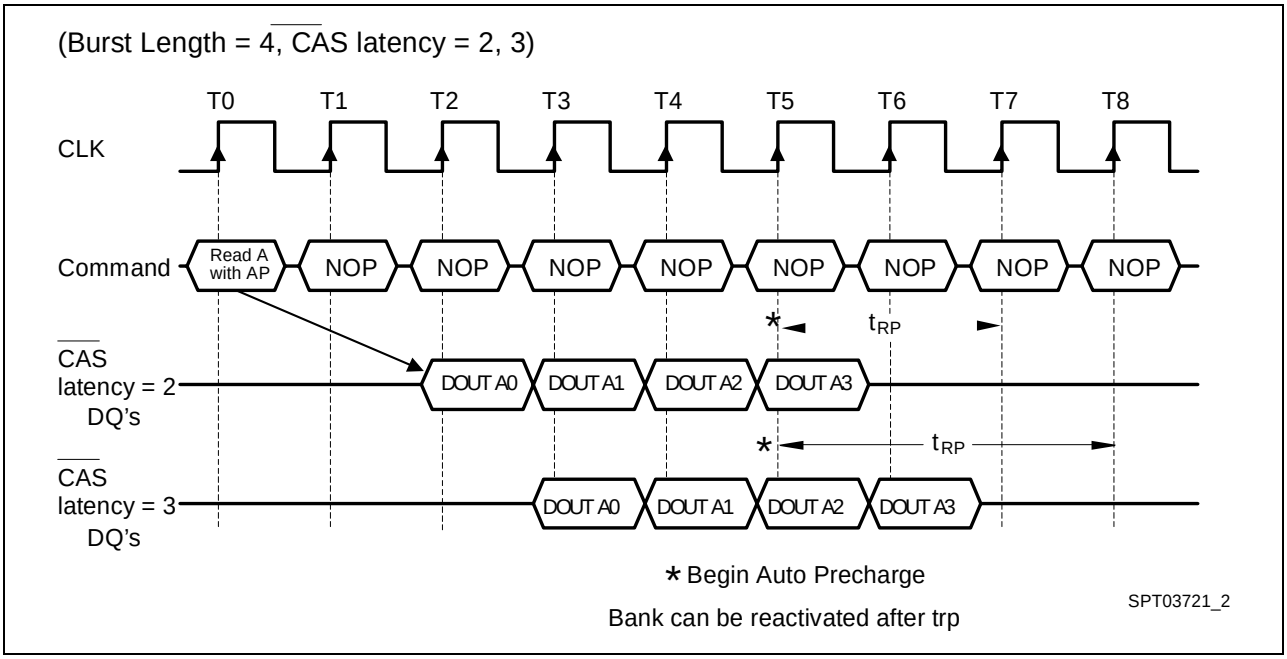


7. Burst Write and Read with Auto Precharge

7.1 Burst Write with Auto-Precharge

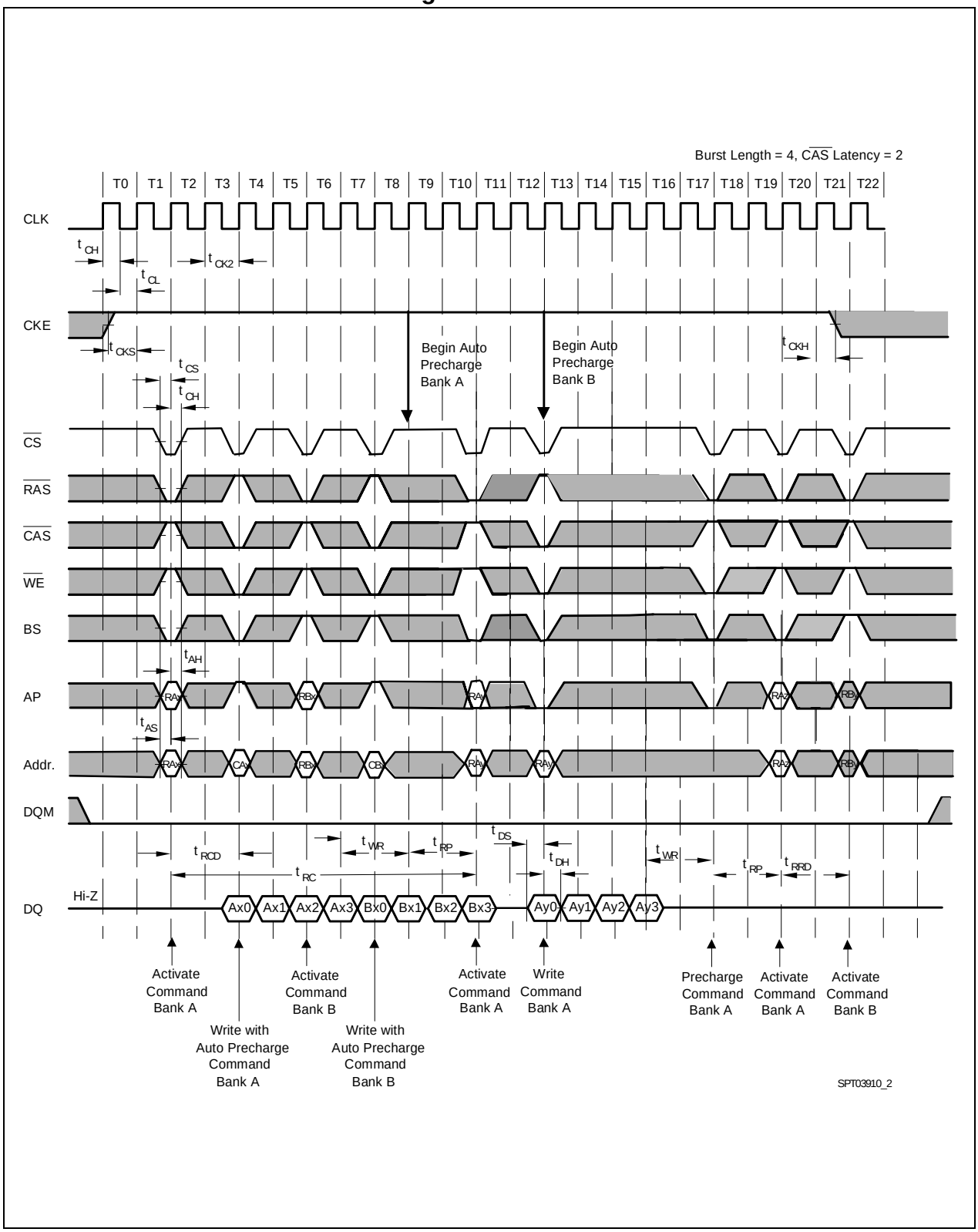


7.2 Burst Read with Auto-Precharge

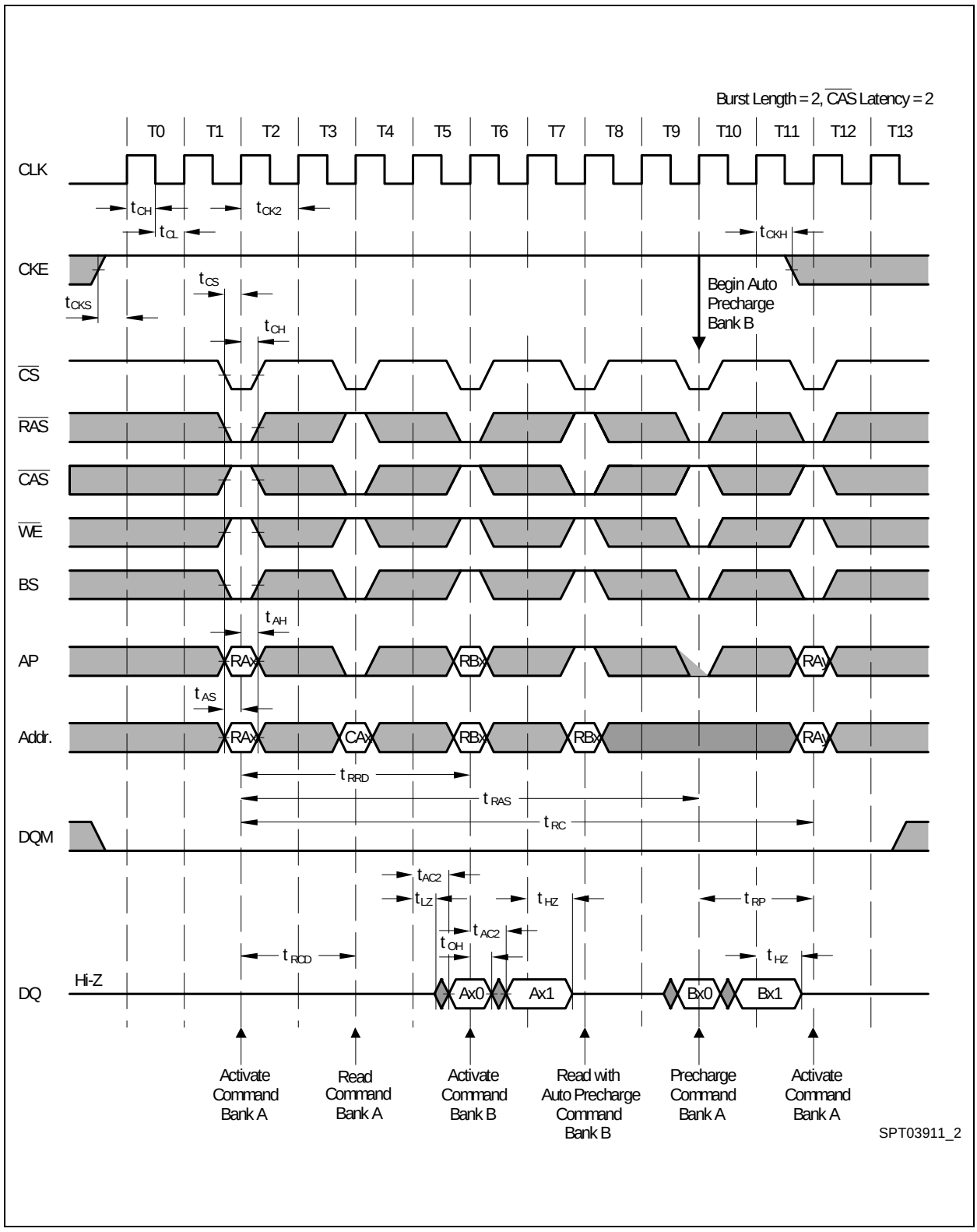


8. AC Parameters

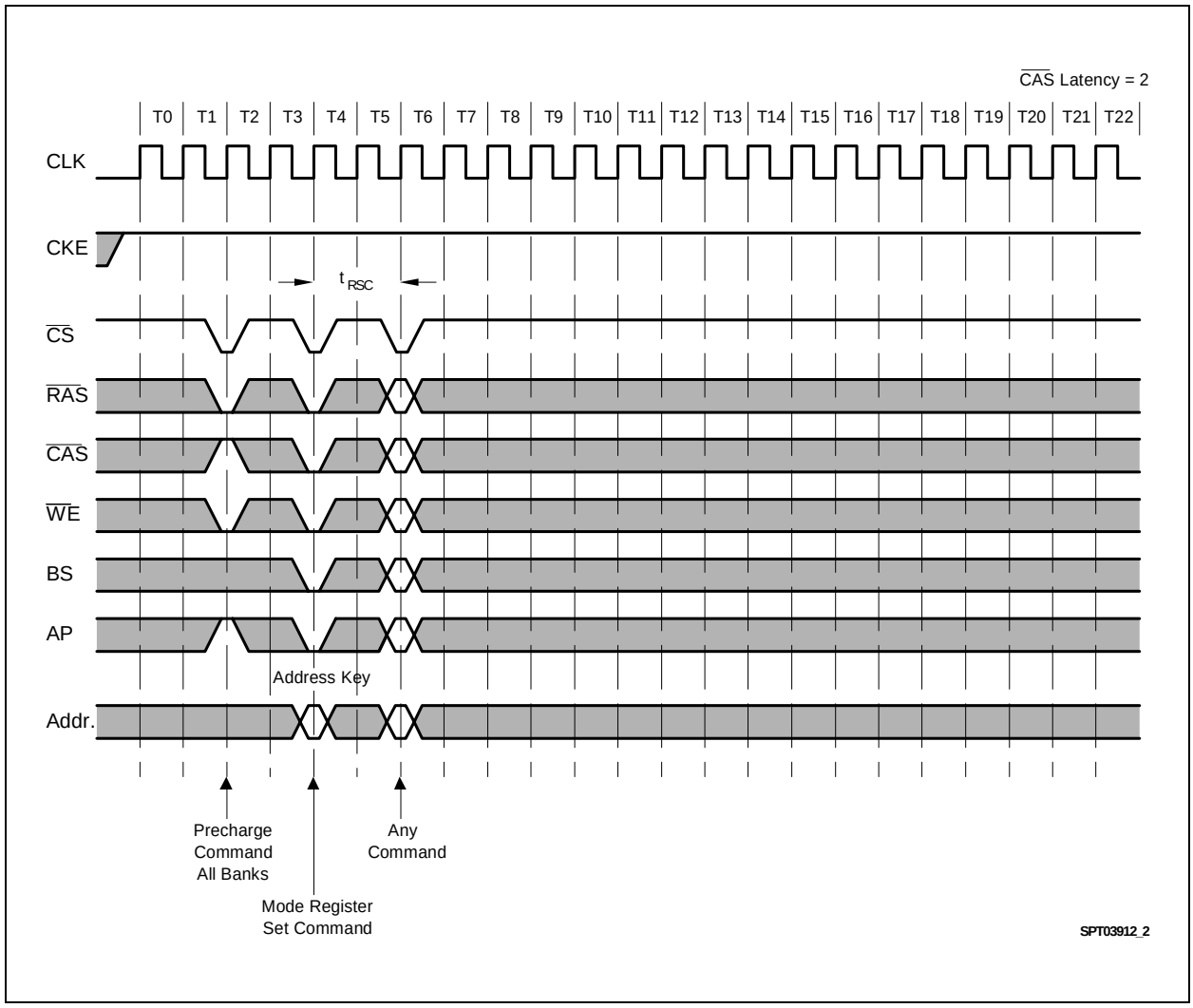
8.1 AC Parameters for a Write Timing



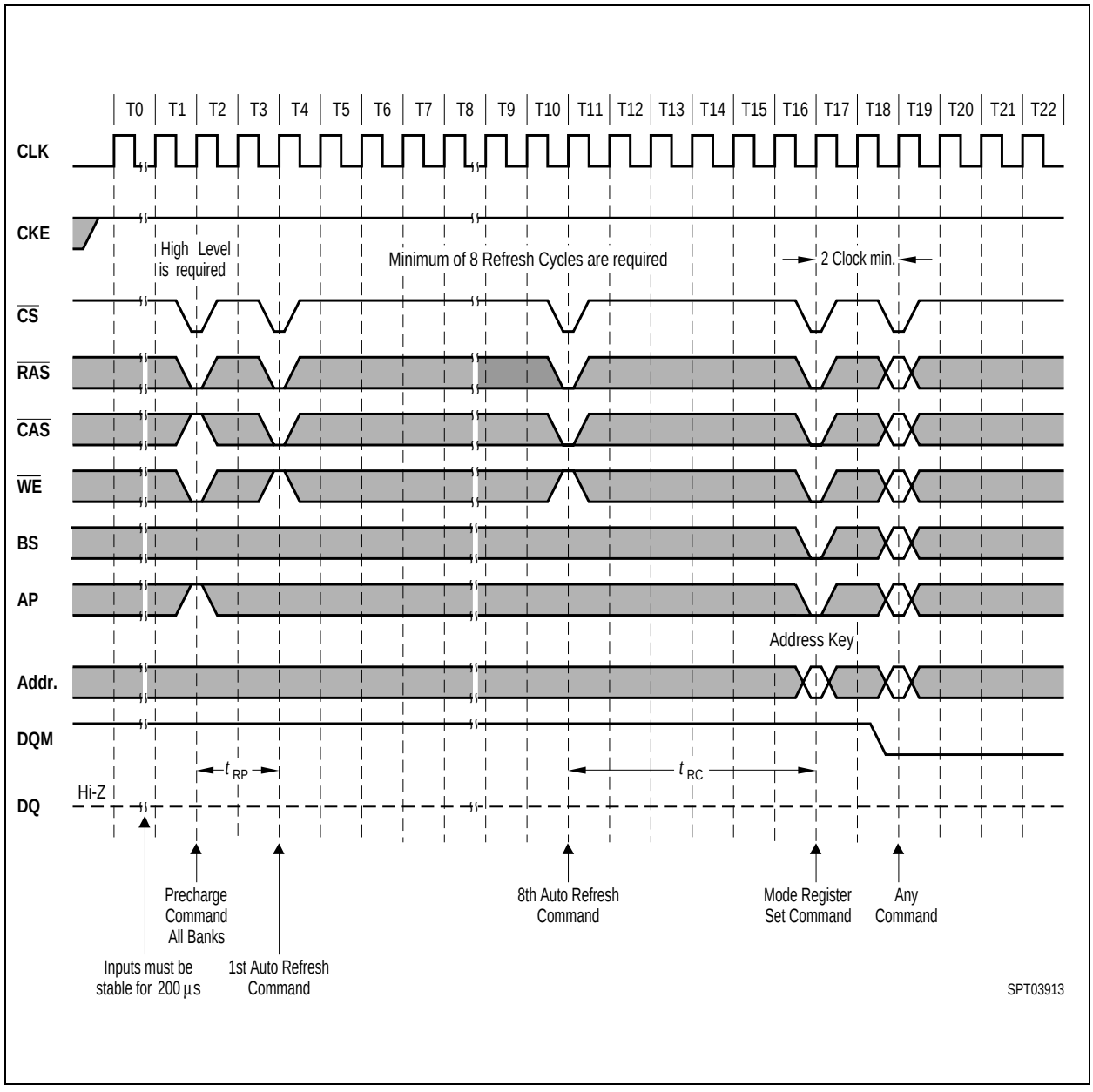
8.2 AC Parameters for a Read Timing



9. Mode Register Set

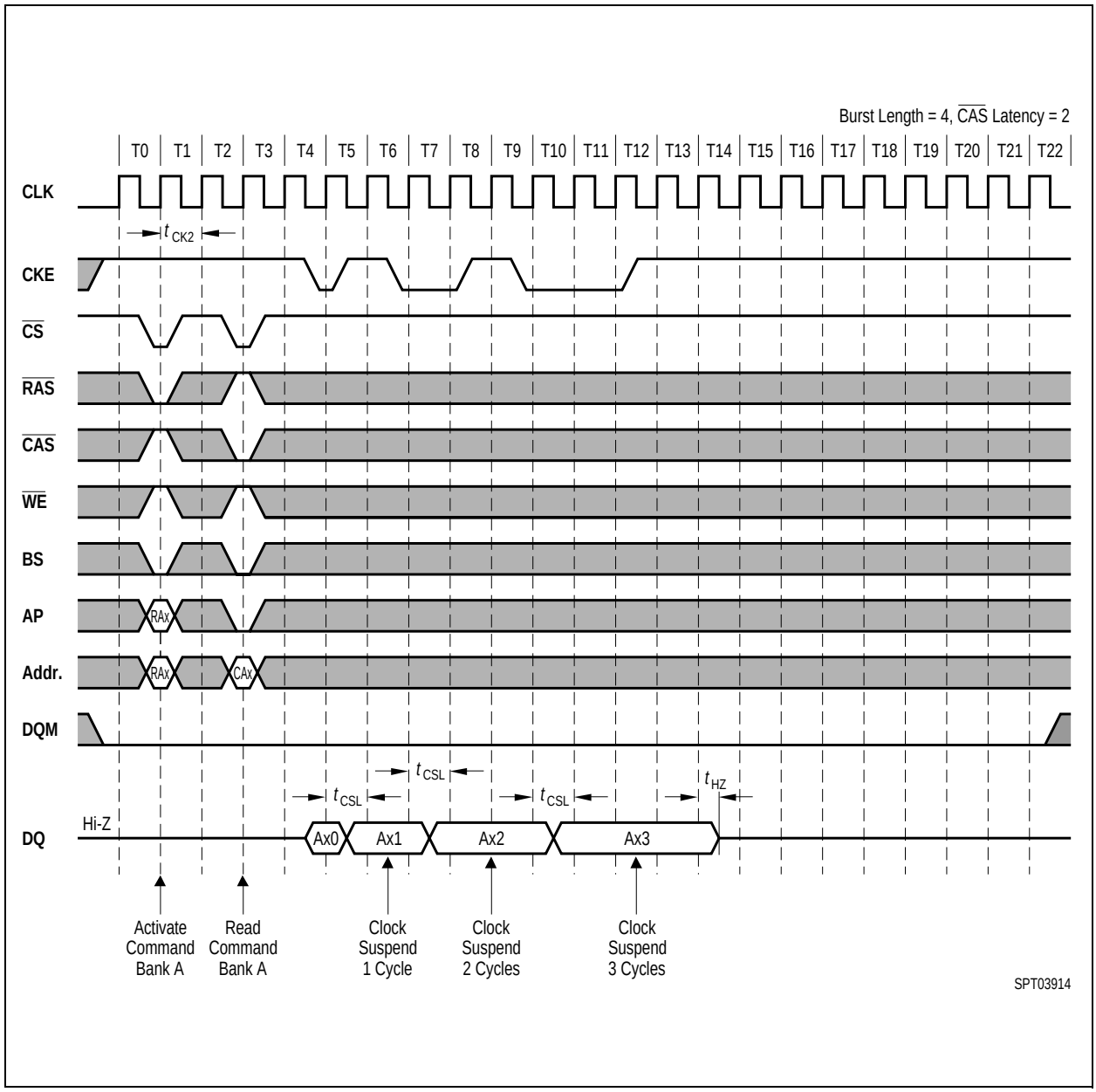


10. Power on Sequence and Auto Refresh (CBR)

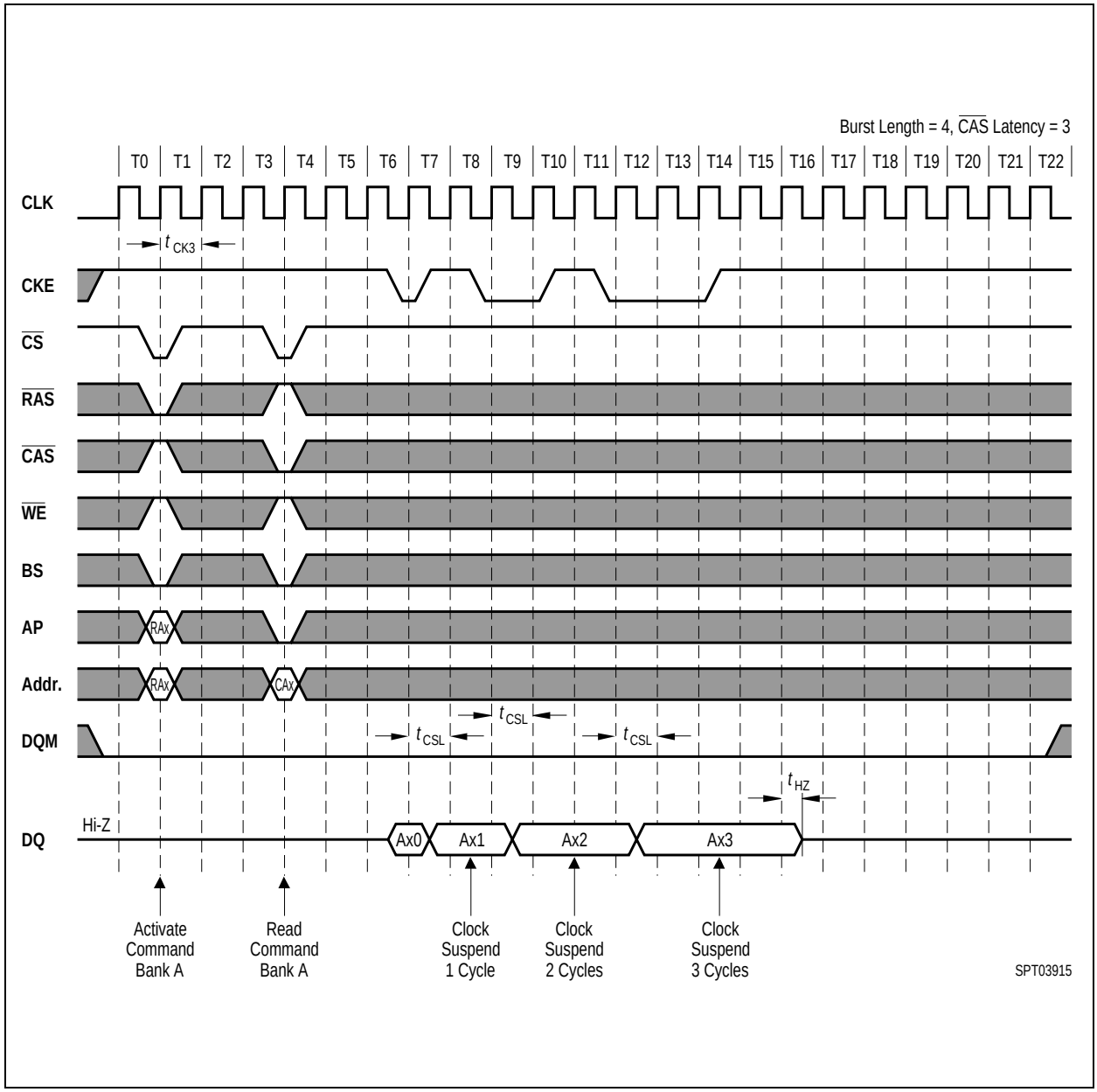


11. Clock Suspension (Using CKE)

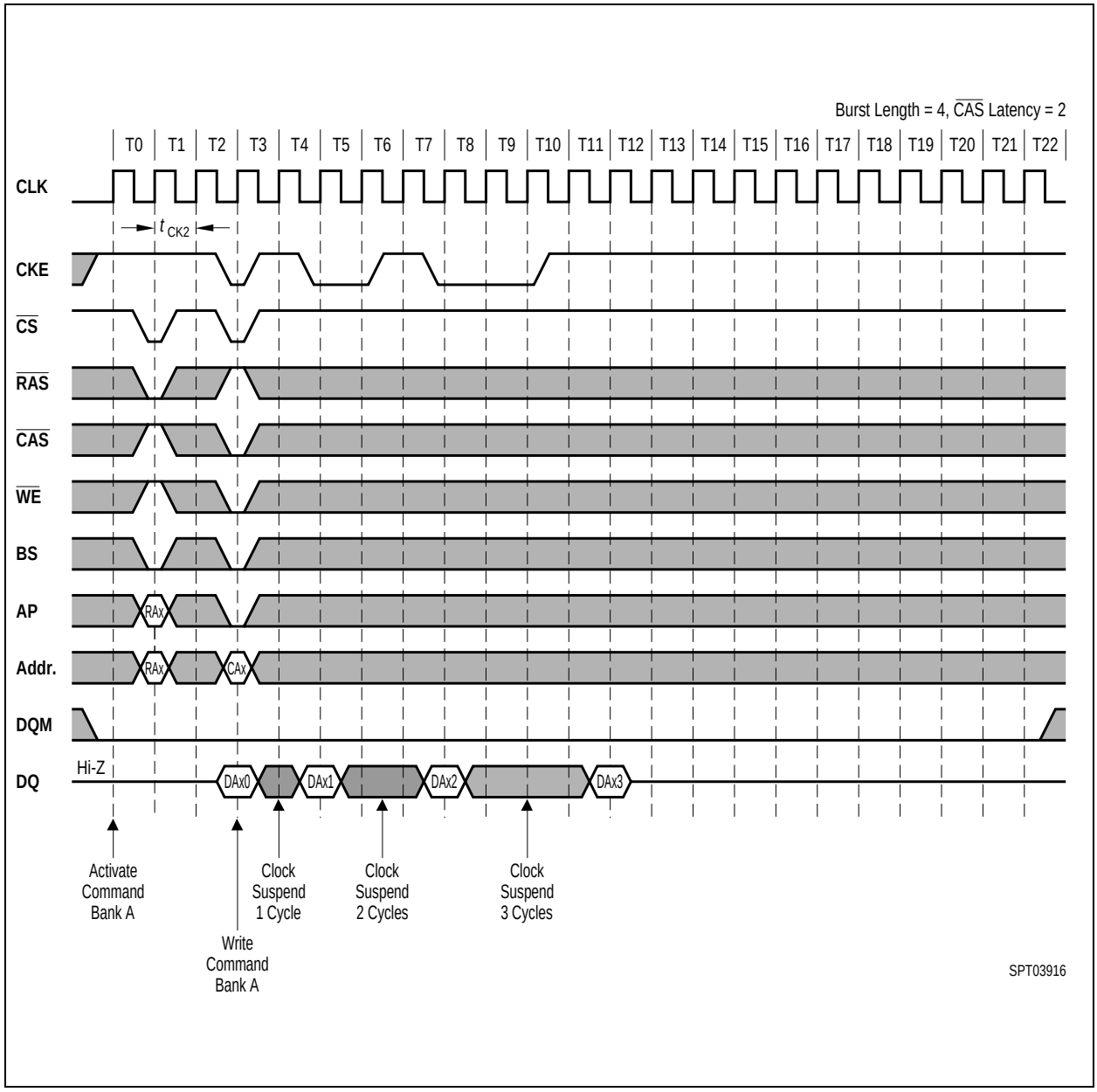
11.1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2



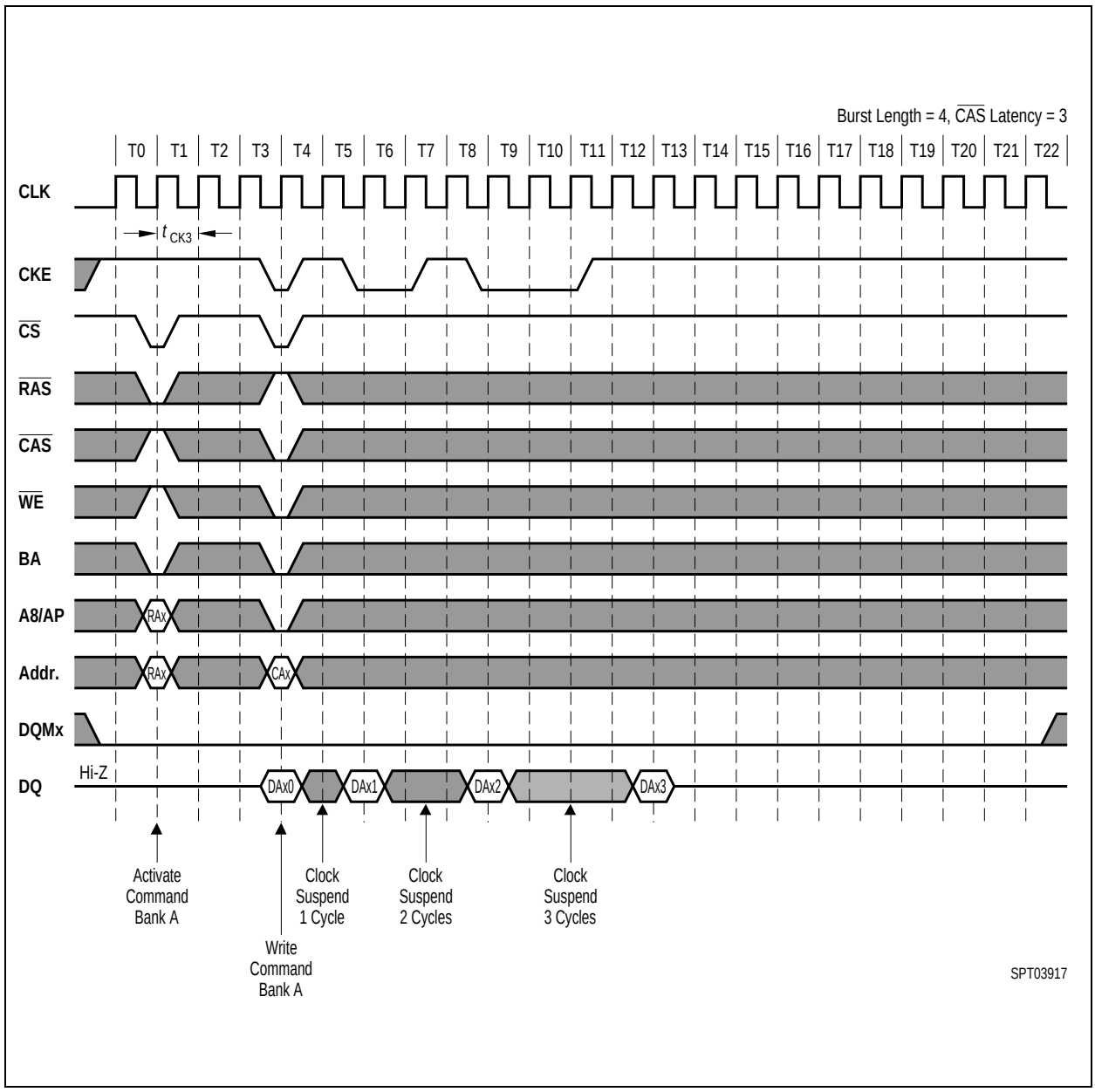
11.2 Clock Suspension During Burst Read $\overline{CAS}$ Latency = 3



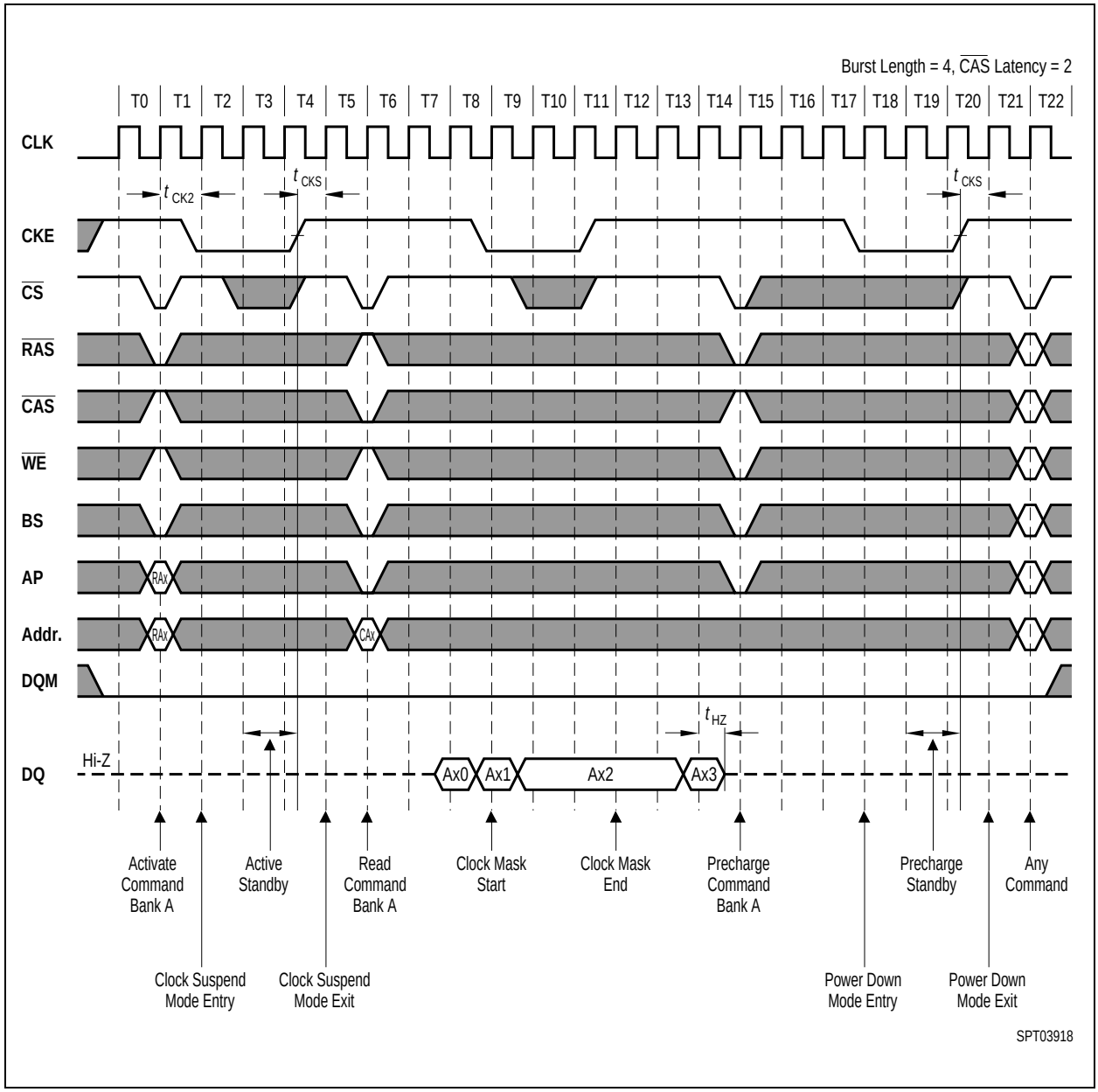
11.3 Clock Suspension During Burst Write $\overline{CAS}$ Latency = 2



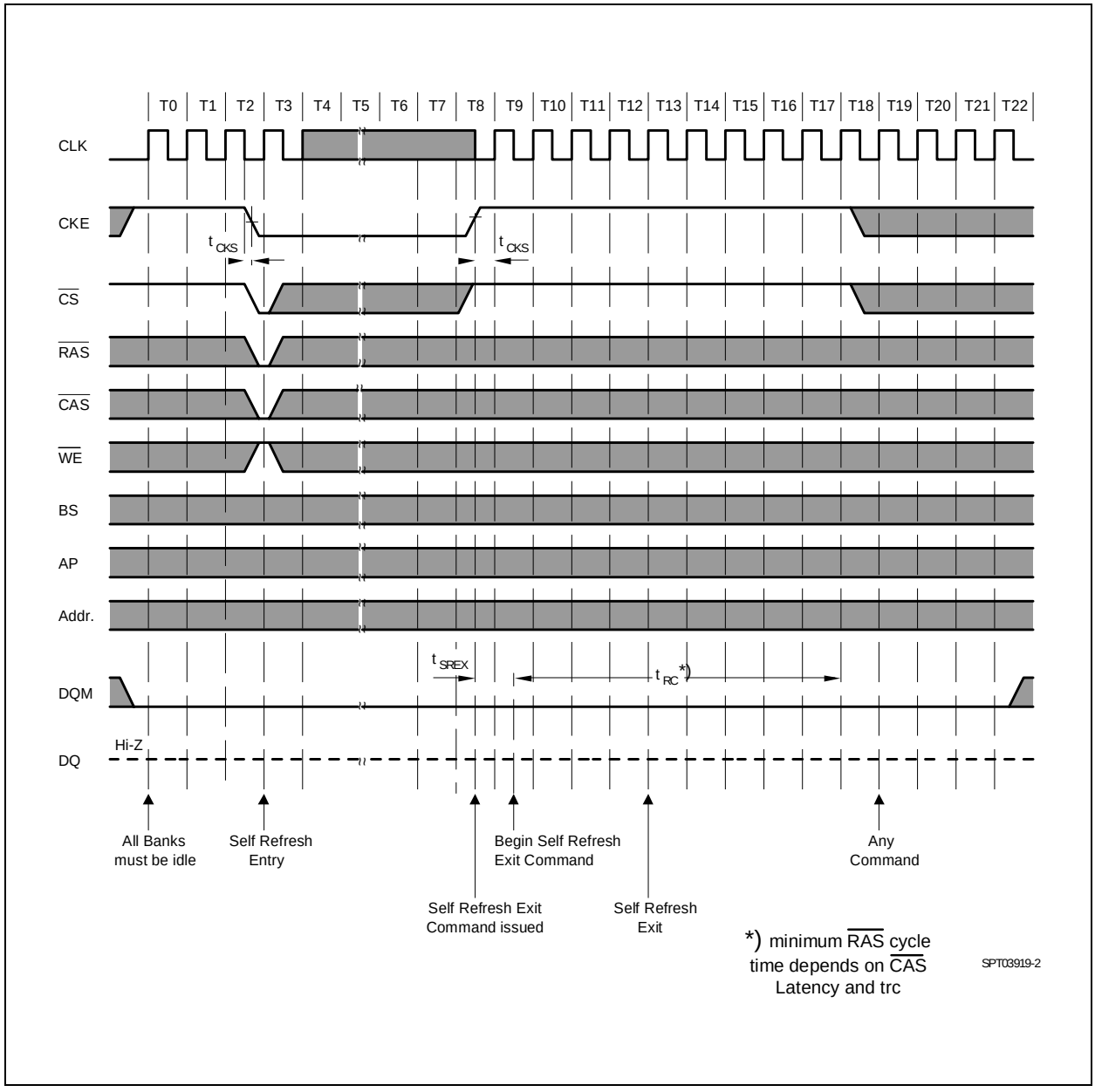
11.4 Clock Suspension During Burst Write $\overline{CAS}$ Latency = 3



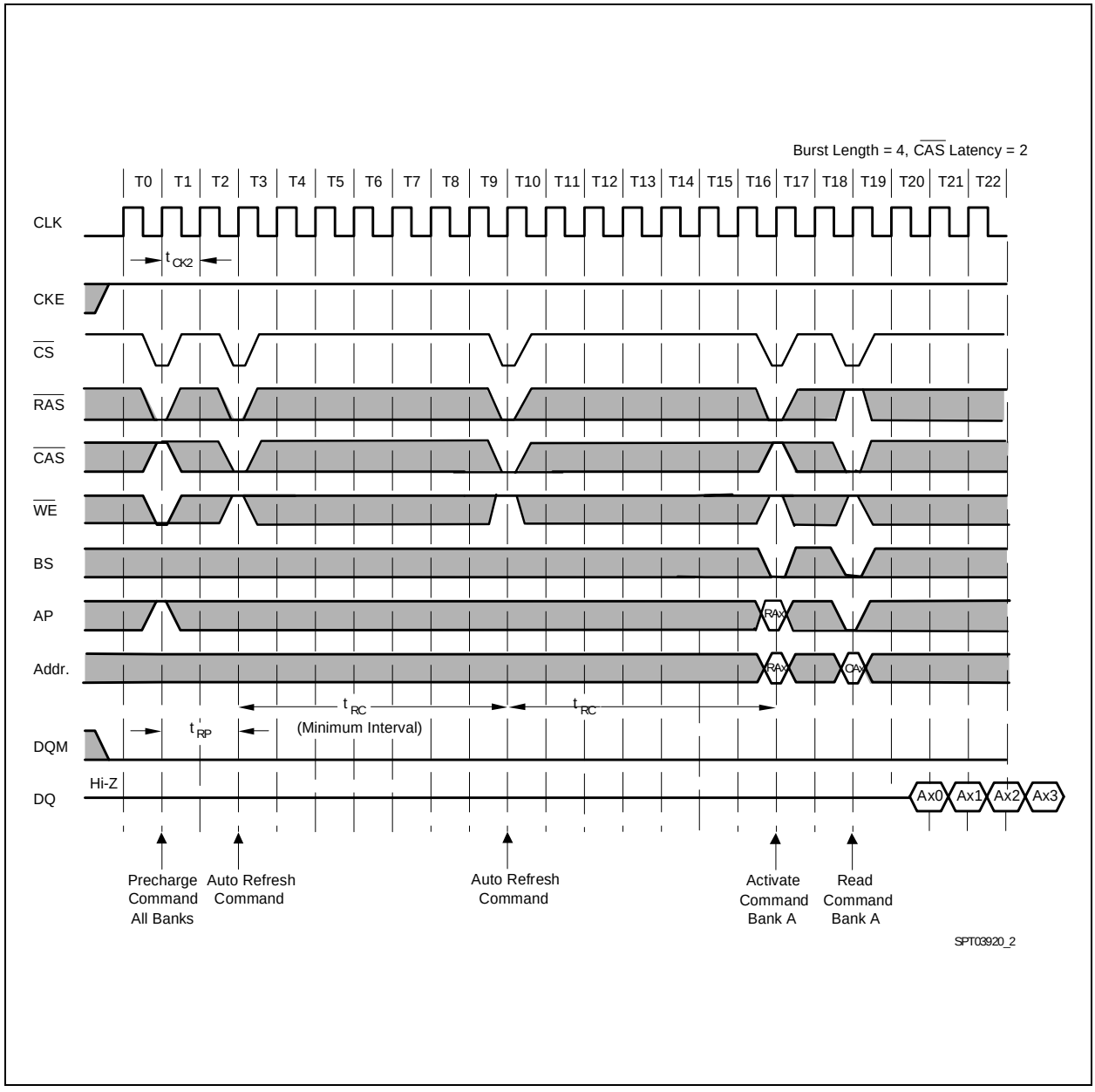
12. Power Down Mode and Clock Suspend



13. Self Refresh (Entry and Exit)

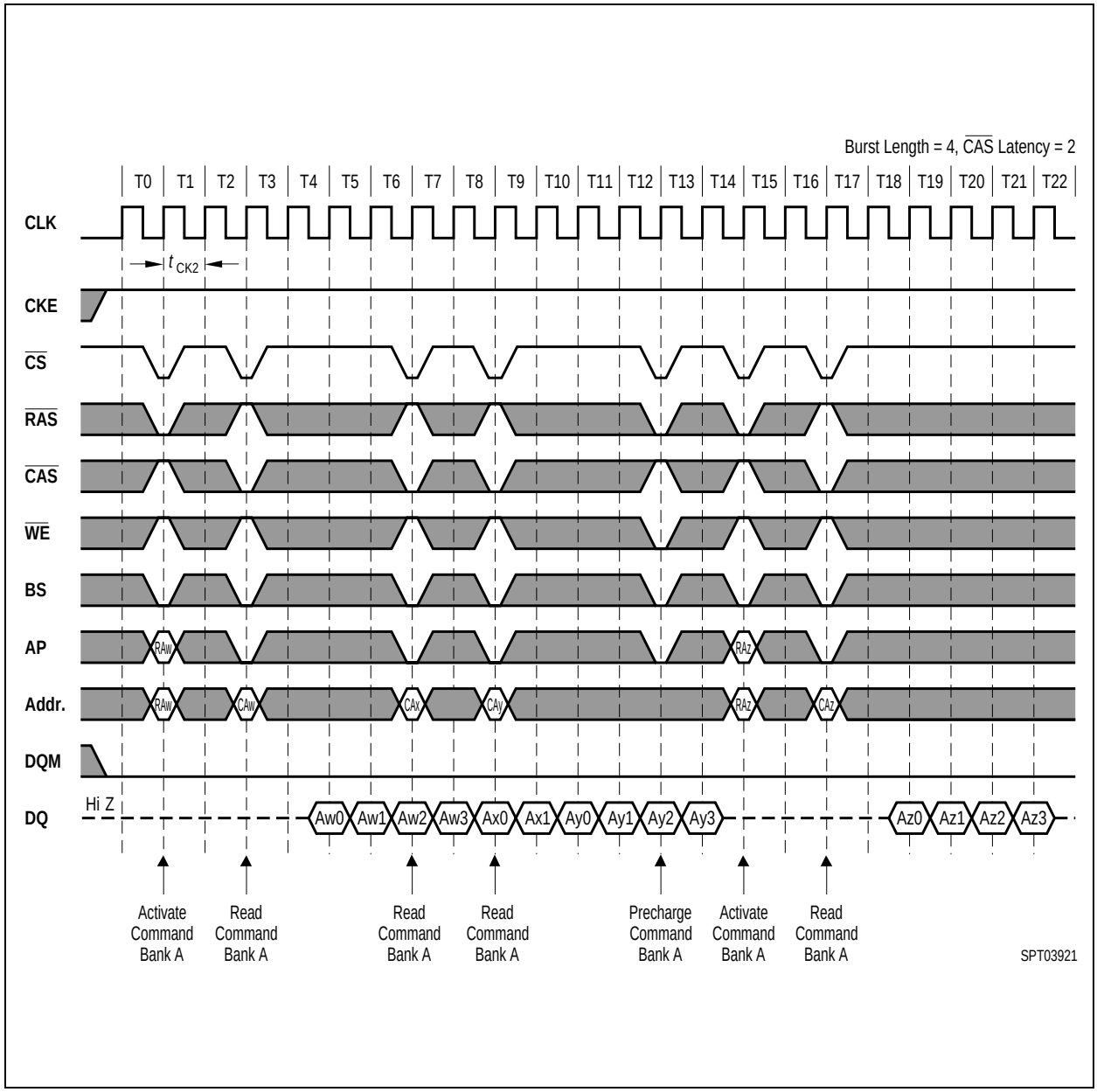


14. Auto Refresh (CBR)

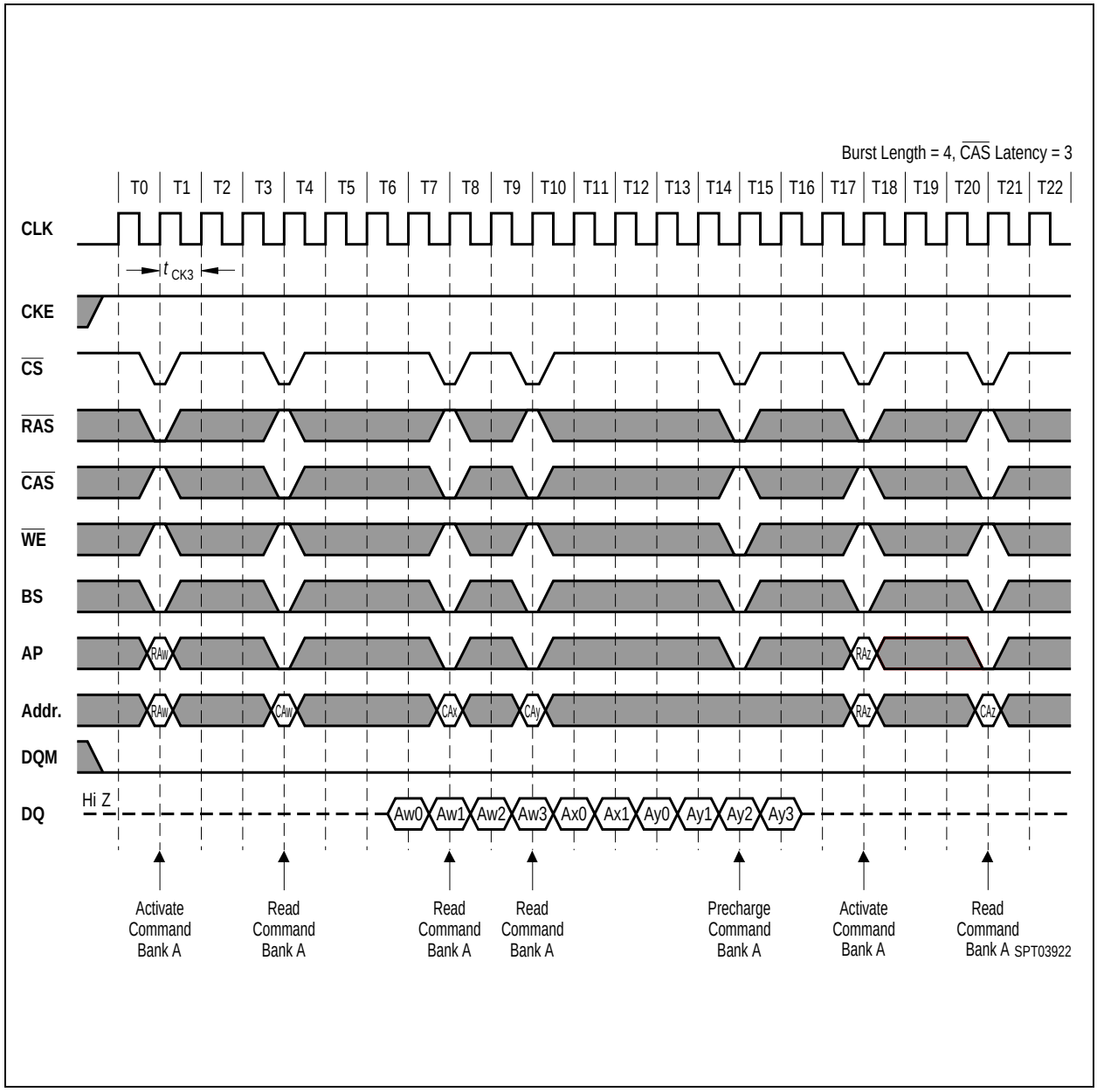


15. Random Column Read (Page within same Bank)

15.1 $\overline{\text{CAS}}$ Latency = 2

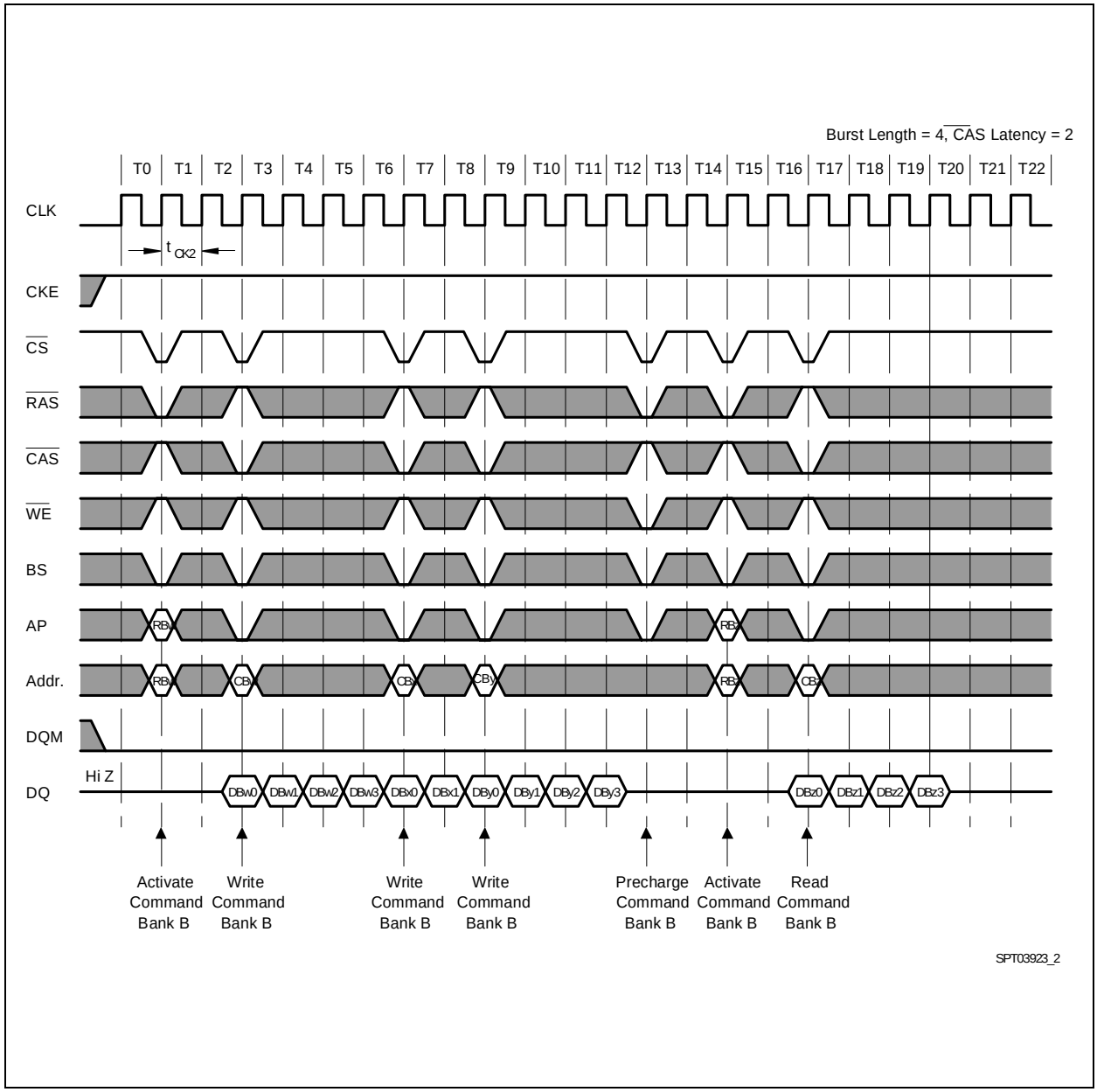


15.2 $\overline{\text{CAS}}$ Latency = 3

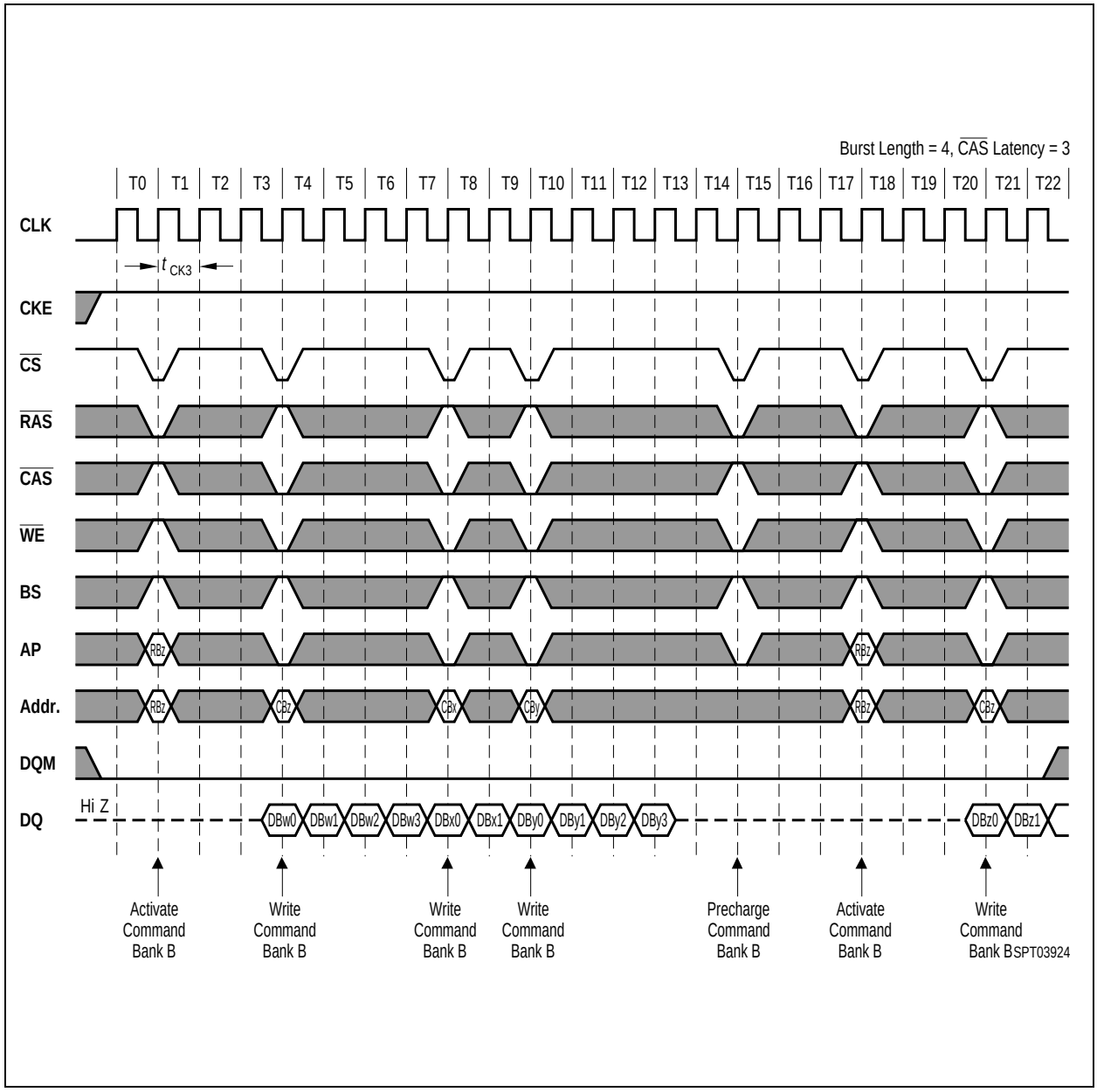


16. Random Column write (Page within same Bank)

16.1 $\overline{\text{CAS}}$ Latency = 2

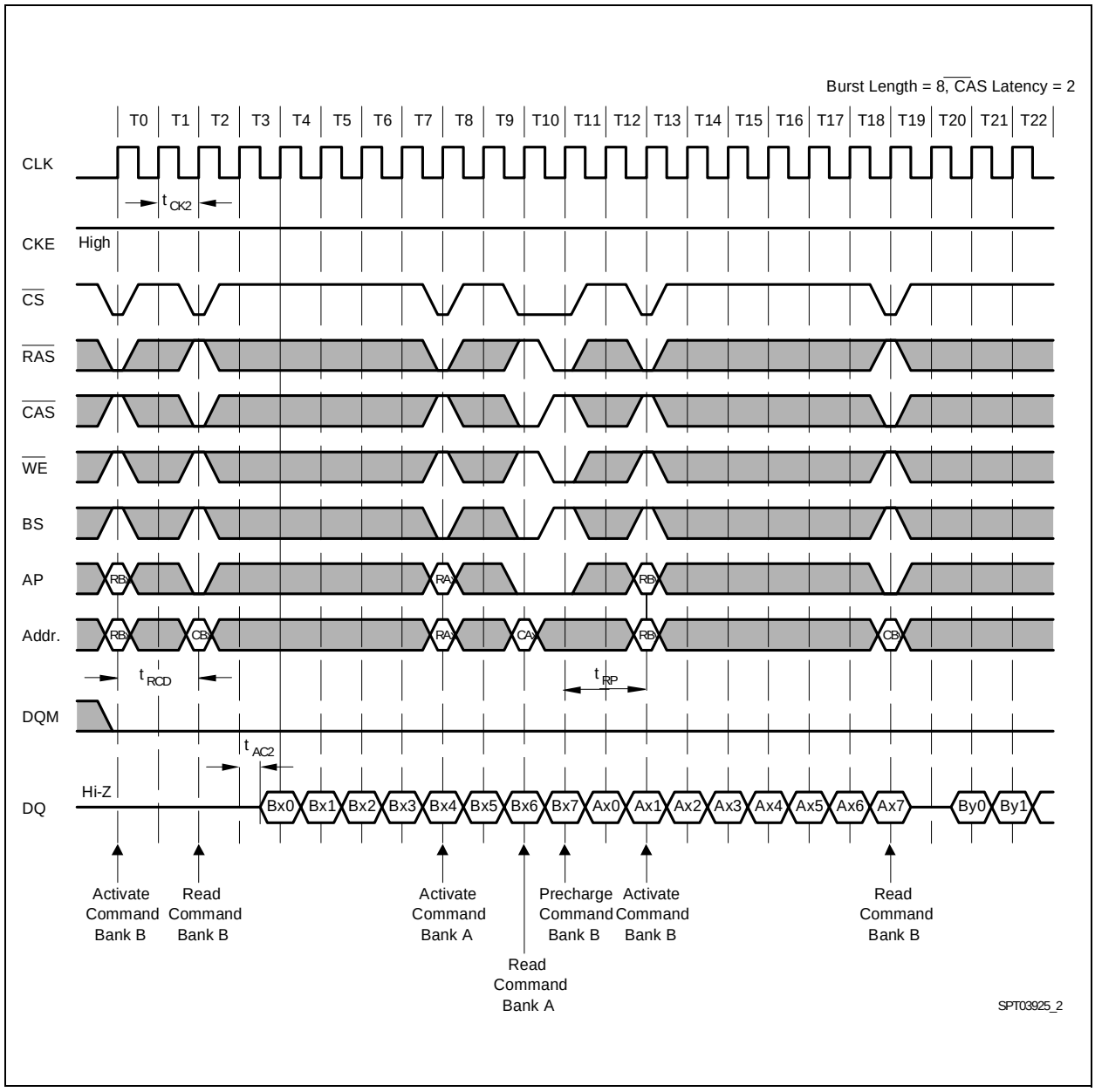


16.2. $\overline{\text{CAS}}$ Latency = 3

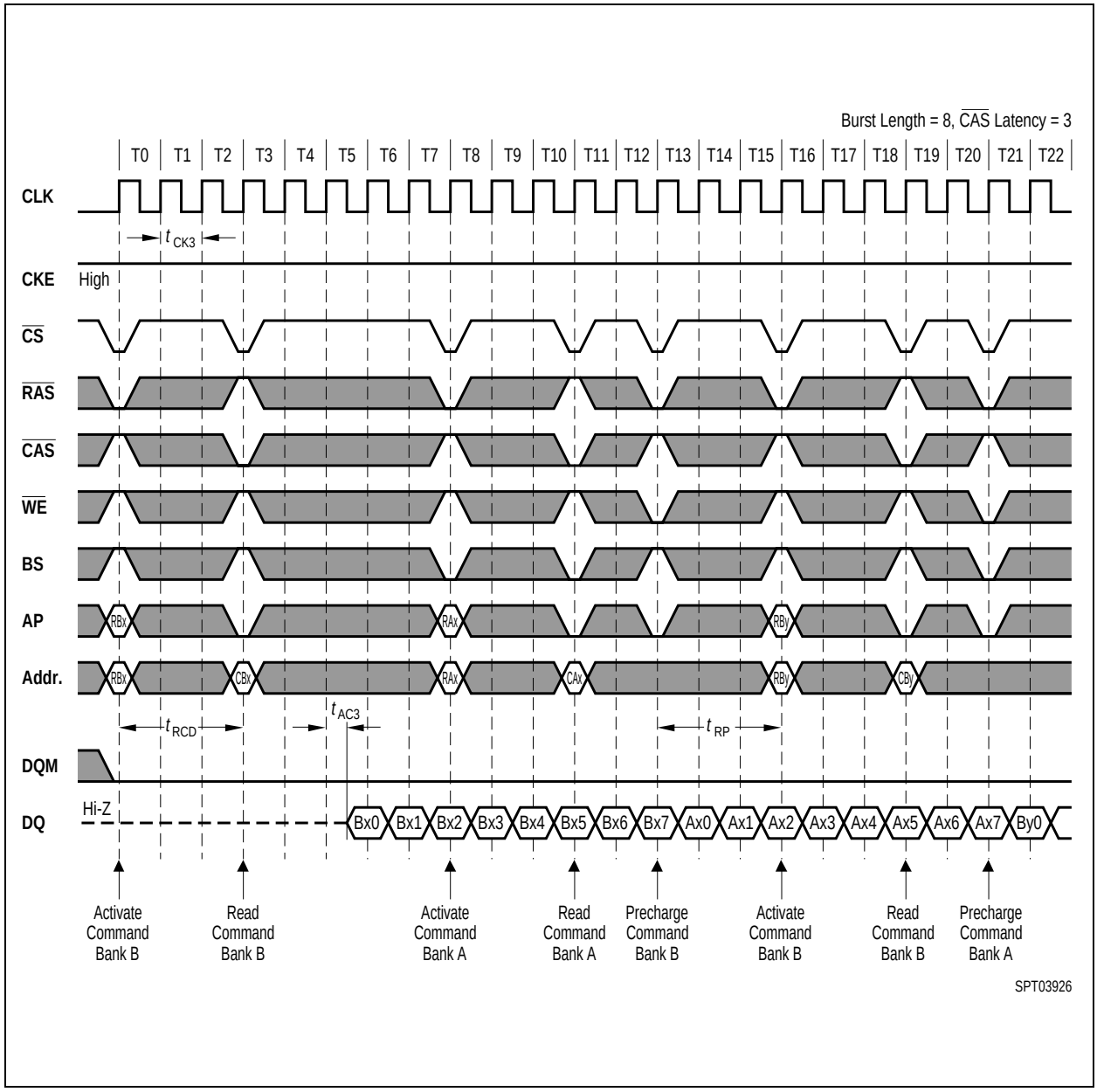


17. Random Row Read (Interleaving Banks) with Precharge

17.1 $\overline{\text{CAS}}$ Latency = 2

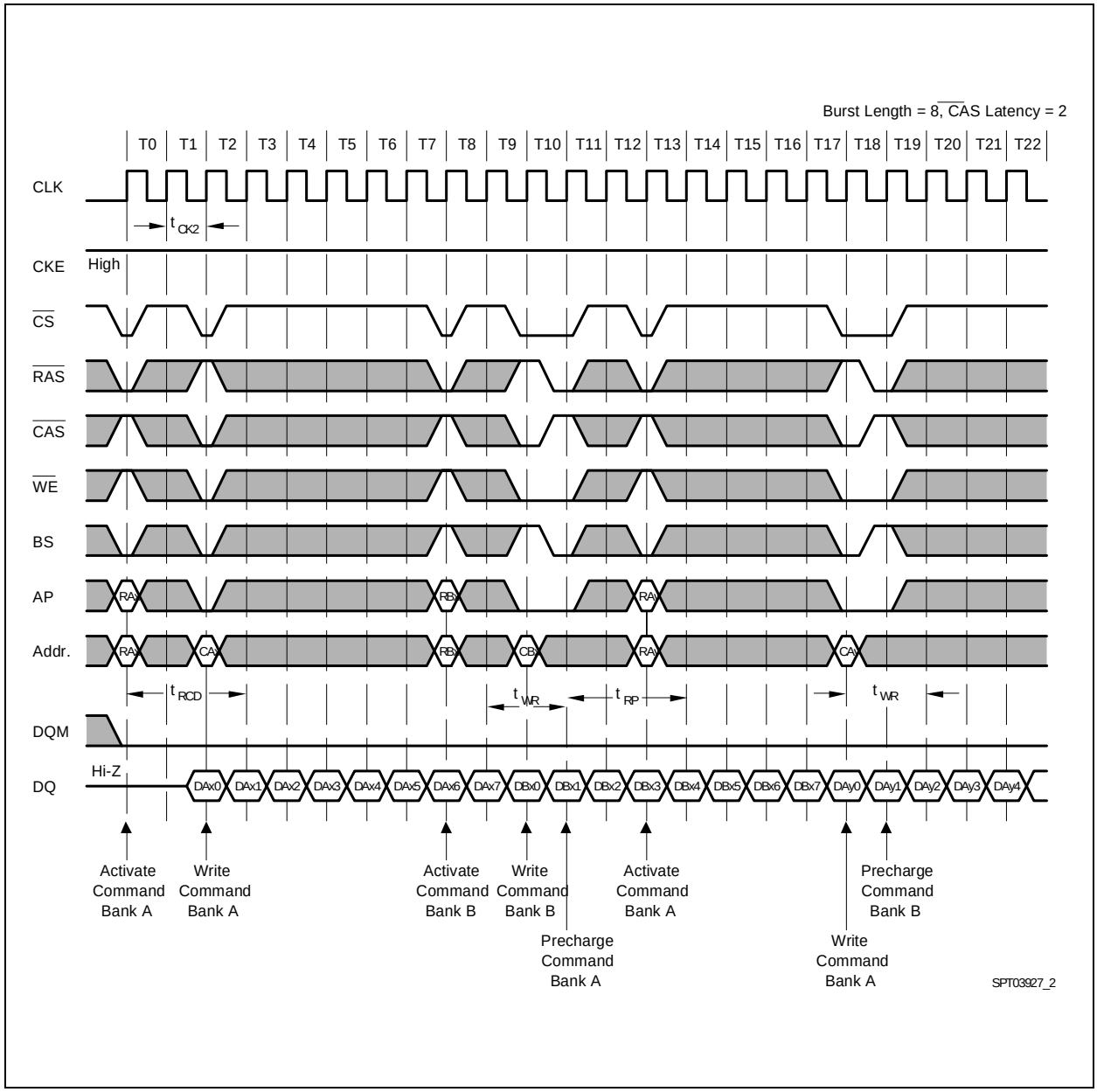


17.2 $\overline{\text{CAS}}$ Latency = 3

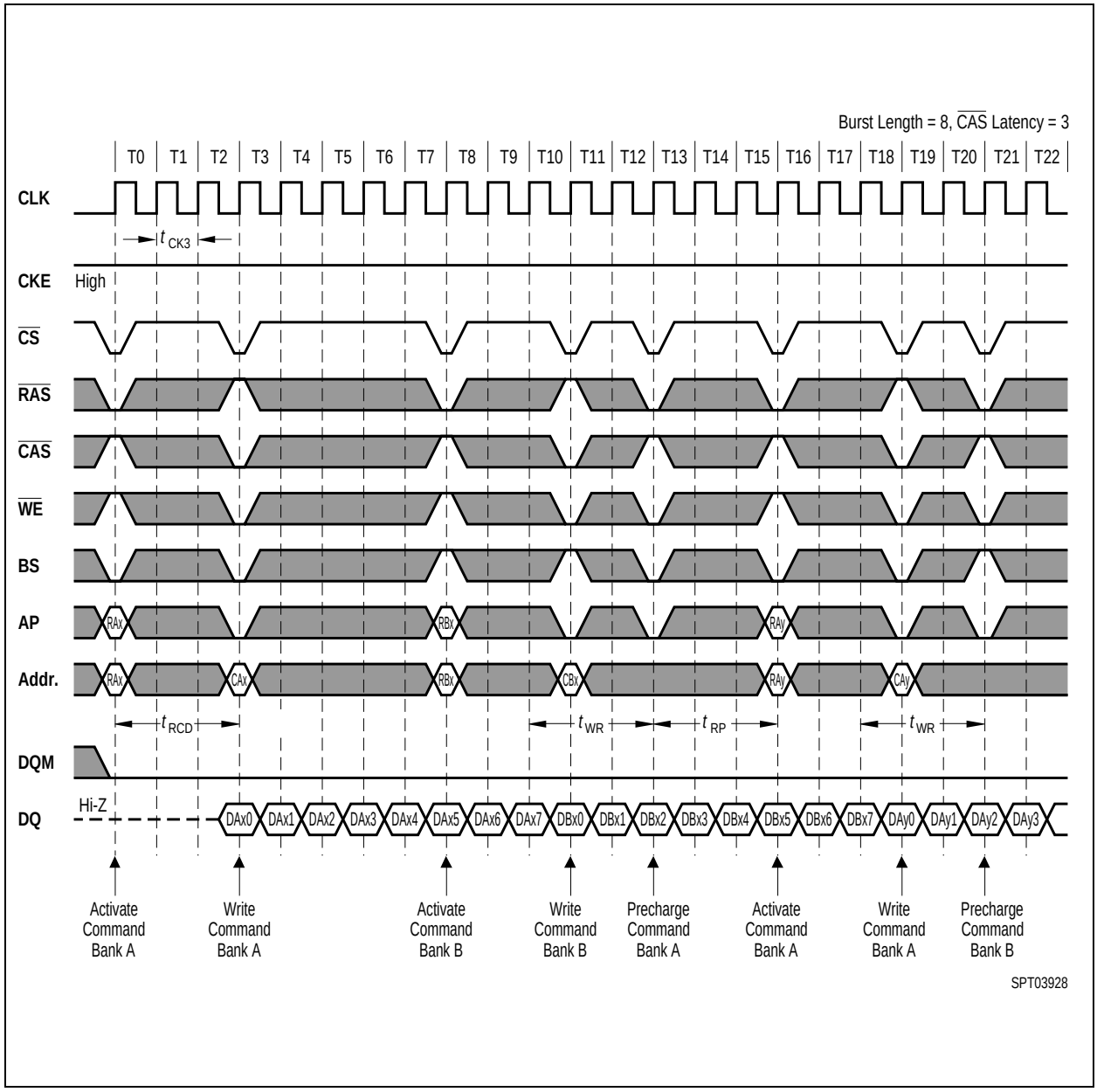


18. Random Row Write (Interleaving Banks) with Precharge

18.1 $\overline{\text{CAS}}$ Latency = 2

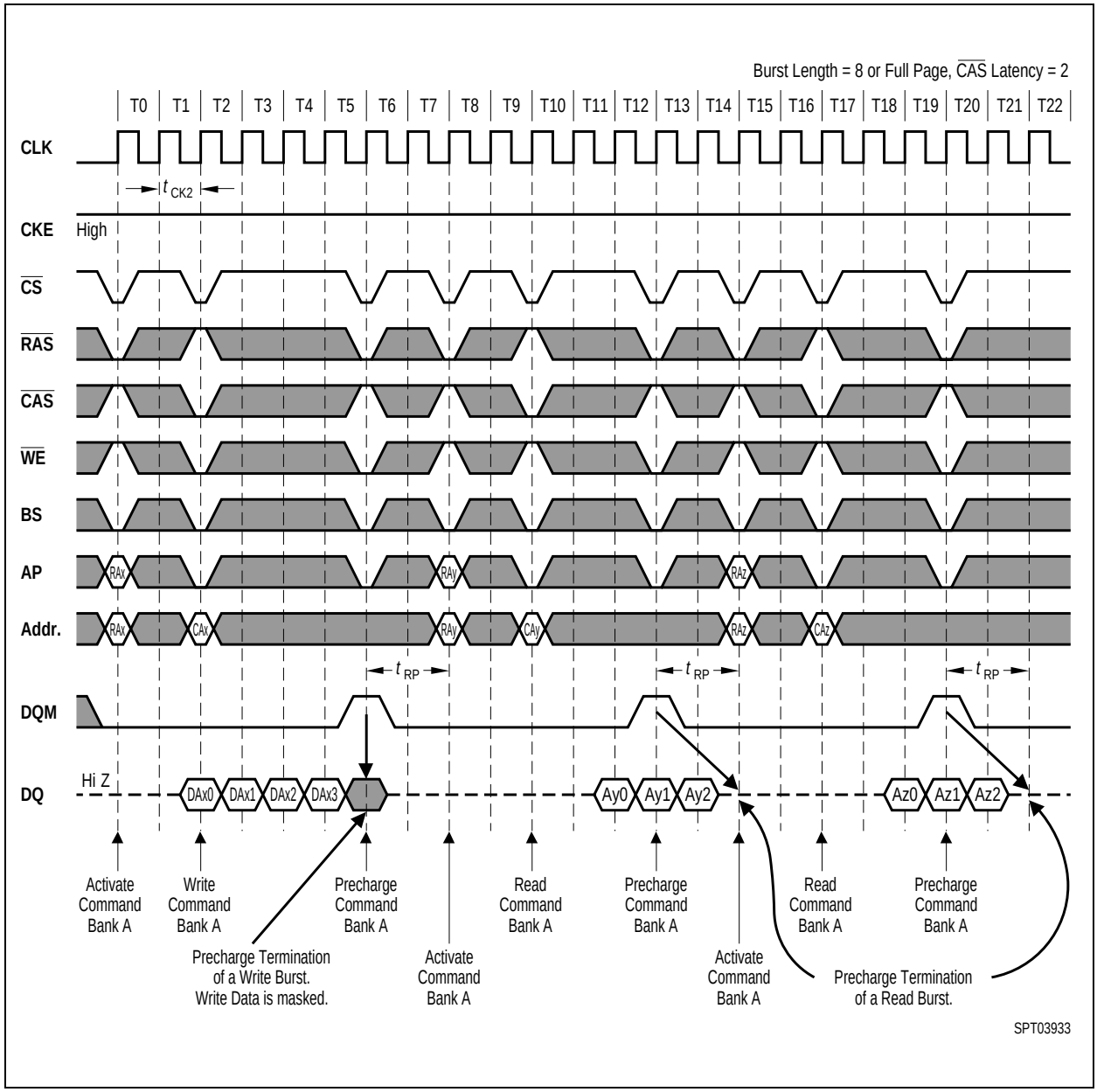


18.2 $\overline{CAS}$ Latency = 3



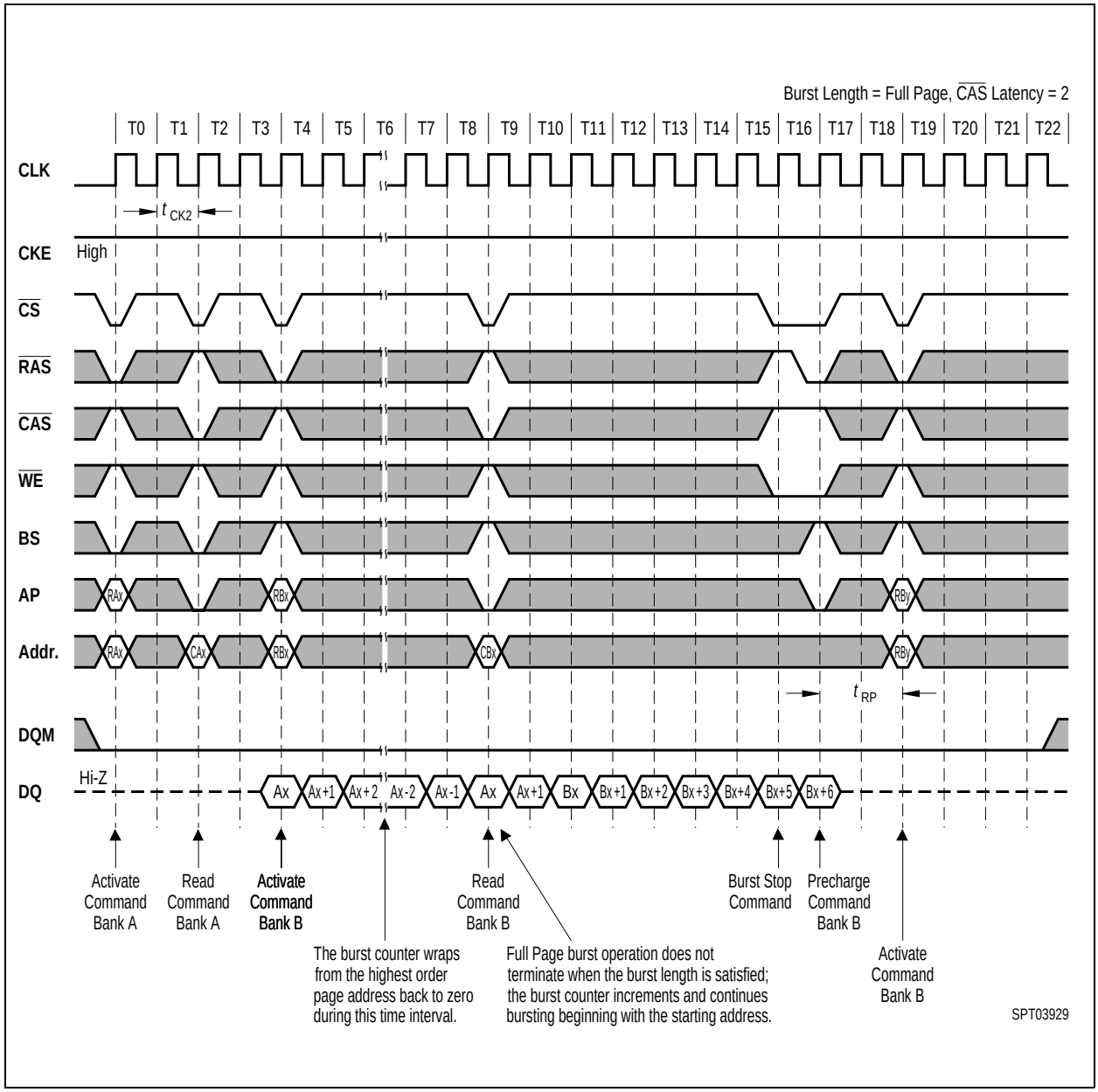
19. Precharge termination of a Burst

19.1 $\overline{CAS}$ Latency = 2



20. Full Page Burst Operation

20.1 Full Page Burst Read, $\overline{CAS}$ Latency = 2



20. Full Page Burst Operation

20.2 Full Page Burst Write, $\overline{CAS}$ Latency = 3

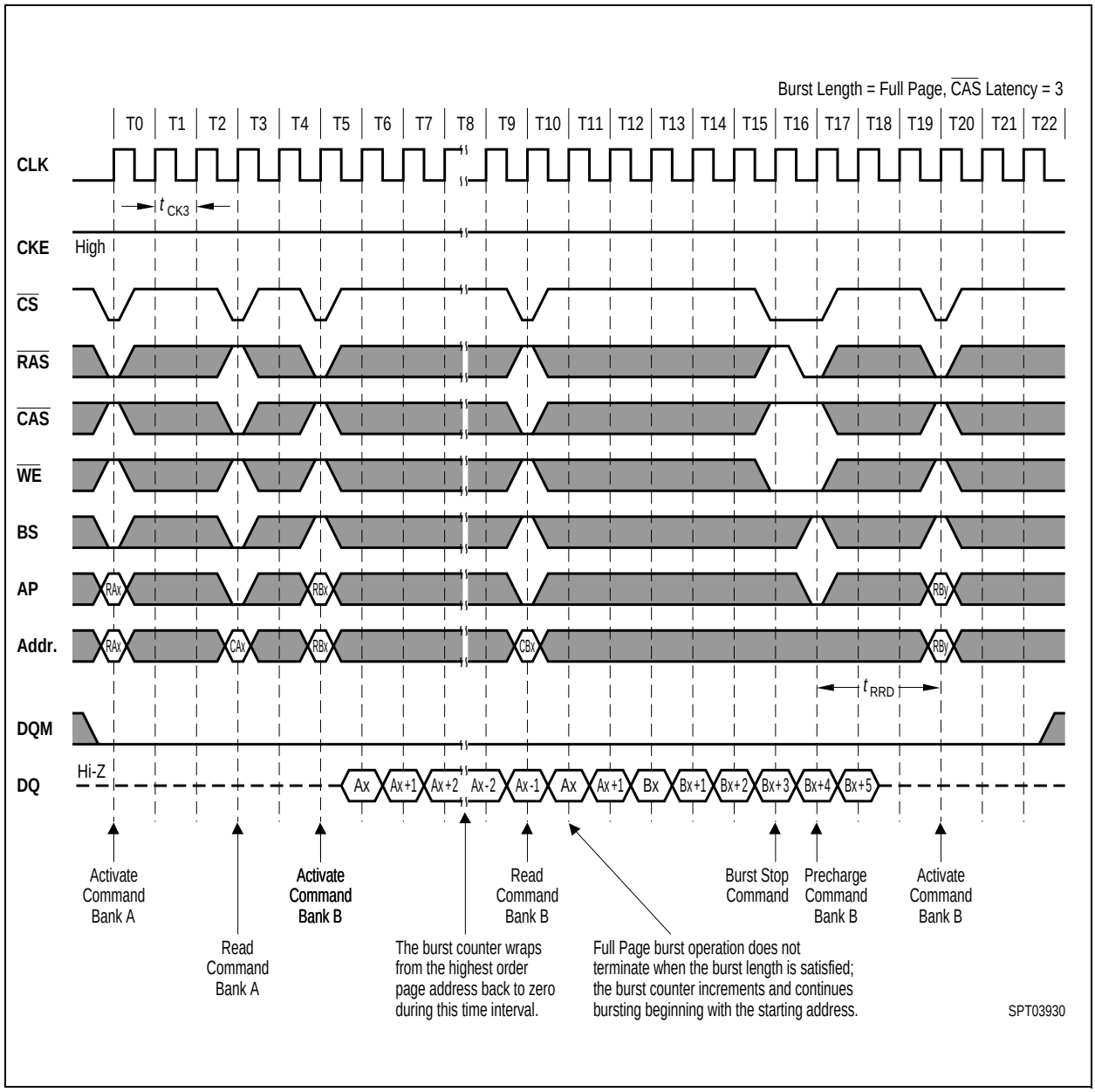


TABLE OF CONTENTS

Attention please !

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies. This infomation describes the type of components and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact INFINEON Technologies Offices in Munich or the INFINEON Technologies Sales Offices and Representatives worldwide.

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest INFINEON Technologies office or representative.

Packing

Please use the recycling operators known to you. We can help you - get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport. For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Ciritcal components[1] of INFINEON Technologies, may only be used in life-support devices or systems[2] with the express written approval of INFINEON Technologies.

1. A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system.

2. Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.